74AC11191

Synchronous 4-Bit Up/Down Binary Counter

The 74AC11191 is a synchronous, 4-bit binary reversible up/down counter. Synchronous counting operation is provided by clocking all flip-flops simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

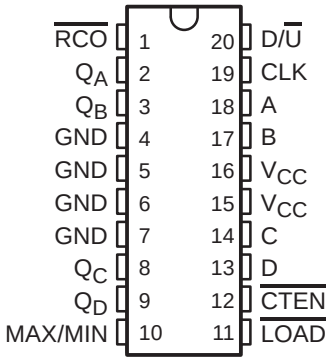
Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SCAS105A – FEBRUARY 1990 – REVISED APRIL 1993

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 74AC11191 is a synchronous, 4-bit binary reversible up/down counter. Synchronous counting operation is provided by clocking all flip-flops simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

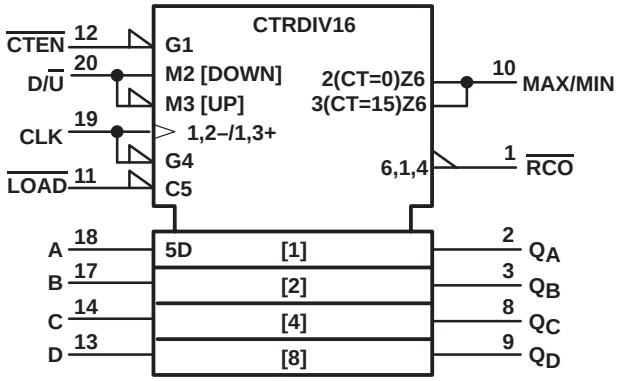
These counters are fully programmable; that is, the outputs may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the level of the clock input. This feature allows the counter to be used as a modulo-N divider by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (15) counting up. The ripple-clock output ($\overline{RCO}$) produces a low-level output pulse under those same conditions but only while the clock input is low. The counter can easily be cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The 74AC11191 is characterized for operation from – 40°C to 85°C.

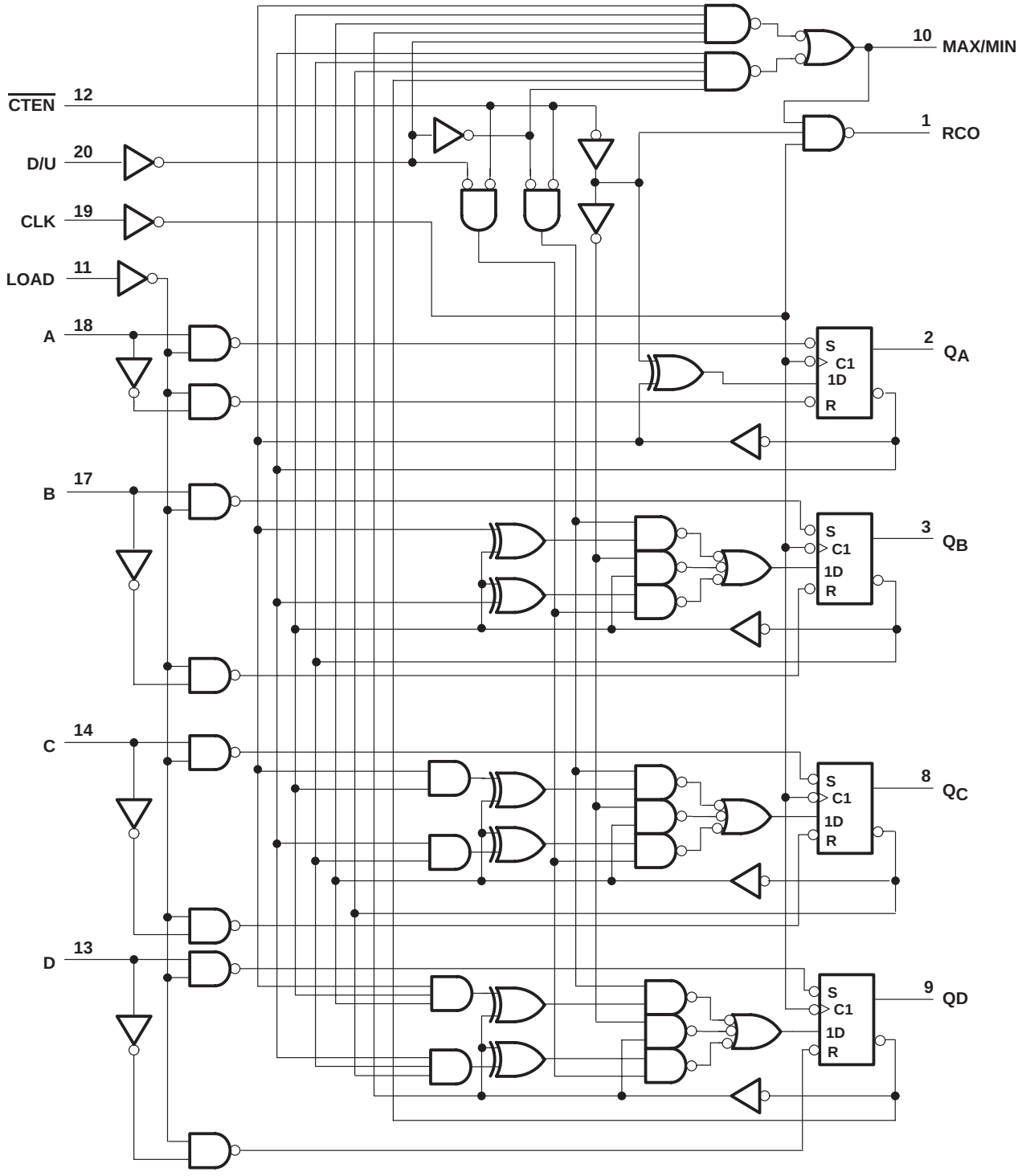
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

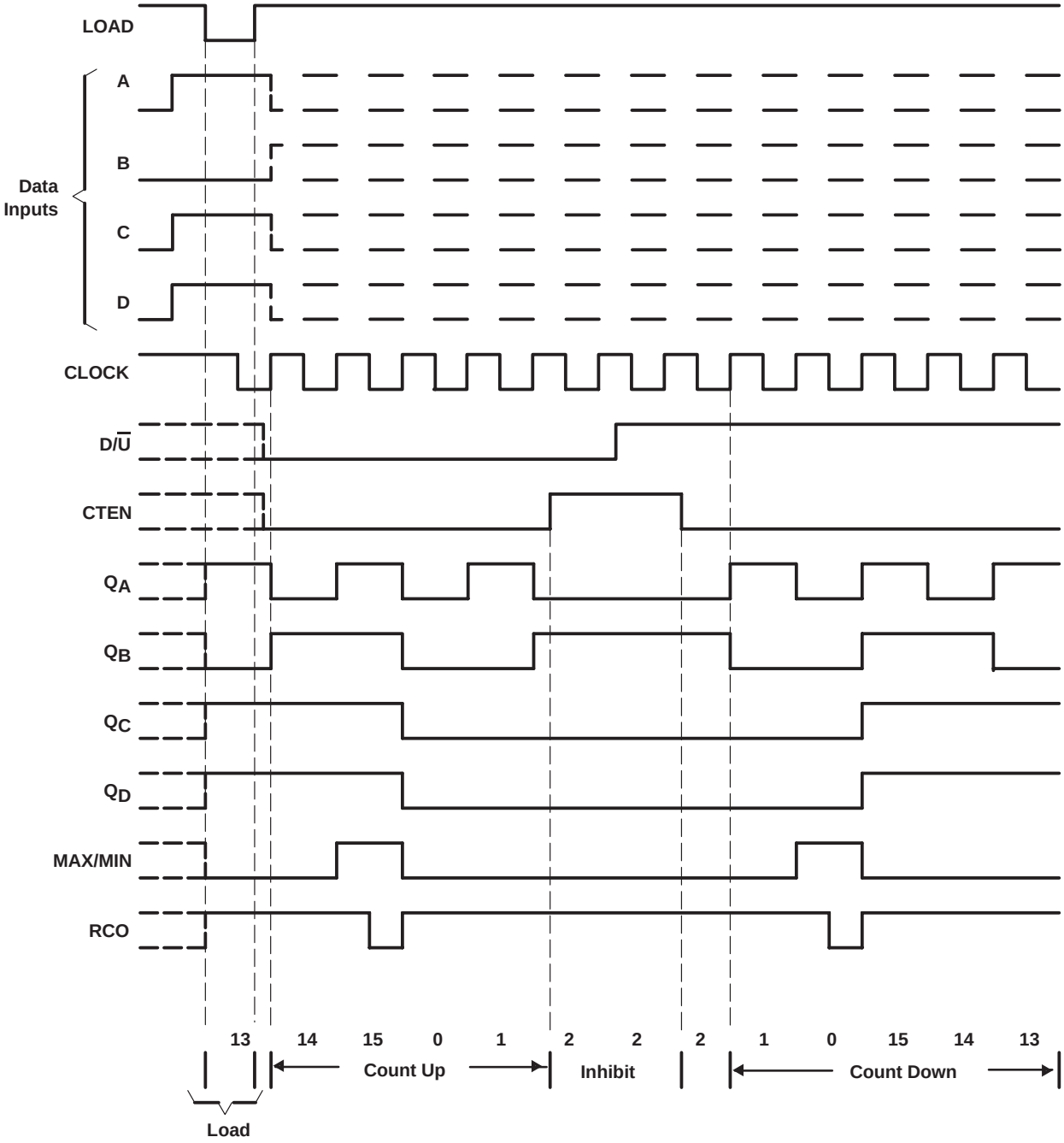
logic diagram (positive logic)



typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND pins . . . . . ± 150 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4	mA
		V_{CC} = 4.5 V			–24	
		V_{CC} = 5.5 V			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		– 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	50	0	50	MHz
t_w	Pulse duration	$\overline{LOAD}$ low	4.8		4.8		ns
		CLK high or low	10		10		
t_{su}	Setup time	Data before $\overline{LOAD}$↑	4		4		ns
		$\overline{CTEN}$ before CLK↑	12.5		12.5		
		D/$\overline{U}$ before CLK↑	13.5		13.5		
		$\overline{LOAD}$ inactive before CLK↑	2.5		2.5		
t_h	Hold time	Data after $\overline{LOAD}$↑	1		1		ns
		$\overline{CTEN}$ after CLK↑	0		0		
		D/$\overline{U}$ after CLK↑	0		0		

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	$\overline{LOAD}$ low	4		4		ns
		CLK high or low	7.2		7.2		
t_{su}	Setup time	Data before $\overline{LOAD}\uparrow$	3		3		ns
		$\overline{CTEN}$ before CLK$\uparrow$	8		8		
		D/$\overline{U}$ before CLK$\uparrow$	8.5		8.5		
		$\overline{LOAD}$ inactive before CLK$\uparrow$	2		2		
t_h	Hold time	Data after $\overline{LOAD}\uparrow$	1.5		1.5		ns
		$\overline{CTEN}$ after CLK$\uparrow$	0.5		0.5		
		D/$\overline{U}$ after CLK$\uparrow$	0		0		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			50	80		50		MHz
t_{PLH}	LOAD	Any Q	3.7	10.7	13.4	3.7	14.9	ns
t_{PHL}			3.6	9.3	12.3	3.6	14.1	
t_{PLH}	LOAD	MAX/MIN	5	14.2	18.7	5	21.1	ns
t_{PHL}			4.6	12.6	17.5	4.6	19.6	
t_{PLH}	LOAD	RCO	5.2	15.4	20.2	5.2	22.9	ns
t_{PHL}			6	15.7	21.6	6	24.7	
t_{PLH}	A, B, C, or D	Any Q	3.4	9.8	12.3	3.4	13.8	ns
t_{PHL}			3.5	8.9	12.1	3.5	13.7	
t_{PLH}	A, B, C, or D	MAX/MIN	4.7	13.5	18.2	4.7	20.7	ns
t_{PHL}			4	11.8	17.1	4	19.3	
t_{PLH}	A, B, C, or D	RCO	5	14.7	19.9	5	22.5	ns
t_{PHL}			5.3	15.1	21.1	5.3	24.3	
t_{PLH}	CLK	RCO	2.8	8.7	11.5	2.8	12.9	ns
t_{PHL}			2.8	7.8	10.6	2.8	11.9	
t_{PLH}	CLK	Any Q	2.2	7.5	9.8	2.2	11.1	ns
t_{PHL}			2.7	7.5	11	2.7	12.7	
t_{PLH}	CLK	MAX/MIN	3.7	9.9	12.2	3.7	13.8	ns
t_{PHL}			4.1	10.2	14.4	4.1	16	
t_{PLH}	D/U	RCO	4.1	11.2	14.4	4.1	15.9	ns
t_{PHL}			4.1	10.2	14.3	4.1	16.5	
t_{PLH}	D/U	MAX/MIN	2.7	8.7	11.5	2.7	12.7	ns
t_{PHL}			3.1	8.3	11.8	3.1	13.6	
t_{PLH}	CTEN	RCO	2.5	7.2	9	2.5	10.3	ns
t_{PHL}			2.6	6.6	8.8	2.6	10	

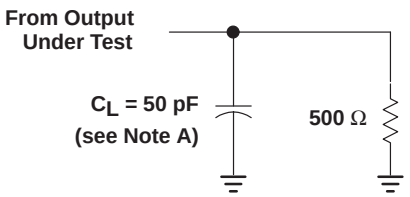
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100	135		100		MHz
t_{PLH}	LOAD	Any Q	3.1	6.7	9.4	3.1	10.6	ns
t_{PHL}			3	6.4	9	3	10.2	
t_{PLH}	LOAD	MAX/MIN	4.3	8.8	12.5	4.3	14.3	ns
t_{PHL}			4	8.4	12	4	13.7	
t_{PLH}	LOAD	RCO	4.5	9.7	13.7	4.5	15.4	ns
t_{PHL}			5	10.1	14.4	5	16.3	
t_{PLH}	A, B, C, or D	Any Q	2.9	6.2	8.7	2.9	9.8	ns
t_{PHL}			3	6.1	8.7	3	9.8	
t_{PLH}	A, B, C, or D	MAX/MIN	4.1	8.4	12.2	4.1	13.7	ns
t_{PHL}			3.5	8	11.8	3.5	13.4	
t_{PLH}	A, B, C, or D	RCO	4.3	9.2	13.5	4.3	15.1	ns
t_{PHL}			4.7	9.7	14	4.7	16	
t_{PLH}	CLK	RCO	2.4	5.9	8.4	2.4	9.1	ns
t_{PHL}			2.9	5.6	7.7	2.9	8.7	
t_{PLH}	CLK	Any Q	1.9	5.2	7.6	1.9	8.4	ns
t_{PHL}			2.4	5.4	8	2.4	9.4	
t_{PLH}	CLK	MAX/MIN	3	6.5	8.8	3	10.4	ns
t_{PHL}			3.6	7.1	10.4	3.6	10.8	
t_{PLH}	D/U	RCO	3.5	7.2	10.2	3.5	11.3	ns
t_{PHL}			3.5	6.9	10	3.5	11.5	
t_{PLH}	D/U	MAX/MIN	2.3	5.7	8.1	2.3	9.1	ns
t_{PHL}			2.7	5.9	8.6	2.7	9.7	
t_{PLH}	CTEN	RCO	2.1	4.9	6.8	2.1	7.7	ns
t_{PHL}			2.2	4.8	6.7	2.2	7.7	

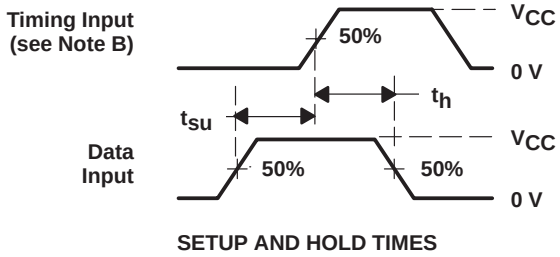
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	66	pF

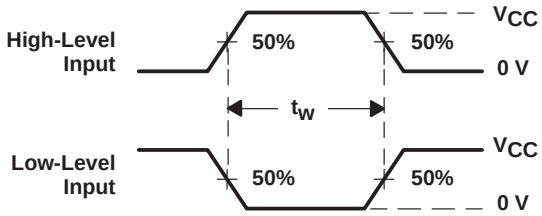
PARAMETER MEASUREMENT INFORMATION



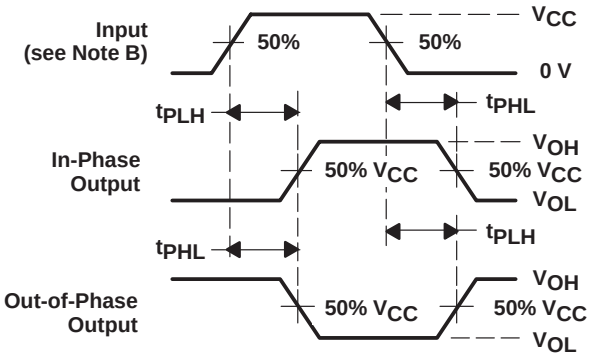
LOAD CIRCUIT



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74AC11191DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
74AC11191N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265