

F100183

2 x 8-Bit Recode Multiplier

The F100183 is a 2 x 8-bit recode multiplier designed to perform high-speed hardware multiplication. In conjunction with the F100182 Wallace Tree Adder, the F100179 Carry Lookahead, and the F100180 High-speed Adder, the F100183 performs parallel multiplication of two signed numbers in twos complement product. All inputs have 50 kΩ pull-down resistors.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.



F100183 2 x 8-Bit Recode Multiplier

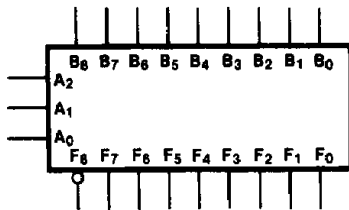
General Description

The F100183 is a 2 x 8-bit recode multiplier designed to perform high-speed hardware multiplication. In conjunction with the F100182 Wallace Tree Adder, the F100179 Carry Lookahead, and the F100180 High-speed Adder, the

F100183 performs parallel multiplication of two signed numbers in twos complement form to produce a signed twos complement product. All inputs have 50 k Ω pull-down resistors.

Ordering Code: See Section 8

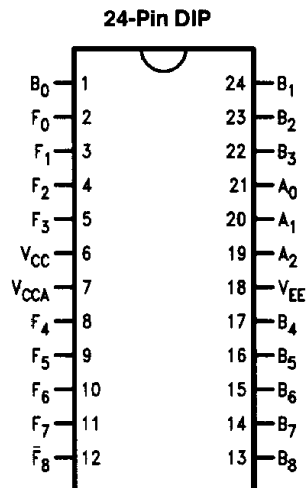
Logic Symbol



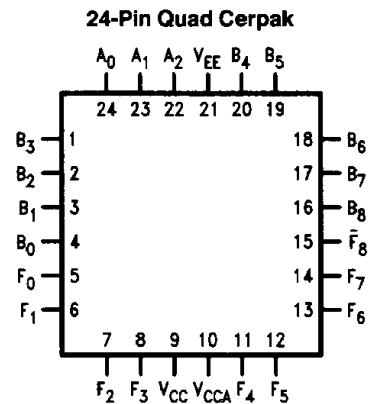
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Pin Names	Description
A ₀ -A ₂	Multiplier (Recode) Inputs
B ₀ -B ₈	Multiplicand Inputs
F ₀ -F ₇	Partial Product Outputs
\bar{F}_8	Sign Extension Output

Connection Diagrams

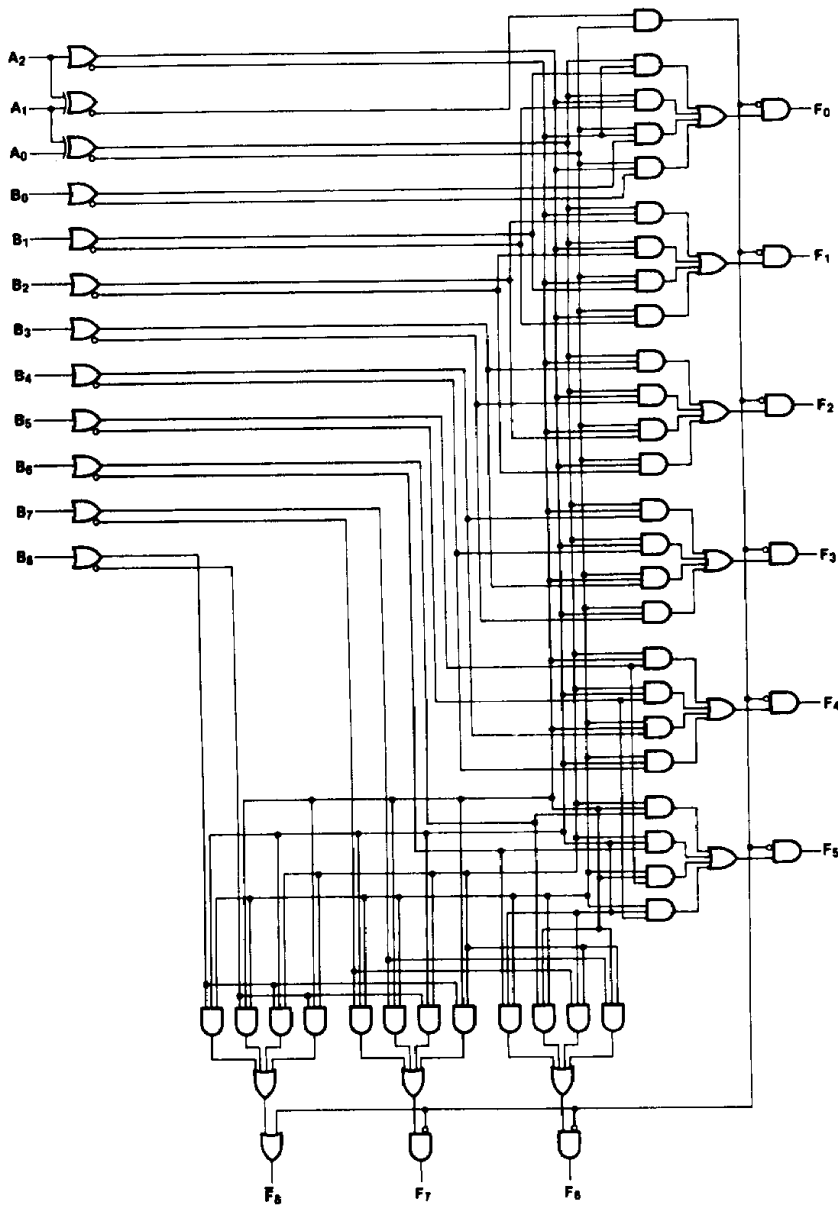


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Logic Diagram



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Truth Table

Inputs			Recode Mode	Outputs								
A ₂	A ₁	A ₀		F ₈ ⁻	F ₇ ⁻	F ₆ ⁻	F ₅ ⁻	F ₄ ⁻	F ₃ ⁻	F ₂ ⁻	F ₁ ⁻	F ₀ ⁻
L	L	L	0	H	L	L	L	L	L	L	L	L
L	L	H	+1	B ₈ ⁻	B ₈	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁
L	H	L	+1	B ₈ ⁻	B ₈	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁
L	H	H	+2	B ₈ ⁻	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀
H	L	L	-2	B ₈	B ₇ ⁻	B ₆ ⁻	B ₅ ⁻	B ₄ ⁻	B ₃ ⁻	B ₂ ⁻	B ₁ ⁻	B ₀ ⁻
H	L	H	-1	B ₈	B ₈ ⁻	B ₇ ⁻	B ₆ ⁻	B ₅ ⁻	B ₄ ⁻	B ₃ ⁻	B ₂ ⁻	B ₁ ⁻
H	H	L	-1	B ₈	B ₈ ⁻	B ₇ ⁻	B ₆ ⁻	B ₅ ⁻	B ₄ ⁻	B ₃ ⁻	B ₂	B ₁
H	H	H	0	H	L	L	L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{EE} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50 mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	-1025	-955	-880	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1810	-1705	-1620			
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610			
V_{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL}(\text{Min})$	

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	-1020		-870	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1810		-1605			
V_{OHC}	Output HIGH Voltage	-1030			mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1595			
V_{IH}	Input HIGH Voltage	-1150		-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL}(\text{Min})$	

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	-1035		-880	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830		-1620			
V_{OHC}	Output HIGH Voltage	-1045			mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610			
V_{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830		-1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL}(\text{Min})$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

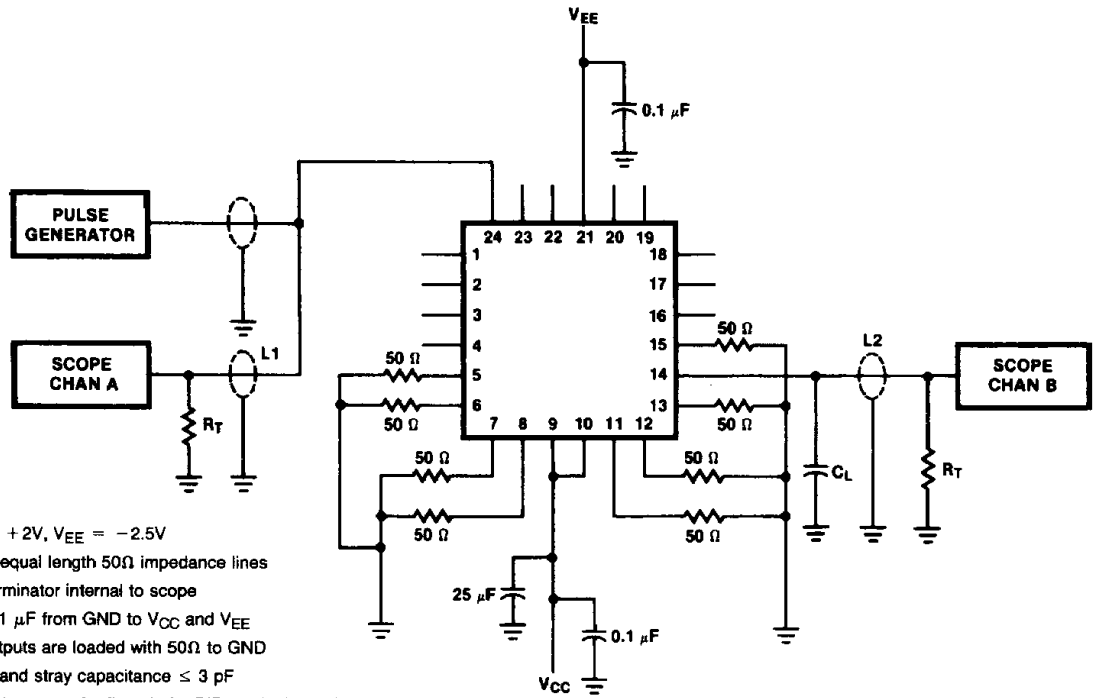
Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current B ₀ -B ₈ A ₀ A ₁ A ₂			215 215 285 310	μA	$V_{IN} = V_{IH} (Max)$
I_{EE}	Power Supply Current	-250	-170	-115	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A ₀ -A ₂ to F ₀ -F ₇	1.10	3.90	1.10	3.80	1.10	4.20	ns	<i>Figures 1 and 2</i>
t_{PLH} t_{PHL}	Propagation Delay A ₀ -A ₂ to \bar{F}_8	0.90	3.20	1.00	3.10	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay B ₀ -B ₈ to F ₀ -F ₇	0.80	2.20	0.90	2.15	0.90	2.50	ns	<i>Figures 1 and 2</i>
t_{PLH} t_{PHL}	Propagation Delay B ₈ to \bar{F}_8	0.80	2.00	0.90	2.00	0.90	2.50	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.50	0.45	2.40	0.45	2.60	ns	<i>Figures 1 and 2</i>

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A ₀ -A ₂ to F ₀ -F ₇	1.10	3.70	1.10	3.60	1.10	4.00	ns	<i>Figures 1 and 2</i>
t_{PLH} t_{PHL}	Propagation Delay A ₀ -A ₂ to \bar{F}_8	0.90	3.00	1.00	2.90	1.00	3.40	ns	
t_{PLH} t_{PHL}	Propagation Delay B ₀ -B ₈ to F ₀ -F ₇	0.80	2.00	0.90	1.95	0.90	2.30	ns	<i>Figures 1 and 2</i>
t_{PLH} t_{PHL}	Propagation Delay B ₈ to \bar{F}_8	0.80	1.80	0.90	1.80	0.90	2.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.40	0.45	2.30	0.45	2.50	ns	<i>Figures 1 and 2</i>

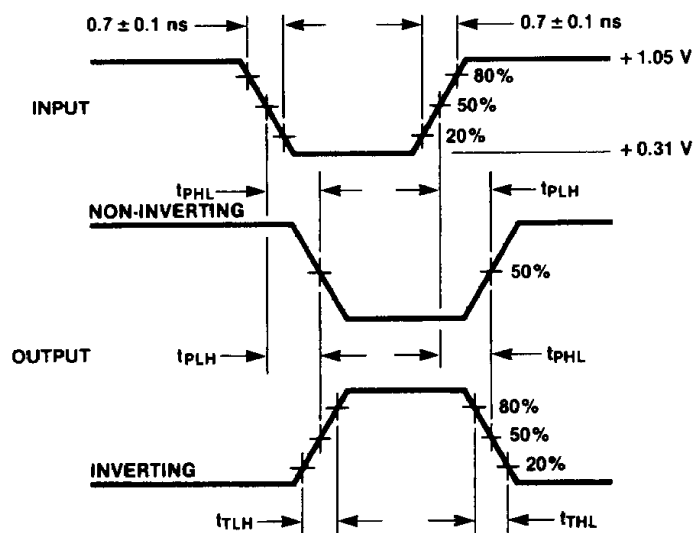


Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- $C_L =$ Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

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FIGURE 2. Propagation Delay and Transition Times

Application

F100183 is a 2 x 8-bit recode multiplier that performs parallel multiplication using two's complement arithmetic. In multiplying, the multiplier is partitioned into recode groups, then each recode group operates on the multiplicand to provide a partial product at the same time. The F100183, 2 x 8-bit recode multiplier provides partial products in 3.6 ns.

The F100182, 9-Bit Wallace Tree Adder combines the partial products to obtain the partial sum and partial carries in an additional 10.7 ns. Then the Carry Lookahead generator and 6-bit adder combine the results of a 16 x 16-bit multiply

for a total of 24.3 ns. The propagation delays and package count for implementing various size multipliers are listed in Tables I and II.

Multiplication of two's complement binary numbers is accomplished by first obtaining all the partial products. Then the weighted partial products are added together to yield the final result. In the Wallace Tree method of multiplication the sign bit is treated the same as the rest of the bits to obtain a signed result.

TABLE I. Propagation Delay Summation*

Array Size	Recode Multiplier 100183	Wallace Tree Adder 100182	High-speed Adder 100180	Carry Lookahead 100179	Total (Max) Delay
16 x 16	3.6	10.7	7.3	2.7	= 24.3 ns
17 x 17 thru 24 x 24	3.6	21.4	7.3	2.7	= 35.0 ns
25 x 25 thru 48 x 48	3.6	21.4	7.3	5.4	= 37.7 ns
49 x 49 thru 72 x 72	3.6	21.4	7.3	8.1	= 40.4 ns
73 x 73	3.6	32.1	7.3	10.8	= 53.8 ns

*Worst case, Flatpak

Application (Continued)**TABLE II. Package Count**

	100102 100117	100183	100182	100180	100179	=	Total
16 x 16	6	16	32	6	2	=	62
18 x 18	7	27	38	6	2	=	70
24 x 24	9	36	60	8	2	=	115
32 x 32	11	64	96	11	4	=	186
36 x 36	13	80	116	12	4	=	225
64 x 64	24	256	328	22	6	=	634

For a quick review of the twos complement number format see Table III. Note that subtraction is accomplished by adding the negative number. An example of changing from a positive number to a negative number is shown.

```

1011  negative number-5

0100  bits inverted
+0001  add one
-----
0101  Results 5

```

TABLE III. Twos Complement Format

Sign Bit	Magnitude			Decimal Number
	2 ²	2 ¹	2 ⁰	
0	1	1	1	+7
0	1	1	0	+6
0	1	0	1	+5
0	1	0	0	+4
0	0	1	1	+3
0	0	1	0	+2
0	0	0	1	+1
0	0	0	0	+0
1	1	1	1	-1
1	1	1	0	-2
1	1	0	1	-3
1	1	0	0	-4
1	0	1	1	-5
1	0	1	0	-6
1	0	0	1	-7
1	0	0	0	-8

Multiplication Algorithm

In the multiplication algorithm used, the multiplier ($Y_n \dots Y_0$) is partitioned into recode groups and each recode group operates on the multiplicand ($X_n \dots X_0$) as in Figure 4. The F100183, 2 x 8-bit recode multiplier partitions the multiplier ($X_n \dots X_0$) into groups of eight and the multiplicand ($Y_n \dots Y_0$) into groups of two. Each recode group is two bits wide but requires three bits to determine the partial products. Table IV lists the significance of the various recode groups. The partial product is ± 0 , \pm multiplicand, or \pm two times the multiplicand. A forced zero is required to establish the least significant bit of the first recode group. By connecting recode multipliers in parallel the partial products are available at the same time. The weighted partial products ($A_n \dots A_0$, $B_n \dots B_0$) ... are added together using F100182, 9-bit Wallace Tree Adders. The results of the partial sum and partial

carry are combined together using Carry Lookahead generators and 6-bit adders. An example of using recode multiplication is shown in Figure 3: multiplier (117_{10}) 01110101 times multiplicand (105_{10}) 01101001. The first recode group 010 requires adding the multiplicand; the second recode group 010 also requires adding the multiplicand; the third group 110 requires subtracting the multiplicand (the same as inverting each digit and adding 1); the fourth group 011 requires adding twice the multiplicand. Combining the results of four groups, 12285_{10} , we have the correct answer.

TABLE IV. Recode Product

Recode Group			Recode Value	Partial Product
Y_{i+1}	Y_i	Y_{i-1}		
0	0	0	+0	Add zero
0	0	1	+1	Add multiplicand
0	1	0	+1	Add multiplicand
0	1	1	+2	Add twice the multiplicand
1	0	0	-2	Subtract twice the multiplicand
1	0	1	-1	Subtract the multiplicand
1	1	0	-1	Subtract the multiplicand
1	1	1	-0	Subtract zero

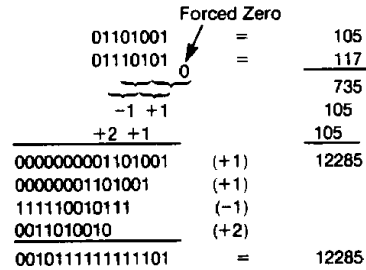


FIGURE 3. Recode Multiplication Example

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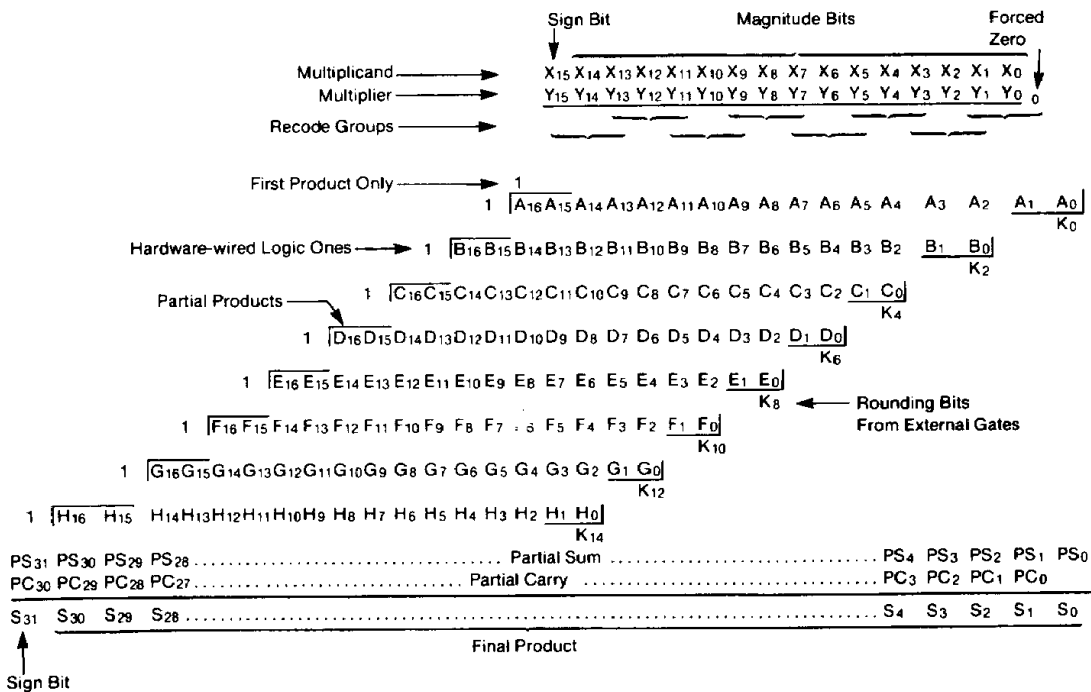


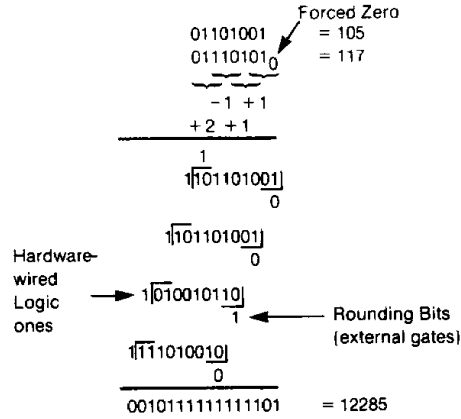
FIGURE 4. 16 x 16 Multiply

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Hardware Implementation

For the hardware implementation of the F100183 recode multiplier the sign bit is connected to the B₈ input, and B₇ through B₀ are the magnitude bits. Two extend the word length greater than eight bits, the B₀ and B₈ inputs of adjacent devices are connected together (see Figure 7). The device outputs F₀ through F₇ are used as the partial products; these correspond to A₀ through A₇, or A₈ through A₁₅, or B₀ through B₇, etc. To reduce the hardware, the F₈ bit (A₁₆ in Figure 7) is used as the sign bit of the partial product. The sign bits are extended by using hardware wired logic "1s". The ones are located in front of each partial product with an extra "1" at the sign bit of the first partial product as in Figure 4. The logic "1s" are wired as inputs into the Wallace Tree Adders as shown in Figure 6. If the recode group requires the multiplicand to be added, then the F100183 outputs the correct partial products to be added. But when the recode group requires that the multiplicand be subtracted, then the F100183 outputs the ones complement. External gates are required to generate a "1" to be added to the ones complement to complete the twos complement for the partial product (Figure 7). These external gates generate the rounding bits, K₀ . . . K_n, which are input to the Wallace Tree Adder. Figures 4, 6 and 7 show the location. An example of multiplication which has the rounding bits and the hardware wired logic "1s" is shown in Figure 5.

The weighted partial products are added together using F100182, 9-bit Wallace Tree Adders as shown in Figure 6. The output is a partial sum and partial carry which can be reduced to the final product using Carry Lookahead and 6-bit adders. See Figure 8.



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FIGURE 5. Example of Multiplication Using Rounding Bits

Hardware Implementation (Continued)

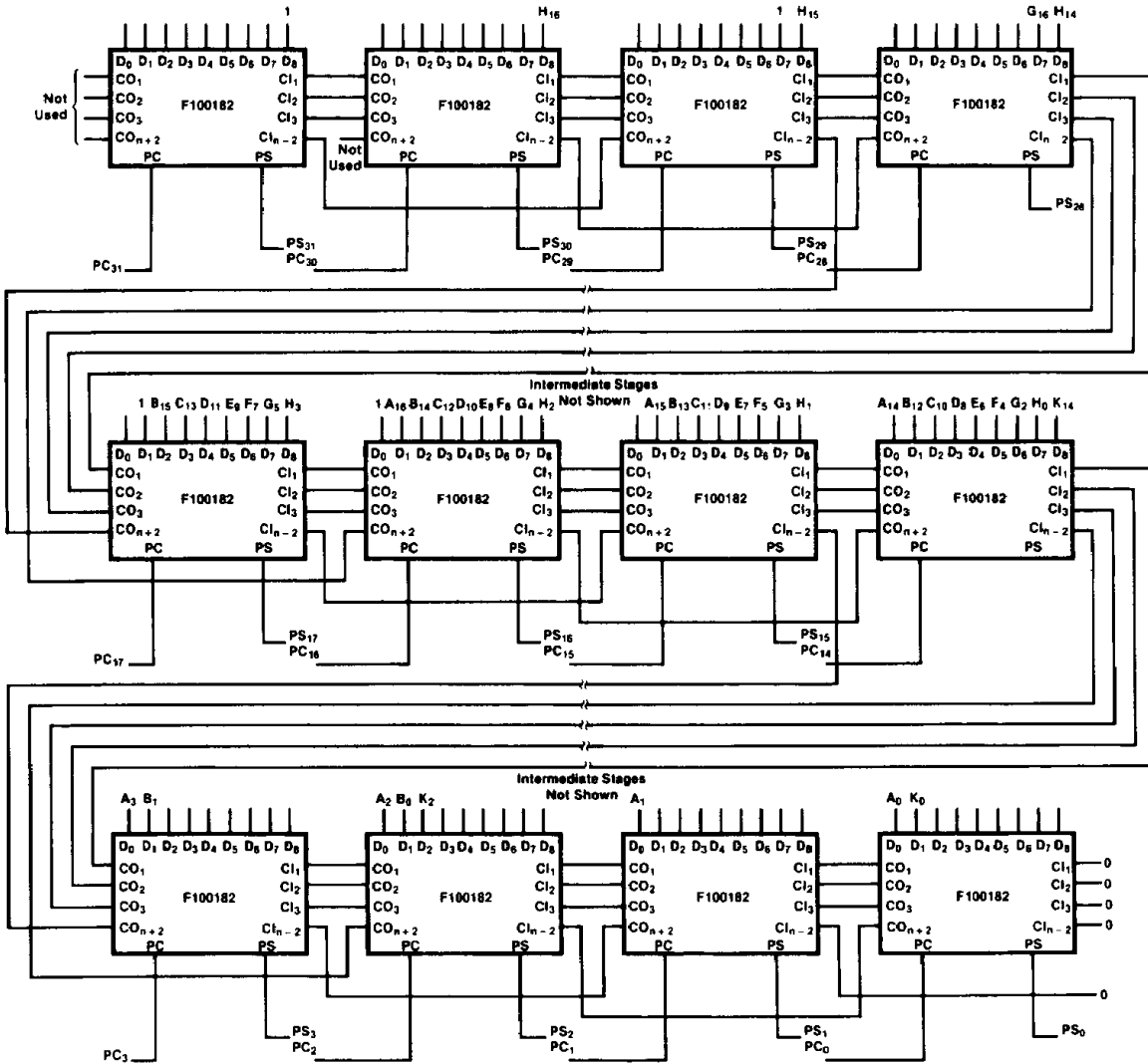


FIGURE 6. F100182 Hook-up for 16 x 16 Multiplier

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Hardware Implementation (Continued)

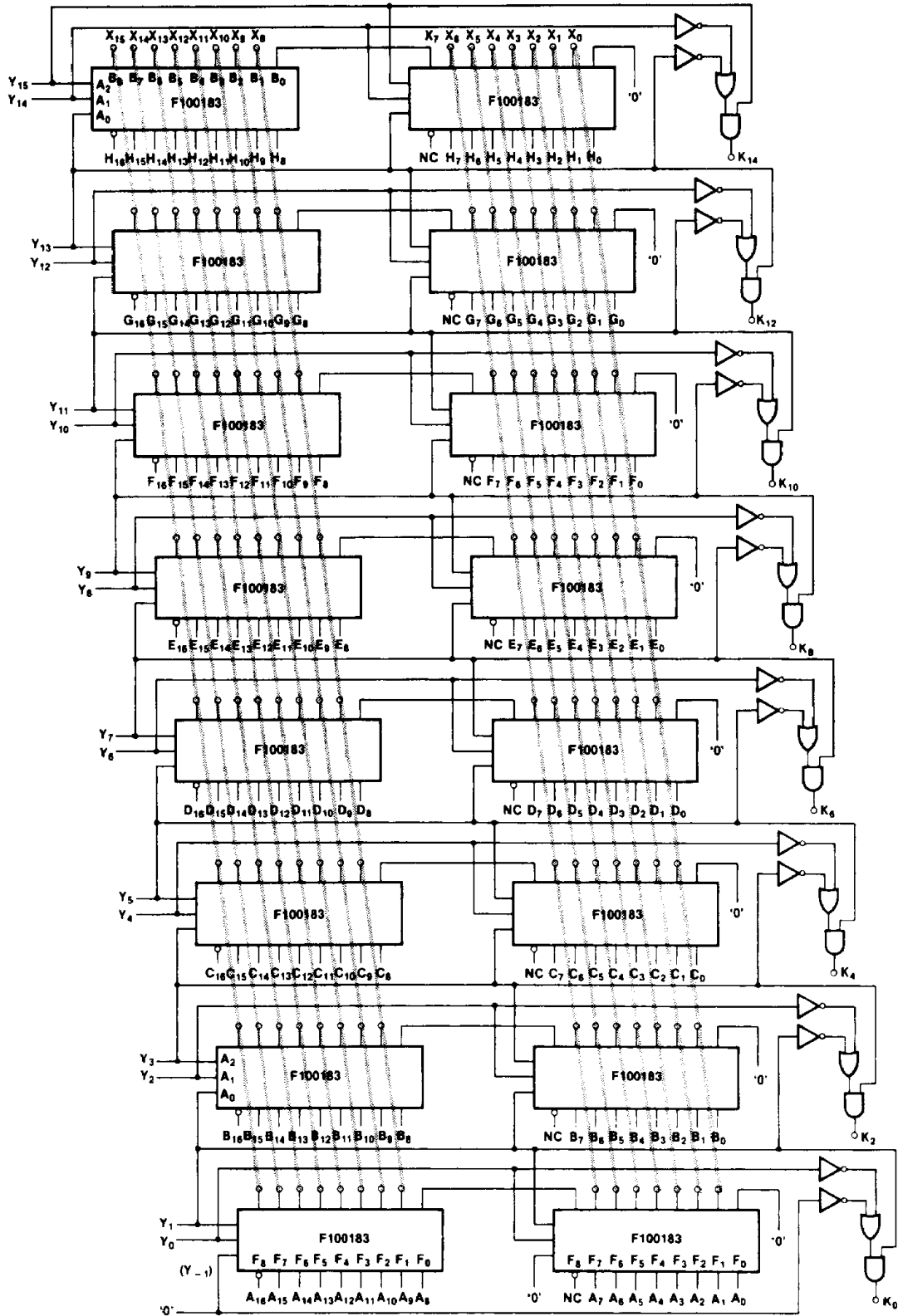
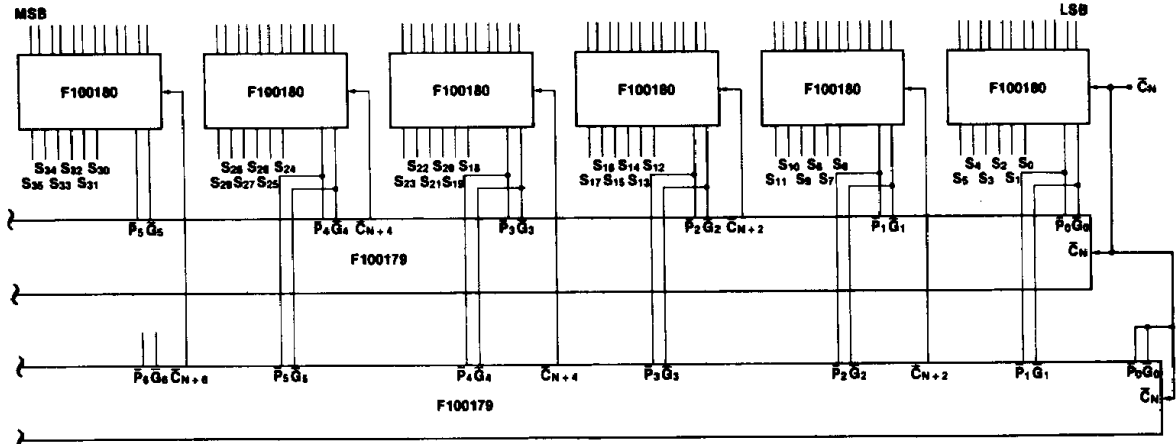


FIGURE 7. F100183 Hook-up for 16 x 16 Multiplier

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Hardware Implementation (Continued)



TL/F/9875-13

FIGURE 8. Final Summation for 16 x 16 Multiplier