

# HEF4511B

## BCD to 7-segment latch/decoder/driver

Rev. 7 — 11 November 2011

Product data sheet

## 1. General description

The HEF4511B is a BCD to 7-segment latch/decoder/driver with four address inputs (D0 to D3), an active HIGH latch enable input (LE), an active LOW ripple blanking input (BL), an active LOW lamp test input (LT), and seven active HIGH NPN bipolar transistor segment outputs (Qa to Qg).

When LE is LOW and BL is HIGH, the state of the segment outputs (Qa to Qg) is determined by the data on D0 to D3. When LE goes HIGH, the last data present on D0 to D3 is stored in the latches and the segment outputs remain unchanged. When LT is LOW, all of the segment outputs are HIGH independent of all other input conditions. With LT HIGH, a LOW on BL forces all segment outputs LOW. The inputs LT and BL do not affect the latch circuit.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

## 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

## 3. Ordering information

**Table 1. Ordering information**

All types operate from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Type number	Package		
	Name	Description	Version
HEF4511BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4511BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



#### 4. Functional diagram

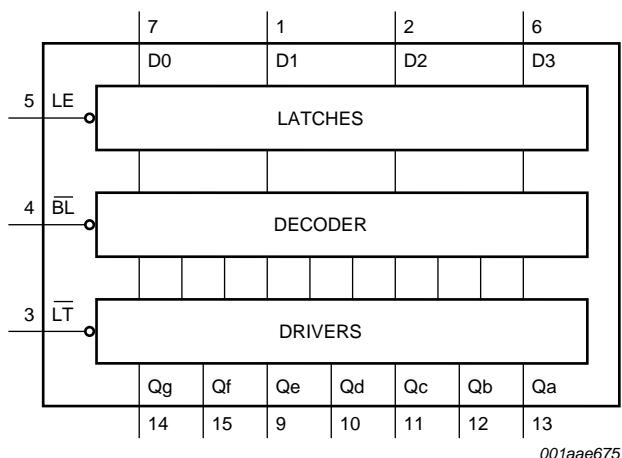


Fig 1. Functional diagram

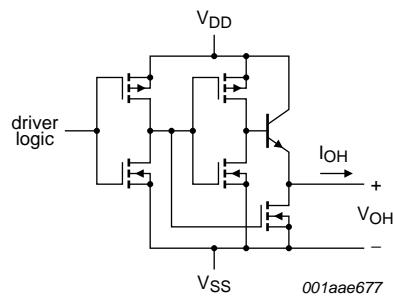
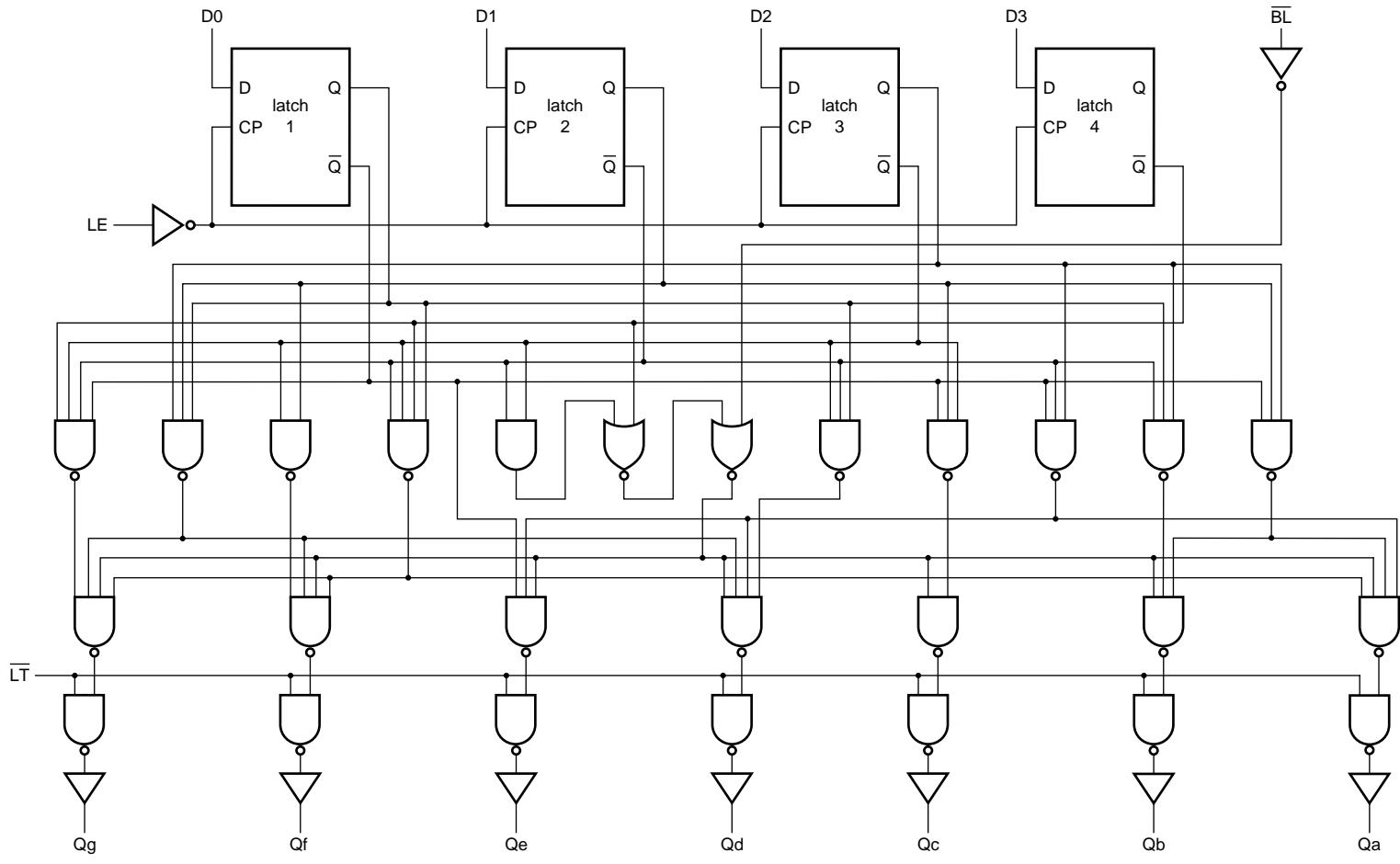


Fig 2. Schematic diagram of output stage

Fig 3. Logic diagram



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## 5. Pinning information

### 5.1 Pinning

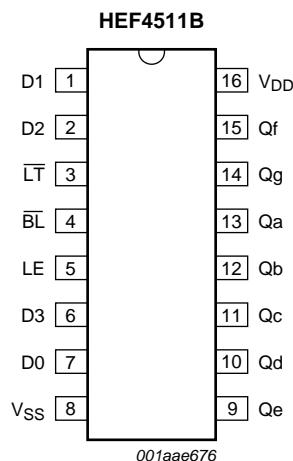


Fig 4. Pin configuration DIP16 and SO16

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
LT	3	lamp test input (active LOW)
BL	4	ripple blanking input (active LOW)
LE	5	latch enable input (active HIGH)
D0 to D3	7, 1, 2, 6	address (data) input
V <sub>SS</sub>	8	ground supply voltage
Qa to Qg	13, 12, 11, 10, 9, 15, 14	segment output
V <sub>DD</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs							Outputs								Display
LE	BL	LT	D3	D2	D1	D0	Qa	Qb	Qc	Qd	Qe	Qf	Qg		
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8	
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank	
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0	
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1	
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2	
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3	
L	H	H	L	H	L	L	H	H	H	L	L	H	H	4	
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5	
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6	
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7	
L	H	H	H	L	L	H	H	H	H	H	H	H	H	8	
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9	
L	H	H	H	L	H	X	L	L	L	L	L	L	L	blank	
L	H	H	H	H	X	X	L	L	L	L	L	L	L	blank	
H	H	H	X	X	X	X	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; N.C. = no change.

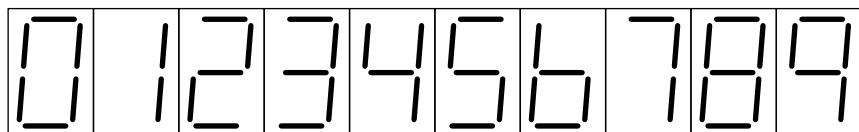


Fig 5. Seven segment digital display with segment designation

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{DD} + 0.5 \text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{DD} + 0.5 \text{ V}$	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{OH}$	HIGH-level output current		[1] -25	-	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = 125 \text{ °C}$			
		DIP16 package	[2] -	750	mW
		SO16 package	[3] -	500	mW
$P$	power dissipation	per output	-	100	mW

[1] A destructive high current mode may occur if  $V_I$  and  $V_O$  are not constrained to the range  $V_{SS} \leq V_I \leq V_O \leq V_{DD}$ .

[2] For DIP16 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[3] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5 \text{ V}$	-	-	3.75	μs/V
		$V_{DD} = 10 \text{ V}$	-	-	0.5	μs/V
		$V_{DD} = 15 \text{ V}$	-	-	0.08	μs/V

## 9. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0 \text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40 \text{ }^{\circ}\text{C}$		$T_{amb} = +25 \text{ }^{\circ}\text{C}$		$T_{amb} = +85 \text{ }^{\circ}\text{C}$		$T_{amb} = +125 \text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1 \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1 \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	see <a href="#">Table 7</a>	-	-	-	-	-	-	-	-	-	-
$V_{OL}$	LOW-level output voltage	$ I_O  < 1 \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5 \text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6 \text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5 \text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5 \text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4 \text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5 \text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5 \text{ V}$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.1$	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0 \text{ A}$	5 V	-	5	-	5	-	150	-	150	$\mu\text{A}$
			10 V	-	10	-	10	-	300	-	300	$\mu\text{A}$
			15 V	-	20	-	20	-	600	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

**Table 7. Static characteristics for  $V_{OH}$**  $V_{SS} = 0 \text{ V}$ 

Symbol	Parameter	$I_{OH}$	$V_{DD}$	$T_{amb} = -40 \text{ }^{\circ}\text{C}$		$T_{amb} = +25 \text{ }^{\circ}\text{C}$		$T_{amb} = +85 \text{ }^{\circ}\text{C}$		$T_{amb} = +125 \text{ }^{\circ}\text{C}$		Unit
		mA	V	Min	Min	Typ	Min	Min	Min	Min		
$V_{OH}$	HIGH-level output voltage	0	5 V	4.10	4.10	4.40	4.10	4.10	4.10	4.10	V	
			10 V	9.10	9.10	9.90	9.10	9.10	9.10	9.10	V	
			15 V	14.10	14.10	14.40	14.10	14.10	14.10	14.10	V	
		5	5 V	-	-	4.30	-	-	-	-	V	
			10 V	-	-	9.30	-	-	-	-	V	
			15 V	-	-	14.30	-	-	-	-	V	
		10	5 V	3.60	3.60	4.25	3.30	3.20	3.20	3.20	V	
			10 V	8.75	8.75	9.25	8.45	8.35	8.35	8.35	V	
			15 V	13.75	13.75	14.30	13.45	13.35	13.35	13.35	V	
		15	5 V	-	-	4.20	-	-	-	-	V	
			10 V	-	-	9.20	-	-	-	-	V	
			15 V	-	-	14.20	-	-	-	-	V	
		20	5 V	2.80	2.80	4.20	2.50	2.30	2.30	2.30	V	
			10 V	8.10	8.10	9.20	7.80	7.60	7.60	7.60	V	
			15 V	13.10	13.10	14.20	12.80	12.60	12.60	12.60	V	
		25	5 V	-	-	4.15	-	-	-	-	V	
			10 V	-	-	9.20	-	-	-	-	V	
			15 V	-	-	14.20	-	-	-	-	V	

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics** $V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ }^{\circ}\text{C}$ ; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	Dn $\rightarrow$ Qn; see <a href="#">Figure 6</a>	5 V	$128 \text{ ns} + (0.55 \text{ ns/pF})C_L$	-	155	310	ns
			10 V	$49 \text{ ns} + (0.23 \text{ ns/pF})C_L$	-	60	120	ns
			15 V	$32 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	40	80	ns
	LE $\rightarrow$ Qn; see <a href="#">Figure 6</a>		5 V	$133 \text{ ns} + (0.55 \text{ ns/pF})C_L$	-	160	320	ns
			10 V	$49 \text{ ns} + (0.23 \text{ ns/pF})C_L$	-	60	120	ns
			15 V	$37 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	45	90	ns
	BL $\rightarrow$ Qn; see <a href="#">Figure 6</a>		5 V	$93 \text{ ns} + (0.55 \text{ ns/pF})C_L$	-	120	240	ns
			10 V	$39 \text{ ns} + (0.23 \text{ ns/pF})C_L$	-	50	100	ns
			15 V	$27 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	35	70	ns
	$\overline{LT} \rightarrow$ Qn; see <a href="#">Figure 6</a>		5 V	$52 \text{ ns} + (0.55 \text{ ns/pF})C_L$	-	80	160	ns
			10 V	$19 \text{ ns} + (0.23 \text{ ns/pF})C_L$	-	30	60	ns
			15 V	$12 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	20	40	ns

**Table 8. Dynamic characteristics ...continued** $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ ; for test circuit see [Figure 8](#).

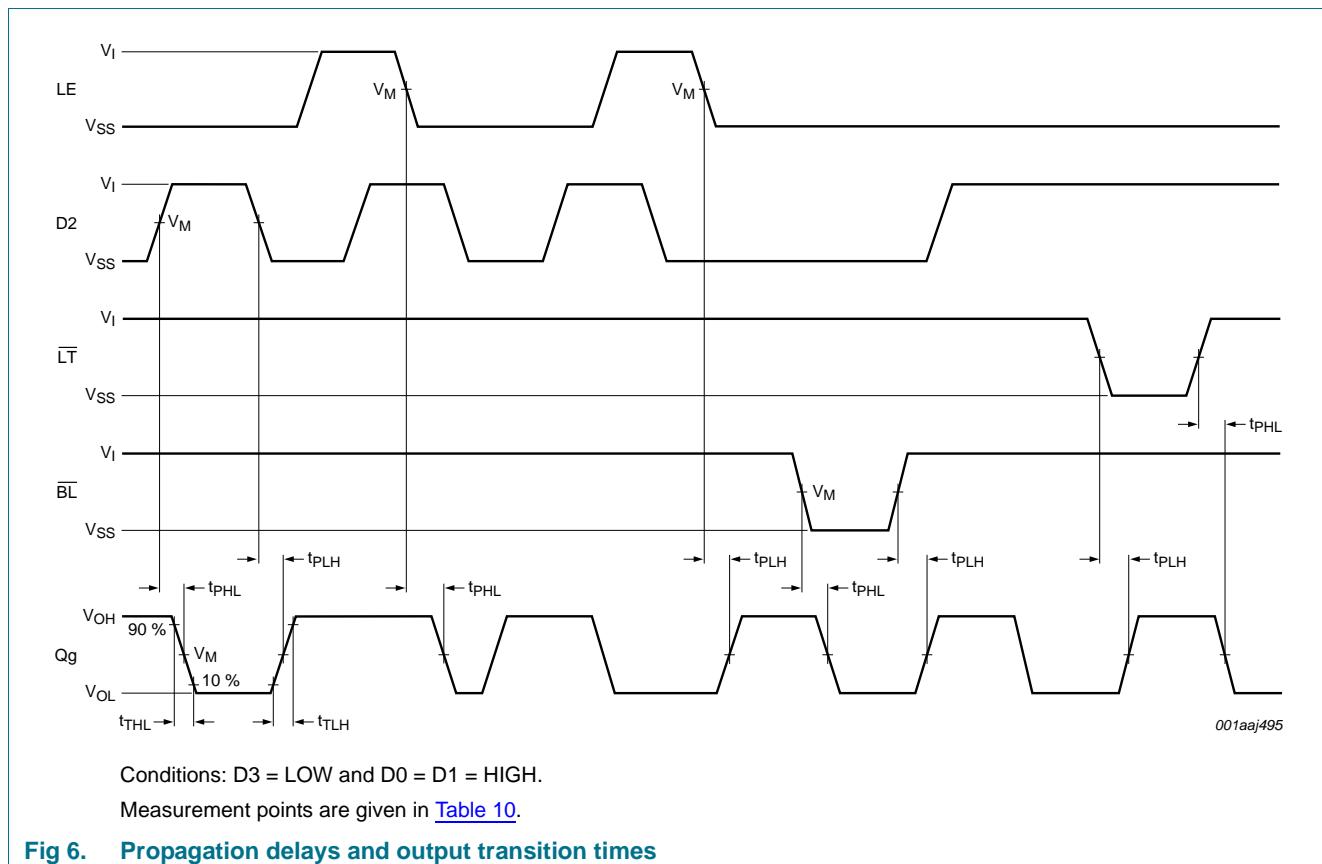
Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{PLH}$	LOW to HIGH propagation delay	Dn $\rightarrow$ Qn; see <a href="#">Figure 6</a>	5 V	$108 \text{ ns} + (0.55 \text{ ns/pF})C_L$	-	135	270	ns
			10 V	$44 \text{ ns} + (0.23 \text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	40	80	ns
	LE $\rightarrow$ Qn; see <a href="#">Figure 6</a>		5 V	$133 \text{ ns} + (0.55 \text{ ns/pF})C_L$	-	160	320	ns
			10 V	$59 \text{ ns} + (0.23 \text{ ns/pF})C_L$	-	70	140	ns
			15 V	$42 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	50	100	ns
	$\overline{BL} \rightarrow Qn$ ; see <a href="#">Figure 6</a>		5 V	$78 \text{ ns} + (0.55 \text{ ns/pF})C_L$	-	105	210	ns
			10 V	$29 \text{ ns} + (0.23 \text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	30	60	ns
	$\overline{LT} \rightarrow Qn$ ; see <a href="#">Figure 6</a>		5 V	$33 \text{ ns} + (0.55 \text{ ns/pF})C_L$	-	60	120	ns
			10 V	$19 \text{ ns} + (0.23 \text{ ns/pF})C_L$	-	30	60	ns
			15 V	$17 \text{ ns} + (0.16 \text{ ns/pF})C_L$	-	25	50	ns
$t_{THL}$	HIGH to LOW output transition time	see <a href="#">Figure 6</a>	5 V	$10 \text{ ns} + (1.00 \text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9 \text{ ns} + (0.42 \text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6 \text{ ns} + (0.28 \text{ ns/pF})C_L$	-	20	40	ns
$t_{TLH}$	LOW to HIGH output transition time	see <a href="#">Figure 6</a>	5 V	$20 \text{ ns} + (1.00 \text{ ns/pF})C_L$	-	25	50	ns
			10 V	$13 \text{ ns} + (0.06 \text{ ns/pF})C_L$	-	16	32	ns
			15 V	$10 \text{ ns} + (0.06 \text{ ns/pF})C_L$	-	13	26	ns
$t_{su}$	set-up time	Dn $\rightarrow$ LE; see <a href="#">Figure 7</a>	5 V		50	25	-	ns
			10 V		25	12	-	ns
			15 V		20	9	-	ns
$t_h$	hold time	Dn $\rightarrow$ LE; see <a href="#">Figure 7</a>	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		25	12	-	ns
$t_w$	pulse width	LE input LOW; minimum width; see <a href="#">Figure 7</a>	5 V		80	40	-	ns
			10 V		40	20	-	ns
			15 V		35	17	-	ns

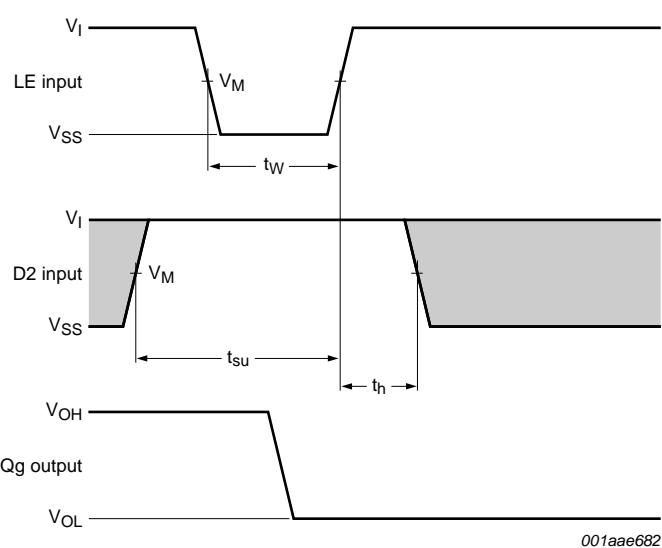
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

**Table 9. Dynamic power dissipation  $P_D$**  $P_D$  can be calculated from the formulas shown.  $V_{SS} = 0 \text{ V}$ ;  $t_r = t_f \leq 20 \text{ ns}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz;
		10 V	$P_D = 4000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_o$ = output frequency in MHz;
		15 V	$P_D = 10000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs.

## 11. Waveforms



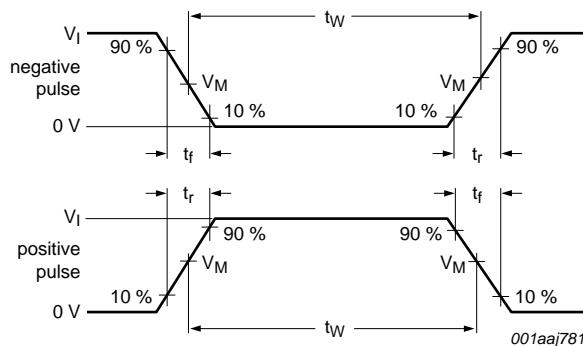


The shaded area indicates where the input is permitted to change for predictable output performance.

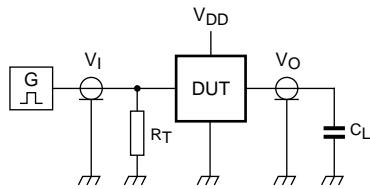
Conditions: D3 = LOW and D0 = D1 =  $\overline{BL} = \overline{LT}$  = HIGH.

Measurement points are given in [Table 10](#).

**Fig 7. Waveforms showing minimum LE pulse width, set-up, and hold time for Dn to LE**



a. Input waveforms



b. Test circuit

Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

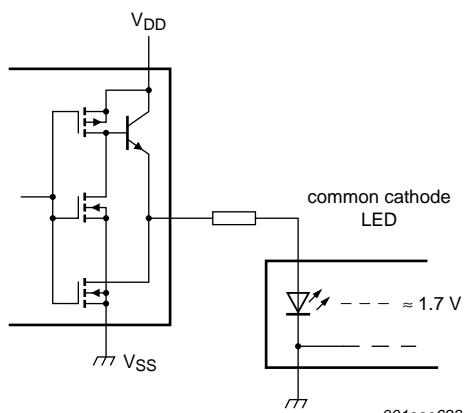
Fig 8. Test circuit for measuring switching times

Table 10. Measurement points and test data

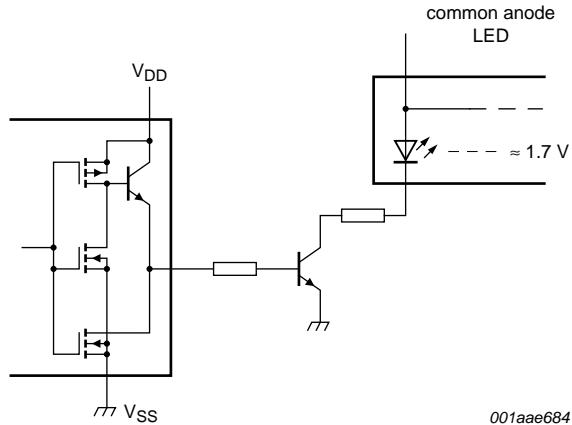
Supply voltage	Input			Load
	$V_I$	$V_M$	$t_r, t_f$	
5 V to 15 V	$V_{DD}$	$0.5V_I$	$\leq 20$ ns	50 pF

## 12. Application information

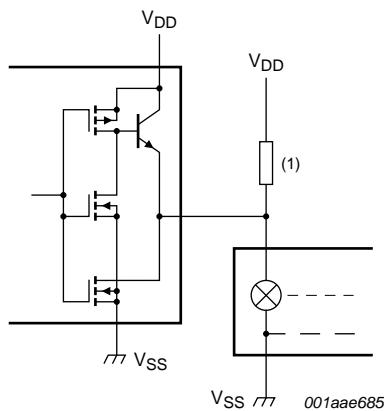
- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays



**Fig 9. Connection to common cathode LED display readout**

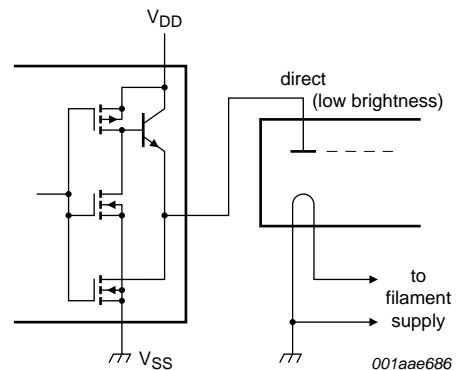


**Fig 10. Connection to common anode LED display readout**

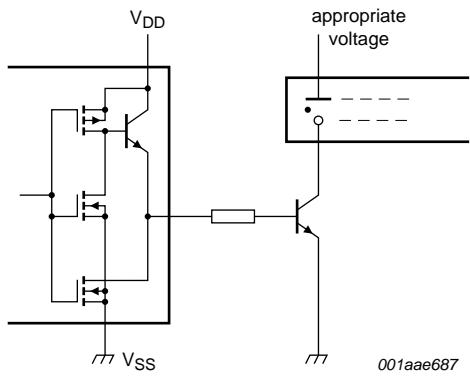


(1) A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

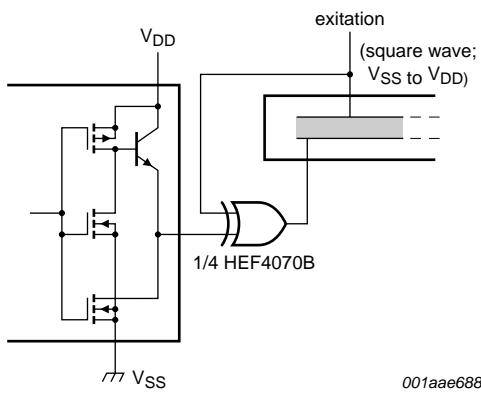
**Fig 11. Connection to incandescent display readout**



**Fig 12. Connection to fluorescent display readout**



**Fig 13. Connection to gas discharge display readout**



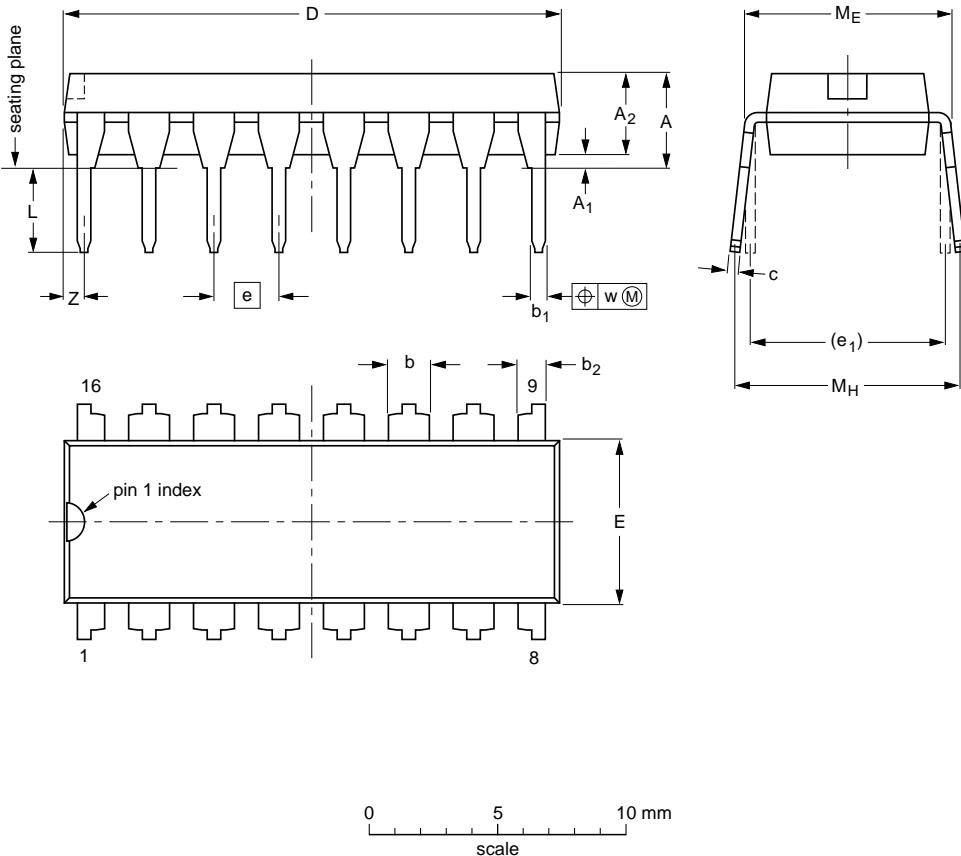
**Fig 14. Connection to LCD readout**

Direct DC drive of LCDs not recommended for life of LCD readouts.

## 13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

### Note

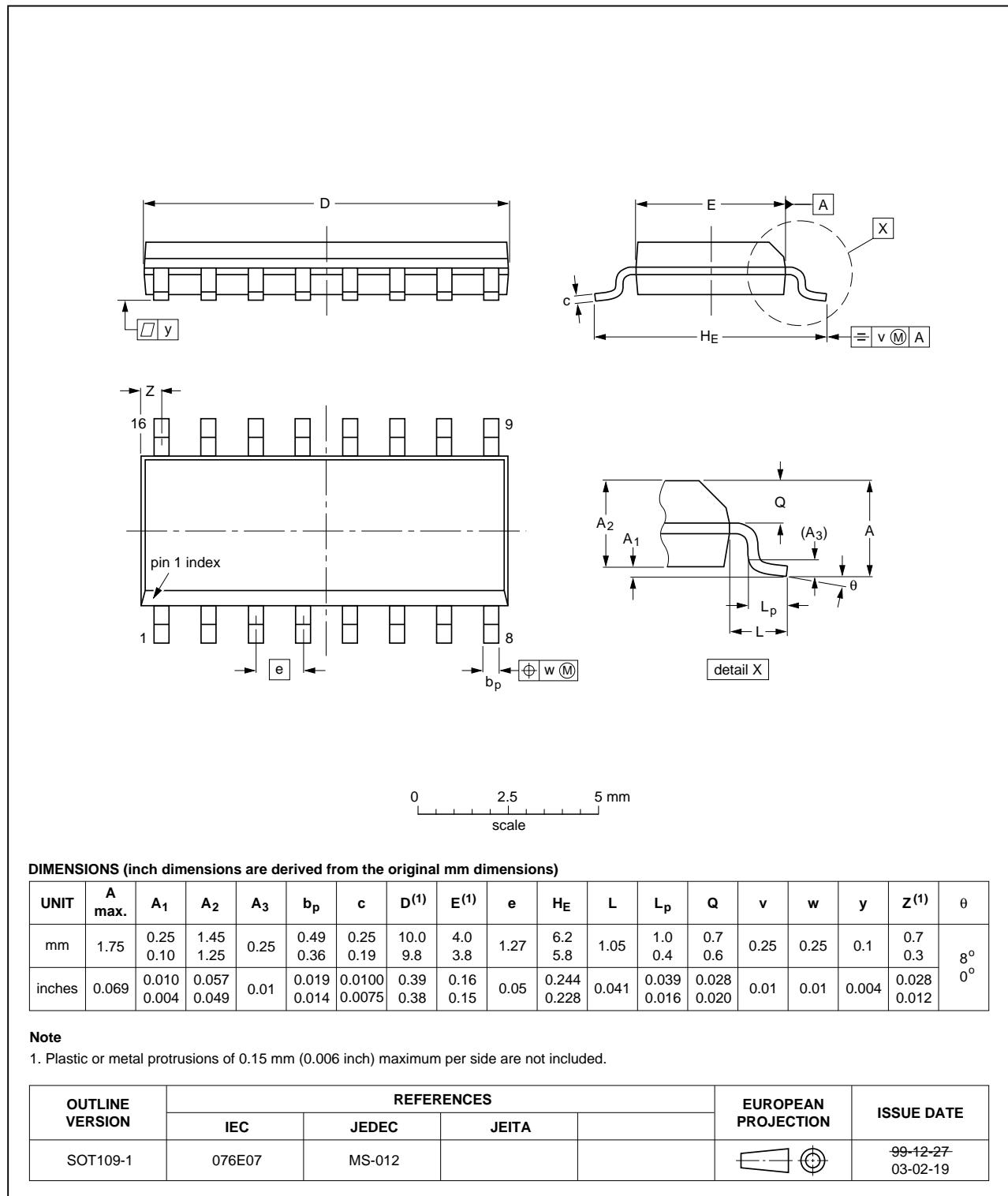
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 15. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



## DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

## Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 16. Package outline SOT109-1 (SO16)

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4511B v.7	20111111	Product data sheet	-	HEF4511B v.6
Modifications:		<ul style="list-style-type: none"><li>Section Applications removed</li><li>• <a href="#">Table 6</a>: <math>I_{OH}</math> minimum values changed to maximum</li></ul>		
HEF4511B v.6	20091207	Product data sheet	-	HEF4511B v.5
HEF4511B v.5	20090813	Product data sheet	-	HEF4511B v.4
HEF4511B v.4	20090305	Product data sheet	-	HEF4511B_CNV v.3
HEF4511B_CNV v.3	19950101	Product specification	-	HEF4511B_CNV v.2
HEF4511B_CNV v.2	19950101	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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