

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40373B

MSI

Octal transparent latch with 3-state outputs

Product specification
File under Integrated Circuits, IC04

January 1995

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DESCRIPTION

The HEF40373B is an 8-bit transparent latch with 3-state buffered outputs. The output stages have high current output capability suitable for driving highly capacitive loads. The latch outputs follow the data inputs when the latch enable (E) is HIGH. When E is LOW, the data that meets the set-up times is latched. The 3-state outputs are controlled by the output enable input $\overline{EO}$. A HIGH on

$\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device features hysteresis on the E input to improve noise rejection. Schmitt-trigger action in the E input makes the circuit highly tolerant to slower input rise and fall times.

The HEF40373B is pin and functionally compatible with the TTL '373' device.

Supply voltage range: 3 to 15 V.

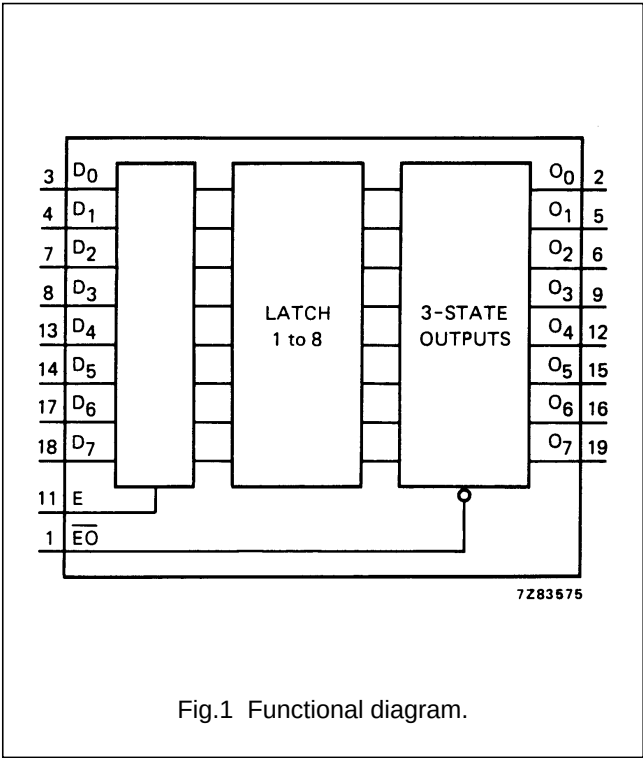


Fig.1 Functional diagram.

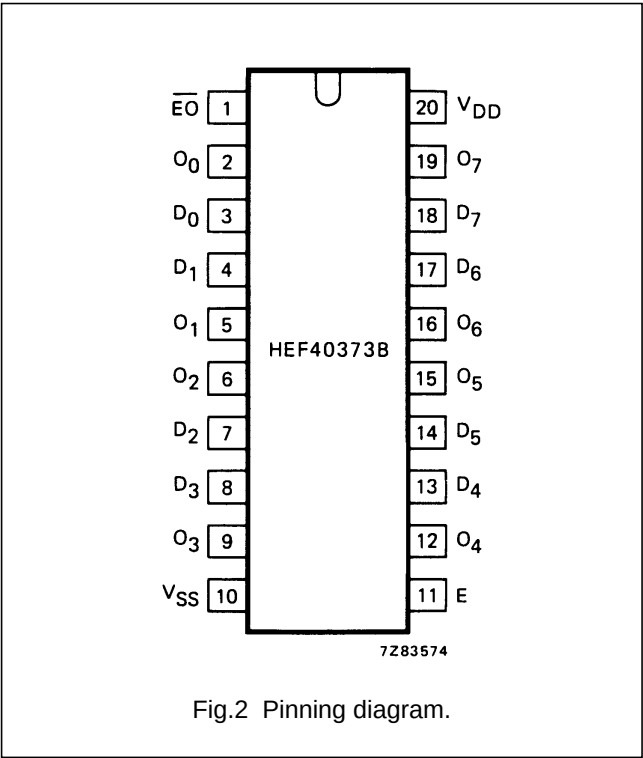


Fig.2 Pinning diagram.

- HEF40373BP(N): 20-lead DIL; plastic (SOT146-1)
- HEF40373BD(F): 20-lead DIL; ceramic (cerdip) (SOT152)
- HEF40373BT(D): 20-lead SO; plastic (SOT163-1)
- (): Package Designator North America

PINNING

- D₀ to D₇ data inputs
- E latch enable input
- $\overline{EO}$ output enable input (active LOW)
- O₀ to O₇ 3-state buffered outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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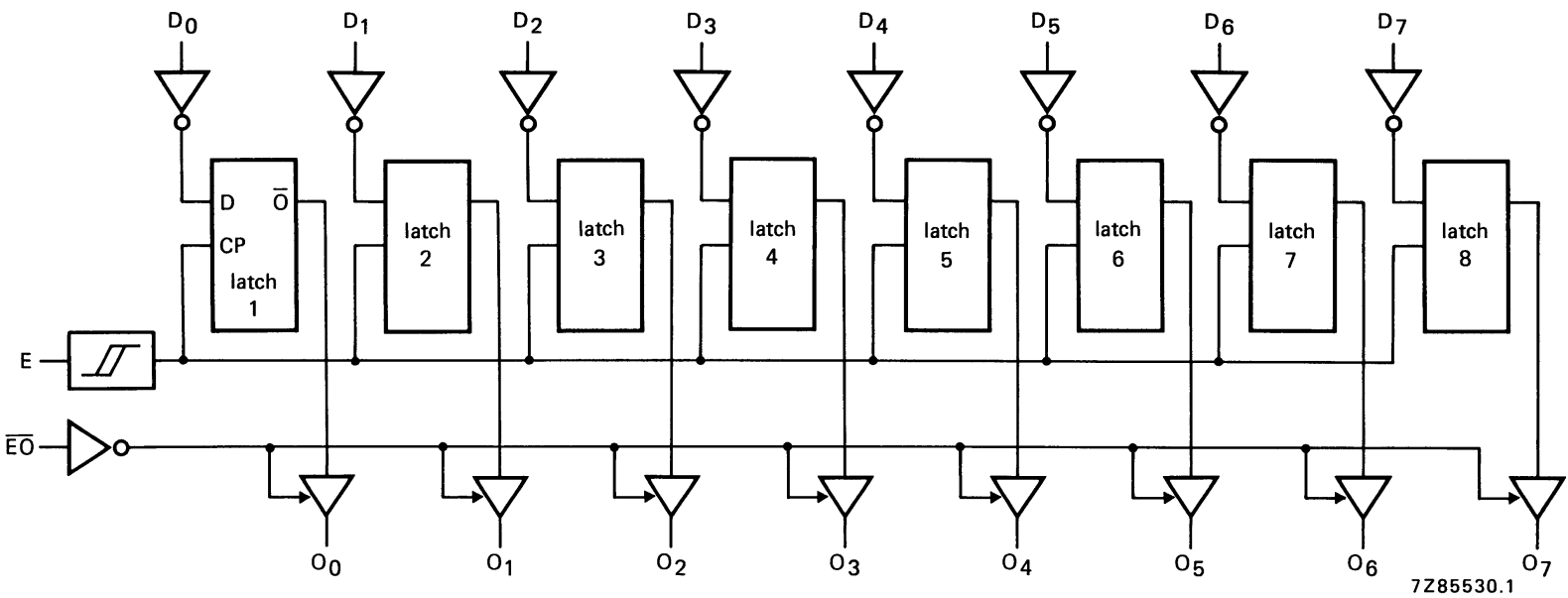


Fig.3 Logic diagram.

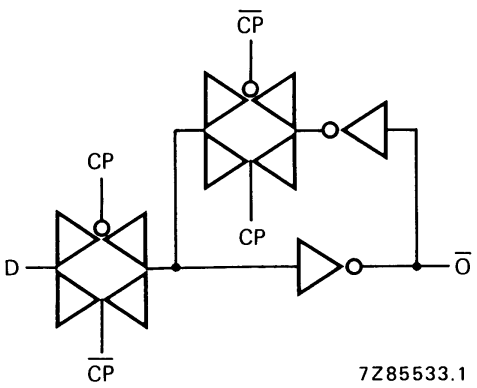


Fig.4 Logic diagram (one latch).

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FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS O ₀ TO O ₇
	$\overline{EO}$	E	D _n		
enable & read register	L	H	L	L	L
	L	H	H	H	H
latch & read register	L	L	l	L	L
	L	L	h	H	H
latch register & disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Notes

- H = HIGH state (the more positive voltage)
 h = HIGH state (one set-up time prior to the HIGH-to-LOW enable transition)
 L = LOW state (the less positive voltage)
 l = LOW state (one set-up time prior to the HIGH-to-LOW enable transition)
 Z = high impedance OFF-state

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RATINGS

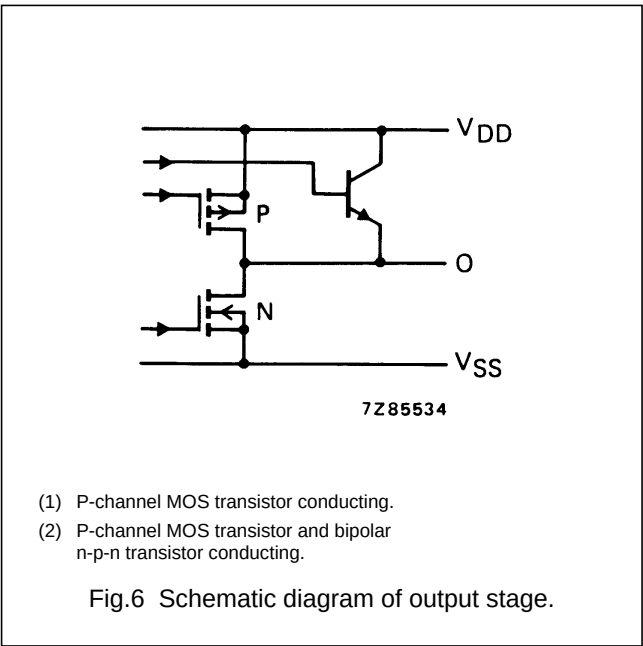
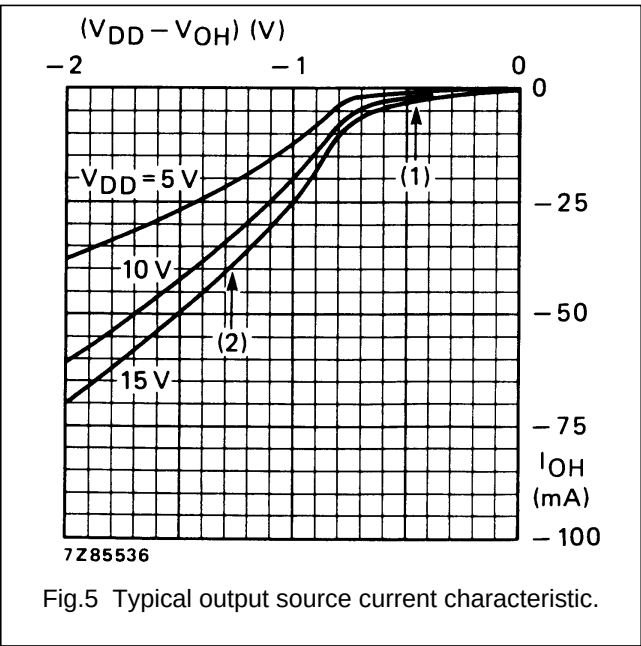
Limiting values in accordance with the Absolute Maximum System (IEC 134)
See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10	mA
D.C. source or sink current into any output	$\pm I_O$	max.	25	mA
D.C. current into the supply terminals	$\pm I$	max.	100	mA

DC CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	T_{amb} (°C)					
					-40		+25		+85	
					MIN.	TYP.	MIN.	TYP.	MIN.	TYP.
Output current HIGH	5	4,6		$-I_{OH}$	0,75	0,6	1,2	0,45	mA	
	10	9,5			1,85	1,5	3,0	1,1	mA	
	15	13,5			14,5	15	50	15,5	mA	
Output current HIGH	5	3,6		$-I_{OH}$	9,3	10	24	10,7	mA	
	10	8,4			14,4	15	46	15,0	mA	
	15	13,2			19,5	20	62	19,8	mA	
Output current LOW	5		0,4	I_{OL}	2,9	2,3	5,4	1,75	mA	
	10		0,5		9,5	7,6	17	5,50	mA	
	15		1,5		30,0	25	45	19,0	mA	
Hysteresis voltage at enable input (E)	5			V_H	220				mV	
	10				250				mV	
	15				320				mV	



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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays							
E → O _n	5			150	300	ns	138 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		60	120	ns	59 ns + (0,01 ns/pF) C _L
	15			40	80	ns	36 ns + (0,07 ns/pF) C _L
E → O _n	5			125	250	ns	122 ns + (0,06 ns/pF) C _L
LOW to HIGH	10	t _{PLH}		50	100	ns	48 ns + (0,03 ns/pF) C _L
	15			40	80	ns	39 ns + (0,02 ns/pF) C _L
Output transition times	5			40	80	ns	see Fig.7
HIGH to LOW	10	t _{THL}		20	40	ns	
	15			15	30	ns	
LOW to HIGH	5			30	60	ns	
	10	t _{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO} \rightarrow O_n$	5			65	130	ns	
HIGH	10	t _{PHZ}		30	60	ns	
	15			25	50	ns	
LOW	5			75	150	ns	
	10	t _{PLZ}		40	80	ns	
	15			30	60	ns	
Output enable times							
$\overline{EO} \rightarrow O_n$	5			65	130	ns	
HIGH	10	t _{PZH}		30	60	ns	
	15			25	50	ns	
LOW	5			85	170	ns	
	10	t _{PZL}		35	70	ns	
	15			25	50	ns	
Set-up time	5		15	7		ns	
D _n → E	10	t _{su}	10	5		ns	
	15		10	5		ns	
Hold time	5		25	15		ns	
D _n → E	10	t _{hold}	15	4		ns	
	15		10	3		ns	
Minimum latch enable pulse width LOW	5		60	30		ns	
	10	t _{WEL}	30	15		ns	
	15		20	10		ns	

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AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	3 325 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	14 200 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	37 425 f _i + ∑ (f _o C _L) × V _{DD} ²	

