

HEF40193B

4-bit up/down binary counter

Rev. 8 — 18 November 2011

Product data sheet

1. General description

The HEF40193B is a 4-bit synchronous up/down binary counter. The counter has a count-up clock input (CPU), a count-down clock input (CPD), an asynchronous parallel load input (\overline{PL}), four parallel data inputs (D0 to D3), an asynchronous master reset input (MR), four counter outputs (Q0 to Q3), an active LOW terminal count-up (carry) output (\overline{TCU}), and an active LOW terminal count-down (borrow) output (\overline{TCD}).

The counter outputs change state on the LOW-to-HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. The outputs \overline{TCU} and \overline{TCD} are normally HIGH. When the circuit has reached the maximum count state of '15', the next HIGH-to-LOW transition of CPU will cause \overline{TCU} to go LOW. \overline{TCU} will stay LOW until CPU goes HIGH again. Likewise, output \overline{TCD} will go LOW when the circuit is in the zero state and CPD goes LOW. When \overline{PL} is LOW, the information on D0 to D3 is asynchronously loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Package		Version
	Name	Description	
HEF40193BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF40193BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



4. Functional diagram

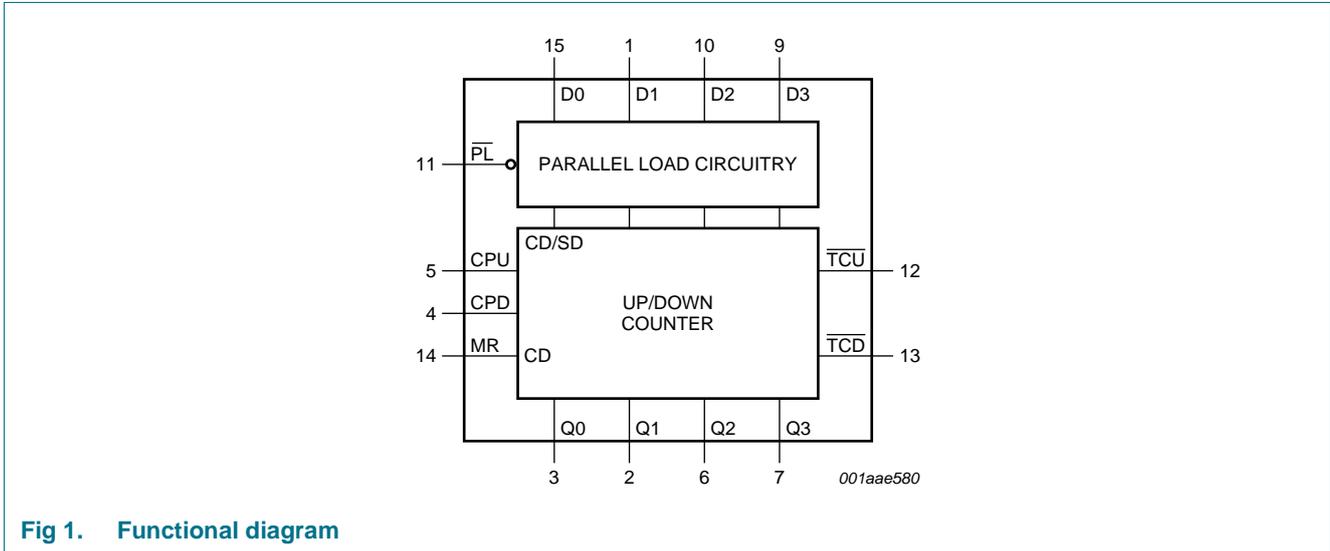
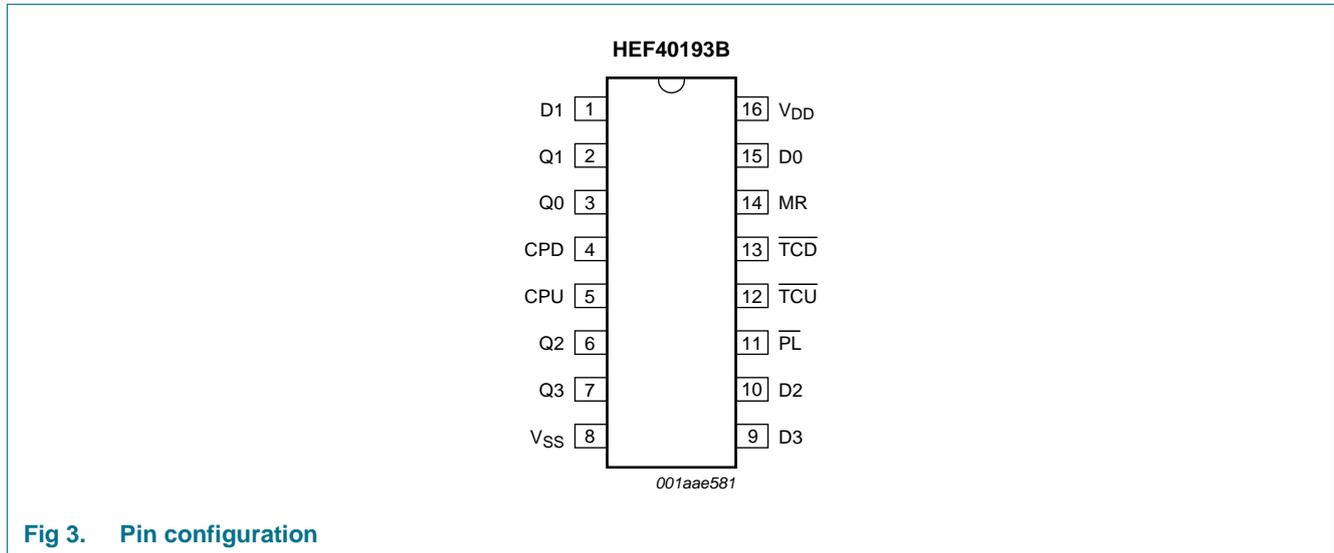


Fig 1. Functional diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
D0 to D3	15, 1, 10, 9	parallel data input
CPU	5	count-up clock pulse input (LOW-to-HIGH, edge-triggered)
CPD	4	count-down clock pulse input (LOW-to-HIGH, edge-triggered)
$\overline{\text{PL}}$	11	parallel load input (active LOW)
MR	14	master reset input (asynchronous)
Q0 to Q3	3, 2, 6, 7	buffered counter output
$\overline{\text{TCU}}$	12	buffered terminal count-up (carry) output (active LOW)
$\overline{\text{TCD}}$	13	buffered terminal count-down (borrow) output (active LOW)
V _{DD}	16	supply voltage
V _{SS}	8	ground supply voltage

6. Functional description

Table 3. Function table [1]

MR	$\overline{\text{PL}}$	CPU	CPD	Mode
H	X	X	X	reset (asynchronous)
L	L	X	X	parallel load
L	H	↑	H	count-up
L	H	H	↑	count-down

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition.

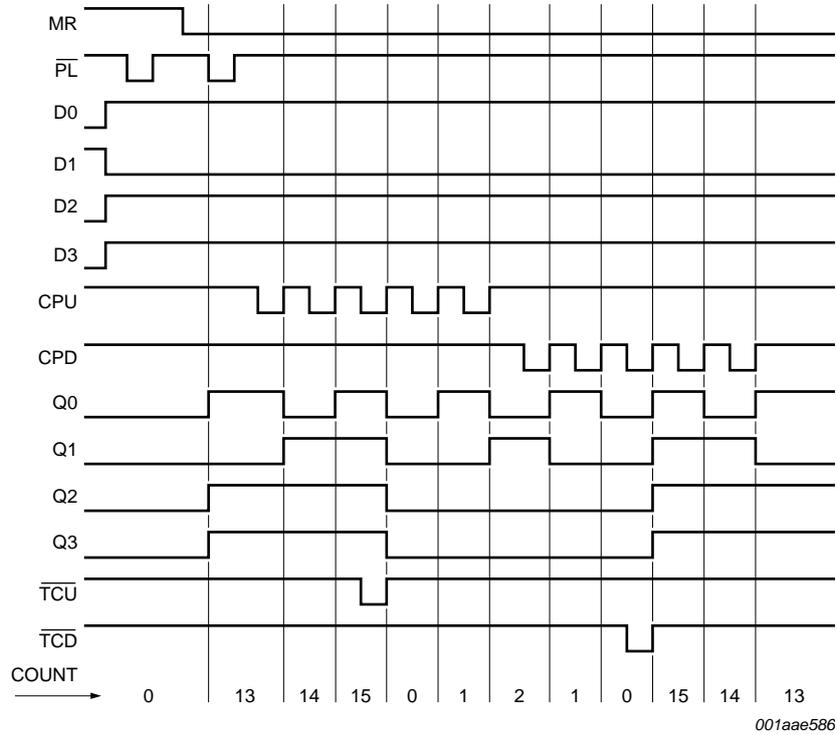


Fig 4. Timing diagram

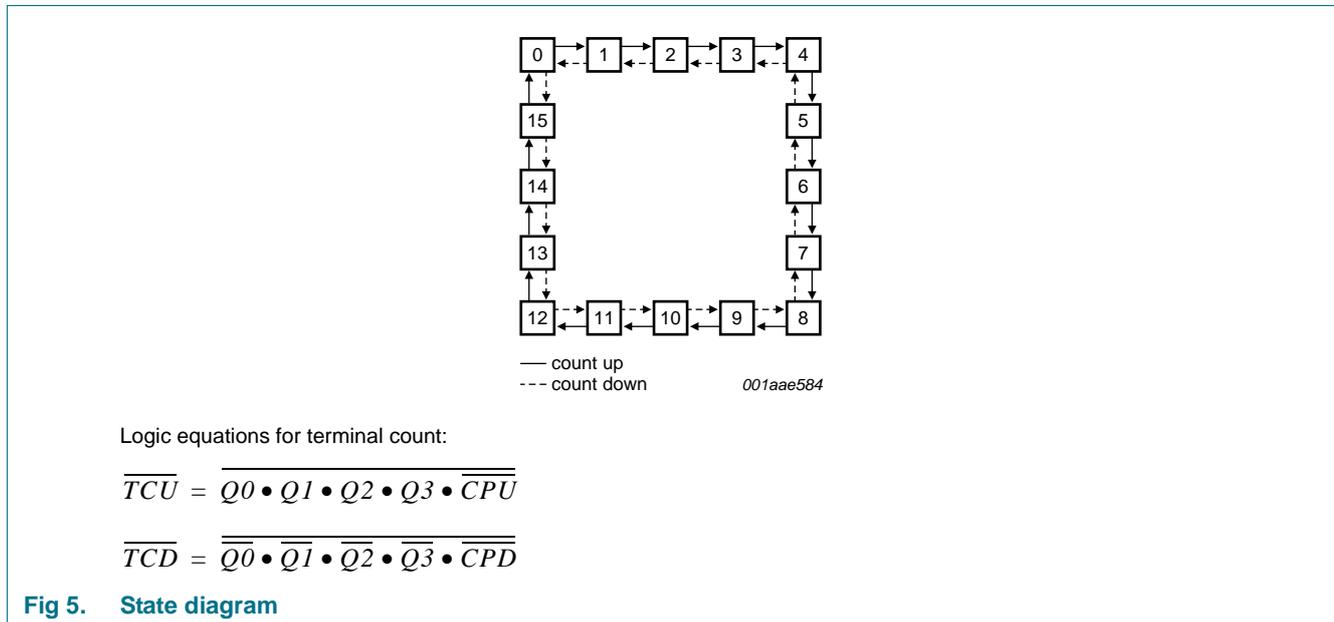


Fig 5. State diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	DIP16 package	[1] -	750	mW
		SO16 package	[2] -	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	supply voltage		3	-	15	V
V _I	input voltage		0	-	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C

Table 5. Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{\text{amb}} = -40\text{ }^\circ\text{C}$		$T_{\text{amb}} = 25\text{ }^\circ\text{C}$		$T_{\text{amb}} = 85\text{ }^\circ\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.3	-	± 0.3	-	± 1.0	μA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	CPU to Qn; see Figure 6	5 V	183 ns + (0.55 ns/pF)C _L	-	210	415	ns
			10 V	74 ns + (0.23 ns/pF)C _L	-	85	165	ns
			15 V	52 ns + (0.16 ns/pF)C _L	-	60	120	ns
	CPD to Qn; see Figure 6	5 V	183 ns + (0.55 ns/pF)C _L	-	210	425	ns	
		10 V	74 ns + (0.23 ns/pF)C _L	-	85	170	ns	
		15 V	57 ns + (0.16 ns/pF)C _L	-	60	125	ns	
	CPU to $\overline{\text{TCU}}$; see Figure 6	5 V	98 ns + (0.55 ns/pF)C _L	-	125	250	ns	
		10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns	
		15 V	27 ns + (0.16 ns/pF)C _L	-	35	70	ns	
	CPD to $\overline{\text{TCD}}$; see Figure 6	5 V	113 ns + (0.55 ns/pF)C _L	-	140	280	ns	
		10 V	44 ns + (0.23 ns/pF)C _L	-	55	110	ns	
		15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns	
	MR to Qn; see Figure 6	5 V	168 ns + (0.55 ns/pF)C _L	-	195	390	ns	
		10 V	69 ns + (0.23 ns/pF)C _L	-	80	160	ns	
		15 V	52 ns + (0.16 ns/pF)C _L	-	60	120	ns	
	MR to $\overline{\text{TCD}}$	5 V	338 ns + (0.55 ns/pF)C _L	-	365	730	ns	
		10 V	119 ns + (0.23 ns/pF)C _L	-	130	265	ns	
		15 V	92 ns + (0.16 ns/pF)C _L	-	100	205	ns	
	$\overline{\text{PL}} \rightarrow \text{Qn}$	5 V	158 ns + (0.55 ns/pF)C _L	-	185	360	ns	
		10 V	64 ns + (0.23 ns/pF)C _L	-	75	150	ns	
		15 V	47 ns + (0.16 ns/pF)C _L	-	55	110	ns	

Table 7. Dynamic characteristics ...continued $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t _{PLH}	LOW to HIGH propagation delay	CPU to Qn; see Figure 6	5 V	143 ns + (0.55 ns/pF)C _L	-	170	340	ns
			10 V	59 ns + (0.23 ns/pF)C _L	-	70	140	ns
			15 V	42 ns + (0.16 ns/pF)C _L	-	50	100	ns
		CPD to Qn; see Figure 6	5 V	143 ns + (0.55 ns/pF)C _L	-	170	340	ns
			10 V	59 ns + (0.23 ns/pF)C _L	-	70	140	ns
			15 V	42 ns + (0.16 ns/pF)C _L	-	50	100	ns
		CPU to $\overline{\text{TCU}}$; see Figure 6	5 V	68 ns + (0.55 ns/pF)C _L	-	95	185	ns
			10 V	29 ns + (0.23 ns/pF)C _L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C _L	-	30	60	ns
		CPD to $\overline{\text{TCD}}$; see Figure 6	5 V	73 ns + (0.55 ns/pF)C _L	-	100	195	ns
			10 V	29 ns + (0.23 ns/pF)C _L	-	40	85	ns
			15 V	22 ns + (0.16 ns/pF)C _L	-	30	65	ns
		MR to $\overline{\text{TCU}}$	5 V	118 ns + (0.55 ns/pF)C _L	-	145	285	ns
			10 V	49 ns + (0.23 ns/pF)C _L	-	60	115	ns
			15 V	37 ns + (0.16 ns/pF)C _L	-	45	90	ns
$\overline{\text{PL}}$ to Qn	5 V	118 ns + (0.55 ns/pF)C _L	-	145	290	ns		
	10 V	49 ns + (0.23 ns/pF)C _L	-	60	120	ns		
	15 V	37 ns + (0.16 ns/pF)C _L	-	45	90	ns		
t _t	transition time	see Figure 6	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
f _{max}	maximum frequency	see Figure 6	5 V		2.5	5	-	MHz
			10 V		7	14	-	MHz
			15 V		9	18	-	MHz
t _w	pulse width	CPU or CPD LOW; minimum width; see Figure 6	5 V		150	75	-	ns
			10 V		50	25	-	ns
			15 V		35	20	-	ns
		MR input HIGH; minimum width; see Figure 6	5 V		180	90	-	ns
			10 V		70	35	-	ns
			15 V		60	30	-	ns
		$\overline{\text{PL}}$ input LOW; minimum width; see Figure 6	5 V		120	60	-	ns
			10 V		45	20	-	ns
			15 V		30	15	-	ns
t _{rec}	recovery time	MR input; see Figure 6	5 V		125	65	-	ns
			10 V		70	35	-	ns
			15 V		50	25	-	ns
		$\overline{\text{PL}}$ input see Figure 6	5 V		90	45	-	ns
			10 V		35	15	-	ns
			15 V		25	10	-	ns

Table 7. Dynamic characteristics ...continued

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t _{su}	set-up time	Dn to \overline{PL} ; see Figure 6	5 V		160	80	-	ns
			10 V		60	30	-	ns
			15 V		50	25	-	ns
t _h	hold time	Dn to \overline{PL} ; see Figure 6	5 V		+10	-70	-	ns
			10 V		+5	-25	-	ns
			15 V		+5	-20	-	ns

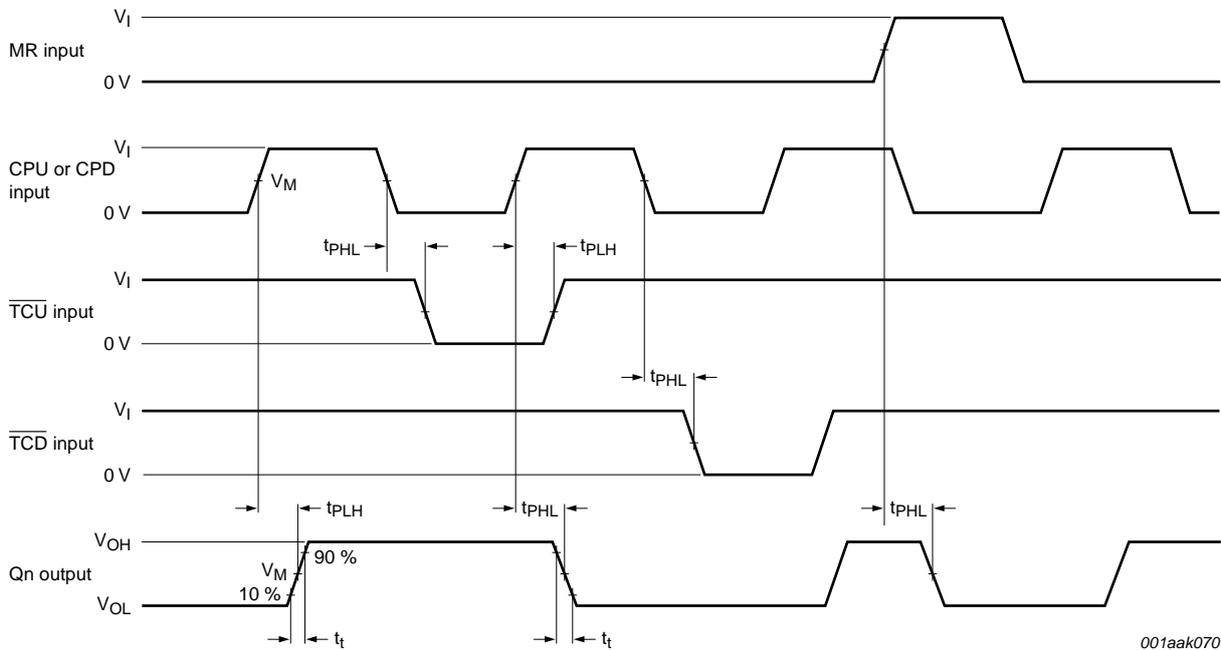
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

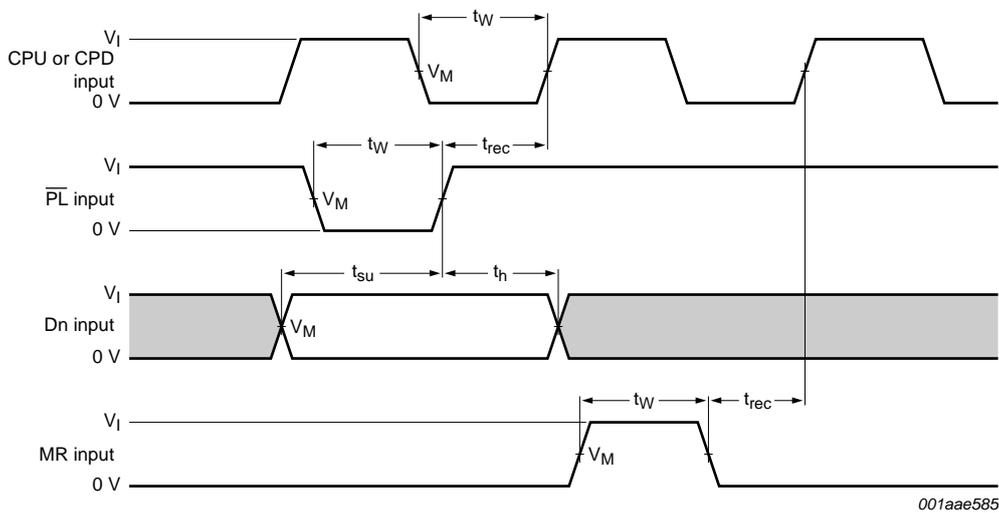
P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 2700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 7500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.

11. Waveforms



a. Propagation delays and output transition times



b. \overline{PL} and MR recovery times, CPU, CPD, \overline{PL} and MR minimum pulse widths, and Dn to \overline{PL} set-up and hold times

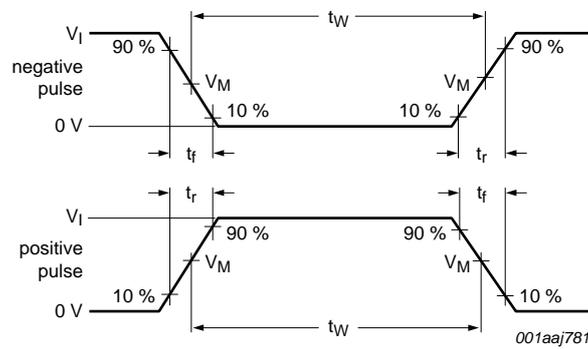
V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.

Set-up and hold times are shown as positive values but may be specified as negative values.

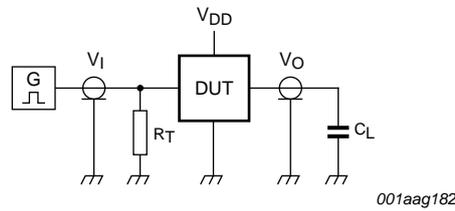
The shaded area is where the data can change for predictable performance.

Measurement points are given in [Table 9](#).

Fig 6. Waveforms showing switching times



a. Input waveforms



b. Test circuit

Test data is given in [Table 9](#).

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 7. Test circuit for switching times

Table 9. Measurement points and test data

Supply voltage	Input			Load
	V_I	V_M	t_r, t_f	C_L
5 V to 15 V	V_{DD}	$0.5V_I$	≤ 20 ns	50 pF

12. Application information

Some examples of applications for the HEF40193B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage synchronous counting

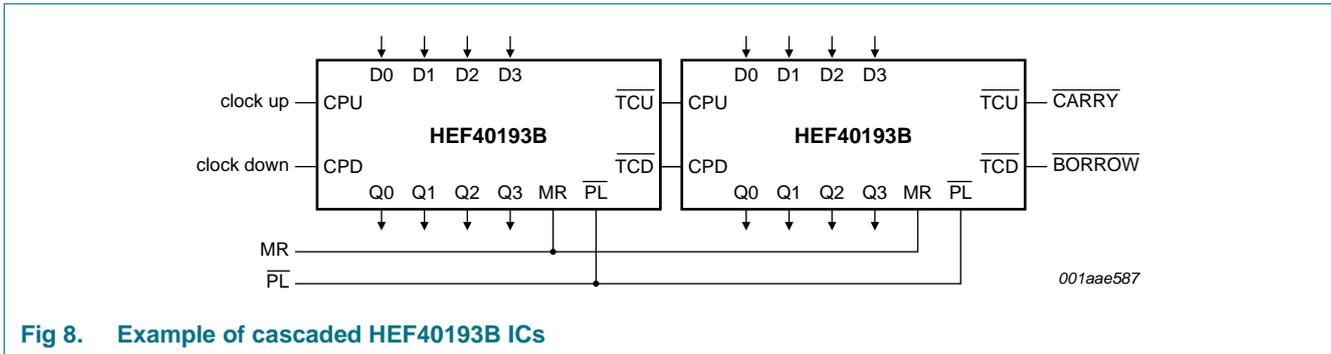


Fig 8. Example of cascaded HEF40193B ICs

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

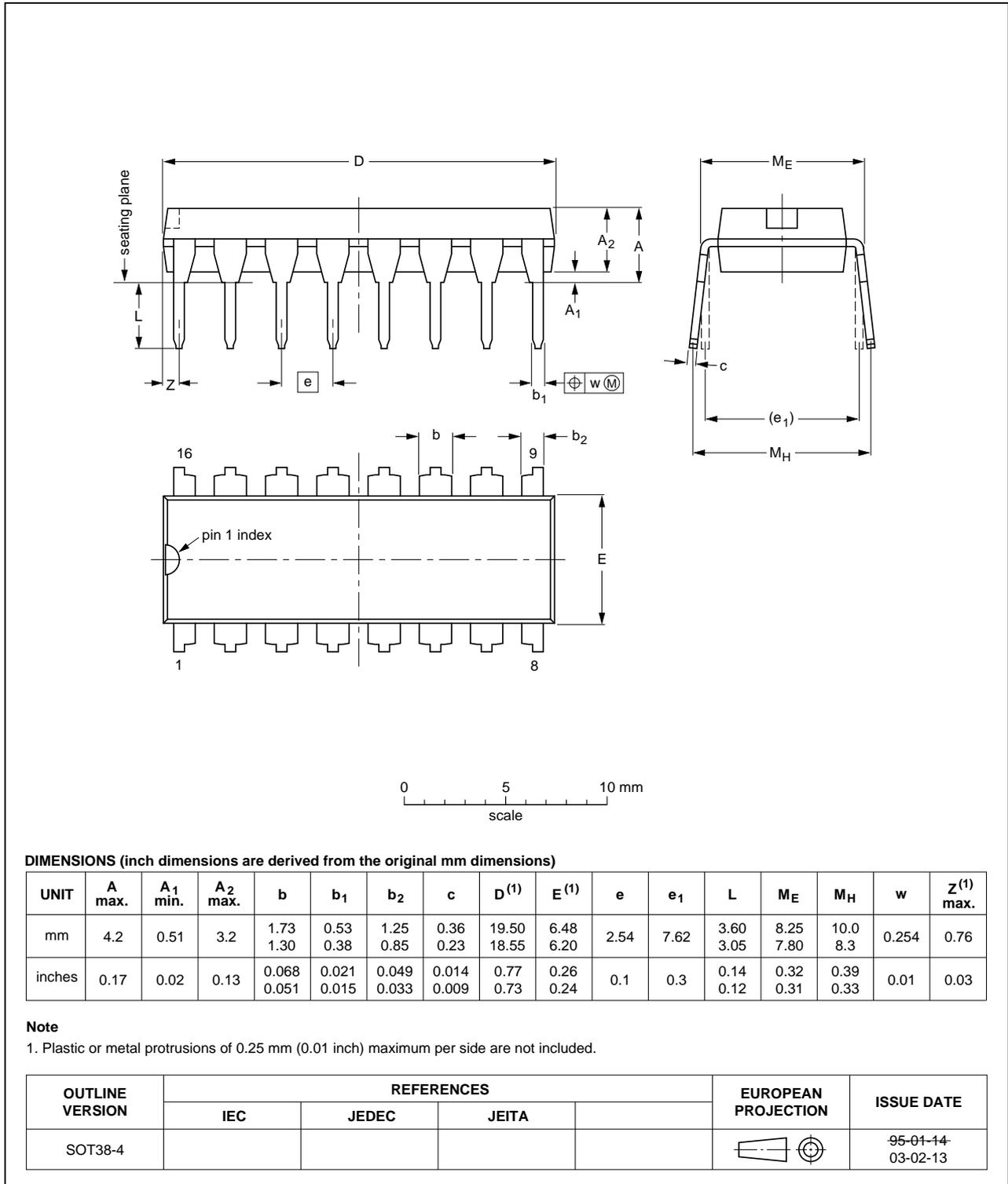


Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

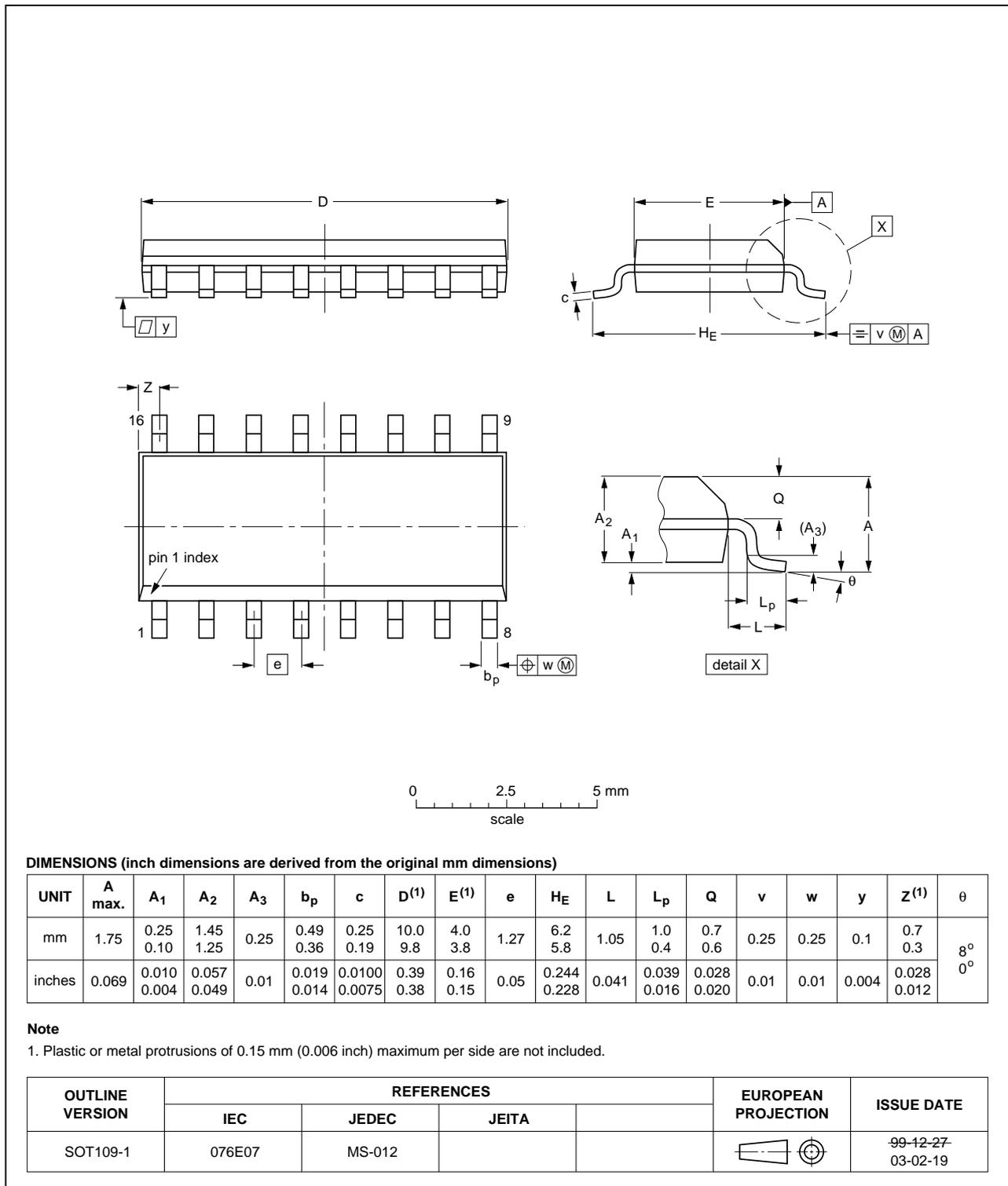


Fig 10. Package outline SOT109-1 (SO16)

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40193B v.8	20111118	Product data sheet	-	HEF40193B v.7
Modifications:	<ul style="list-style-type: none">• Legal pages updated.• Changes in “General description” and “Features and benefits”.• Section “Applications” removed.			
HEF40193B v.7	20110914	Product data sheet	-	HEF40193B v.6
HEF40193B v.6	20091222	Product data sheet	-	HEF40193B v.5
HEF40193B v.5	20090615	Product data sheet	-	HEF40193B v.4
HEF40193B v.4	20090505	Product data sheet	-	HEF40193B_CNV v.3
HEF40193B_CNV v.3	19950101	Product specification	-	HEF40193B_CNV v.2
HEF40193B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
7	Limiting values	6
8	Recommended operating conditions	6
9	Static characteristics	7
10	Dynamic characteristics	8
11	Waveforms	11
12	Application information	13
13	Package outline	14
14	Revision history	16
15	Legal information	17
15.1	Data sheet status	17
15.2	Definitions	17
15.3	Disclaimers	17
15.4	Trademarks	18
16	Contact information	18
17	Contents	19

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 18 November 2011

Document identifier: HEF40193B