74LVC646A

Octal bus transceiver/register; 3-state

Rev. 04 — 29 June 2004 **Product data sheet**

1. General description

The 74LVC646A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

The 74LVC646A consists of non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the A or B bus will be clocked in the internal registers, as the appropriate clock (CPAB or CPBA) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at high-impedance port may be stored in either the A or B register, or in both. With the select source inputs (SAB and SBA) stored and real-time (transparent mode) data can be multiplexed. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), A data may be stored in the B register and/or B data may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses A or B may be driven at a time.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B/JESD36
- CMOS low-power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Supports partial power-down applications; inputs/outputs are high-impedance when V_{CC} = 0 V
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay An, Bn to Bn, An	C_L = 50 pF; V_{CC} = 3.3 V		-	3.0	-	ns
f_{max}	maximum clock frequency	C_L = 50 pF; V_{CC} = 3.3 V		-	250	-	MHz
C_I	input capacitance			-	5.0	-	pF
$C_{I/O}$	input/output capacitance			-	10.0	-	pF
C_{PD}	power dissipation capacitance per latch	V_{CC} = 3.3 V; outputs enabled	[1] [2]	-	15	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC646AD	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC646ADB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC646APW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram

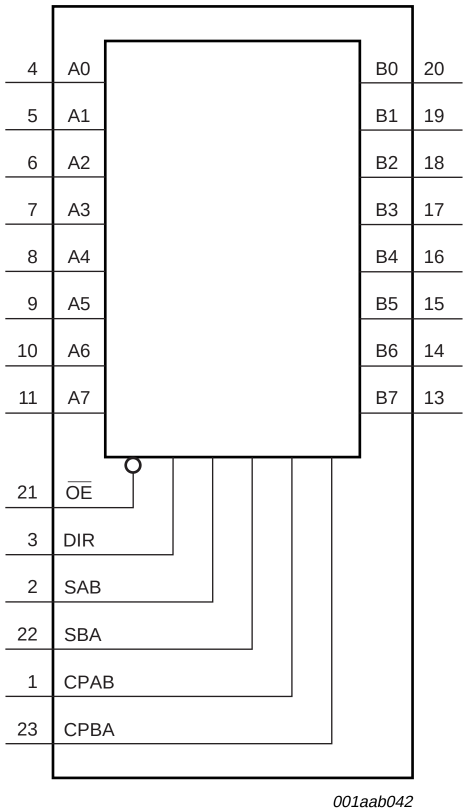


Fig 1. Functional diagram.

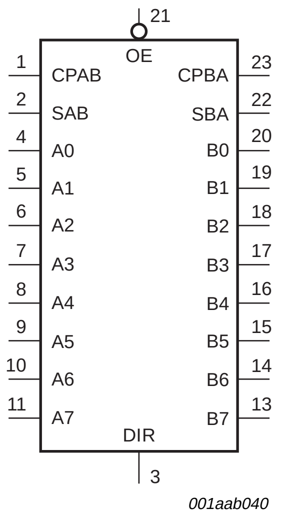


Fig 2. Logic symbol.

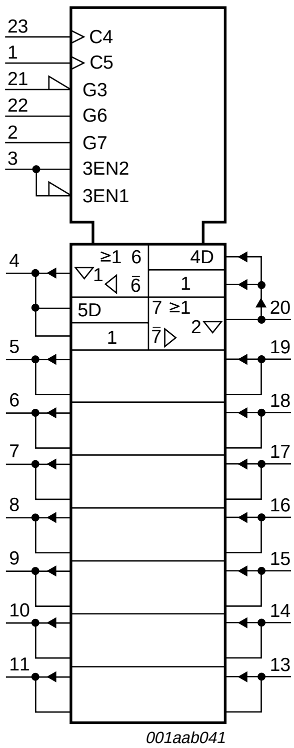


Fig 3. IEC logic symbol.

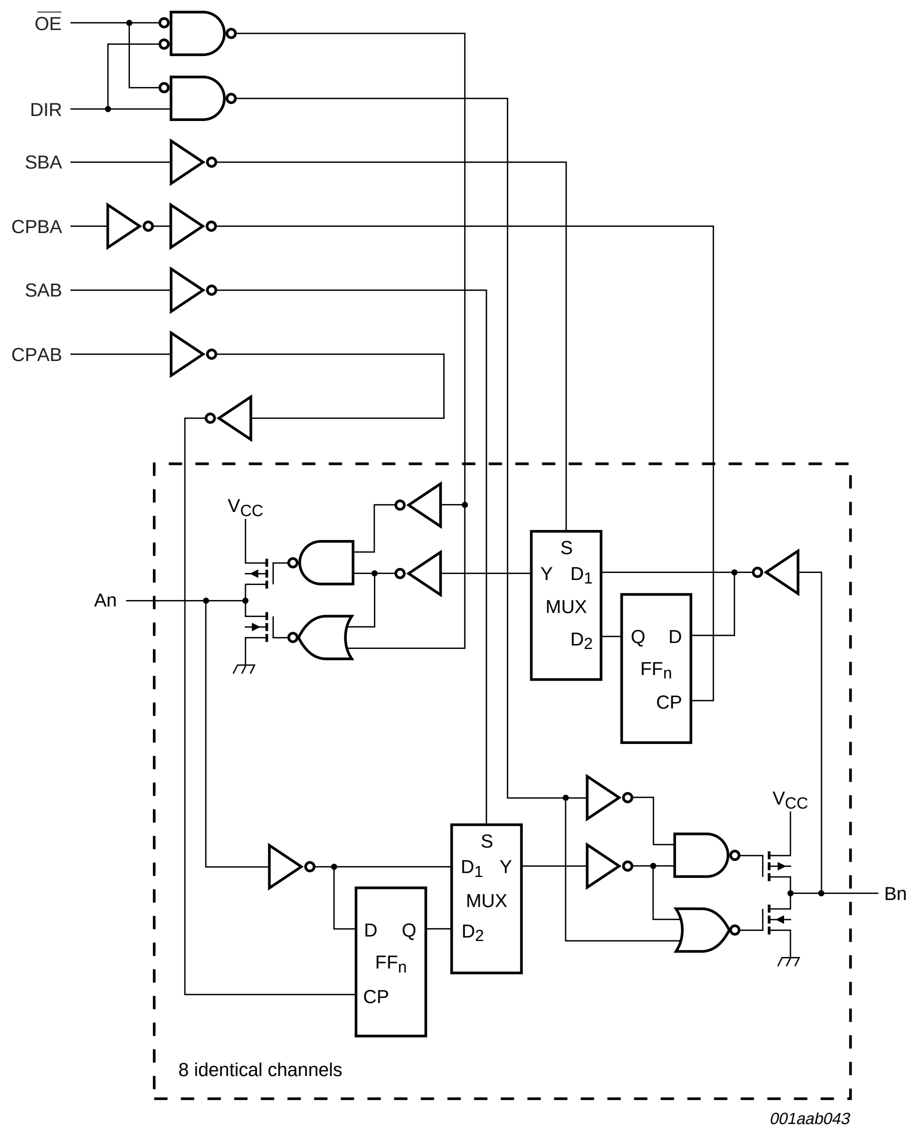


Fig 4. Logic diagram.

6. Pinning information

6.1 Pinning

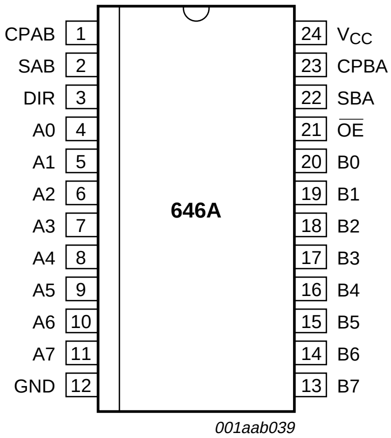


Fig 5. Pin configuration.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CPAB	1	A to B clock input (LOW-to-HIGH; edge-triggered)
SAB	2	A to B select source input
DIR	3	direction control input
A0	4	A data input/output
A1	5	A data input/output
A2	6	A data input/output
A3	7	A data input/output
A4	8	A data input/output
A5	9	A data input/output
A6	10	A data input/output
A7	11	A data input/output
GND	12	ground (0 V)
B7	13	B data input/output
B6	14	B data input/output
B5	15	B data input/output
B4	16	B data input/output
B3	17	B data input/output
B2	18	B data input/output
B1	19	B data input/output
B0	20	B data input/output
$\overline{OE}$	21	output enable input (active LOW)

Table 3: Pin description *…continued*

Symbol	Pin	Description
SBA	22	B to A select source input
CPBA	23	B to A clock input (LOW-to-HIGH, edge-triggered)
V_{CC}	24	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Input						Data I/O		Function
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A0 to A7	B0 to B7	
X	X	↑	X	X	X	input	un [2]	store A and B unspecified
X	X	X	↑	X	X	un [2]	input	store B and A unspecified
H	X	↑	↑	X	X	input	input	store A and B data
H	X	H or L	H or L	X	X	input	input	hold storage; isolation
L	L	X	X	X	L	output	input	real-time B data to A bus
L	L	X	H or L	X	H	output	input	stored B data to A bus
L	H	X	X	L	X	input	output	real-time A data to B bus
L	H	H or L	X	H	X	input	output	stored A data to B bus

[1] un = unspecified;
H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH level transition.

[2] The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e. data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

8. Limiting values

Table 5: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[1]	–0.5	V_{CC} + 0.5	V
		output 3-state	[1]	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA

Table 5: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	HIGH or LOW state	0	-	V_{CC}	V
		3-state	0	-	5.5	V
T_{amb}	operating ambient temperature	in free air	–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V		V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V		-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	[2]	V_{CC} – 0.2	V_{CC}	-	V
		I_O = –12 mA; V_{CC} = 2.7 V		V_{CC} – 0.5	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V		V_{CC} – 0.6	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V		V_{CC} – 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	[2]	-	GND	0.2	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.55	V

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V		-	±0.1	±5	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	[3]	-	0.1	±10	µA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V; V_{CC} = 0 V		-	0.1	±10	µA
I_{CC}	quiescent supply current	I_O = 0 A; V_I = V_{CC} or GND; V_{CC} = 3.6 V		-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per pin	I_O = 0 A; V_I = V_{CC} – 0.6 V; V_{CC} = 2.7 V to 3.6 V	[2]	-	5	500	µA
C_I	input capacitance			-	5.0	-	pF
$C_{I/O}$	input/output capacitance			-	10.0	-	pF
T_{amb} = –40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V		V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V		-	-	0	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V		V_{CC} – 0.3	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V		V_{CC} – 0.65	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V		V_{CC} – 0.75	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V		V_{CC} – 1	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V		-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V		-	-	±20	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	[3]	-	-	±20	µA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V; V_{CC} = 0 V		-	-	±20	µA
I_{CC}	quiescent supply current	I_O = 0 A; V_I = V_{CC} or GND; V_{CC} = 3.6 V		-	-	40	µA
ΔI_{CC}	additional quiescent supply current per pin	I_O = 0 A; V_I = V_{CC} – 0.6 V; V_{CC} = 2.7 V to 3.6 V		-	-	5000	µA

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

[3] For transceivers, the parameter I_{OZ} includes the input leakage current.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; see Figure 11 for test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay An, Bn to Bn, An	see Figure 6					
		V_{CC} = 1.2 V		-	17	-	ns
		V_{CC} = 2.7 V		1.5	-	7.8	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.0	6.8	ns
	propagation delay CPAB, CPBA to Bn, An	see Figure 7					
		V_{CC} = 1.2 V		-	19	-	ns
		V_{CC} = 2.7 V		1.5	-	8.6	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.7	7.6	ns
	propagation delay SAB, SBA to Bn, An	see Figure 8					
		V_{CC} = 1.2 V		-	19	-	ns
		V_{CC} = 2.7 V		1.5	-	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.4	8.5	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to An and Bn	see Figure 9					
		V_{CC} = 1.2 V		-	20	-	ns
		V_{CC} = 2.7 V		1.5	-	8.8	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.1	7.8	ns
	3-state output enable time DIR to An and Bn	see Figure 10					
		V_{CC} = 1.2 V		-	20	-	ns
		V_{CC} = 2.7 V		1.5	-	8.9	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.3	7.9	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to An and Bn	see Figure 9					
		V_{CC} = 1.2 V		-	10	-	ns
		V_{CC} = 2.7 V		1.5	-	7.1	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.2	6.1	ns
	3-state output disable time DIR to An and Bn	see Figure 10					
		V_{CC} = 1.2 V		-	10	-	ns
		V_{CC} = 2.7 V		1.5	-	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.0	6.0	ns
t_W	clock pulse width HIGH or LOW of CPAB or CPBA	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		3.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	3.3	1.9	-	ns
t_{su}	set-up time An, Bn to CPAB, CPBA	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.6	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	0.35	-	ns

Table 8: Dynamic characteristics *…continued*

GND = 0 V; see Figure 11 for test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	hold time An, Bn to CPAB, CPBA	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	−0.3	-	ns
f_{max}	maximum clock pulse frequency	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	MHz
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[2]	150	250	-	MHz
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance per latch	V_{CC} = 3.3 V; outputs enabled	[4] [5]	-	15	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay An, Bn to Bn, An	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	10.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	8.0	ns
	propagation delay CPAB, CPBA to Bn, An	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	11.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	9.5	ns
	propagation delay SAB, SBA to Bn, An	see Figure 8					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	12.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	11.0	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to An and Bn	see Figure 9					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	11.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	10.0	ns
	3-state output enable time DIR to An and Bn	see Figure 10					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	11.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	10.0	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to An and Bn	see Figure 9					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	8.0	ns
	3-state output disable time DIR to An and Bn	see Figure 10					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	7.5	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; see Figure 11 for test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_W	clock pulse width HIGH or LOW of CPAB or CPBA	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		3.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		3.3	-	-	ns
t_{su}	set-up time An, Bn to CPAB, CPBA	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.6	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	-	ns
t_h	hold time An, Bn to CPAB, CPBA	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	MHz
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	-	-	MHz
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.5	ns

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

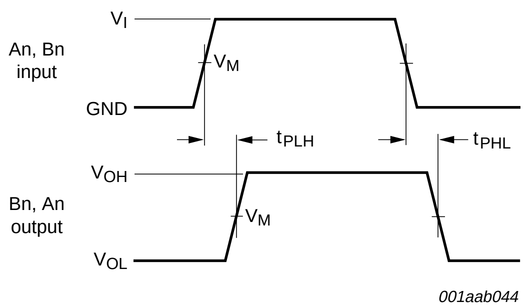
V_{CC} = supply voltage in V;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[5] The condition is V_I = GND to V_{CC}.

12. Waveforms



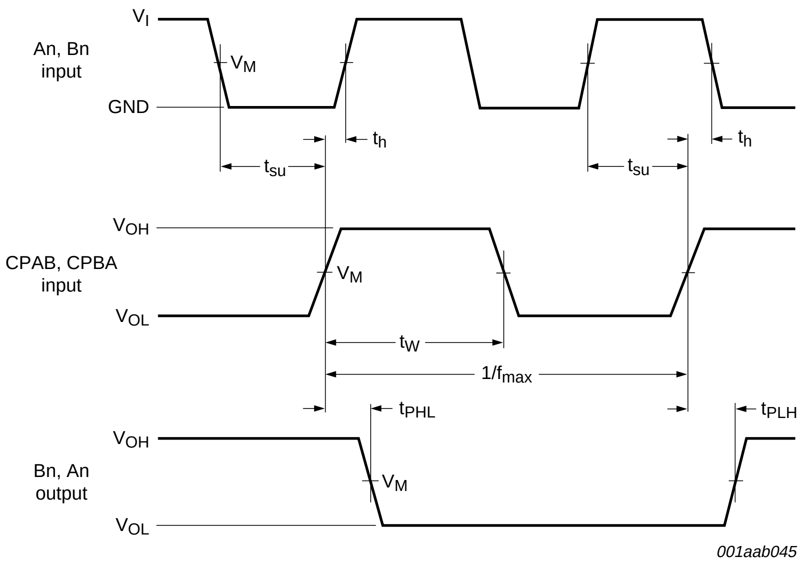
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 6. Input (An and Bn) to output (Bn and An) propagation delays.

Table 9: Measurement points

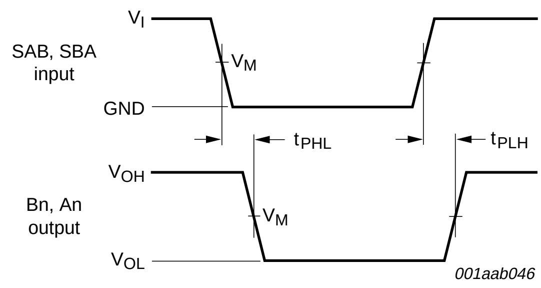
Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
≥ 2.7 V	1.5 V	1.5 V



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

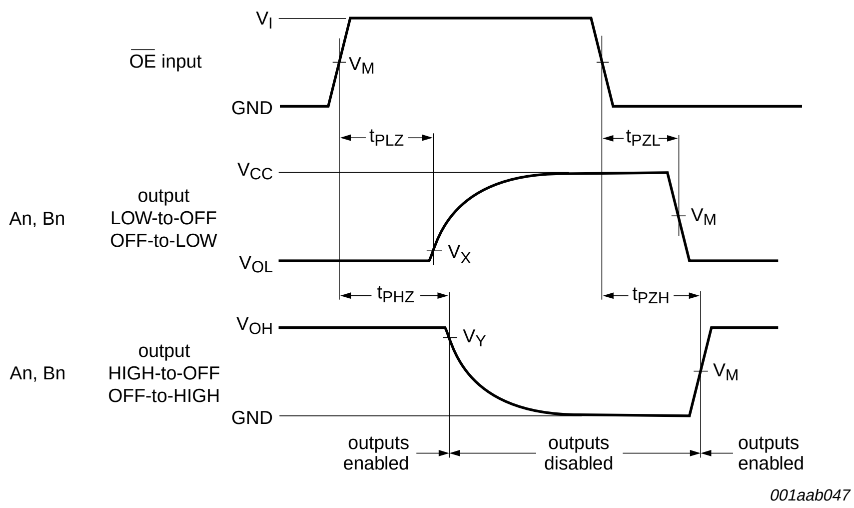
Fig 7. The An, Bn to CPAB, CPBA set-up and hold times, clock CPAB and CPBA pulse width, maximum clock pulse frequency and the CPAB, CPBA to output Bn, An propagation delays.



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 8. The input SAB and SBA to output Bn and An propagation delay times.



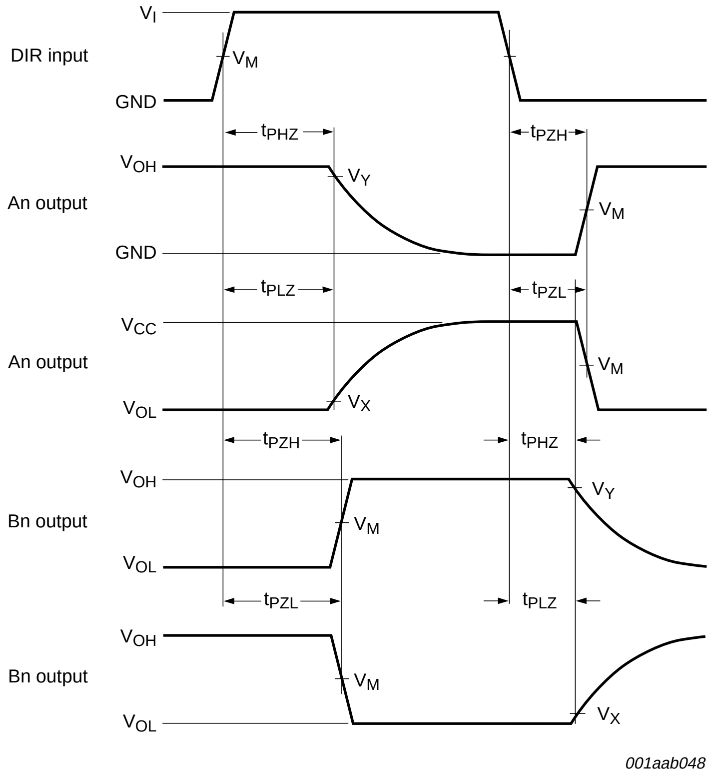
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 9. The input $\overline{OE}$ to output An and Bn 3-state enable and disable times.

Table 10: Measurement points

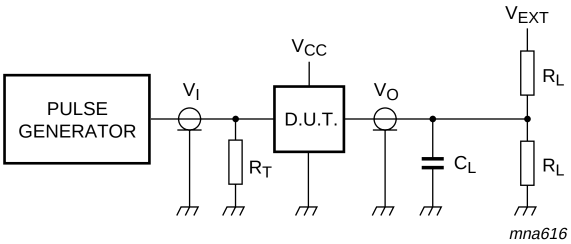
Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.1 × V_{CC}	V_{OH} – 0.1 × V_{CC}
≥ 2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 10. The input showing the input DIR to output An, Bn 3-state enable and disable times.



Test data is given in Table 11.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

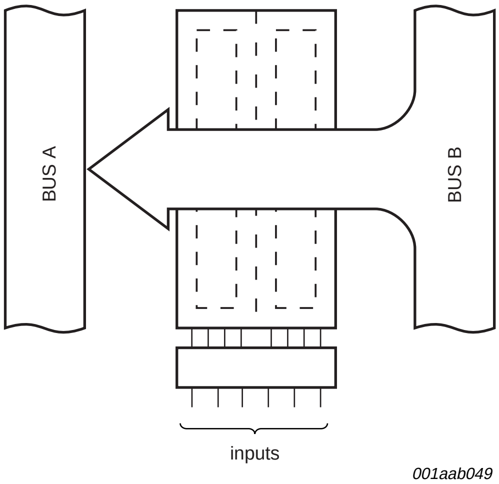
Fig 11. Load circuitry for switching times.

Table 11: Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω [1]	open	GND	2 × V_{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}

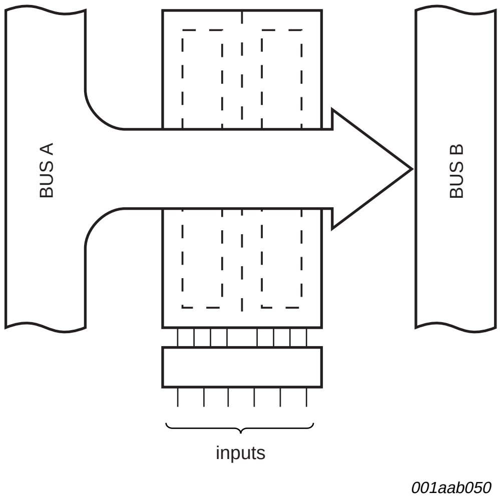
[1] The circuit performs better when R_L = 1000 Ω.

13. Application information



Values for inputs are given in Table 12.

Fig 12. Real-time transfer; bus B to bus A.

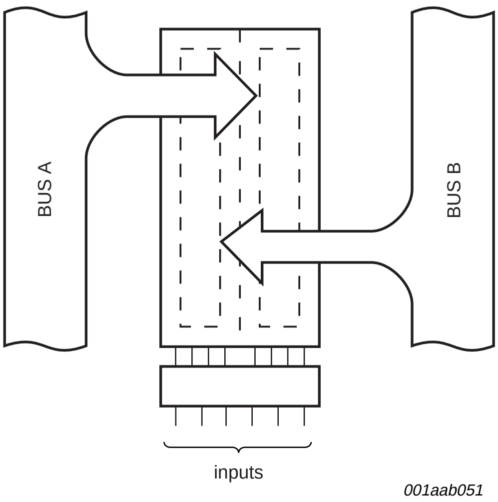


Values for inputs are given in Table 12.

Fig 13. Real-time transfer; bus A to bus B.

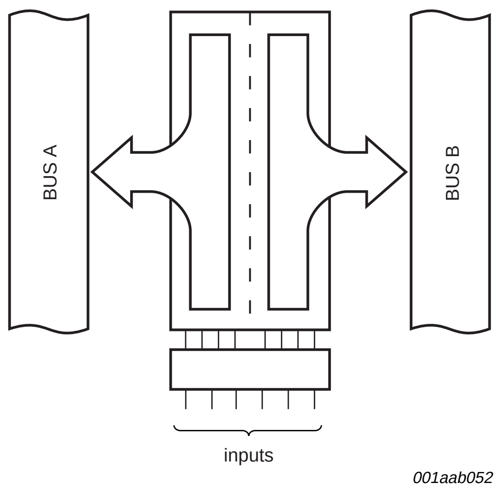
Table 12: Real-time transfer

Direction	Input					
	$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
Bus B to bus A	L	L	X	X	X	L
Bus A to bus B	L	H	X	X	L	X



Values for inputs are given in Table 13.

Fig 14. Bus A and bus B to storage.



Values for inputs are given in Table 13.

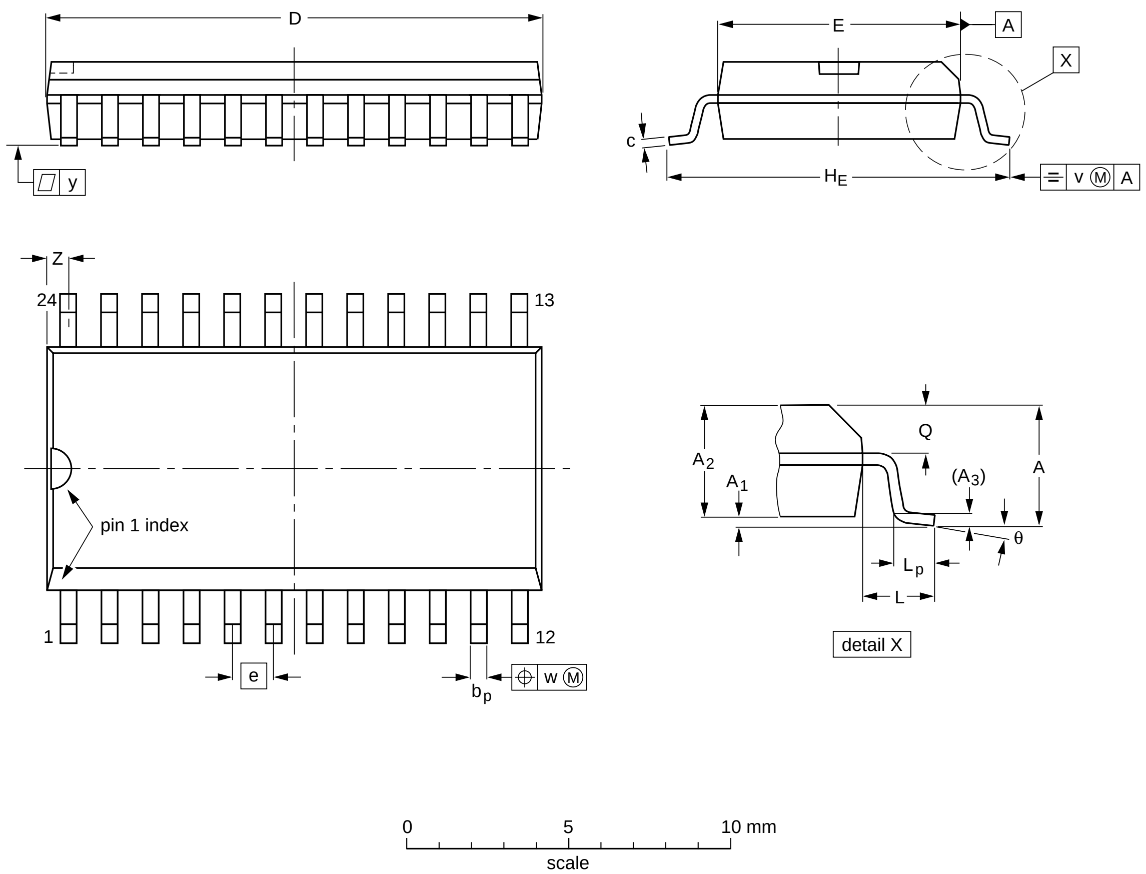
Fig 15. Storage to bus A or bus B.

Table 13: Storage transfer

Function	Input					
	$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
Bus A to storage	X	X	↑	X	X	X
Bus B to storage	X	X	X	↑	X	X
Bus A and B to storage	H	X	↑	↑	X	X
Storage to bus A	L	L	X	H or L	X	H
Storage to bus B	L	H	H or L	X	H	X

14. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

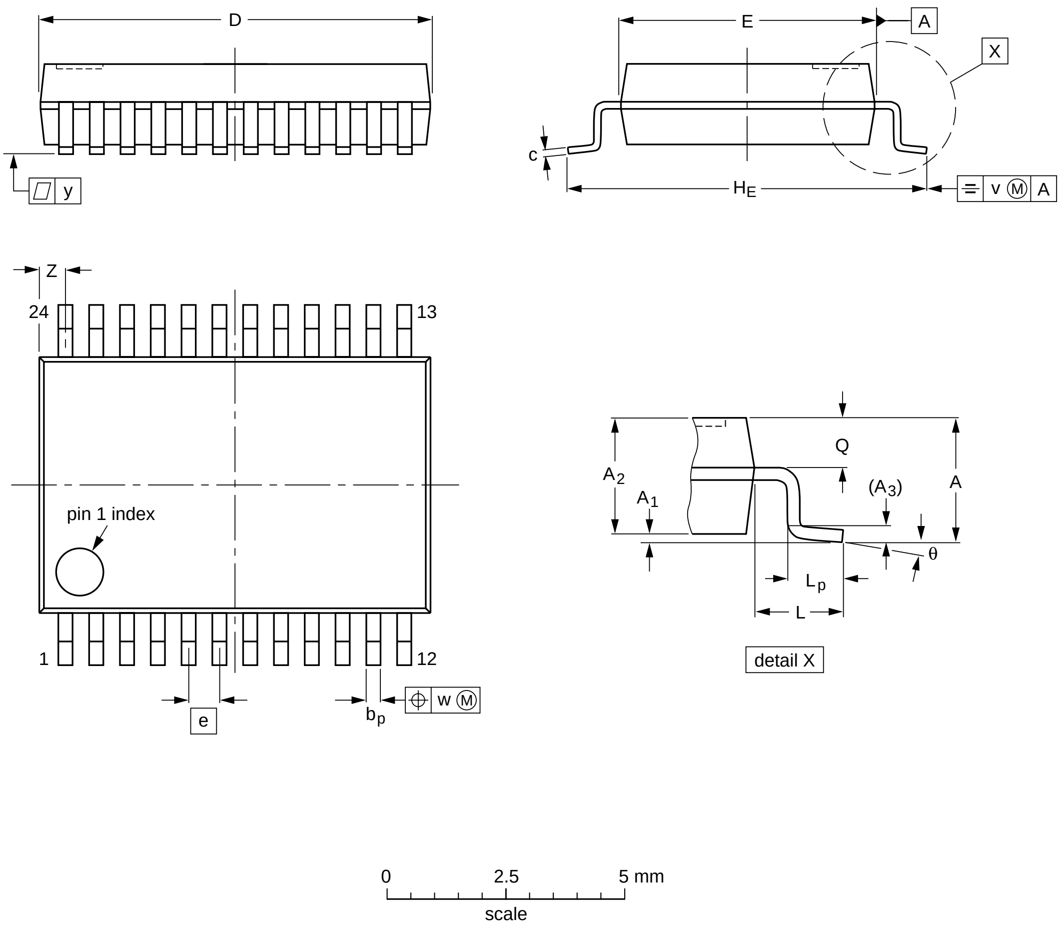
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 16. Package outline SO24.

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

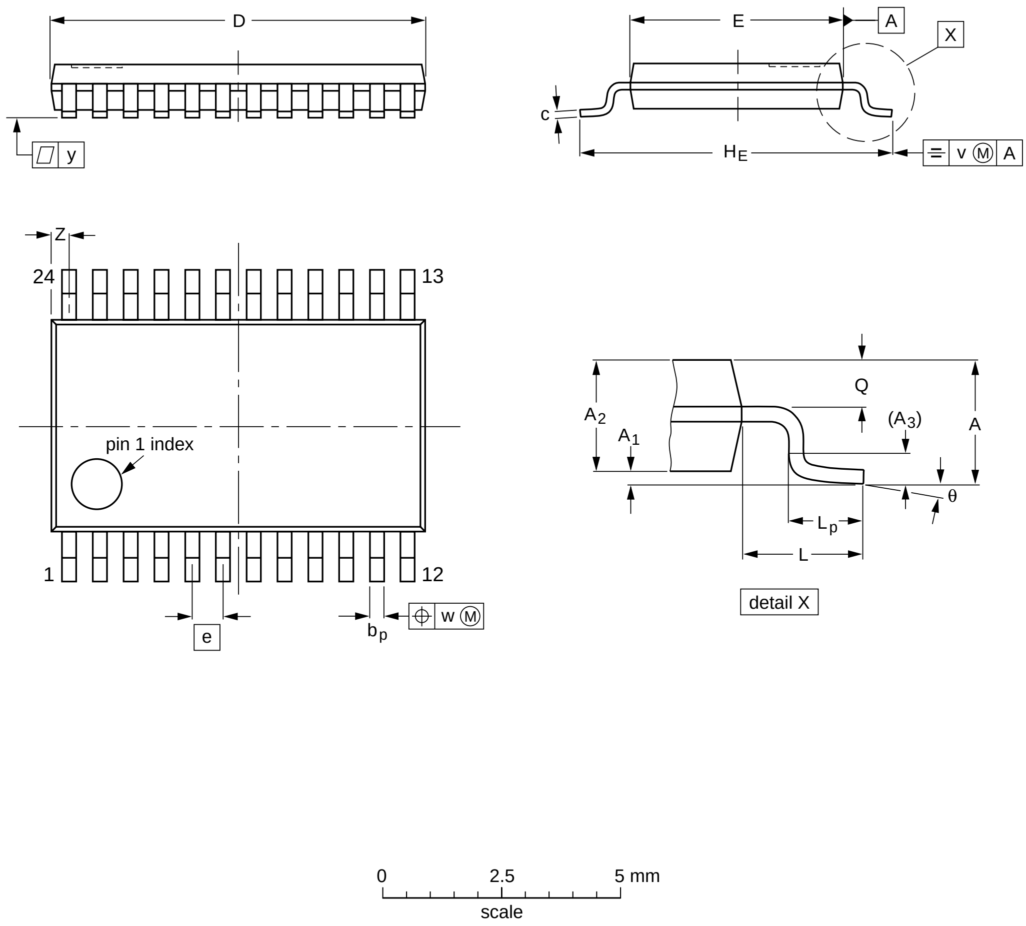
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 17. Package outline SSOP24.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 18. Package outline TSSOP24.

15. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LVC646A_4	20040629	Product data sheet	-	9397 750 13249	74LVC646A_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Table 1: updated various values • Table 7: added values for T_{amb} = –40 °C to +125 °C • Table 8: updated various values • Table 8: added values for T_{amb} = –40 °C to +125 °C.				
74LVC646A_3	20000621	Product specification	-	9397 750 07235	74LVC646A_2
74LVC646A_2	19980729	Product specification	-	9397 750 04516	74LVC646A_1
74LVC646A_1	19980302	Product specification	-	9397 750 03391	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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20. Contents

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