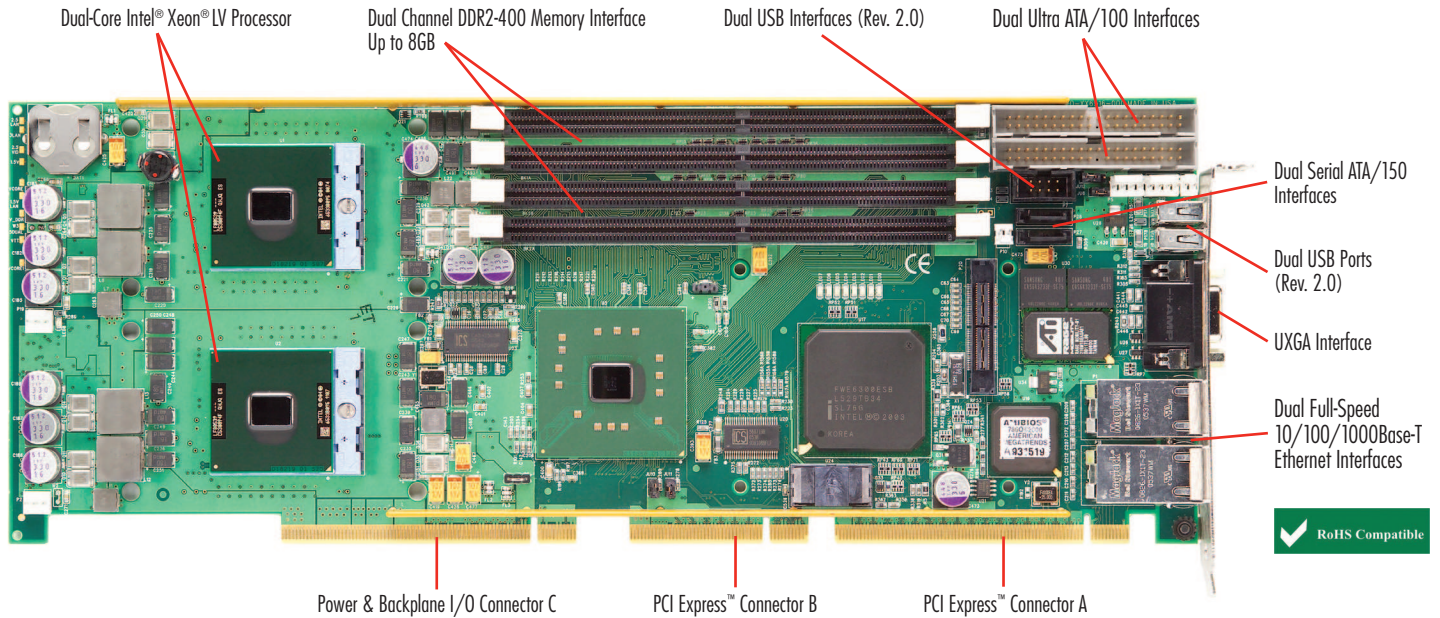


SLT (SHB Express™) SYSTEM HOST BOARD



Trenton's SLT system host board (SHB) features two, dual-core processors that together provide four execution cores per SLT. The SLT's two Dual-Core Intel® Xeon® LV processors deliver superior processing capability and system performance using about half as much power as compared to previous generations of low voltage Intel Xeon processors. The SLT is a server-class PICMG® 1.3 SHB that supports one x4 and two x8 PCI Express links to a PICMG 1.3 backplane. An additional x4 PCIe link to a backplane is available using Trenton's IOB31 expansion module. These links support PCI Express, PCI and PCI-X option cards on a PICMG 1.3 server-class backplane.

PROCESSORS:

Dual-Core Intel® Xeon® LV Processors at 1.66GHz to 2.0GHz*
 Processor Package: Micro-FCPGA (478-pin)

*Higher speeds as available

The Dual-Core Intel® Xeon® LV processors on the SLT support a 667MHz system bus as well as the Intel® Chip Multi-Processing (CMP) based architecture. Intel® CMP makes dual-core functionality on each processor possible. This new architecture along with the processors' advanced power management optimizes the CPUs millions of instructions per second per watt (MIPS/Watt) specification which in turn maximizes the SLT's system performance without generating excessive heat. Other processor features include:

- Dual Core, 2MB L2 Cache
- 31W Thermal Design Power
- Enhanced Intel SpeedStep Technology (EIST)

CHIPSET:

Increased system performance is made possible by the Intel® E7520 chipset's ability to support a 667MHz system bus. The chipset configuration on Trenton's SLT board supports two registered DDR2-400 memory channels. Data bottlenecks are reduced by the three PCI Express™ interfaces that provide high bandwidth (4GB/s) connections between the ports on the Memory Controller Hub (MCH) and external I/O devices or option cards.

PCI EXPRESS™ INTERFACES:

High-speed serial links that make up PCI Express (PCIe) interfaces typically have data rates twice that of PCI interfaces. A basic PCIe link consists of at least one pair of differentially driven transmit and receive signal lines. PCI Express link bandwidth is increased linearly by adding signal pairs to form multiple lanes or wider lane widths. The most common PCIe links used today are configured to have lane widths of x1, x4, x8 or x16. Trenton's SLT system host board provides two x8 PCI Express links, one x4 PCI Express link and five PCIe reference clocks on edge connectors A and B. Trenton's optional IOB31 module used with the SLT provides an additional x4 PCIe link to the backplane. The PCI Express links are used on PICMG 1.3 backplanes to support PCI Express option cards and bridge chips that provide PCI/PCI-X option card support. During system initialization the SLT automatically negotiates with the PCI Express cards connected to the PCIe links in order to set up communication between the devices. The net result is that the SLT system host board supports communication to x1, x4, x8, x16 PCI Express boards as well as PCI/PCI-X cards via PCI Express-to-PCI/PCI-X bridge chip technology on the backplane.

DDR2-400 MEMORY:

The DDR2-400 interface is a dual channel interface originating at the Memory Controller hub with each channel terminating at two DIMM module sockets, for a total of four memory sockets. The SLT uses ECC registered PC2-3200 DIMMs and supports a maximum memory capacity of 8GB and a minimum memory interface bandwidth of 3.2GB/s per channel. The total effective memory interface bandwidth increases to 6.4GB/s when at least one PC2-3200 DIMM is used in each memory channel.

STANDARDS:

- PCI Express™ Base Specification 1.0a
- SHB Express™ System Host Board PCI Express Specification - PCI Industrial Computer Manufacturers Group (PICMG®) 1.3

PCI EXPRESS™ CONFIGURATION AND BUS SPEEDS:

PCI Express - Edge Connectors A & B	- Two x8 links, one x4 link
	- Five reference clocks
PCI Express - (on-board only)	- One x4 link
PCI-X (on-board only)	- 64-bit/66MHz
PCI (on-board only)	- 32-bit/33MHz
Hub Link 1.5	- 266MB/s
System or FSB	- 667MHz

SERIAL ATA/150 PORTS (DUAL):

The primary and secondary Serial ATA (SATA) ports on the SLT boards comply with the SATA 1.0 specification and support two independent SATA storage devices such as hard disks and CD-RW devices. SATA technology provides lower-pin counts, reduced signaling voltages, simplified cabling, CRC error detection and hot-plug device support. SATA produces higher performance interfacing by providing data transfer rates up to 150MB per second on each port.

DUAL ETHERNET INTERFACES - 10/100/1000BASE-T:

The SLT uses an internal PCI-X bus to connect the I/O Controller hub to the Ethernet controller chip. This design feature provides high-speed dual Gigabit Ethernet on LAN ports 1 and 2. The SHB also supports 10Mb/s or 100Mb/s Ethernet networks. RJ-45 connectors on the I/O bracket provide the mechanical interface to the Ethernet networks.



