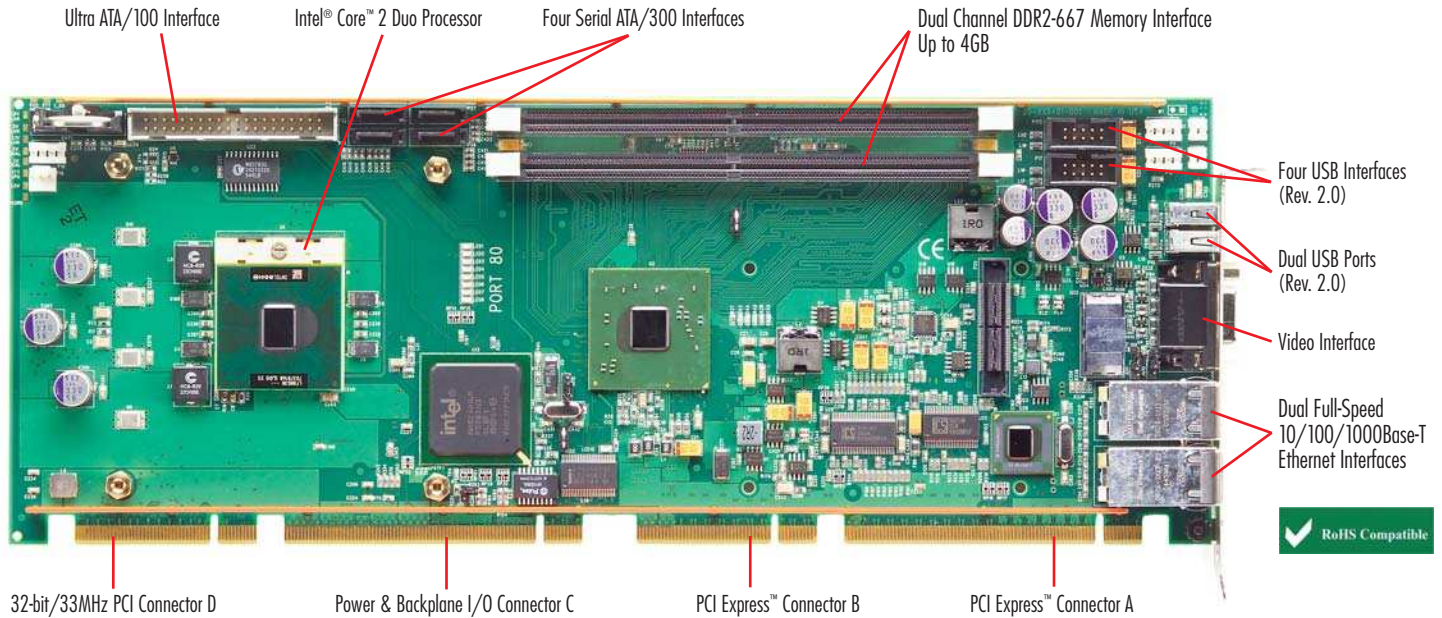


TML (SHB Express™) SYSTEM HOST BOARD



Trenton's TML is a graphics-class, PICMG® 1.3 system host board (SHB) that offers dual-core processor performance with a low profile passive heat sink. The SHB supports x16, x4 and x1 PCI Express™ links, and a 32-bit/33MHz PCI interface to a PICMG 1.3 backplane. The TML handles a wide range of system option cards, from the latest x16 PCI Express video cards to legacy 32-bit/33MHz PCI cards. The dual-core processor options feature shared 2MB or 4MB L2 cache memories. The Intel® 945G MCH and Intel® ICH7R ICH unlock the advanced capabilities of the TML SHB.

PROCESSOR:

Intel® Core™ 2 Duo Processor at 2.0GHz to 2.33GHz*

Intel® Core™ 2 Duo Processor at 1.66GHz to 2.0GHz*

Processor Package: FCPGA6 plugs into an mPGA 478 socket

*Higher speeds as available

The Intel® processor options on the TML support a 533MHz and 667MHz system bus. All processor options support 32-bit applications and the Intel® Core™ 2 Duo Processor T7400 supports 64-bit applications. Other processor features include:

- Dual Core, 2MB or 4MB L2 Cache
- Low thermal design power ratings
- Intel® Active Management Technology (Intel AMT 1.0)
- Enhanced Intel SpeedStep® Technology (EIST)

CHIPSET:

The Intel® 945G chipset combines advanced video and graphics capabilities with high-bandwidth interfaces such as a dual-channel DDR2-667, 667MHz FSB, PCI Express x16 graphics port and PCI Express x4 and x1 links to a PICMG 1.3 backplane. An Intel® ICH7R provides eight USB 2.0 and four SATA/300 ports. The ICH7R's SATA controller supports independent DMA, Advanced Host Controller Interface (AHCI) and integrated RAID level 0, 1, 5 and 10 functionality.

PCI EXPRESS™ INTERFACES:

Trenton's TML graphics-class system host board provides one x16 PCI Express link on the SHB's edge connectors A and B. This x16 PCIe link is designed to support PCI Express video/graphics cards on an SHB Express™ (PICMG 1.3) backplane. A x4 PCI Express link and five PCI Express reference clocks are also included on edge connectors A and B. An additional x1 PCI Express link between the TML and backplane can be provided by Trenton's optional IOB31 I/O Expansion Module. The x4 and x1 PCI Express links are used on SHB Express backplanes to support PCI Express option cards and the bridge chips that provide PCI/PCI-X cards via PCI Express-to-PCI/PCI-X bridge chip technology. The TML also provides a 32-bit/33MHz PCI bus interface on edge connector D.

DDR2-667 MEMORY:

The DDR2-667 interface is a dual-channel interface originating at the Memory Controller Hub, with each channel terminating at a DIMM module socket. The TML supports system memory transfer rates of either 400, 533 or 667MHz using unbuffered, non-ECC, PC2-3200, PC2-4200 or PC2-5300 DIMMs. Maximum memory capacity is 4GB. When using a single PC2-5300 DIMM, the memory interface bandwidth is 5.4GB/s, and when using two PC2-5300 DIMMs with equal memory capacities the TML's peak memory bandwidth increases to 10.7GB/s.

VIDEO INTERFACE:

The TML supports three video connection options:

- Direct connection via the chipset's Intel® Graphics Media Accelerator 950 with faster graphics and 3D performance
- A x16 PCI Express graphics port that provides 3.5 times more bandwidth than an AGP 8X interface
- ADD2 video and graphic cards

PCI EXPRESS™ CONFIGURATION AND BUS SPEEDS:

PCI Express - Edge Connectors A & B - One x16 link, one x4 link
 - Five reference clocks
 PCI Express - (on-board only) - Two x1 links
 PCI - 32-bit/33MHz
 System or FSB - 533MHz or 667MHz

SERIAL ATA/300 PORTS (FOUR):

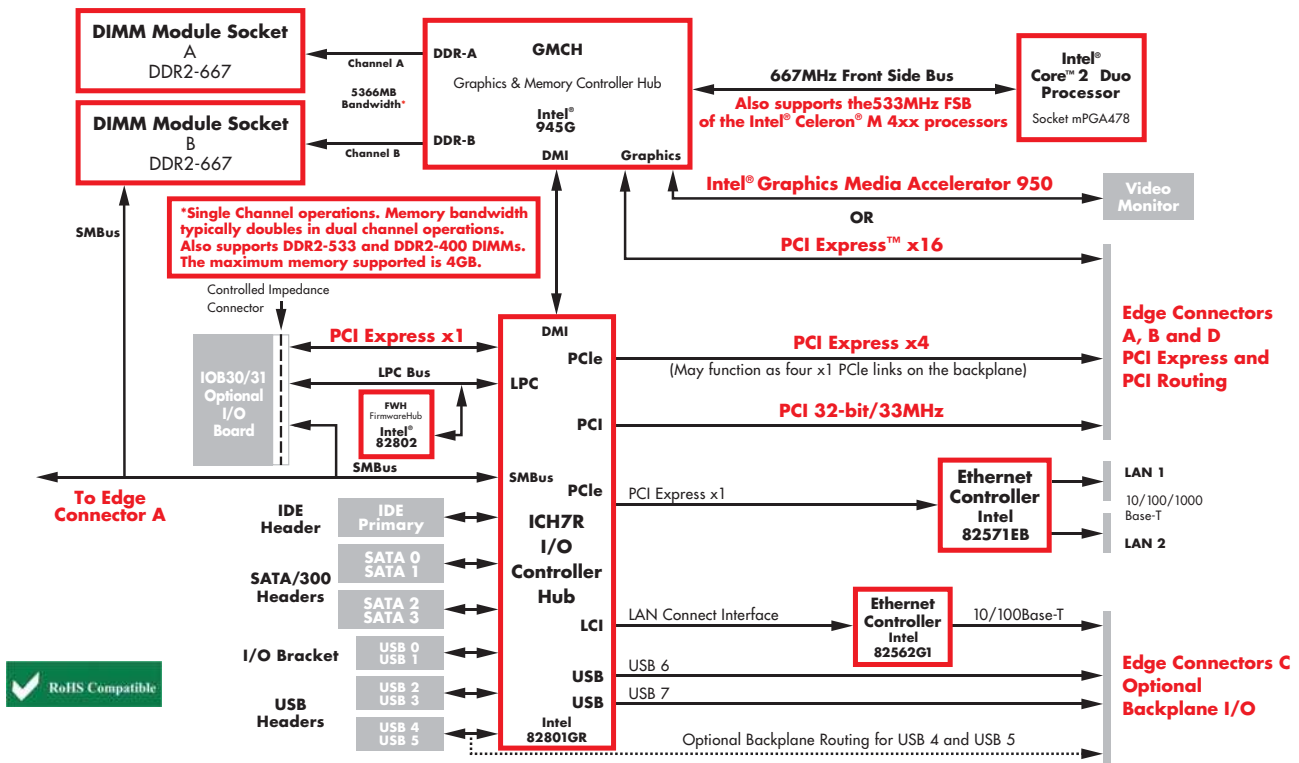
The primary and secondary Serial ATA (SATA) ports on the TML board support four independent SATA storage devices such as hard disks and CD-RW devices. SATA produces higher performance interfacing by providing data transfer rates up to 300MB per second on each port. The TML's ICH7R I/O Controller hub features Intel® Matrix Storage Technology, which allows the ICH7R's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5, and 10 implementations.

ETHERNET INTERFACES:

The TML uses an internal x1 PCI Express link to connect the I/O Controller hub to the dual-port Gigabit Ethernet controller chip. This design feature enables dual 10/100/1000Base-T Ethernet interfaces on LAN1 and LAN2. The LAN ports have RJ-45 connectors on the I/O bracket to provide the mechanical interfaces to the Ethernet networks. The ICH7R's internal LAN Interconnect Interface (LCI) provides an additional 10/100Base-T Ethernet interface for use on PICMG® 1.3 backplanes via the SHB's edge connector C.



Dependable, always.



EIGHT UNIVERSAL SERIAL BUS INTERFACES (USB 2.0):

A total of eight USB 2.0 interfaces are supported by the TML. USB ports 0 and 1 are on the I/O bracket and ports 2, 3, 4 and 5 have header connectors on the TML. USB ports 4 and 5 can be routed to edge connector C for use on a PICMG® 1.3 backplane. The backplane routing for USB 4 and 5 is a factory-build option. Contact Trenton for ordering details. USB ports 6 and 7 are routed directly to the TML's edge connector C.

BIOS (FLASH):

The TML uses AMIBIOS®. The flash BIOS resides in the SHB's Firmware Hub (FWH). AMIBIOS8 contains features such as:

- Support for flash devices for BIOS upgrading
- Integrated support for USB mass storage devices such as USB, CD-ROM, CD-RW, etc.
- Boot from network, USB mass storage devices, IDE or ATAPI
- Serial port console redirection to support headless operation (requires optional IOB30/IOB31)
- SATA/ATA/ATAPI support includes 48-bit LBA addressing to support SATA/ATA/IDE hard drive capacities over 137GB

STANDARDS:

- PCI Express™ Base Specification 1.0a
- SHB Express™ System Host Board PCI Express Specification - PCI Industrial Computer Manufacturers Group (PICMG®) 1.3

AGENCY APPROVALS:

Designed for UL60950, CAN/CSA C22.2 No. 60950-00, EN55022:1998 Class B, EN61000-4-2:1995, EN61000-4-3:1997, EN61000-4-4:1995, EN61000-4-5:1995, EN61000-4-6:1996, EN61000-4-11:1994

TML APPLICATION CONSIDERATIONS:

Power Requirements:

Typical Values - CPU Idle State:

CPU	+5V	+12V	+3.3V
2.16GHz†	2.20A	1.70A	2.60A
2.0GHz*	2.20A	0.75A	2.60A

Typical Values - 100% CPU Stress State:

CPU	+5V	+12V	+3.3V
2.16GHz†	3.00A	3.20A	2.60A
2.0GHz*	3.00A	2.00A	2.60A

-12V @ <100mA

Tolerance for all voltages is +/- 5% and must be applied by the PICMG 1.3 backplane to edge connector C. (†) Intel® Core™ 2 Duo T7400, (*) Intel® Core™ Duo T2500.

Temperature/Environment:

Operating Temperature: 0° to 60° C.
 Airflow Requirement: 200LFM continuous airflow when using the passive heat sink
 Storage Temperature: -40° to 70° C.
 Humidity: 5% to 90% non-condensing

Mechanical:

PASSIVE COOLING SOLUTION: The TML has a board stack-up height of .76" (1.93cm) with the SHB's passive heat sink cooling solution. Airflow of at least 200LFM must always be present across the SHB's passive heat sink.

ACTIVE COOLING SOLUTION: The TML's optional active cooling solution has a cooling fan mounted on the passive heat sink resulting in a board stack-up height of 1.16" (2.95cm). Order the TML's active cooling option for chassis designs with an available airflow of less than 200LFM. The overall TML dimensions are 13.330" (33.86cm) L x 4.976" (12.64cm) H. The relative PICMG 1.3 SHB height off the backplane is the same as a PICMG 1.0 SBC due to the shorter PCI Express backplane connectors.

ADDITIONAL TML FEATURES:

System Hardware Monitor:

- The functions monitored are:
 - Voltage: +3.3V, +/-12V, +5V and VCORE
 - Fan speed
 - Temperature

I/O Features:

- One EIDE Ultra ATA/100 interface
- Optional IOB30 I/O plug-in expansion board includes:
 - Enhanced bi-directional parallel interface
 - PS/2 mouse and keyboard interface (mini DIN connector)
 - Floppy drive interface
 - Two high-speed serial ports

ORDERING INFORMATION:

Model Name: TML			
Model #	CPU Speed	Intel® No.	Embedded CPU
6490-358-xM	2.16GHz	T7400†	Yes
6490-207-xM	2.0GHz	T2500	Yes
(xM = Memory)			
† Intel® Core™ 2 Duo			

The stated bus speed, memory and communication interface speeds are component maximums; actual system performance may vary.

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