Advanced

GT25F512

512K Bits

SPI Serial Flash

Table of Contents

1. Features

- Single Power Supply Operation
  - Low voltage range: 2.7 V - 3.6 V
- Low standby current 1uA (max.)
- Low Power Consumption
  - Low read current : 4 mA (max.)
  - Low erase current : 1 mA (max.)
  - Low program current : 1 mA (max.)
- Serial Peripheral Interface (SPI) Compatible
  - Supports single- or dual-output
  - Supports SPI Modes 0 and 3
  - Maximum 33 MHz clock rate for normal read
  - Maximum 66 MHz clock rate for fast read
- Page Program (up to 256 Bytes)
  - Typical 3 ms
- Page, Sector, Block or Chip Erase
  - Page/Sector erase: 3 ms (max.)
  - Block/Chip erase: 4 ms (max.)
- Memory Organization
  - Array: 64K x 8 (512K-bits)
  - Two equal Blocks of 32K Bytes
  - Each Block has eight sectors
  - Each sector has sixteen pages, each 256 Bytes
- Hardware Write Protection
  - Protect and unprotect the device from write operation by Write Protect ($\overline{WP}$) Pin
- Software Write Protection
  - The Block Protect (BP2, BP1, BP0) bits allow partial or entire memory to be configured as read only
- Lockable 256 byte OTP security sector
- High Product Endurance
  - Guaranteed 1,000,000 program/erase cycles single sector
  - More than 100 years data retention
- Industrial Standard 8-Pin packages, Lead-free (Pb-free), halogen-free:
  - 150 mil SOIC
  - 3 x 4.4 mm TSSOP
  - 2 x 3 x 0.55 mm UDFN

2. General Description

The GT25F512 are 512Kbit Serial Peripheral Interface (SPI) Flash memories, providing single- or dual output.

The devices are designed to support a 33 MHz clock rate in normal read mode, and 66 MHz in fast read, the fastest in the industry. The devices use a single low voltage power supply, wide operating voltage ranging from 2.7 Volt to 3.6 Volt, to perform read, erase and program operations. The devices can be programmed in standard EEPROM programmers.

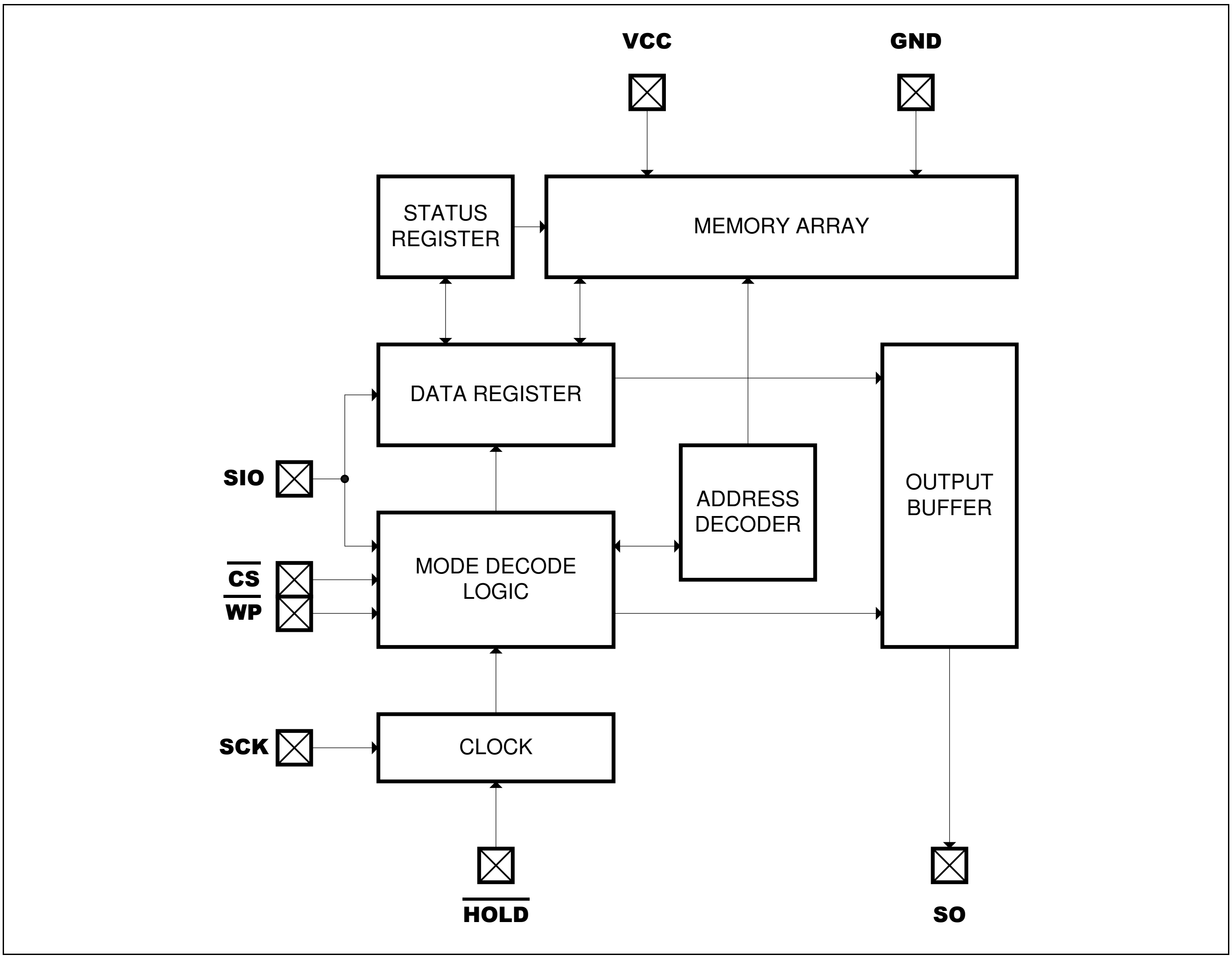
The GT25F512 are accessed through a 4-wire SPI Interface consisting of Serial Data Input/Output (SIO), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable ($\overline{CS}$) pins. They comply with all recognized command codes and operations. The dual-output fast read operation provides and effective serial data rate of 132MHz.

The devices support page program/erase mode, where 1 to 256 bytes data can be programmed into the memory in one program operation. These devices are divided into 16 uniform 4K-Bytes sectors or 2 uniform 32K-Bytes blocks.

The GT25F512 are offered in 8-pin SOIC 150mil, 8-contact UDFN and 8-pin TSSOP. The devices operate at wide temperatures between -40℃ to +85℃.

In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, no instructions should be sent to the device until the supply voltage has reached an acceptable stable level above the reset threshold voltage.

3. Functional Block Diagram

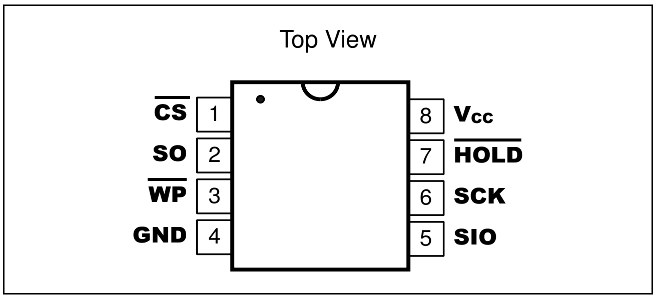


Serial Interface Description

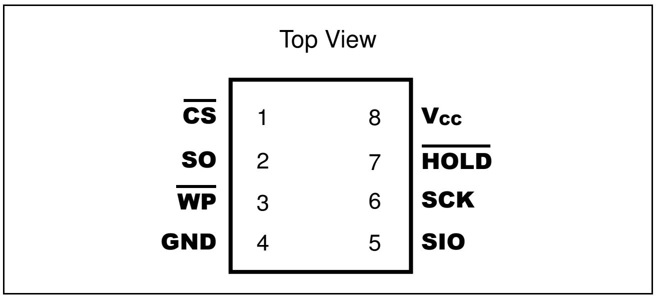
Master:	The device that provides a clock signal.
Slave:	GT25F512.
Transmitter/Receiver:	The GT25F512 has data input/output (SIO) and data output (SO).
MSB	MSB (Most Significant Bit) is the first bit being transmitted or received.
Op-Code:	Operational instruction code typically sent to the GT25F512 is the first byte of information transmitted after $\overline{\text{CS}}$ is Low. If the Op-Code is a valid instruction as listed in Table 5.6, then it will be decoded appropriately. It is prohibited to send an invalid Op-Code.

4. Pin Configuration

4.1 8-Pin SOIC and TSSOP



4.2 8-Lead UDFN



4.3 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	$\overline{\text{CS}}$	I	Chip Select
2	SO	O	Serial Data Output
3	$\overline{\text{WP}}$	I	Write Protect Input
4	GND	-	Ground
5	SIO	I/O	Serial Data Input and Output
6	SCK	I	Serial Clock
7	$\overline{\text{HOLD}}$	I	Hold function
8	V_{CC}	-	Supply Voltage

4.4 Pin Descriptions

Chip Select ($\overline{\text{CS}}$)

The $\overline{\text{CS}}$ pin is used to enable or disable the device. Upon power-up, $\overline{\text{CS}}$ must follow the supply voltage. When the device is ready for instruction input, this signal requires a High-to-Low transition. Once $\overline{\text{CS}}$ is stable at Low, the device is enabled. Then the master and slave can communicate among each other through SCK, SIO, and SO pins. Upon completion of transmission, $\overline{\text{CS}}$ must be driven to High in order to stop the operation or start the internal write operation. And the device will enter into standby mode, unless an internal write operation is in progress. During this mode, SO becomes high impedance.

Serial Clock (SCK)

Under the SPI modes (0, 0) and (1, 1), this clock signal provides synchronization between the master and GT25F512. Typically, Op-Codes, addresses and data are latched from SIO at the rising edge of SCK, while data from SO/SIO are clocked out at the falling edge of SCK.

Serial Data Input (SIO)

Data Input pin and output pin.

Serial Data Output (SO)

Data output pin.

Write Protect ($\overline{\text{WP}}$)

This active Low input signal is utilized to initiate Hardware Write Protection mode. This mode prevents the Block Protection bits and the WPEN bit in the Status Register from being modified. To activate the Hardware Write Protection, $\overline{\text{WP}}$ must be Low simultaneously when WPEN is set to 1.

Hold ($\overline{\text{HOLD}}$)

This feature is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SIO, SO, SCK). The $\overline{\text{HOLD}}$ signal transitions must occur only when SCK is Low and be held stable during SCK transitions. Connecting $\overline{\text{HOLD}}$ to High disables this feature. Section 5.17 shows Hold timing.

5. Device Operation

5.1 Status Register

The Status Register accessible by the user consists of 8-bits data for write protection control and write status. It becomes Read-Only under any of the following conditions: Hardware Write Protection is enabled or WEN is set to 0. If neither is true, it can be modified by a valid instruction.

Table 5.1: Status Register

Bit	Symbol	Name	Description
0	$\overline{\text{RDY}}$	Ready	When $\overline{\text{RDY}}$ = 0, device is ready for an instruction. When $\overline{\text{RDY}}$ = 1, device is busy. As busy, device only accepts Read Status Register command.
1	WEN	Write Enable	This represents the write protection status of the device. When WEN = 0, Status Register and entire array cannot be modified, regardless the setting of WPEN, $\overline{\text{WP}}$ pin or block protection. Write Enable command (WREN) can be used to set WEN to 1. Upon power-up stage, WEN is reset to 0.
2	BP0	Block Protect Bit	Despite of the status on WPEN, $\overline{\text{WP}}$ or WEN, BP0, BP1 and BP2 configure any combinations of the corresponding blocks being protected (Table 5.2). They are non-volatile memory and programmed to 0 by factory. Note: a Chip Erase instruction is executed successfully only if BP0, BP1 and BP2 are set as “0”s.
3	BP1	Block Protect Bit	
4	BP2	Block Protect Bit	
5	X	Don’t Care	Values can be either 0 or 1, but are not retained. Mostly always 0, except during write operation.
6	X	Don’t Care	
7	WPEN/OTP_LOCK	Write Protect Enable/OTP Mode	This bit can be utilized to enable Hardware Write Protection, together with $\overline{\text{WP}}$ pin. If enabled, Status Register becomes read-only. However, the memory array is not protected by this mode. Hardware Write Protection requires the setting of $\overline{\text{WP}}$ = 0 and WPEN = 1. Otherwise, it is disabled. WPEN cannot be altered from 1 to 0 if $\overline{\text{WP}}$ is already set to Low. (Table 5.3 for write protection). In OTP mode, this bit is served as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK value is equal 0, after OTP_LOCK is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP_LOCK bit can only be programmed once. Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Note: During internal write cycles, bits 0 to 7 are temporarily 1's.

Table 5.2: Block Protection by BP0, BP1 and BP2

Level	Status Register Bits			Array Addresses Protected
	BP2	BP1	BP0	
0	Not used	0	0	None
1 (1/4)	Not used	0	1	All
2 (1/2)	Not used	1	0	All
3 (All)	Not used	1	1	All

Table 5.3: Write Protection

WPEN	$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register (WPEN, BP1, BP0)
0	X	Not Enabled	0	Read-only	Read-only	Read-only
0	X	Not Enabled	1	Read-only	Unprotected	Unprotected
1	0	Enabled	0	Read-only	Read-only	Read-only
1	0	Enabled	1	Read-only	Unprotected	Read-only
X	1	Not Enabled	0	Read-only	Read-only	Read-only
X	1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

Table 5.4: Address Key

Name	GT25F512
A_N	A_{15}-A_0
Don't Care Bits	A_{23}-A_{16}

Table 5.5: Manufacturer and Device Identification Definition

OP Code	DID_7-DID_0
ABh	05h

OP Code	MID_{15}-MID_8	MID_7-MID_0	DID_{15}-DID_8
9Fh	C4h	9Dh	20h

OP Code	Address	MID_7-MID_0	DID_7-DID_0	MID_{15}-MID_8
90h	00h	9Dh	05h	C4h

OP Code	Address	DID_7-DID_0	MID_7-MID_0	MID_{15}-MID_8
90h	01h	05h	9Dh	C4h

5.2 Op-Code Instructions

The operations of the GT25F512 are controlled by a set of instruction Op-Codes (Table 5.6) that are clocked-in serially via SI pin. To initiate an instruction, the chip select ($\overline{CS}$) must be Low. Subsequently, each Low-to-High transition of the clock (SCK) will latch a stable level from SIO. After the 8-bit Op-Code, it may continue to latch-in an address and/or data from SIO accordingly, or to output data from SO. During data output, data are latched out at the falling edge of SCK. All communications start with MSB first. Upon the transmission of the last bit but prior to any following Low-to-High transition on SCK, $\overline{CS}$ must be brought to High in order to end the transaction and start the operation. The device will enter into Standby Mode after the operation is completed.

Table 5.6: Instruction Op-Codes [1,2,3]

Name	Op-Code	Operation	Address				Data (SIO)	Data (SO)
WRSR	01h	Write Status Register	N/A	N/A	N/A	N/A	D_7-D_0	N/A
PP	02h	Page program	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	N/A	D_7-D_0, ...	N/A
READ	03h	Read Data at Normal Read Mode	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	N/A	N/A	D_7-D_0, ...
WRDI	04h	Reset Write Enable Latch/Exit OTP Mode	N/A	N/A	N/A	N/A	N/A	N/A
RDSR	05h	Read Status Register	N/A	N/A	N/A	N/A	N/A	D_7-D_0 -
WREN	06h	Set Write Enable Latch	N/A	N/A	N/A	N/A	N/A	N/A
PEP	0Ah	Page Erase & Program	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	N/A	D_7-D_0, ...	N/A
FREAD	0Bh	Fast Read Data at Fast Read Mode	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	xxxxxxxx	N/A	D_7-D_0, ...
SE	20h/D7h	Sector Erase	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	N/A	N/A	N/A
EOTP	3Ah	Enter OTP Mode						
FRDO	3Bh	Fast Read Dual Output at Fast Read Mode	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	xxxxxxxx	D_6, D_4, D_2, D_0	D_7, D_5, D_3, D_1
BE	52h/D8	Block Erase	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	N/A	N/A	N/A
CE	60h/C7h	Chip Erase	N/A	N/A	N/A	N/A	N/A	N/A
RPID[4]	90h	Read Manufacture ID and Device ID	xxxxxxxx	xxxxxxxx	00h	N/A	N/A	MID_7-MID_0, DID_7-DID_0, MID_{15}-MID_8
RJID	9Fh	Read JEDEC 1-Byte Manufacture ID and 2-Bytes Product ID	N/A	N/A	N/A	N/A	N/A	MID_{15}-MID_8, MID_7-MID_0, DID_{15}-DID_8,
RDID	ABh	Read Device ID	xxxxxxxx	xxxxxxxx	xxxxxxxx	N/A	N/A	DID_7-DID_0, ...
PE	DBh	Page Erase	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	N/A	N/A	N/A

Notes: [1] x = Don't care bit (recommended to be "0"). N/A: Not appliable

[2] Only legal Op-Codes listed above are permitted. Any illegal commands are prohibited and may cause unexpected behaviors.

[3] Some address bits may be don't care (Table 5.4).

[4] When the last byte address is 00h, the SO will output the manufacturer ID first, but when the address is 01h, the SO will output device ID first. (Table 5.5)

5.3 Write Enable

When V_{CC} is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR) or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a Write Enable (WREN) instruction is necessary to set WEN to 1 (Section 5.17).

5.4 Write Disable

The device can be completely protected from modification by resetting WEN to 0 through the Write Disable (WRDI) instruction (Section 5.17).

5.5 Read Status Register

The Read Status (RDSR) instruction reviews the status of Write Protect Enable, Block Protection setting, Write Enable state and $\overline{RDY}$ status (Table 5.1). RDSR is the only instruction accepted when an internal write cycle is underway. It is recommended that the status of Write Enable and $\overline{RDY}$ be checked, especially prior to an attempted modification of data. These 8 bits information can be repeatedly output on SO after the initial Op-Code (Section 5.17).

5.6 Write Status Register

The Write Status Register (WRSR) instruction allows the user to choose a Block Protection setting and set or reset the WPEN bit. The values of the other data bits incorporated into WRSR can be 0 or 1 and are not stored in the Status Register. WRSR will be ignored unless both following conditions are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled (Refer to Table 5.1). Except for $\overline{RDY}$ status, the values in the Status Register remain unchanged until the moment when the write cycle is completed and the register is updated. Note that WPEN can be changed from 1 to 0 only if $\overline{WP}$ is already set High. Once completed, WEN is reset for complete chip write protection (Fig. 5-5).

Note: In the OTP mode, WRSR command will ignore input data and program OTP_LOCK bit to 1.

5.7 Read Data

This instruction includes an Op-Code and 24-bit address, then results the selected data to be shifted out from SO. Following the first data byte, additional sequential data can be output. If the data byte of the last address is initially output, then address will rollover to the first address in the array, and the output could loop indefinitely. At any time, a rising $\overline{CS}$ signal ceases the operation (Section 5.17).

5.8 Fast Read Data

This instruction is used to read memory data at up to a 66 MHz clock.

The instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SIO line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line, with each bit shifted out at a maximum frequency F_{CT}, during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 0000h address, allowing the entire memory to be read with this single instruction. At any time, a rising $\overline{CS}$ signal ceases the operation (Section 5.17).

5.9 Fast Read Dual Output

The FRDO instruction is used to read memory data on two output pins each at up to a 66 MHz clock.

The FRDO instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SIO line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO and SIO lines, with each pair of bits shifted out at a maximum frequency F_{SCK}, during the falling edge of SCK. The first bit (MSb) is shifted out from SO, while simultaneously the second bit is shifted out from SIO.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDO instruction. FRDO instruction is terminated by driving $\overline{CS}$ signal high. (Section 5.17)

5.10 Read Device ID / Wake-up (RDID)

The Read Device ID instruction (RDID), ABh, is to read out the Device ID1, 05h (Table 5.5). It is also served as an alternative command to wake-up the device.

The RDI instruction code is followed by three dummy bytes, each bit being latched-in on SIO during the rising edge of SCK. Then the Device ID is shifted out on SO with the MSB first, each bit been shifted out during the falling edge of SCK. The RDI instruction is ended by $\overline{CS}$ goes high. The Device ID outputs repeatedly if continuously send the additional clock cycles on SCK while $\overline{CS}$ is at low. (Section 5.17)

5.11 Read JEDEC Identification (RJID)

The Read JEDEC Identification (RDID) instruction, 9Fh, allows the 8-bit JEDEC manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte.

Any Read Identification (RJID) instruction while an Erase or Program cycle is in progress, is not decoded and has no effect on the cycle that is in progress. The Read Identification (RJID) instruction should not be issued while the device is power down.

The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on SO, each bit being shifted out during the falling edge of SCK. The instruction sequence is shown in Section 5.17. The Read Identification (RJID) instruction is terminated by driving Chip Select High at any time during data output.

When Chip Select is driven High, the device is put in the Standby mode. Once in the Standby mode, the device waits to be selected, so that it can receive, decode and execute instructions. (Section 5.17)

5.12 Read Product ID (RPID)

The Read Product ID instruction (RPID), 90h, is to read out product information, including manufacturer ID and the specific device ID.

This instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code "90h" followed by a last 8-bit address (A_7-A^0) of 00h. Then it shifts out 9Dh being the Manufacturer ID1 (MID_7-MID_0), Device ID1 (DID_7-DID_0) and Manufacturer ID2 (MID_{15}-MID_8) on the falling edge of SCK with most significant bit (MSB) first. If the last 8-bit address is initially set to 01h, the Device ID1 (DID_7-DID_0) is shifted out first, then followed by Manufacturer ID1 (MID_7-MID_0), and Manufacturer ID2 (MID_{15}-MID_8) will be read first. (Table 5.5 & Section 5.17)

5.13 Page Operation

5.13.1 Page Program (PP)

The Page Program (PP) instruction, 02h, contains an Op-Code, a 24-bit address and the first data byte. Additional data bytes may be supplied sequentially after the first byte. Each PP instruction can affect up to 256 bytes of data in a page. Each page has a starting address XXXXXXXX XXXXXXXX 00000000 and an ending address XXXXXXXX XXXXXXXX 11111111. After the last byte of data in a page is input, the address rolls over to the beginning of the same page. If more than 256 bytes of data is input during a single instruction, then only the last 256 bytes will be retained, but the initial data will be overwritten.

If less than 256 bytes of data were sent to the device, then the remaining bytes within the page will not be programmed and will remain in the erased state (FFh), if erased operation is performed previously.

The contents of the array defined by Block Protection cannot be modified as long as that block configuration is selected. The contents of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction is initiated prior to PP. Once PP operation is completed, WEN is reset for complete chip write protection (Section 5.17). Besides, Hardware Write Protection has no affect on the memory array.

Note: A program operation can alter "1"s into "0"s, but an erase operation is required to change "0"s back to "1"s. A byte cannot be reprogrammed without being erased first

5.13.2 Page Erase & Program (PEP)

The PEP instruction is almost identical to Page Program command, except with a look-ahead erase being performed prior page program is performed. (Section 5.17)

5.14 Erase Operation

The memory array of the GT25F512 is organized into sixteen uniform 4K-Byte sectors or two 32K-Byte uniform blocks.

Before a byte can be reprogrammed, the sector or block that contains the byte must be erased (erasing sets bits to "1"). In order to erase the devices, there are four erase instructions available: Page Erase (PE), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE). A page erase operation allows one page data to be erased. And a sector erase operation allows any individual sector to be erased without affecting the data in other sectors. A block erase operation erases any individual block. A chip erase operation erases the whole memory array of a device. A page erase, sectors erase, blocks erase or chip erase operation can be executed prior to any programming operation.

During each erase operation, all instruction will be ignored except the Read Status Register (RDSR) instruction. The progress or completion of the erase operation can be determined by reading the $\overline{\text{RDY}}$ bit in the Status Register using a RDSR instruction. If the $\overline{\text{RDY}}$ bit is "1", the erase operation is still in progress. If the $\overline{\text{RDY}}$ bit is "0", the erase operation has been completed. (Section 5.17)

5.14.1 Page Erase (PE)

This instruction erases a 256-byte page. Before the execution of this instruction, the Write Enable Latch (WEN) must be set via a Write Enable (WREN) instruction. The WEN bit is reset automatically after the completion of sector an erase operation.

This instruction is entered, after chip Select ($\overline{\text{CS}}$) is pulled low to select the device and stays low during the entire instruction sequence The instruction code, and three address bytes are input via SIO. Erase operation will start immediately after chip Select ($\overline{\text{CS}}$) is pulled high. The internal control logic automatically handles the erase voltage and timing. Refer to Section 5.17 for Page Erase Sequence

5.14.2 Sector Erase (SE)

This instruction erases a 4K-Byte sector. Before the execution of this instruction, the Write Enable Latch (WEN) must be set via a Write Enable (WREN) instruction. The WEN bit is reset automatically after the completion of sector an erase operation.

This instruction is entered, after chip Select ($\overline{\text{CS}}$) is pulled low to select the device and stays low during the entire instruction sequence The instruction code, and three address bytes are input via SIO. Erase operation will start immediately after chip Select ($\overline{\text{CS}}$) is pulled high. The internal control logic automatically handles the erase voltage and timing. The sector erase instruction will not be executed if address page is protected by the block protect bits (BP2, BP1, BP0). Refer to Section 5.17 for Sector Erase Sequence.

5.14.3 Block Erase (BE)

This instruction erases a 32K-Byte block of the GT25F512. Before the execution of this instruction, the Write Enable Latch (WEN) must be set via a Write Enable (WREN) instruction. The WEN is reset automatically after the completion of a block erase operation.

The instruction code and three address bytes are input via SI. Erase operation will start immediately after the chip Select ($\overline{\text{CS}}$) is pulled high, otherwise the instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. The block erase instruction will not be executed if address page is protected by the block protect bits (BP2, BP1, BP0). Refer to Section 5.17 for Block Erase Sequence.

5.14.4 Chip Erase (CE)

This instruction erases the entire memory array of a GT25F512. Before the execution of this instruction, the Write Enable Latch (WEN) must be set via a Write Enable (WREN) instruction. The WEN is reset automatically after completion of a chip erase operation.

The instruction code is input via the SIO. Erase operation will start immediately after chip Select ($\overline{\text{CS}}$) is pulled high, otherwise the instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Section 5.17 for Chip Erase Sequence.

The Chip Erase (CE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

5.15 Enter OTP Mode

This Flash has an extra 256 bytes OTP sector, user must issue ENTER OTP MODE command to read, program or erase OTP sector. After entering OTP mode, WPEN bit becomes OTP_LOCK bit and can be read with RDSR command. Program/Erase command will be disabled when OTP_LOCK is ‘1’. And WRSR command will ignore the input data, and then program OTP_LOCK to 1.

User must clear the protect bits before enter OTP mode. OTP sector can only be program and erase when OTP_LOCK equal ‘0’ and BP [1:0] = ‘00’. In OTP mode, user can read other sectors, but program/erase other sectors only allowed when OTP_LOCK equal ‘0’.

User can use WRDI (04h) command to exit OTP mode. Refer to Figure 5-17 for enter OTP mode.

5.16 Illegal Command

Under any circumstances, if any illegal command, not listed in Table 5.6, is sent to the device, it may cause the device to enter into an unknown state, which may or may not cause unexpected behavior. Therefore, it is strongly recommended that only those commands in Table 5.6 are allowed.

5.17. Diagrams

Figure 5-1: Synchronous Data Timing

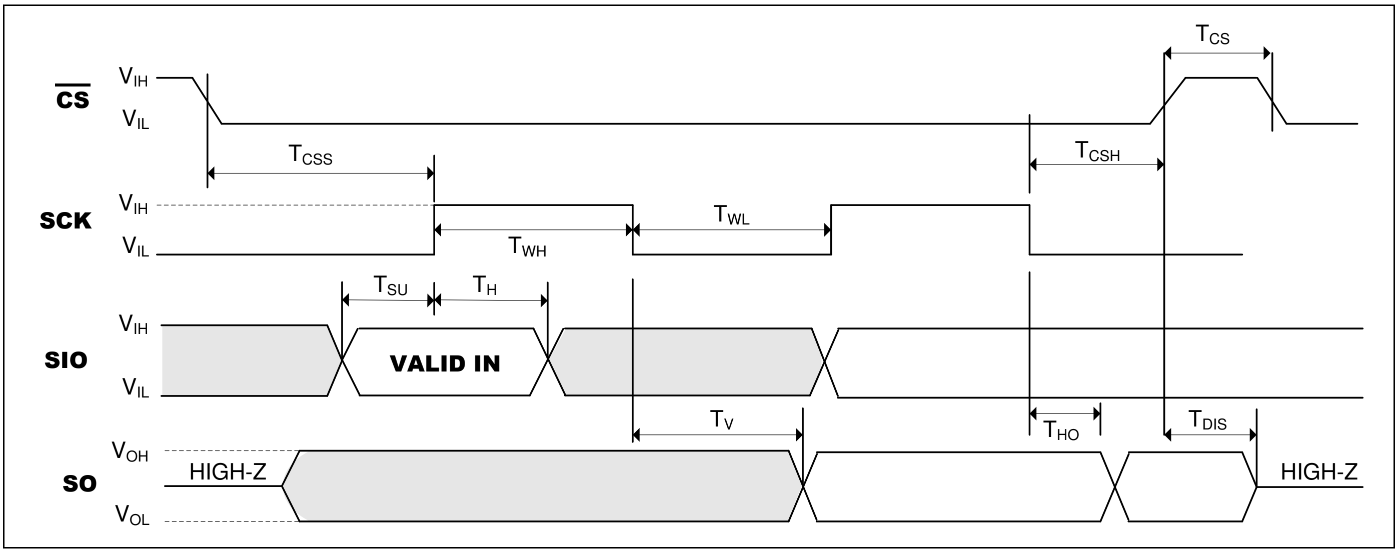


Figure 5-2: HOLD Timing

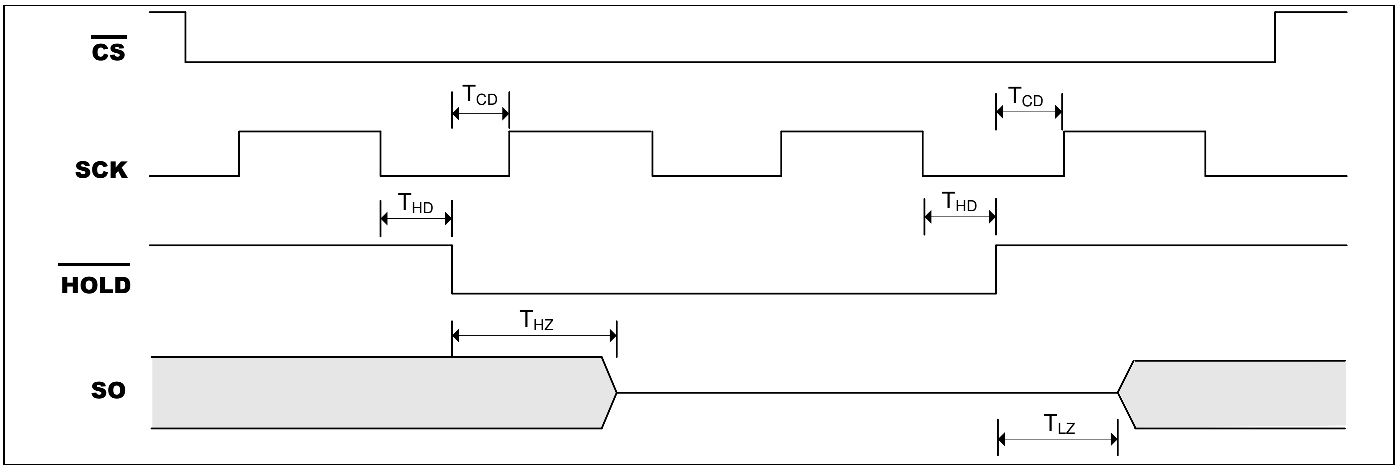
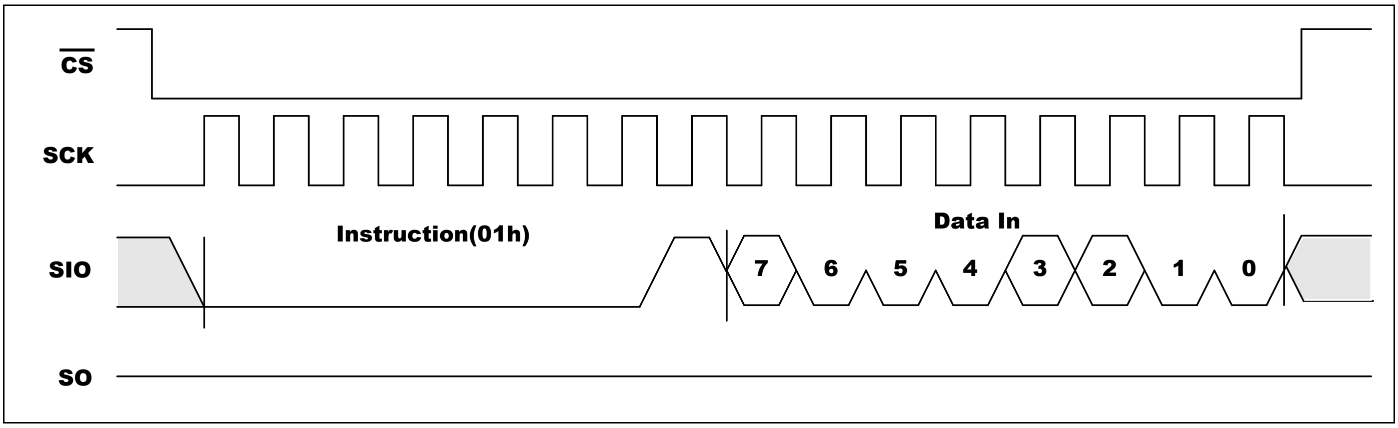


Figure 5-3: Write Status Register (WRSR)



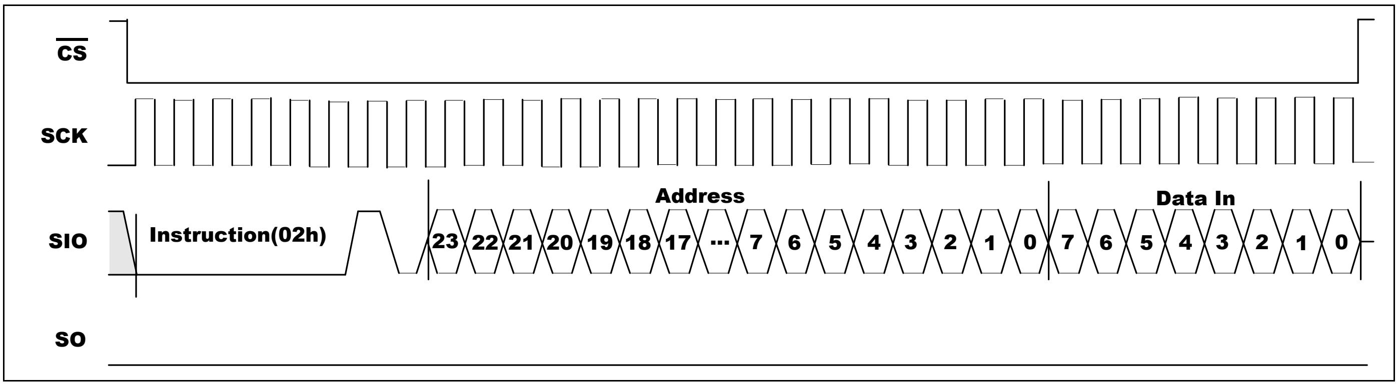


Figure 5-4: Page Program (PP)

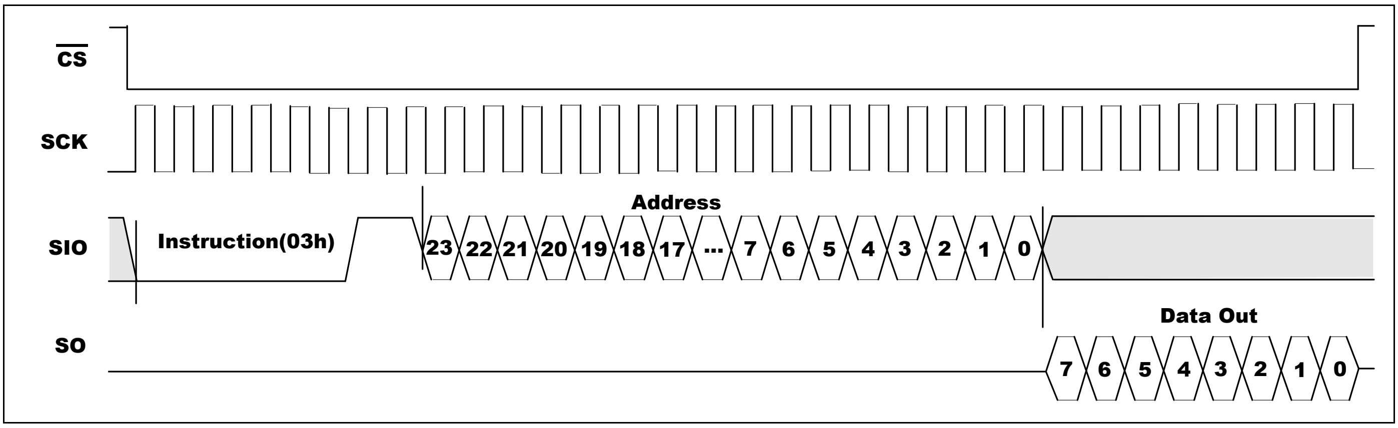


Figure 5-5: Read at Normal Read Mode (READ)

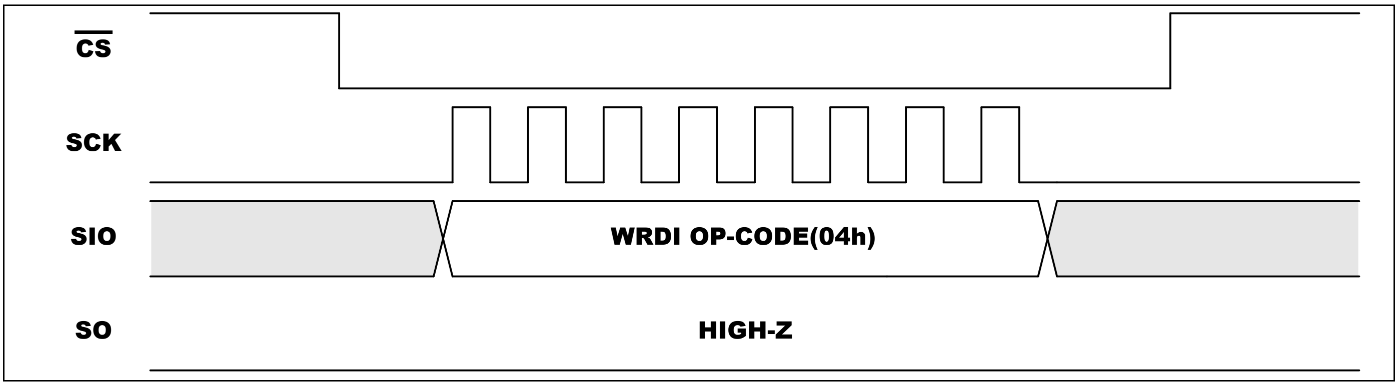


Figure 5-6: Reset Write Enable Latch/Exit OTP mode (WRDI)

Figure 5-7: Read Status Register (RDSR)

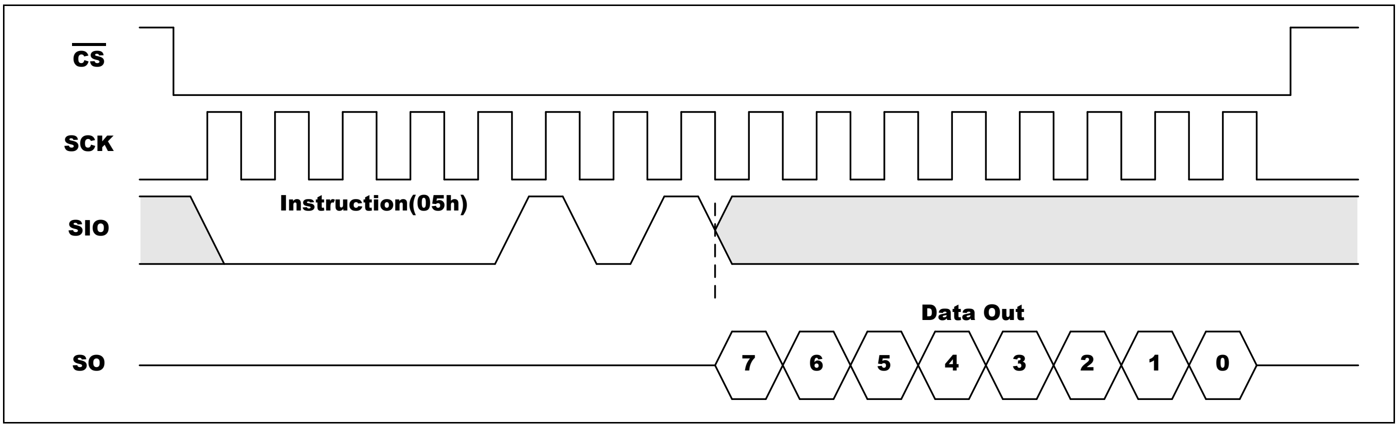


Figure 5-8: Write Enable Latch (WREN)

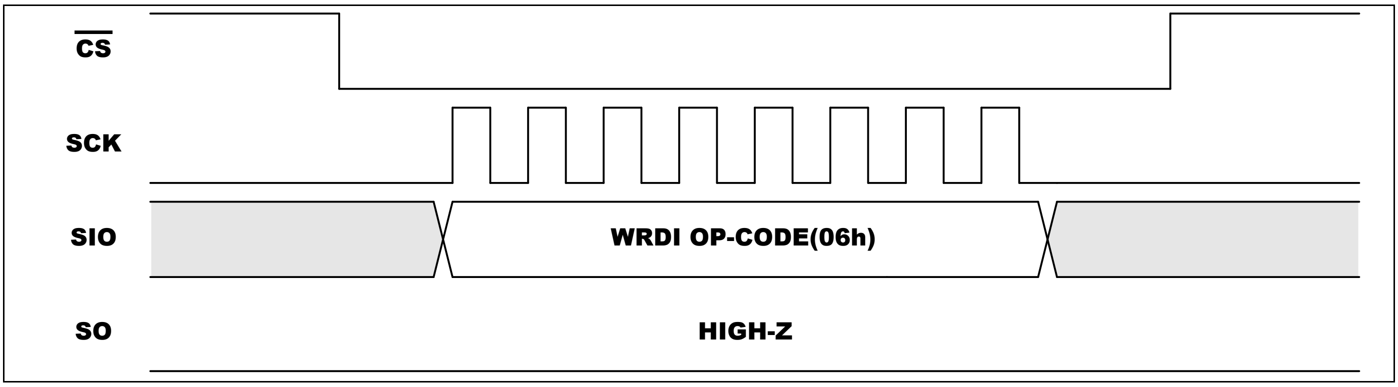
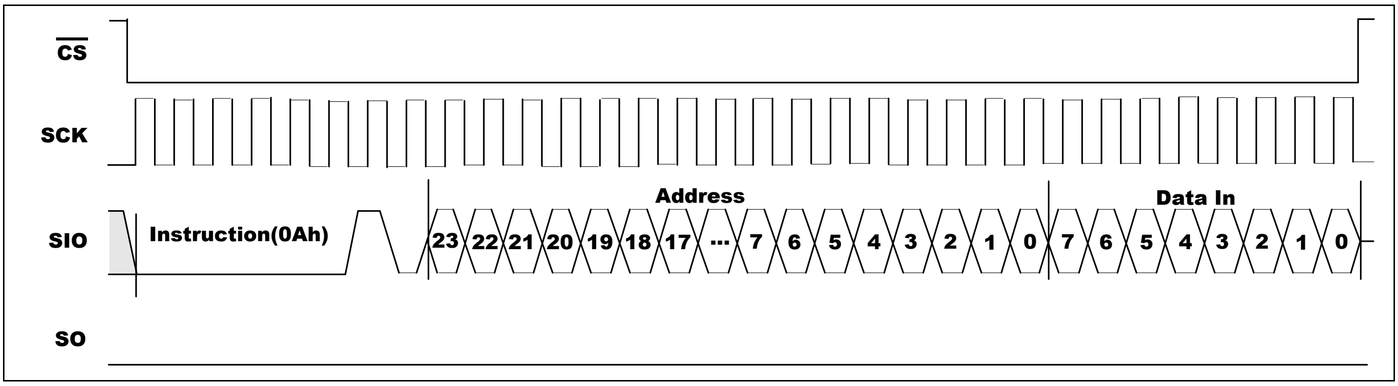


Figure 5-9: Page Erase & Program (PEP)



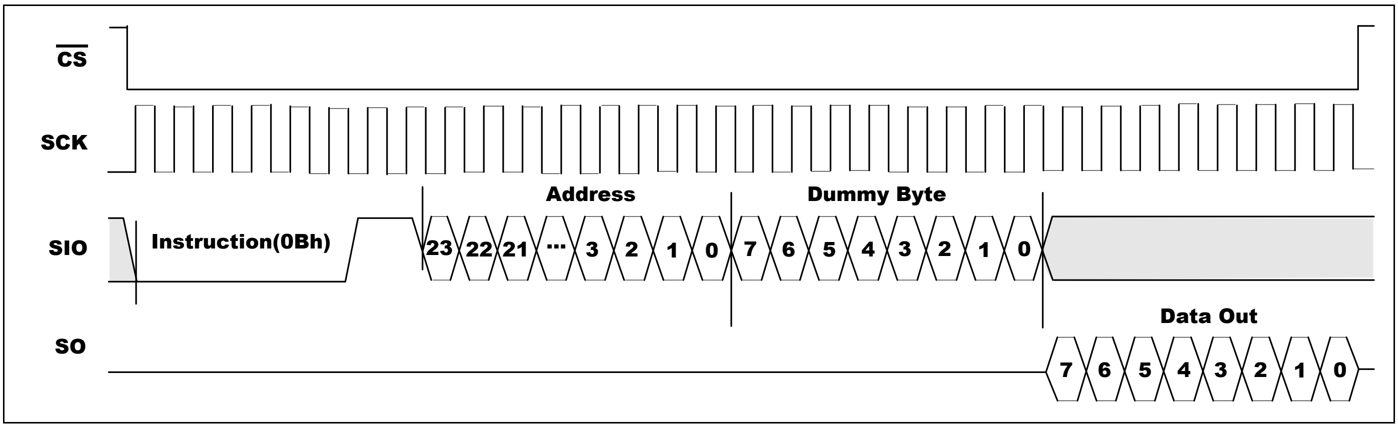


Figure 5-10: Fast Read at Fast Read Mode (FREAD)

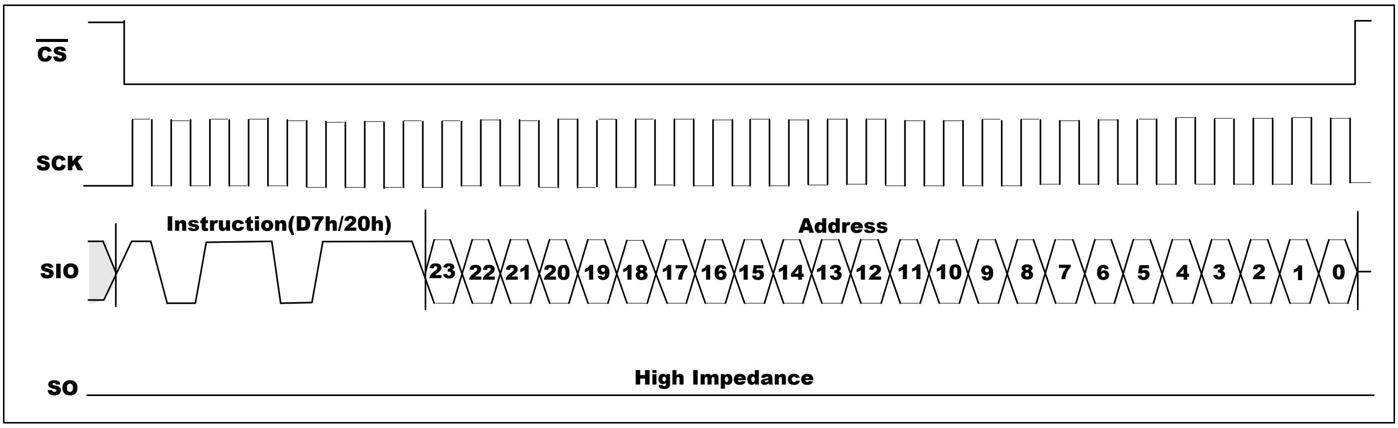


Figure 5-11: Sector Erase (SE)

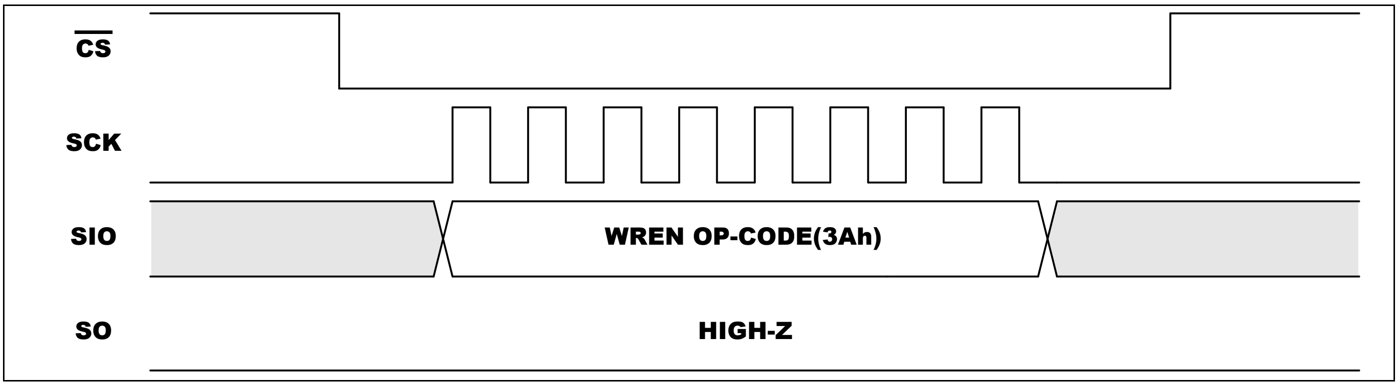


Figure 5-12: Enter OTP Mode (EOTP)

Figure 5-13: Fast Read Dual Output (FRDO)

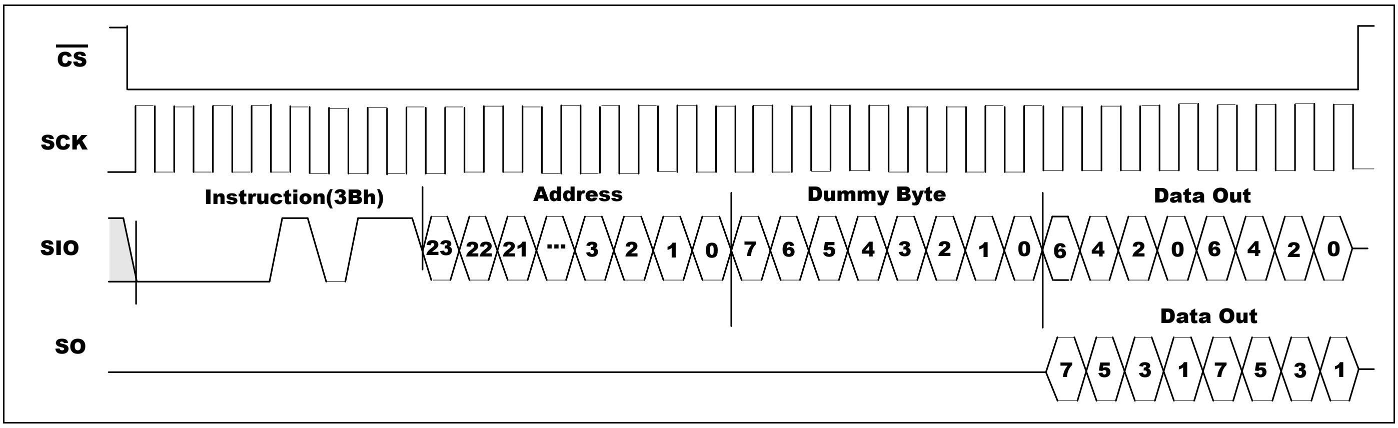


Figure 5-14: Block Erase (BE)

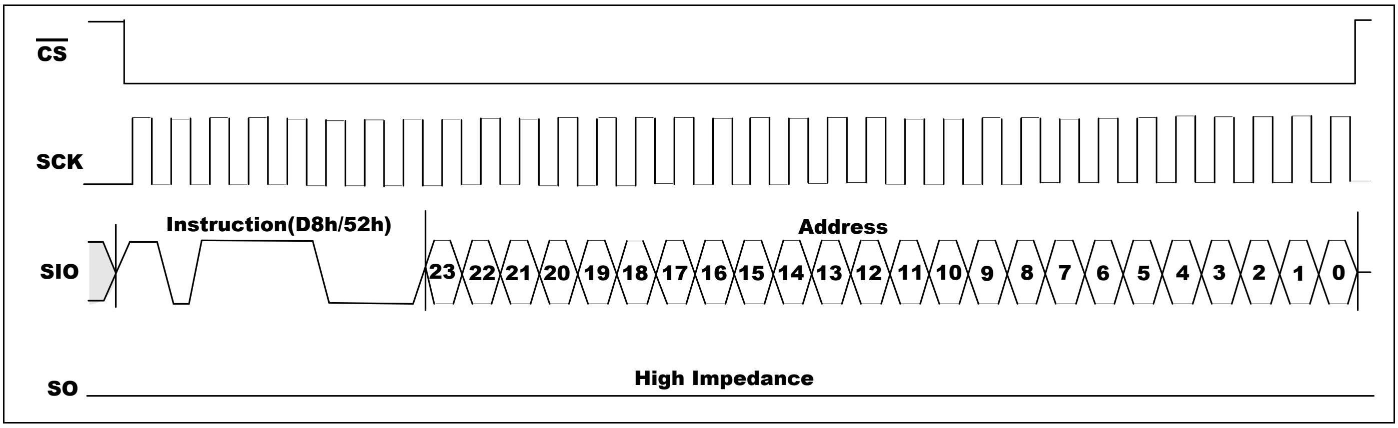


Figure 5-15: Chip Erase (CE)

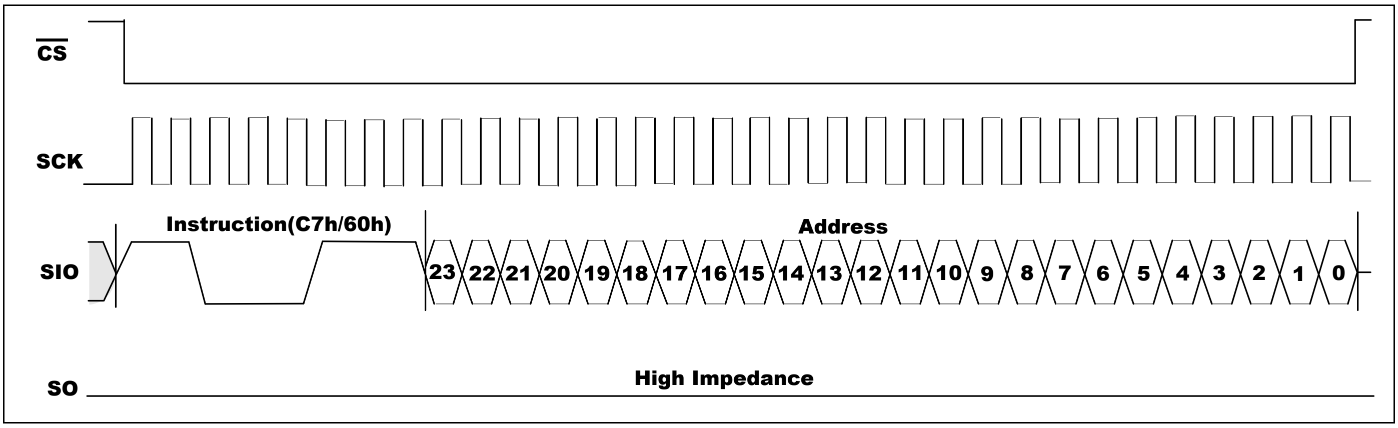


Figure 5-16: Read Product ID (RPID)

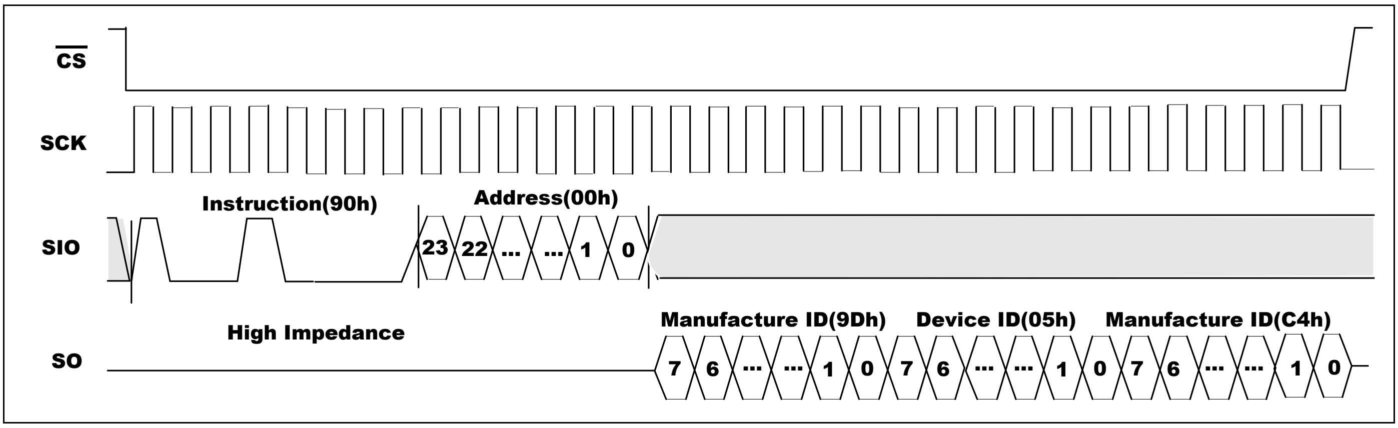


Figure 5-17: Read JEDEC Identification (RJID)

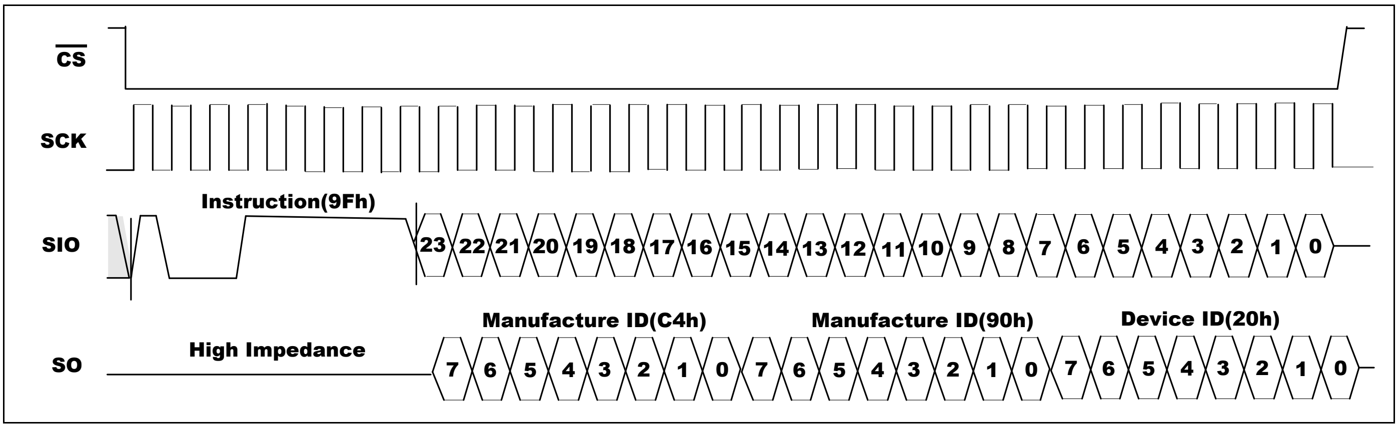


Figure 5-18: Read Device ID / Wake-up(RDID)

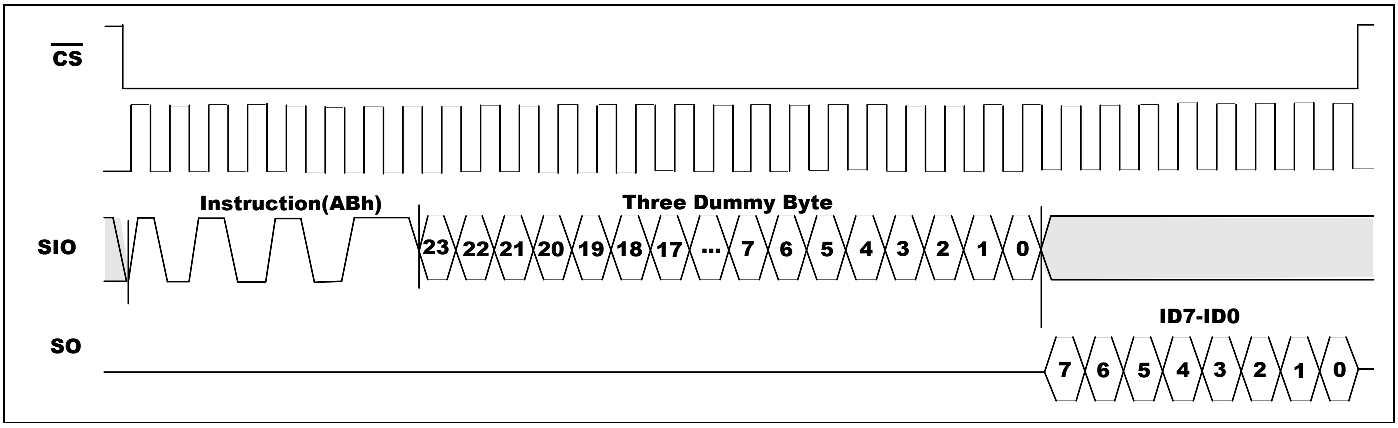
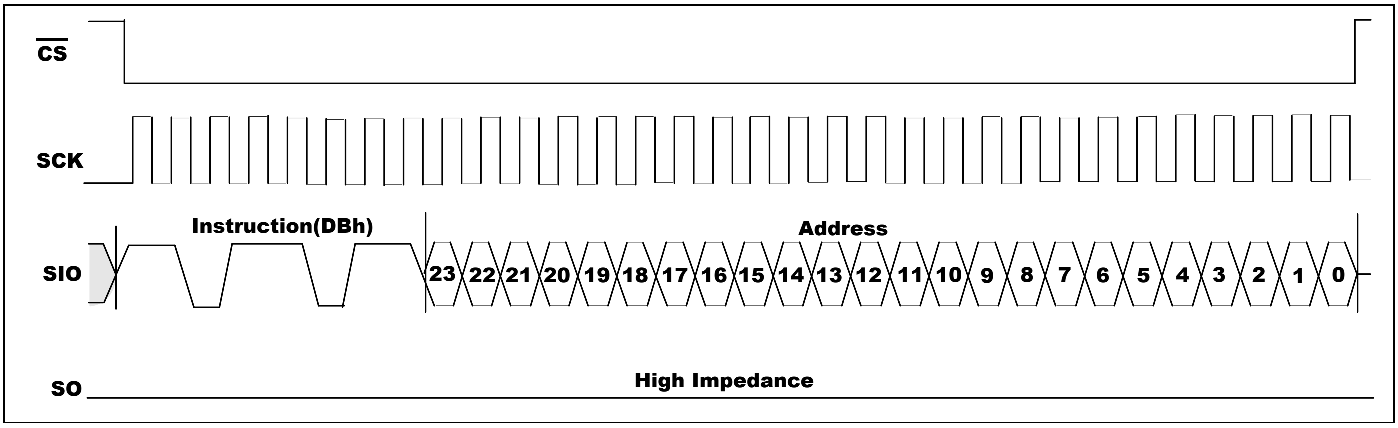


Figure 5-19: Page Erase (PE)



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	–0.5 to V_{CC} + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	℃
T_{STG}	Storage Temperature	–65 to +150	℃
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40℃ to +85℃	2.7V to 3.6V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

6.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: T_A = 25℃, f = 1 MHz, V_{CC} = 5.0V.

6.4 DC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, V_{CC} = 2.7V ~ 3.6V

Symbol	Parameter	V_{CC}	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			2.7		3.6	V
V_{IH}	Input High Voltage			0.7* V_{CC}		V_{CC}+1	V
V_{IL}	Input Low Voltage			-0.3		0.3* V_{CC}	V
I_{LI}	Input Leakage Current		V_{IN} = 0V To V_{CC}	-2		2	µA
I_{LO}	Output Leakage Current		V_{OUT} = 0V To V_{CC}, $\overline{CS}$ = V_{CC}	-2		2	µA
V_{OH}	Output High Voltage	2.7~3.6V	I_{OH} = -0.1mA	V_{CC}-0.2V		—	V
V_{OL}	Output Low Voltage	2.7~3.6V	I_{OL} = 1.6 mA	—		0.4	V
I_{CC1}	Page Program Current	3.6	Write at 33 MHz, SO=Open	—		1	mA
I_{CC2}	Erase Current	3.6	Write at 33 MHz, SO=Open	—		1	mA
I_{CC3}	Read Current	3.6	Read at 33 MHz, SO=Open	—		4	mA
I_{SB}	Standby Current	3.6	V_{IN}= V_{CC} or GND, $\overline{CS}$ = V_{CC}	—		1	µA

6.5 AC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, Supply voltage = 2.7V to 3.6V

Symbol	Parameter[1]	Min.	Typ	Max.	Unit
F_{SCK}	SCK Clock Frequency for fast read mode	0		66	MHz
F_{RSCK}	SCK Clock Frequency for normal read	0		33	MHz
T_{RI}	Input Rise Time	—		8	ns
T_{FI}	Input Fall Time	—		8	ns
T_{WH}	SCK High Time	8		—	ns
T_{WL}	SCK Low Time	8		—	ns
T_{CS}	$\overline{CS}$ High Time	25		—	ns
T_{CSS}	$\overline{CS}$ Setup Time	15		—	ns
T_{CSH}	$\overline{CS}$ Hold Time	5		—	ns
T_{SU}	Data In Setup Time	2		—	ns
T_H	Data In Hold Time	4		—	ns
T_{HD}	$\overline{HOLD}$ Setup Time	15		—	ns
T_{CD}	$\overline{HOLD}$ Hold Time	15		—	ns
T_V[2]	Output Valid	0		8	ns
T_{HO}	Output Hold Time	0		—	ns
T_{LZ}	$\overline{HOLD}$ to Output Low Z	0		200	ns
T_{HZ}	$\overline{HOLD}$ to Output High Z	—		200	ns
T_{DIS}	Output Disable Time	—		100	ns
T_{PP}	Page Program Time / Write Status Register Time	—	3	4	ms
T_{EPS}	Page/Sector Erase Time	—	2	3	ms
T_{EBC}	Block Erase Time	—	3	4	ms
T_{EBC}	Chip Erase Time	—	3	4	ms
T_{VCS}	V_{CC} Set-up Time	50	—	—	us

Notes: [1] The parameters are characterized but not 100% tested.

[2] C_L = 30pF (typical)

7. Ordering Information

Industrial Grade: -40°C to +85°C, Lead-free

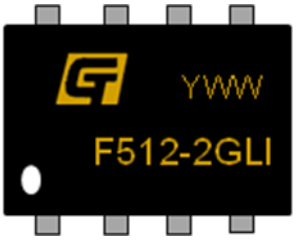
Voltage Range	Part Number*	Package (8-pin)*
2.7V to 3.6V	GT25F512-2GLI-TR	150-mil SOIC
	GT25F512-2ZLI-TR	3 x 4.4 mm TSSOP
	GT25F512-2UDLI-TR	2 x 3 x 0.55 mm UDFN

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The product is packed in tape and reel "-TR" (4K per reel), except UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

8. Top Markings

8.1 SOIC Package



G: Giantec Logo

F512-2GLI: GT25F512-2GLI-TR

YWW: Date Code, Y=year, WW=week

8.2 TSSOP Package

GT: Giantec Logo

F512-2ZLI: GT25F512-2ZLI-TR

YWW: Date Code, Y=year, WW=week

8.3 UDFN Package

GT: Giantec Logo

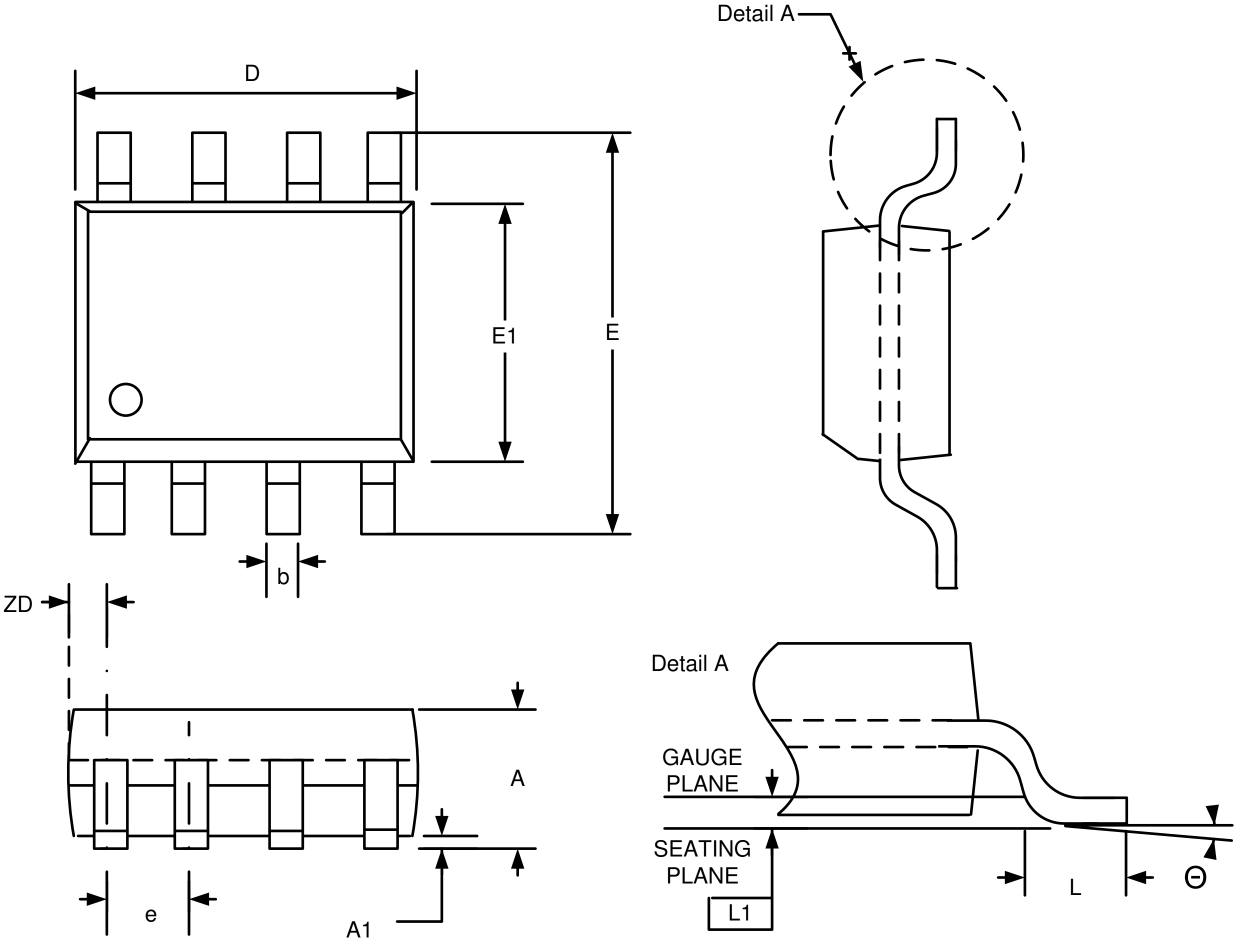
F9: GT25F512-2UDLI-TR

YWW: Date Code, Y=year, WW=week

9. Package Information

9.1 SOIC

8L 150mil SOIC Package Outline

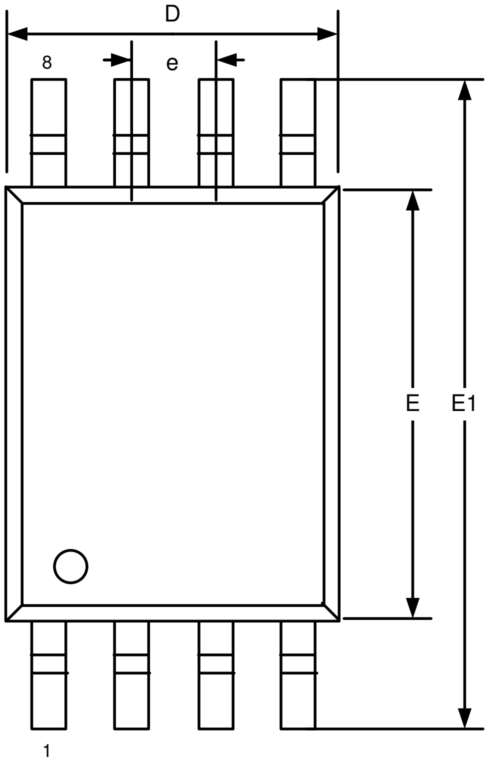


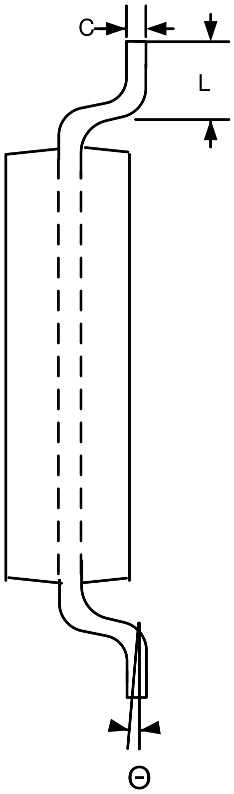
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

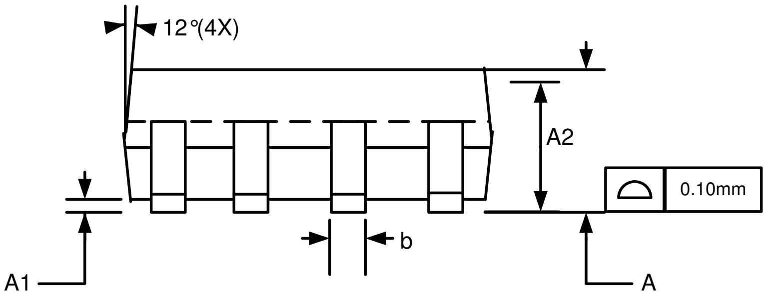
Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

9.2 TSSOP

8L 3x4.4mm TSSOP Package Outline





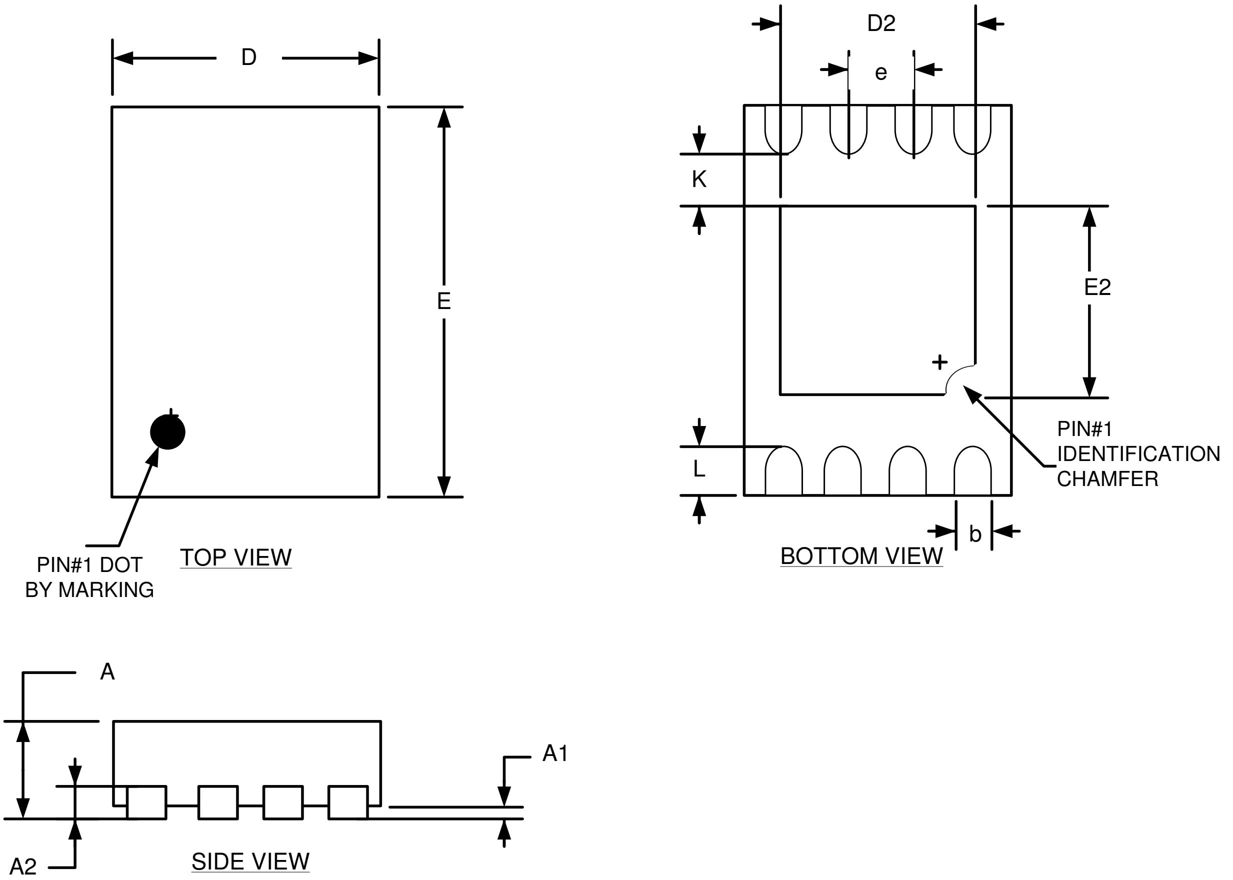


Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.4 BSC			0.252 BSC		
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

9.3 UDFN

8L 2x3mm UDFN Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

10. Revision History

Revision	Date	Descriptions
A0	Oct. 2013	Initial version