

# GT7172



## 3.5MHz, Low Power, CMOS, Rail-to-Rail Dual Operational Amplifier

**Advanced**

### 1. Features

- Single-Supply Operation from +2.2V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product: 3.5MHz (Typ.)
- Low Input Bias Current: 10pA (Typ.)
- Low Offset Voltage: 5mV (Max.)
- Quiescent Current: 270µA per Amplifier (Typ.)
- Operating Temperature: -40°C ~ +125°C
- Available in SOP8 and MSOP8 Packages

### 2. General Description

The GT7172 is wideband, low-noise, low-distortion dual operational amplifier, that offer rail-to-rail inputs/outputs and single-supply operation down to 2.2V. They draw 600uA of quiescent supply current while featuring ultra-low distortion (0.0002% THD+N), as well as low input voltage-noise density (11nV/ $\sqrt{\text{Hz}}$ ) and low input current-noise density (0.5fA/ $\sqrt{\text{Hz}}$ ). These features make the devices an ideal choice for applications that require low distortion and/or low noise.

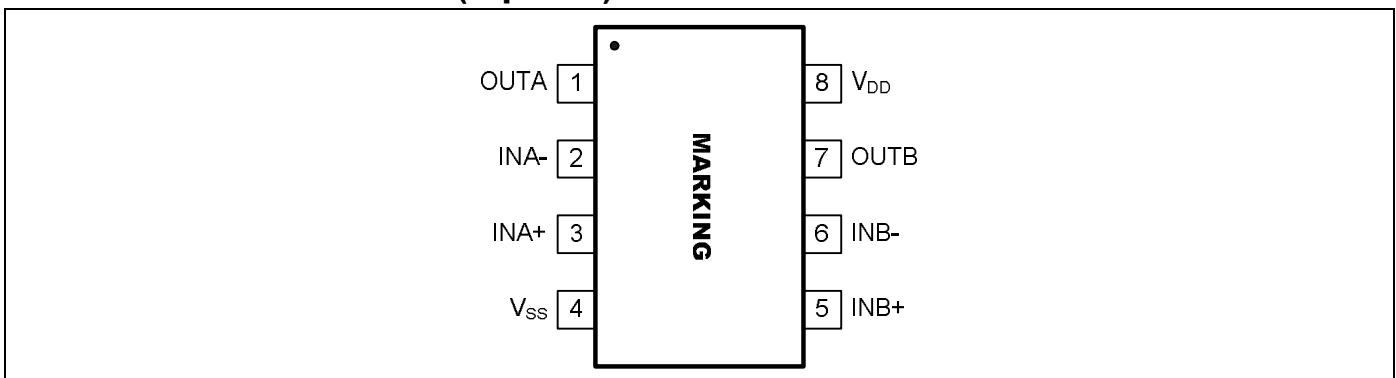
These amplifiers have inputs and outputs which swing rail-to-rail and their input common-mode voltage range includes ground. The maximum input offset of these amplifiers is less than 5mV. The GT7172 are unity-gain stable with a gain-bandwidth product of 3.5MHz. The GT7172 is available in SOP8 and MSOP8 packages. The extended temperature range of -40°C to +125°C over all supply voltages offers additional design flexibility.

### 3. Applications

- Portable Equipment
- Mobile Communications
- Smoke Detector
- Sensor Interface
- Medical Instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

### 4. Pin Configuration

#### 4.1 GT7172 SOP8 and MSOP8 (Top View)



**Figure 1. Pin Assignment Diagram (SOP8 and MSOP8 Package)**

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# **GT7172**

**Note:** Please see section “**Part Markings**” for detailed Marking Information.



# GT7172

## 5. Application Information

### 5.1 Size

GT7172 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the GT7172 series packages save space on printed circuit boards and enable the design of smaller electronic products.

### 5.2 Power Supply Bypassing and Board Layout

GT7172 series operates from a single 2.2V to 5.5V supply or dual  $\pm 1.1V$  to  $\pm 2.75V$  supplies. For best performance, a  $0.1\mu F$  ceramic capacitor should be placed close to the  $V_{DD}$  pin in single supply operation. For dual supply operation, both  $V_{DD}$  and  $V_{SS}$  supplies should be bypassed to ground with separate  $0.1\mu F$  ceramic capacitors.

### 5.3 Low Supply Current

The low supply current (typical  $270\mu A$ ) of GT7172 series will help to maximize battery life. They are ideal for battery powered systems

### 5.4 Operating Voltage

GT7172 series operate under wide input supply voltage (2.2V to 5.5V). In addition, all temperature specifications apply from  $-40^{\circ}C$  to  $+125^{\circ}C$ . Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime

### 5.5 Rail-to-Rail Input

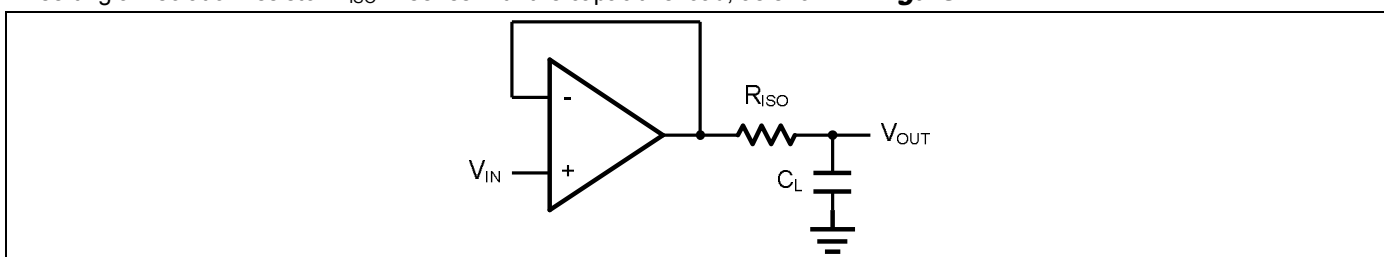
The input common-mode range of GT7172 series extends  $100mV$  beyond the supply rails ( $V_{SS}-0.1V$  to  $V_{DD}+0.1V$ ). This is achieved by using complementary input stage. For normal operation, inputs should be limited to this range.

### 5.6 Rail-to-Rail Output

Rail-to-Rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating in low supply voltages. The output voltage of GT7172 series can typically swing to less than  $10mV$  from supply rail in light resistive loads ( $>100k\Omega$ ), and  $60mV$  of supply rail in moderate resistive loads ( $10k\Omega$ ).

### 5.7 Capacitive Load Tolerance

The GT7172 series can directly drive  $250pF$  capacitive load in unity-gain without oscillation. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. In unity-gain configurations, the capacitive load drive can be improved by inserting an isolation resistor  $R_{ISO}$  in series with the capacitive load, as shown in **Figure 2**.



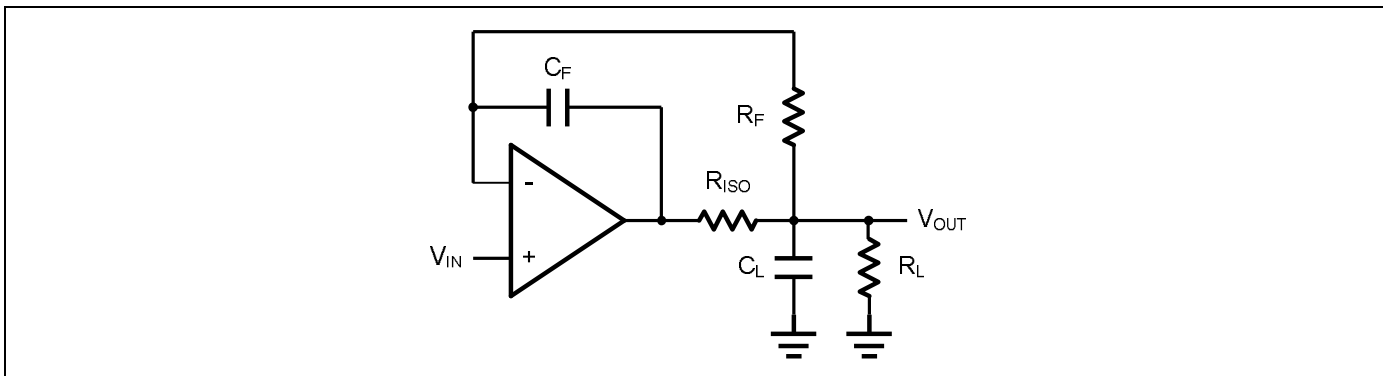
**Figure 2. Indirectly Driving a Capacitive Load Using Isolation Resistor**

The bigger the  $R_{ISO}$  resistor value, the more stable  $V_{OUT}$  will be. However, if there is a resistive load  $R_L$  in parallel with the capacitive load, a voltage divider (proportional to  $R_{ISO}/R_L$ ) is formed, this will result in a gain error.

The circuit in **Figure 3** is an improvement to the one in **Figure 2**.  $R_F$  provides the DC accuracy by feed-forward the  $V_{IN}$  to  $R_L$ .  $C_F$  and  $R_{ISO}$  serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased

# GT7172

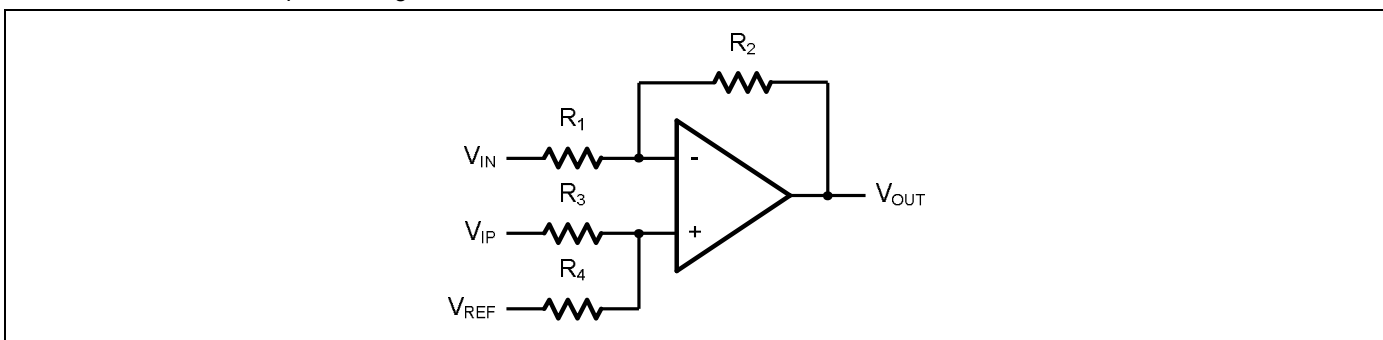
by increasing the value of  $C_F$ . This in turn will slow down the pulse response.



**Figure 3. Indirectly Driving a Capacitive Load with DC Accuracy**

## 5.8 Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common to the two inputs. It is useful as a computational amplifier in making a differential to single-end conversion or in rejecting a common mode signal. **Figure 4.** shows the differential amplifier using GT7172.



**Figure 4. Differential Amplifier**

$$V_{OUT} = \left(\frac{R_1+R_2}{R_3+R_4}\right) \frac{R_4}{R_1} V_{IN} - \frac{R_2}{R_1} V_{IP} + \left(\frac{R_1+R_2}{R_3+R_4}\right) \frac{R_3}{R_1} V_{REF}$$

If the resistor ratios are equal (i.e.  $R_1=R_3$  and  $R_2=R_4$ ), then

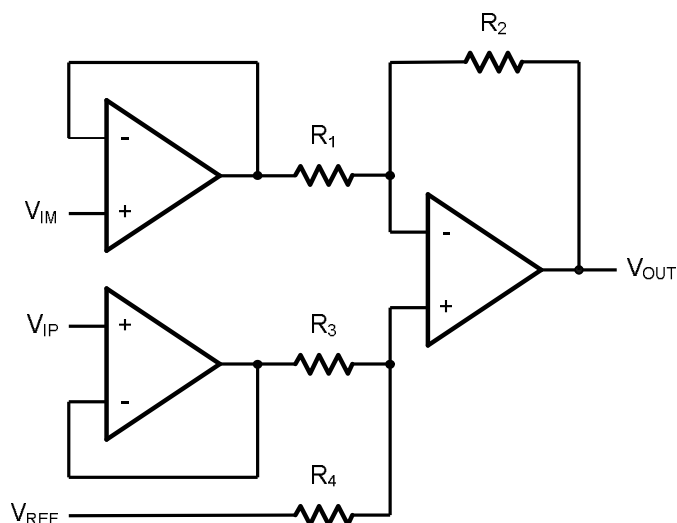
$$V_{OUT} = \frac{R_2}{R_1} (V_{IP} - V_{IN}) + V_{REF}$$

## 5.9 Instrumentation Amplifier

The input impedance of the previous differential amplifier is set by the resistors  $R_1$ ,  $R_2$ ,  $R_3$ , and  $R_4$ . To maintain the high input impedance, one can use a voltage follower in front of each input as shown in the following two instrumentation amplifiers.

## 5.10 Three-Op-Amp Instrumentation Amplifier

The dual GT7172 can be used to build a three-op-amp instrumentation amplifier as shown in **Figure 5.**



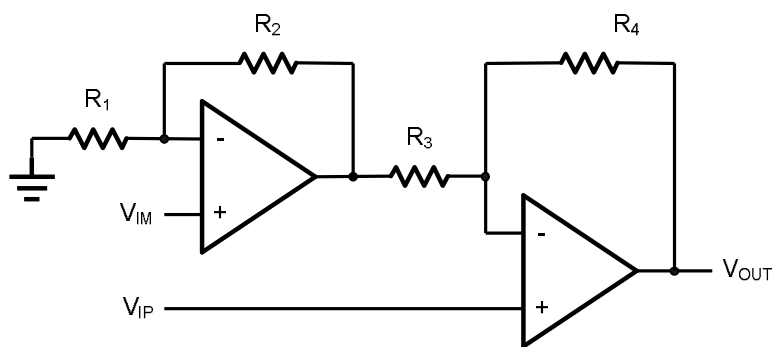
**Figure 5. Three-Op-Amp Instrumentation Amplifier**

The amplifier in **Figure 5** is a high input impedance differential amplifier with gain of  $R_2/R_1$ . The two differential voltage followers assure the high input impedance of the amplifier.

$$V_o = \left(1 + \frac{R_4}{R_3}\right)(V_{IP} - V_{IN})$$

## 5.11 Two-Op-Amp Instrumentation Amplifier

GT7172 can also be used to make a high input impedance two-op-amp instrumentation amplifier as shown in **Figure 6**.

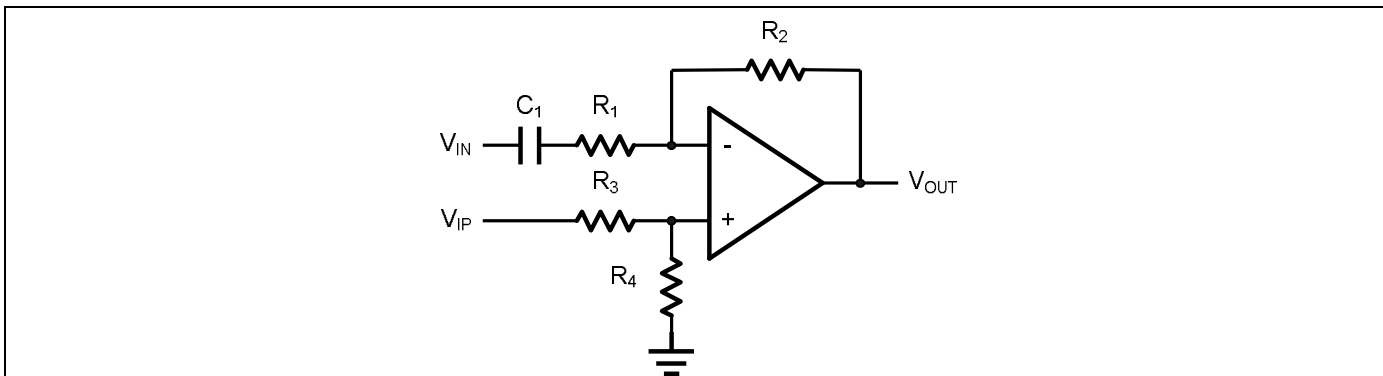


**Figure 6. Two-Op-Amp Instrumentation Amplifier**

Where  $R_1=R_3$  and  $R_2=R_4$ . If all resistors are equal, then  $V_o=2(V_{IP}-V_{IN})$

## 5.12 Single-Supply Inverting Amplifier

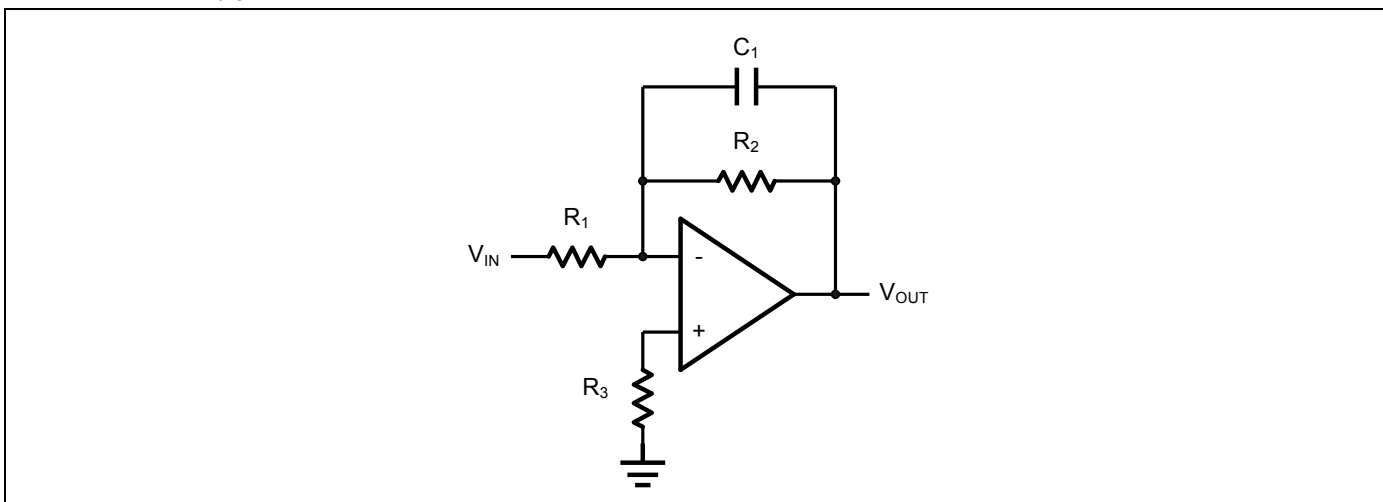
The inverting amplifier is shown in Figure 6. The capacitor  $C_1$  is used to block the DC signal going into the AC signal source  $V_{IN}$ . The value of  $R_1$  and  $C_1$  set the cut-off frequency to  $f_c=1/(2\pi R_1 C_1)$ . The DC gain is defined by  $V_{OUT}=-R_2/R_1 V_{IN}$



**Figure 7. Single Supply Inverting Amplifier**

## 5.13 Low Pass Active Filter

The low pass active filter is shown in **Figure 8**. The DC gain is defined by  $-R_2/R_1$ . The filter has a -20dB/decade roll-off after its corner frequency  $f_c=1/(2\pi R_3 C_1)$ .



**Figure 8. Low Pass Active Filter**

## 5.14 Sallen-Key 2<sup>nd</sup> Order Active Low-Pass Filter

GT7172 can be used to form a 2<sup>nd</sup> order Sallen-Key active low-pass filter as shown in **Figure 9**. The transfer function from  $V_{IN}$  to  $V_{OUT}$  is given by

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{\frac{1}{C_1 C_2 R_1 R_2} A_{LP}}{S^2 + S \left( \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} \frac{A_{LP}}{C_2 R_2} \right) + \frac{1}{C_1 C_2 R_1 R_2}}$$

Where the DC gain is defined by  $A_{LP}=1+R_3/R_4$ , and the corner frequency is given by

$$\omega C = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}}$$

The pole quality factor is given by

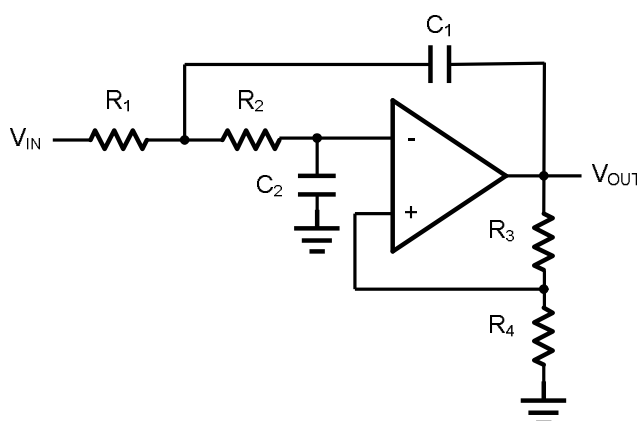
# GT7172

$$\frac{\omega C}{Q} = \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2}$$

Let  $R_1=R_2=R$  and  $C_1=C_2=C$ , the corner frequency and the pole quality factor can be simplified as below

$$\omega_C = \frac{1}{CR}$$

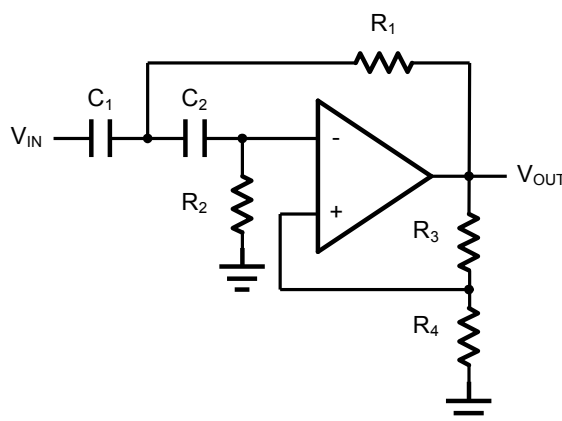
And  $Q=2-R_3/R_4$



**Figure 9. Sallen-Key 2nd Order Active Low-Pass Filter**

## 5.15 Sallen-Key 2<sup>nd</sup> Order high-Pass Active Filter

The 2<sup>nd</sup> order Sallen-key high-pass filter can be built by simply interchanging those frequency selective components  $R_1$ ,  $R_2$ ,  $C_1$ , and  $C_2$  as shown in **Figure 10**.



**Figure 10. Sallen-Key 2nd Order Active High-Pass Filter**

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{S^2 A_{HP}}{S^2 + S\left(\frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} + \frac{1-A_{HP}}{C_1 R_1}\right) + \frac{1}{C_1 C_2 R_1 R_2}}$$

Where  $A_{HP}=1+R_3/R_4$



# GT7172

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage ( $V_{DD}$ to $V_{SS}$ )	-0.5V	+7V
Analog Input Voltage ( $IN+$ or $IN-$ )	$V_{SS}-0.5V$	$V_{DD}+0.5V$
PDB Input Voltage	$V_{SS}-0.5V$	+7V
Operating Temperature Range	-40°C	+125°C
Junction Temperature	+150°C	
Storage Temperature Range	-65°C	+150°C
Lead Temperature (soldering, 10sec)	+300°C	
Package Thermal Resistance ( $T_A=+25^\circ C$ )		
SOP8, $\theta_{JA}$	130°C	
MSOP8, $\theta_{JA}$	210°C	

**Note:** Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



# GT7172

## 6.2 Electrical Characteristics

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L = 100K$  tied to  $V_{DD}/2$ ,  $SHDNB = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Notes 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply-Voltage Range	$V_{DD}$	Guaranteed by the PSRR test	2.2	-	5.5	V
Quiescent Supply Current (per Amplifier)	$I_{DD}$	$V_{DD} = 3V$	-	270	-	$\mu A$
		$V_{DD} = 5V$	-	270	1.2	
Input Offset Voltage	$V_{OS}$	$T_A = +25^\circ C$	-	$\pm 0.4$	$\pm 5$	mV
		$T_A = -40^\circ C$ to $+85^\circ C$	-	-	-	
		$T_A = -40^\circ C$ to $+125^\circ C$	-	-	$\pm 5$	
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$		-	$\pm 0.3$	$\pm 6$	$\mu V/^\circ C$
Input Bias Current	$I_B$	(Note 3)	-	$\pm 1$	$\pm 100$	pA
Input Offset Current	$I_{OS}$	(Note 3)	-	$\pm 1$	$\pm 100$	pA
Input Common-Mode Voltage Range	$V_{CM}$	Guaranteed by the $T_A = 25^\circ C$	-0.2	-	$V_{DD} + 0.2$	V
		CMRR test $T_A = -40^\circ C$ to $+125^\circ C$	0	-	$V_{DD}$	
Common-Mode Rejection Ratio	CMRR	$V_{SS} - 0.2V \leq V_{CM} \leq V_{DD} + 0.2V$ $T_A = +25^\circ C$	-	75	-	dB
		$V_{SS} \leq V_{CM} \leq 5V$ $T_A = +25^\circ C$	65	80	-	
		$V_{SS} - 0.2V \leq V_{CM} \leq V_{DD} + 0.2V$ $T_A = -40^\circ C$ to $+125^\circ C$	-	65	-	
Power-Supply Rejection Ratio	PSRR	$V_{DD} = +2.2V$ to $+5.5V$	75	90	-	dB
Open-Loop Voltage Gain	$A_V$	$R_L = 100k\Omega$ to $V_{DD}/2$ , $100mV \leq V_O \leq V_{DD} - 125mV$	90	100	-	dB
		$R_L = 1k\Omega$ to $V_{DD}/2$ , $200mV \leq V_O \leq V_{DD} - 250mV$	75	85	-	
		$R_L = 500\Omega$ to $V_{DD}/2$ , $350mV \leq V_O \leq V_{DD} - 500mV$	55	65	-	
Output Voltage Swing	$V_{OUT}$	$ V_{IN+} - V_{IN-}  \geq 10mV$ $V_{DD} - V_{OH}$	-	10	35	mV
		$R_L = 10k\Omega$ to $V_{DD}/2$ $V_{OL} - V_{SS}$	-	10	30	
		$ V_{IN+} - V_{IN-}  \geq 10mV$ $V_{DD} - V_{OH}$	-	80	200	
		$R_L = 1k\Omega$ to $V_{DD}/2$ $V_{OL} - V_{SS}$	-	50	150	
		$ V_{IN+} - V_{IN-}  \geq 10mV$ $V_{DD} - V_{OH}$	-	100	350	



# GT7172

		$R_L = 500\Omega$ to $V_{DD}/2$ $V_{OL}-V_{SS}$		80	260	
Output Short-Circuit Current	$I_{SC}$	Sinking or Sourcing	-	$\pm 50$	-	mA
PDB Logic Low	$V_{IL}$		-	-	0.8	V
PDB Logic High	$V_{IH}$		2	-	-	V
Turn-On Time	$T_{ON}$		-	2.2	-	$\mu s$
Turn-Off Time	$T_{OFF}$		-	0.8	-	$\mu s$
Output Leakage Current	$I_{LEAK}$	Shutdown Mode (PDB = $V_{SS}$ ), $V_{OUT} = V_{SS}$ to $V_{DD}$	-	$\pm 0.001$	$\pm 1.0$	$\mu A$
Input Capacitance	$C_{IN}$			10		pF
Gain Bandwidth Product	GBW	$A_V = +1V/V$	-	3.5	-	MHz
Slew Rate	SR	$A_V = +1V/V$	-	1.8	-	V/ $\mu s$
Full Power Bandwidth		$A_V = +1V/V$	-	0.4	-	MHz
Phase Margin	$\phi_m$	$A_V = +1V/V$	-	55°	-	deg
Gain Margin	$G_m$	$A_V = +1V/V$	-	12	-	dB
Settling Time	$t_s$	To 0.01%, $V_{OUT} = 2V$ step $A_V = +1V/V$	-	1	-	$\mu s$
Capacitive-Load Stability	$C_{LOAD}$	No sustained oscillations. $A_V = +1V/V$	-	200	-	pF
Peak-to-Peak Input Noise Voltage (Note 5)	$e_n(p-p)$	$f = 0.1Hz$ to 10Hz	-	5	-	$\mu V_{p-p}$
Input Voltage Noise Density	$e_n$	$f = 10Hz$	-	30	-	nV/ $\sqrt{Hz}$
		$f = 1kHz$	-	11	-	
		$f = 30kHz$	-	7	-	
Input Current Noise Density	$i_n$	$f = 1kHz$				fA/ $\sqrt{Hz}$
Total Harmonic Distortion plus Noise	THD+N	$V_{OUT} = 2V_{PP}$ , $A_V = +1V/V$ , $f = 1kHz$	-	0.0001	-	%
		$R_L = 10k\Omega$ to GND $f = 20kHz$	-	0.002	-	
		$V_{OUT} = 2V_{PP}$ , $A_V = +1V/V$ , $f = 1kHz$	-	0.0002	-	
		$R_L = 1k\Omega$ to GND $f = 20kHz$	-	0.004	-	

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ C$ ; all specifications over the automotive temperature range is guaranteed by design, not production tested.

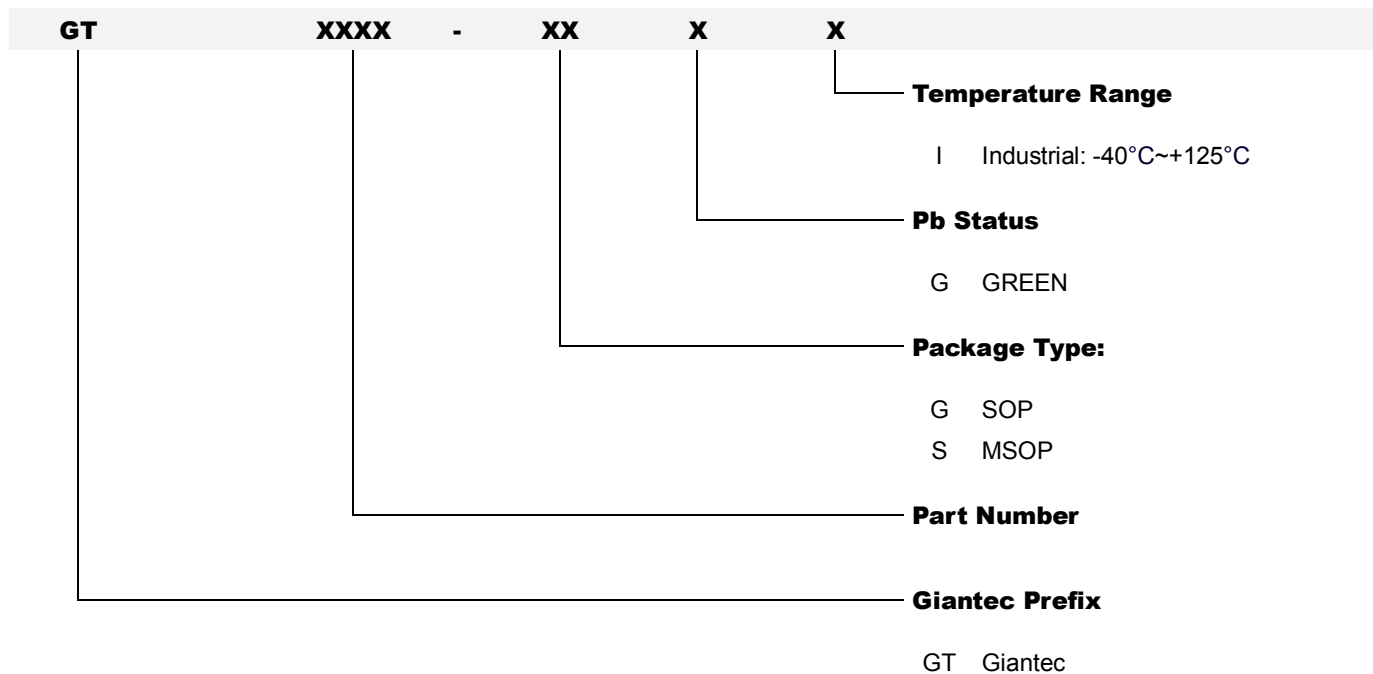
**Note 2:** Parameter is guaranteed by design.

**Note 3:** Peak-to-peak input noise voltage is defined as six times RMS value of input noise voltage.



# GT7172

## 7. Ordering Information



Order Number	Package Description	Package Option
GT7172-GGI-TR	SOP8	Tape and Reel 4000
GT7172-SGI-TR	MSOP8	Tape and Reel 4000



# GT7172

## 8. Part Markings

### 8.1 GT7172-GGI (Top View)

<u>G</u>	<u>T</u>	<u>7</u>	<u>1</u>	<u>2</u>	<u>2</u>	<u>G</u>	<u>G</u>	<u>I</u>
—	—	—	Lot Number			—	—	—
•		<u>Y</u>	<u>Y</u>	<u>W</u>	<u>W</u>	<u>S</u>	<u>V</u>	

#### GT7172GGI

##### Lot Number

States the last 9 characters of the wafer lot information

•

Pin 1 Indicator

YY

Seal Year

00 = 2000

01 = 2001

99 = 2099

WW

Seal Week

01 = Week 1

02 = Week 2

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.

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51 = Week 51

52 = Week 52

S

Subcon Code

J = ASESH

L = ASEKS

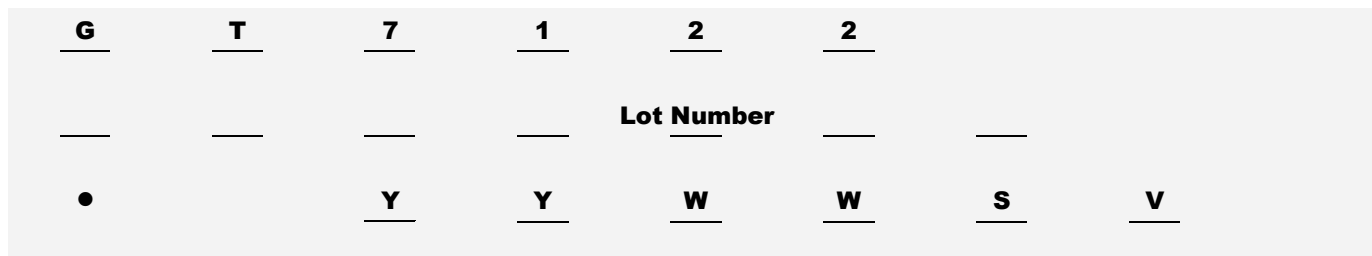
V

Die Version



# GT7172

## 8.2 GT7172-SGI (Top View)



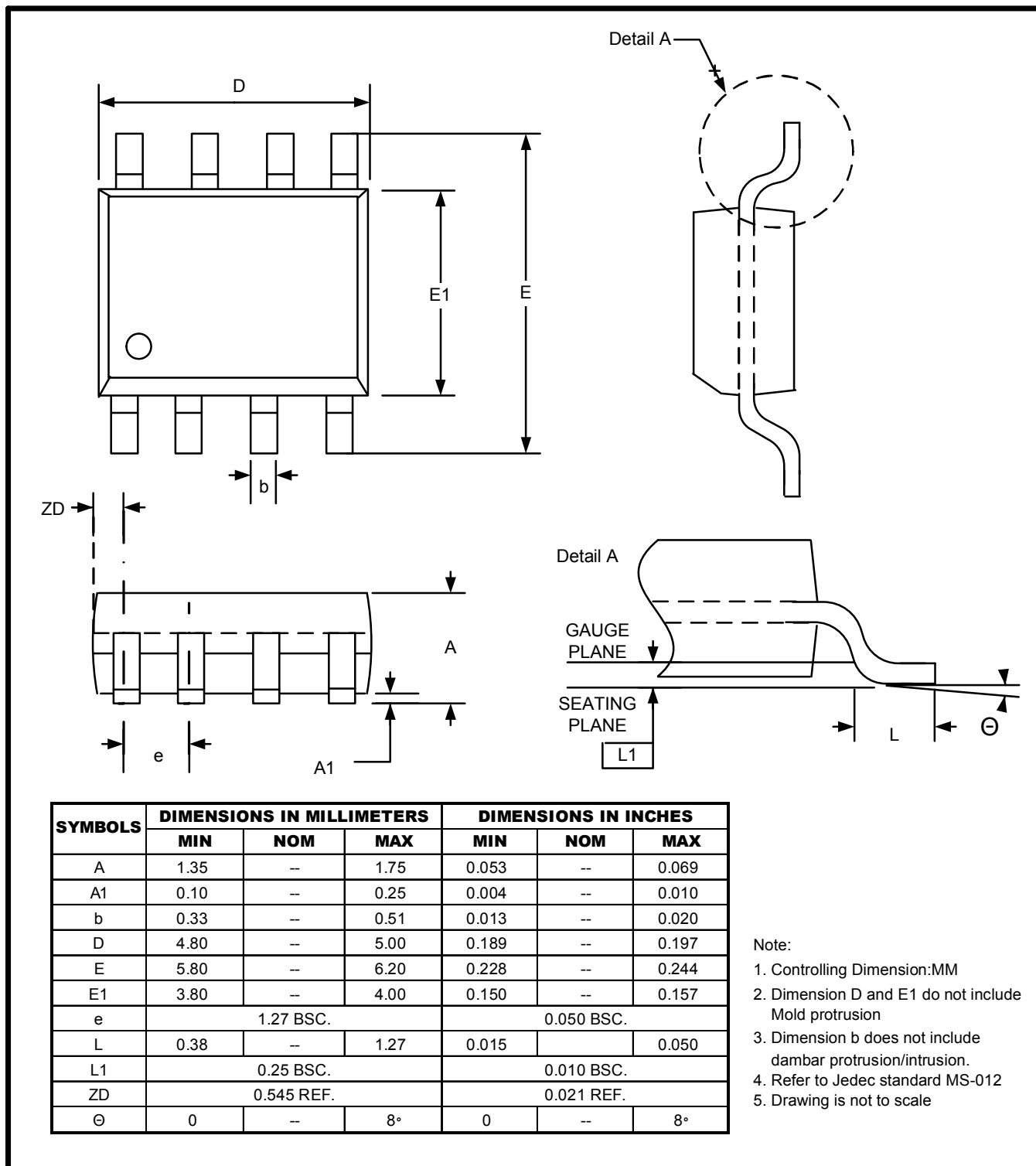
<b>GT7172</b>	GT7172-SGI
<b>Lot Number</b>	States the last 9 characters of the wafer lot information
•	Pin 1 Indicator
<b>YY</b>	Seal Year 00 = 2000 01 = 2001 99 = 2099
<b>WW</b>	Seal Week 01 = Week 1 02 = Week 2 . . . 51 = Week 51 52 = Week 52
<b>S</b>	Subcon Code J = ASESH L = ASEKS
<b>V</b>	Die Version



# GT7172

## 9. Package Information

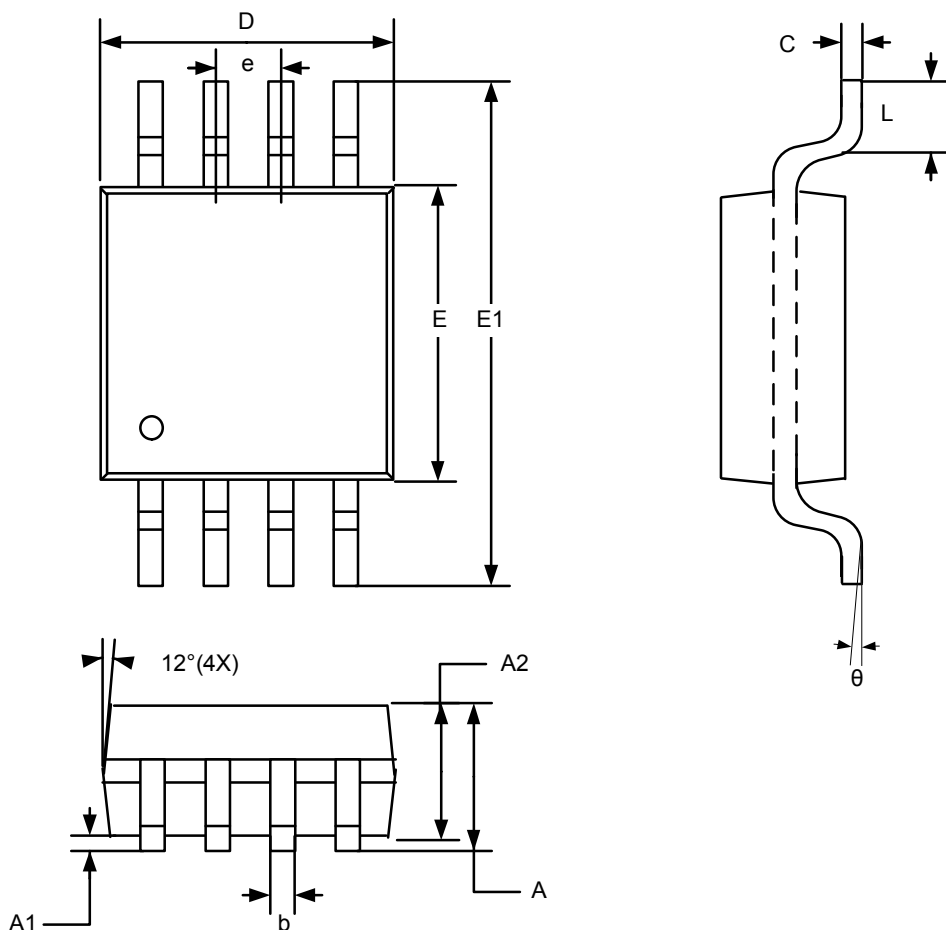
### 9.1 SOP8





# GT7172

## 9.2 MSOP8



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	--	0.15	0.002	--	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.25	--	0.40	0.010	--	0.016
C	0.13	--	0.23	0.005	--	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	4.90 BSC			0.193 BSC		
e	0.65 BSC			0.026 BSC		
L	--	--	0.55	--	--	0.022
Θ	0	--	7°	0	--	7°

- Note:
1. Controlling Dimension:MM
  2. Dimension D and E1 do not include Mold protrusion
  3. Refer to Jedec standard MO187
  4. Drawing is not to scale



# GT7172

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## 10. Revision History

Revision	Date	Descriptions
A0	Oct.,2011	Initial Version