

# GT5010



## Accurate CV/CC Primary-Side Controller

**Advanced**

### 1. Features

- $\pm 5\%$  CV/CC Regulation
- Low standby power less than 30mW
- Eliminates Opto-coupler and all secondary CV/CC control circuitry
- Eliminates control loop compensation
- Innovative current sampling technology
- Programmable line compensation for tighter CC regulation
- Built-in compensation for transformer inductance

### 2. General Description

GT5010 simplifies low power CV/CC charger/adaptor designs by eliminating opto-coupler and secondary control circuitry through innovative primary-side current sampling and control technology. Very tight output voltage and current regulation is realized as shown in the **Figure.1** below.

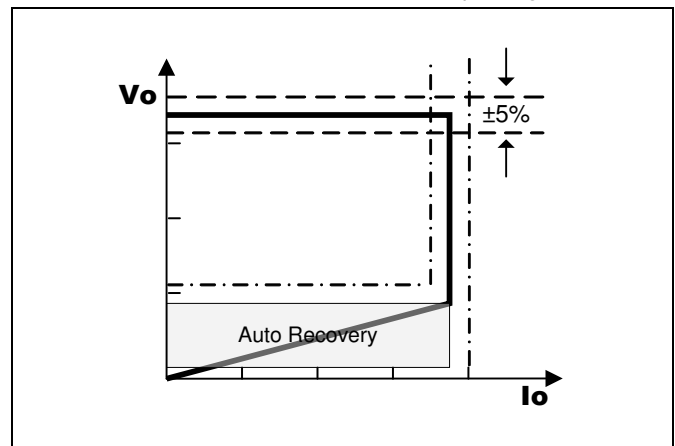
GT5010 proprietary Mixed PWM/PFM operation and Sleeping-mode operation are utilized to achieve low standby power less than 30mW, high efficiency and audio & noise free. The frequency jittering could also greatly reduce EMI filter cost.

GT5010 offers rich protection features including Cycle-by-Cycle peak current limiting, VCC UVLO, OVP and Clamp. The controller continues attempting start-up until the

tolerances

- Programmable Output Cable Compensation
- Built-in Leading Edge Blanking (LEB)
- Cycle-by-Cycle Current Limiting
- VCC Under Voltage Lockout with Hysteresis (UVLO)
- Built-in short circuit protection and output over voltage protection
- Built-in over temperature protection
- SOT-23-6 Package

fault condition is removed. Every restart is a soft start. The GT5010 is available in an SOT-23-6 package.



**Figure 1. Typical CC/CV Curve**

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# GT5010

## 3. Applications

- Cell/cordless Phone Charger
- PDAs/Portable audio devices Charger
- Small Power Adaptor/Charger
- LED driver
- Standby supplies for consumer electronics

## 4. Functional Block Diagram

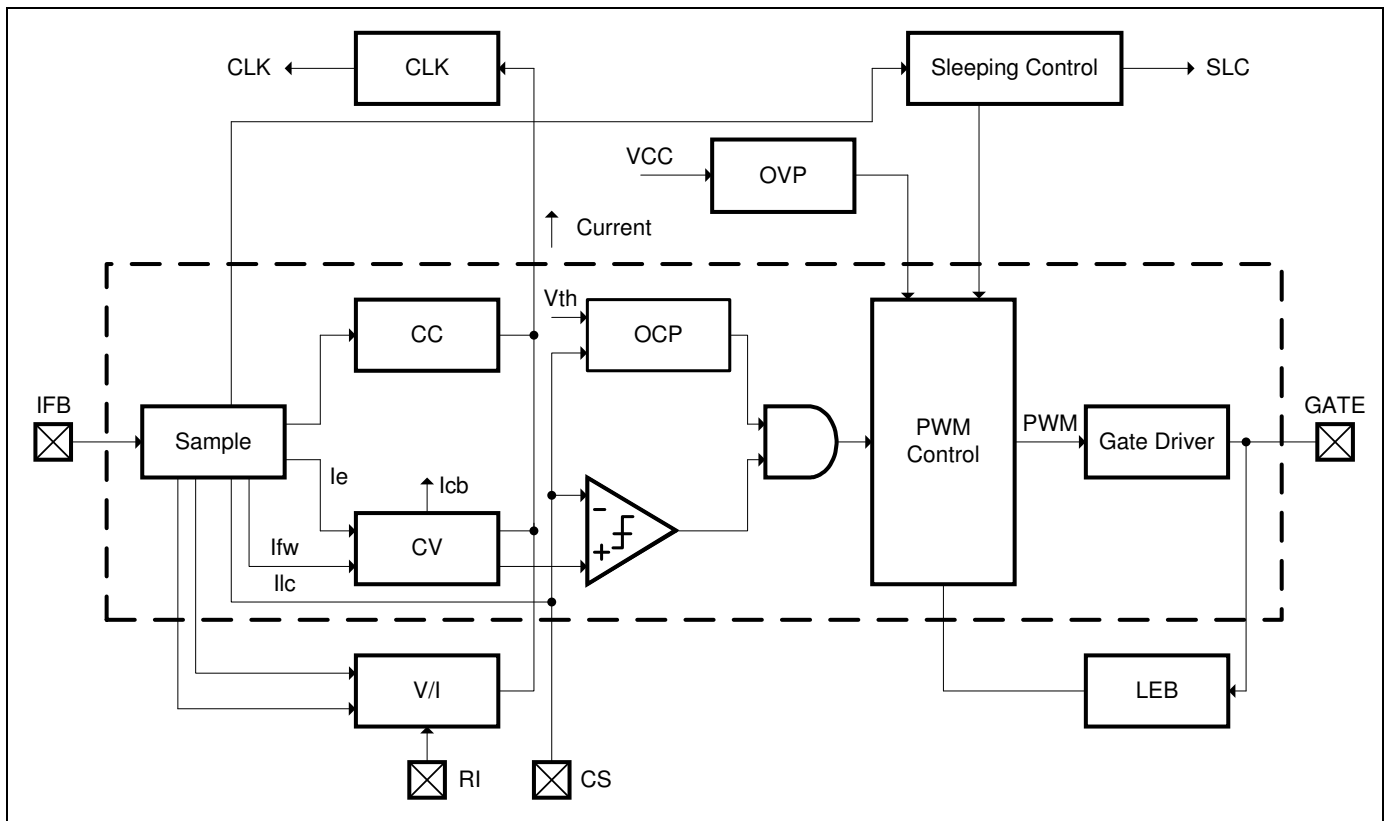


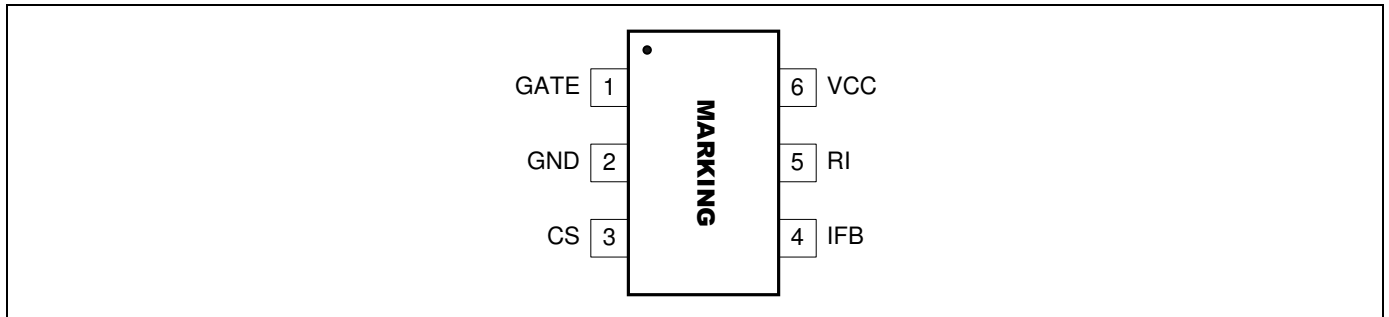
Figure 2. Functional Block Diagram



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## 5. Pin Configuration

### 5.1 Pin Assignment Top View



**Figure 3. Pin Configuration (SOT-23-6 Package)**

**Note:** Please see section “**Part Markings**” for detailed Marking Information.

### 5.2 Pin Descriptions

Pin #	Name	I/O	Function
1	GATE	O	Gate driver output for power MOSFET.
2	GND	-	IC ground
3	CS	I	This pin could detect the primary current by the voltage of sensing resistor connected from Source to GND.
4	IFB	I	Detecting the output information by current sampling
5	RI	O	Programmable output cable voltage loss compensation
6	VCC	-	IC power supply



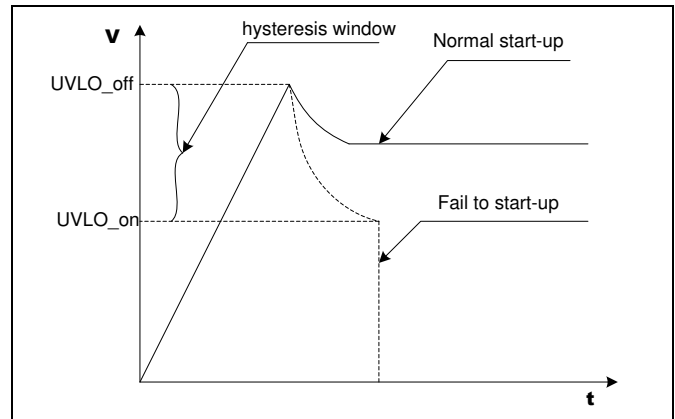
# GT5010

## 6. Functional Description

The GT5010 is an innovative AC-DC controller in which a new proprietary primary-side control technology is employed to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. Additionally, some new technology is adopted to further improve performance.

### 6.1 Start-up

Due to an innovative internal start-up circuit and adaptive sleeping control technology adopted, when the system with GT5010 is powered on, pin VCC can be charged to a voltage higher than start-up threshold UVLO\_off by a very large start-up resistor (>8MΩ), which causes GT5010 to enter into normal operation state. Meanwhile the VCC decoupling capacitor is allowed to use a smaller value (<2μF) compared with traditional design, therefore the start-time can be limited within a reasonable range. After the system enters into normal operation state, pin GATE of IC begins to output PWM driving signal to drive the external Power MOS switch and transfer power to the secondary stage, while a 1~2mA of operation current is required by the controller IC GT5010. At the initial stage of start-up, the current consumed by GT5010 is provided by VCC decoupling capacitor, therefore the voltage on VCC decoupling capacitor will gradually decrease; at the same time, as the output voltage rises up, the voltage of auxiliary coil of the transformer increases proportionally also. Eventually, when the voltage of auxiliary coil reaches the voltage of decoupling capacitor, the auxiliary coil will replace the decoupling capacitor as power supply of the control IC GT5010. The timing diagram of start-up is illustrated in **Figure.4**.



**Figure 4. Timing Diagram of Start-up**

As illustrated in **Figure.4**, a hysteresis window for internal UVLO comparator is necessary to prevent the control IC GT5010 from shutting down due to voltage dip during start-up.

### 6.2 Constant Voltage (CV) Operation

In order to achieve a precise output-voltage regulation, the information about output and load condition must be real-time sensed. For primary side control flyback converter, the output information can be feedback to primary side of the transformer via the auxiliary winding. **Figure.5** illustrates the waveform of auxiliary winding. As shown, during power switch-on, rectified input voltage VIN is mapped to the Auxiliary winding with a coefficient -NAUX/NP. The voltage can be expressed as:

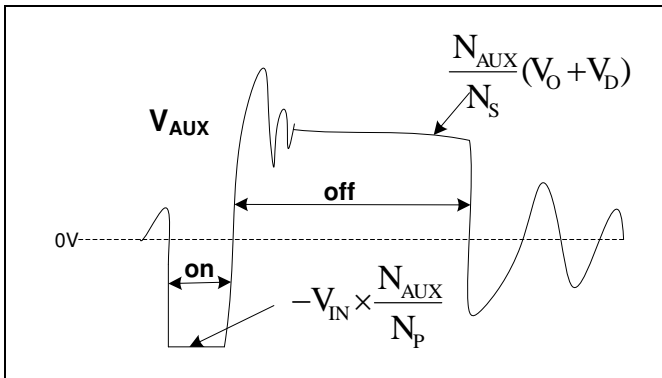
$$V_{AUX} = -V_{IN} \times \frac{N_{AUX}}{N_P}$$

Where NAUX is the turns of Auxiliary winding and NP is the turns of primary winding.

During power switch-off, the voltage at secondary-side winding is mapped to the auxiliary winding, which is expressed as:

$$V_{AUX} = \frac{N_{AUX}}{N_S} (V_O + V_D)$$

Where NS is the turns of secondary-side winding and VD is the voltage drop through the output rectifier diode.



**Figure 5. Waveform of Auxiliary Winding**

As shown in the typical application circuit,  $R_{FB}$  is used to transform the  $V_{AUX}$  voltage to a feedback current signal which is fed into pin  $I_{fb}$  of GT5010.  $I_{fb}$  current is further regulated to the same level as an internal reference current  $I_{ref}$  which can be set by an external resistor  $R_I$  (connected to pin  $R_I$ ), eventually, the regulated output voltage is equal to:

$$V_O = \frac{N_S}{N_{AUX}} \cdot \left( \frac{R_{FB}}{4R_I} + 1 \right) \cdot V_D$$

Where the internal reference current  $I_{ref}$  equals to  $1/4R_I$ . The recommended range for  $R_I$  is from  $7k\Omega$  to  $20k\Omega$ .

### 6.3 Constant current(CC) Operation

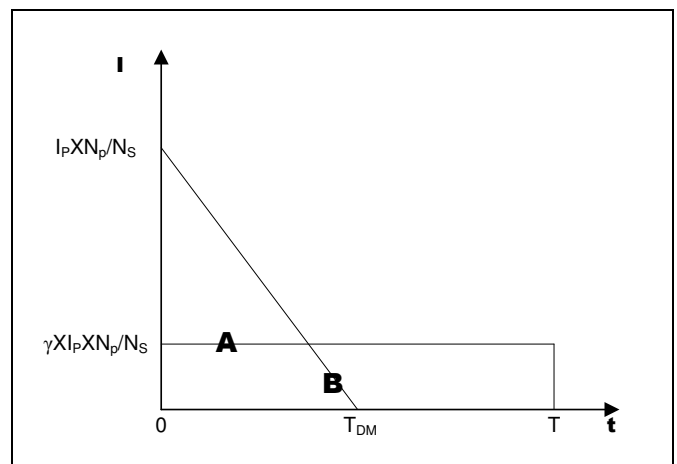
In battery charging and LED lighting applications, constant output current is required regardless of output voltage. In order to regulate output current to a constant level, a ratio regulation algorithm is employed in the control IC.

**Figure.6** illustrates the theory of the algorithm. As shown in **Figure.6**,  $I_p$  is the peak current flowing through the primary-side sense resistor. When switch turns off, the peak current is mapped to secondary-side with a coefficient  $N_P/N_S$ . Due to the demagnetization of secondary-side winding, peak current linearly decreases to zero. The area of the triangle in **Figure.6** indicates the current integration of a cycle at secondary-side winding where  $t_{DM}$  is demagnetization time of the secondary-side inductance  $L_s$ ,  $T$  is a switching period of the power converter system and  $I_P \times N_P/N_S$  is the peak current of secondary-side winding. So, the average output current can be expressed as:

$$I_O = \frac{1}{2} \times \frac{T_{DM}}{T} \times \frac{N_P}{N_S} \times I_P = \frac{1}{2} \times \gamma \times \frac{N_P}{N_S} \times I_P$$

where  $\gamma$  is the ratio of the demagnetizing time to the switching period. Assuming the primary-side peak current  $I_P$  is regulate to a constant level, the constant output current can be obtained by regulating  $\gamma$  to a constant. In the power converter system based on GT5010, constant current can be defined as:

$$I_O = 0.245 \times \frac{N_P}{N_S} \times I_P$$



**Figure 6. Diagram of output current**

On the other hand, maximum output power can be expressed as:

$$P_{O\_MAX} = \frac{1}{2} \times L_P \times I_{P\_MAX}^2 \times f_{MAX}$$

Therefore, constant maximum output current can also be expressed as:

$$I_{O\_MAX} = \frac{1}{2} \times \frac{1}{V_{O\_MAX}} \times L_P \times I_{P\_MAX}^2 \times f_{MAX}$$

Where  $I_{O\_MAX}$  indicates the constant maximum output current,  $V_{O\_MAX}$  indicates the maximum output voltage,  $L_P$  is the inductance of primary-side winding,  $I_{P\_MAX}$  is the maximum primary peak current,  $f_{MAX}$  is the maximum operation frequency.

Obviously, for a given  $I_{O\_MAX}$ ,  $I_{P\_MAX}$ ,  $V_{O\_MAX}$ , the maximum operation frequency can be defined through setting the



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inductance  $L_P$  of primary-side winding.

## 6.4 Output Cable Compensation

The cable compensation is implemented by adding up an offset current over internal reference current  $I_{ref}$ . The offset current that is used to compensate cable drop proportionally increases with output load. The amount of compensation added upon output load can be defined by selecting  $R_I$  and  $R_{FB}$ , according to below equation:

$$\Delta V_C = 0.064 \times \frac{R_I (K\Omega)}{10K\Omega} \times (V_O + V_D)$$

where  $7k\Omega < R_I < 20k\Omega$ .

## 6.5 Built-in Line Compensation

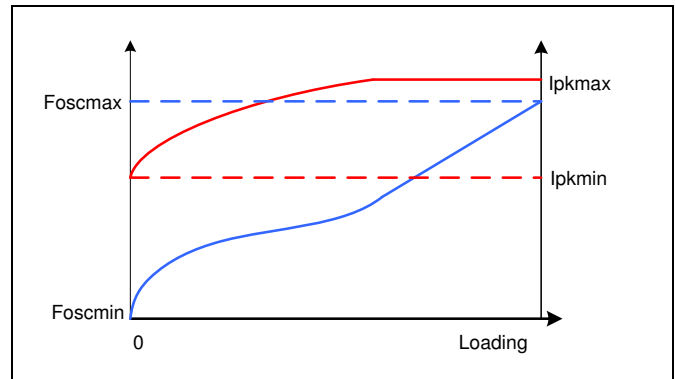
In the flyback converter system with GT5010, line voltage compensation can be simply implemented and programmed by inserting a resistor  $R_{LN}$  between pin CS and current sense resistor  $R_s$ .

The line compensation voltage  $\Delta V_{LN}$  can be calculated according to below equation:

$$\Delta V_{LN} = k \times V_{IN} \times \frac{N_{AUX}}{N_P} \times \frac{R_{LN}}{R_{FB}}$$

## 6.6 Mixed PWM/PFM operation

In order to trade off among different characteristics such as efficiency, no-load standby, audio noise, ripple, a mixed PWM/PFM operation mode is employed in GT5010. Under constant voltage (CV) mode, from middle load to full load, the system with GT5010 operates on a pure PFM mode; from middle load to no-load, the system operates on a combined PWM/PFM mode. **Figure.7** illustrates the trend of frequency and CS peak following load-change.



**Figure 7. Fosc and Ipk vs. Loading**

## 6.7 Protection Features

Complete protection features are integrated into GT5010, which include built-in OVP, OTP, UVLO, OCP, output short/open protection and open loop protection.

With the pin CS, the GT5010 is able to monitor the peak primary current. This allows for cycle by cycle peak current control and limit. When the voltage level of pin CS hits the internal OCP threshold, over current is detected and the IC will immediately turn off the power MOS switch, until the next pulse is generated.

The VCC protections are implemented by UVLO and OVP. The output of GT5010 is shut down when VCC drops below UVLO (ON) threshold or rises above OVP threshold and the power system enters auto-restart sequence. In the event of output short or open, the UVLO (ON) and OVP can be triggered, and the converter can be shut down and enter into auto-restart sequence.

The over temperature protection (OTP) circuitry senses the die temperature. The threshold is set at 140 °C typically. When the die temperature rises above the threshold, the converter is shut down and enters into auto-restart sequence.

If open-loop happens, GT5010 can detect the fault condition and turn off the converter then enters into auto-restart sequence.

## 6.8 Sleeping control technology

In GT5010, an innovative sleeping control technology is employed. As the converter load decreases from full-load to



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no-load, the current consumption of GT5010 dramatically drops from about 2mA to 200 $\mu$ A. Therefore, the efficiency of

converter is significantly improved, and the standby is reduced to a very low level.



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## 7. Electrical Characteristics

### 7.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Power supply (pin6)	VCC	-0.3 to VCC clamp	V
Cab compensation (pin5)	RI	-0.3 to 7	V
IFB input (pin4)	IFB	-0.3 to 7	V
CS input (pin3)	CS	-0.3 to 7	V
Maximum junction temperature	T <sub>JMAX</sub>	150	°C
Storage temperature	T <sub>STO</sub>	-55 to 150	°C
Lead Temperature (Soldering, 10secs)	T <sub>LEA</sub>	260	°C

**Note:** Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



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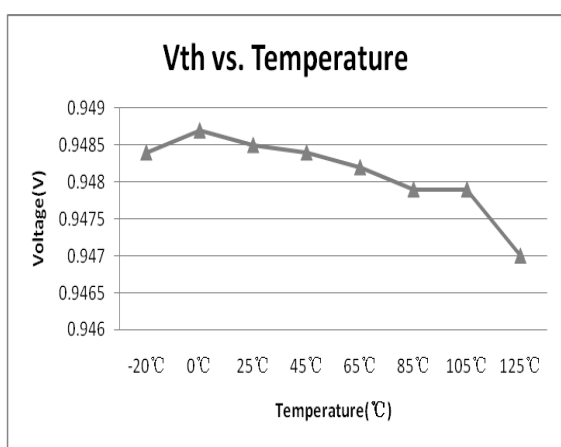
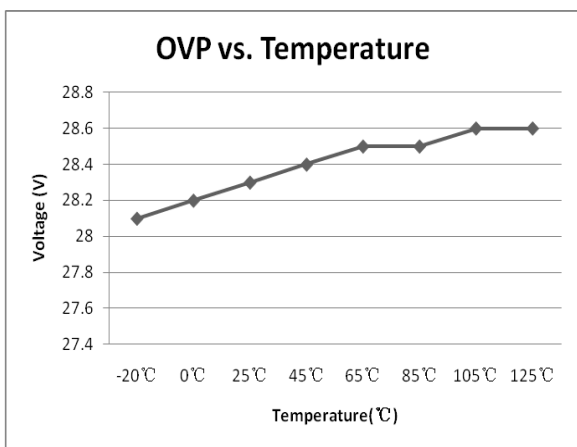
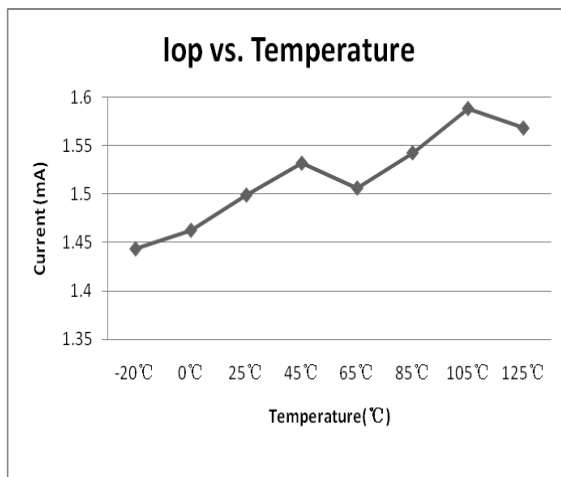
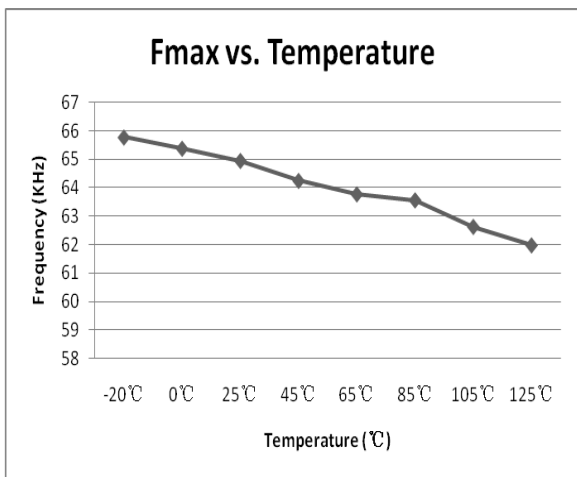
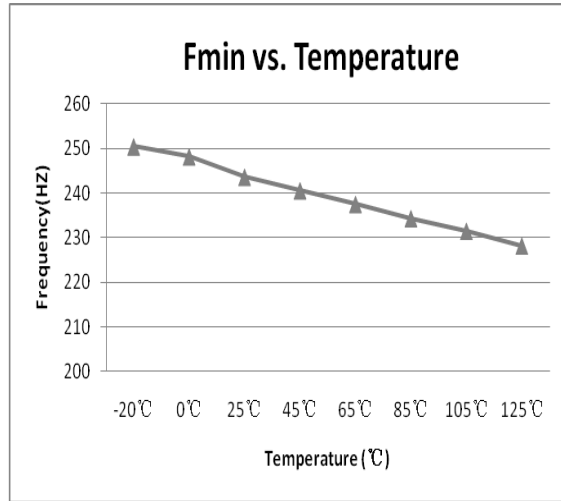
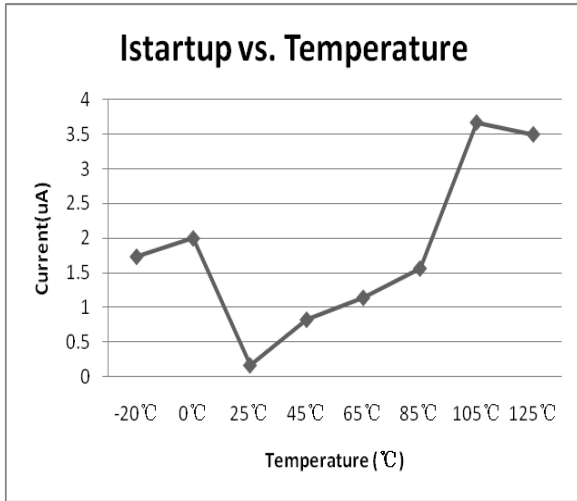
## 7.2 Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Supply Voltage (VCC) Section</b>						
Start up current	I <sub>STARTUP</sub>	VCC=13V	-	2	4	μA
Sleeping current	I <sub>DD_SD</sub>	VCC=16V	-	250	-	μA
Operation current	I <sub>CC_OP</sub>		-	1.5	2.5	mA
VCC Under Voltage Enter threshold	UVLO(ON)	VCC falling	8.1	9.0	9.8	V
VCC Under Voltage Exit threshold	UVLO(OFF)	VCC rising	13.5	14.5	15.5	V
VCC Over Voltage Protection Threshold	OVP	Ramp VCC until gate shut down	26	27.5	29	V
VCC Clamping voltage	VCC <sub>ZB</sub>	I <sub>CC</sub> =10mA	30	32.5	35	V
<b>Frequency Section</b>						
Maximum IC frequency	f <sub>MAX</sub>		55	60	65	kHz
Minimal IC Frequency	f <sub>MIN</sub>		200	260	320	Hz
Frequency shuffling range	Δf/Freq		-	±5	-	%
<b>Current Sense Section</b>						
Turn on LEB time	t <sub>LEB</sub>		-	300	-	ns
Over current threshold	V <sub>TH</sub>		911.8	940	968.2	mV
Input Impedance	Z <sub>SENSE</sub>		100	-	-	kΩ
Soft start time	t <sub>SST</sub>		-	2	-	ms
<b>CC/CV control Section</b>						
Reference voltage for CM EA	I <sub>REF</sub>	R <sub>I</sub> =10kΩ	24.5	25	25.5	μA
Max. Cable compensation current	I <sub>COMP_MAX</sub>	R <sub>I</sub> =10kΩ	-	1.6	-	μA
Over Temperature protection	OTP		-	150	-	°C
<b>Output Section</b>						
Gate Output Clamping	G_clamping		-	17	-	V
Gate Rising Time	t <sub>R</sub>	C <sub>L</sub> =0.5nF	-	44	-	nS
Gate Falling Time	t <sub>F</sub>	C <sub>L</sub> =0.5nF	-	30	-	nS
Max. Output Charge Current	I <sub>CH</sub>		-	-	150	mA
Max. Output Sink Current	I <sub>SINK</sub>		-	-	200	mA



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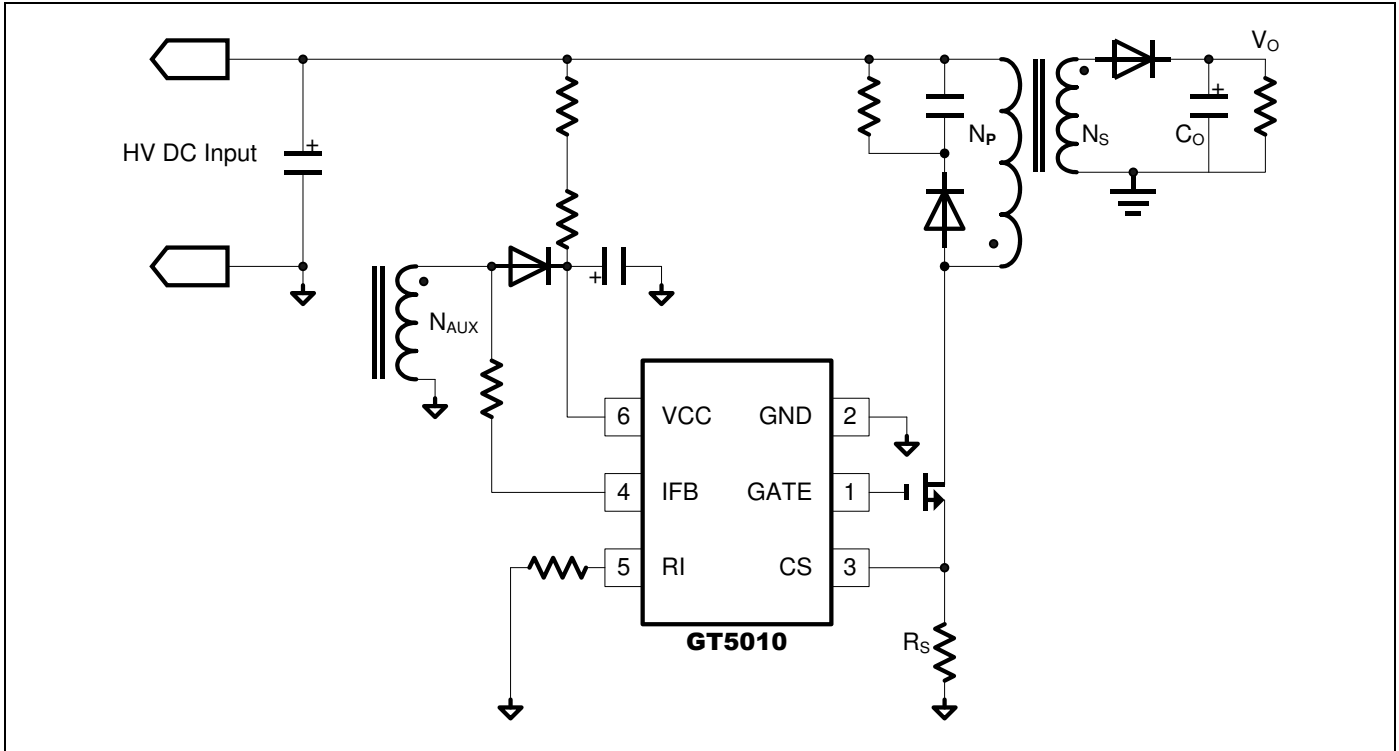
## 8. Typical Performance Characteristics





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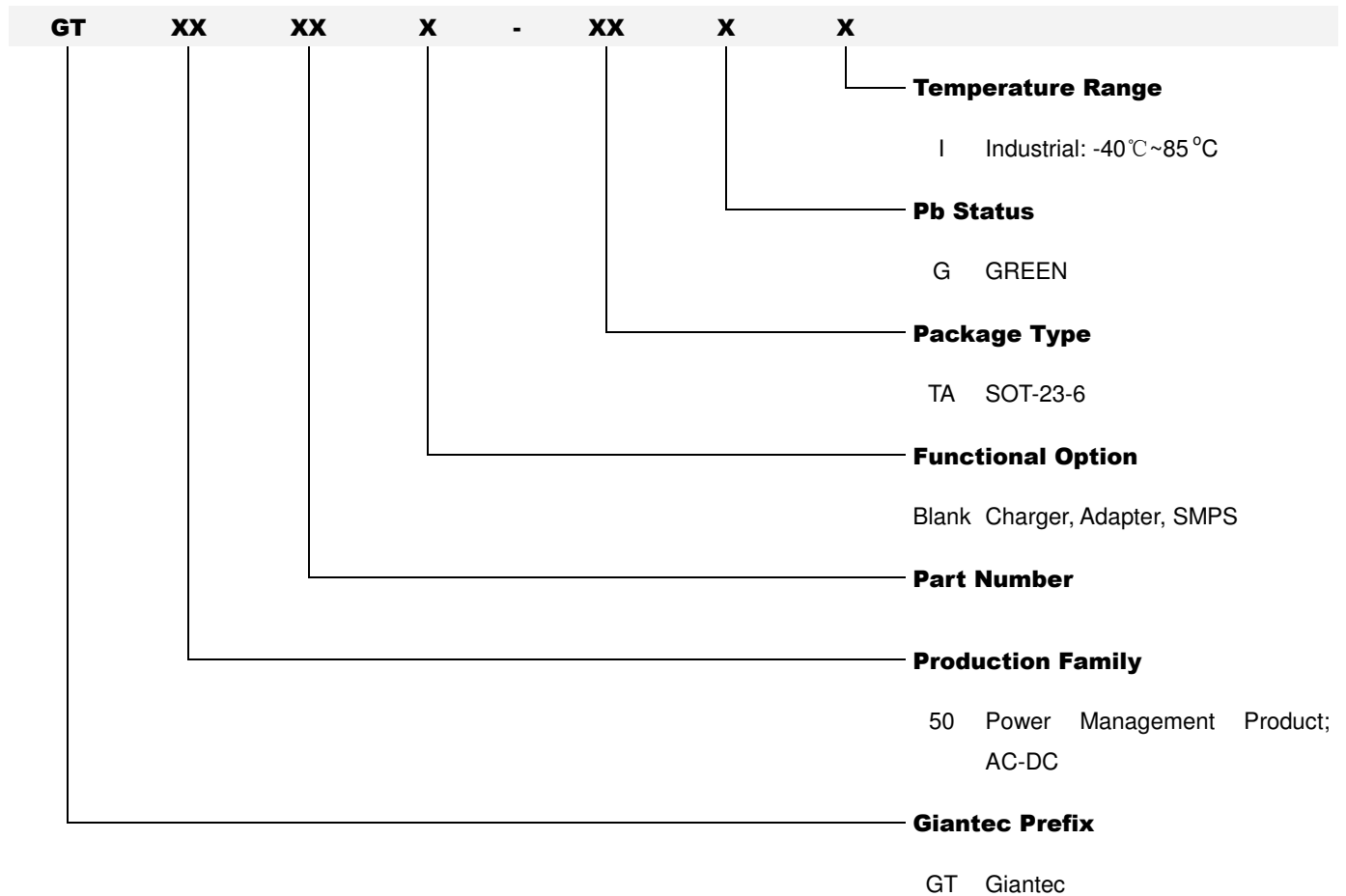
## 9. Typical Application Circuits





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## 10. Ordering Information



Order Number	Package Description	Package Option
GT5010-TAGI-TR	SOT-23-6	Tape and Reel 3000



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## 11. Part Markings

### 11.1 GT5010-TAGI (Top View)



<b>010</b>	GT5010-TAGI		
●	Pin 1 Indicator		
<b>Y</b>	Seal Year	<b>W</b>	Seal Week
2010 (1st half year)	A	Week 01	A
2010 (2nd half year)	B	Week 02	B
2011 (1st half year)	C	.....	
2011 (2nd half year)	D	Week 26	Z
2012 (1st half year)	E	Week 27	A
2012 (2nd half year)	F	Week 28	B
.....	.....	.....	.....
2022 (2nd half year)	Z	Week 52	Z

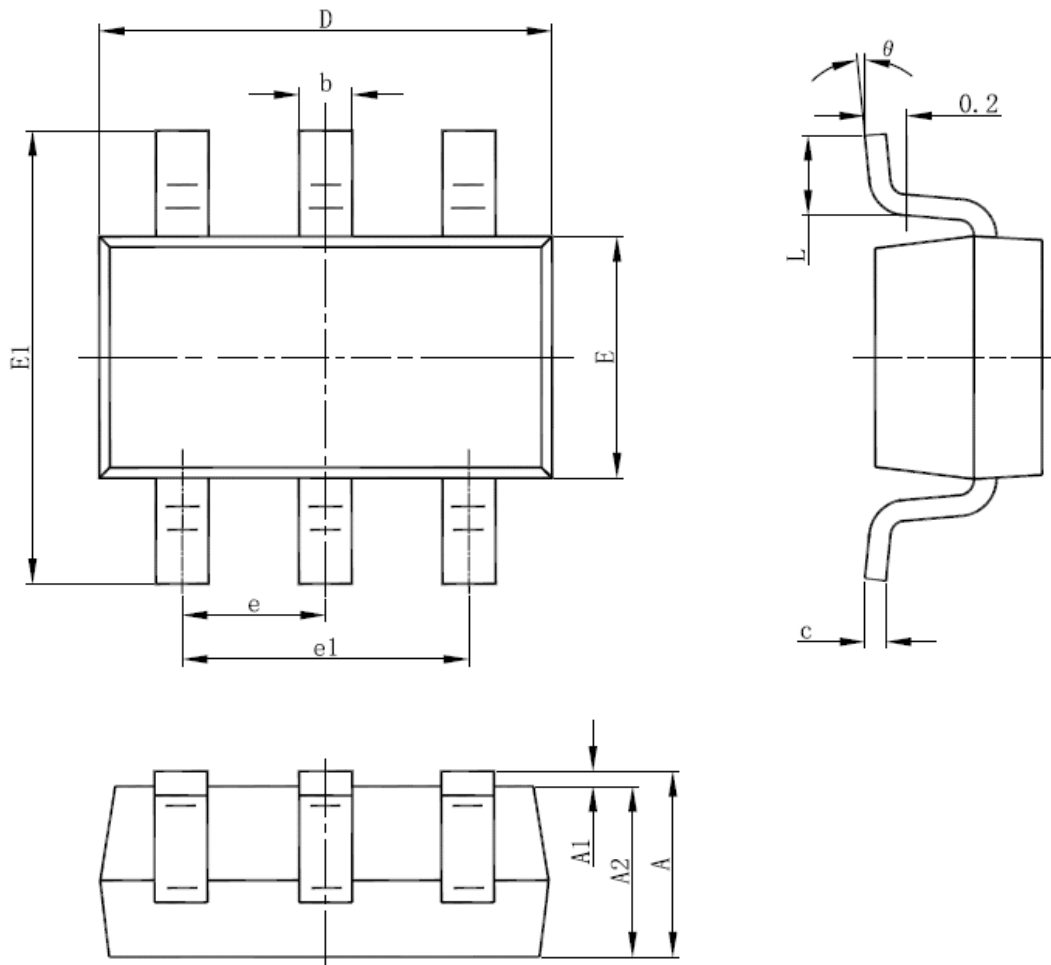


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## 12. Package Information

### 12.1 SOT-23-6

SOT-23-6L PACKAGE OUTLINE DIMENSIONS





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**Table 1. Table of SOT-23-6 Package Dimensions**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°



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## 13. Revision History

Revision	Date	Descriptions
A2	Aug.,2011	Optimise Constant Voltage Char.
A1	May, 2011	Add "Functional Description" Add "Typical Application Circuits"
A0	Aug., 2010	Initial Version