ClearSpeed

CSX700 Floating Point Processor Datasheet

Feature summary

High performance

- 96 GFLOPS double precision floating point (peak)
- Single and double precision, IEEE 754 compliant, FPUs
- Power efficient architecture

Features

- Professional Software Development Kit (SDK)
- Two multi-threaded processing cores, each with:
  - Array of 96 Processing Elements (PE)
  - Double and single precision floating-point acceleration in every PE
  - Controller with 8 Kbyte instruction and 4 Kbyte data cache
- PCI-Express x16 (Gen. 1 rev 1.1) host interface
- 2 x 128 Kbyte on-chip SRAM
- 2 x 8 Gbytes of external DDR2 DRAM support
- High speed chip-chip interface (CCBR)
- Configuration/debug port (HDP)
- JTAG boundary scan (IEEE compliant)

Applications

Designed for data-intensive and high-compute applications

- Finance
- Radar systems
- Bio-informatics
- Signal processing
- Medical imaging

Electrical

- 1.0V core supply
- 1.8V and 3.3V I/O supplies
- 1.2V and 1.8V analog supplies

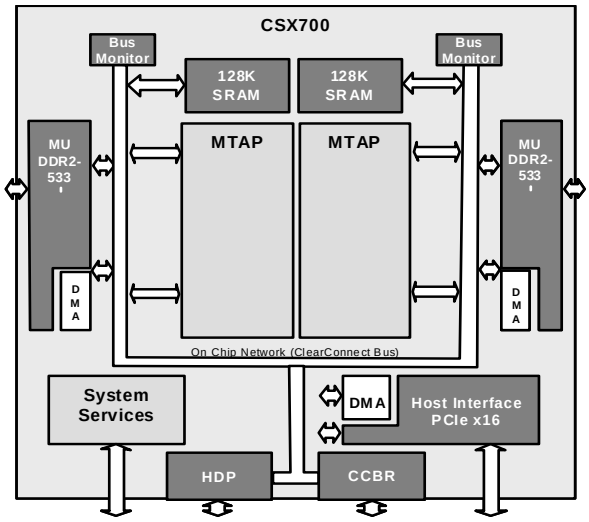
Mechanical/thermal

- 40 mm x 40 mm thermally enhanced flip-chip package
- 1429 balls on 1 mm pitch
- 680 signal pins (including analog supplies)
- Power dissipation 10W typical

Description

The CSX700 is a high performance, low power floating point coprocessor. It is designed for use in a variety of applications in high performance computing and embedded systems.

The CSX700 is the second product in ClearSpeed's family of floating point application accelerators. The CSX processors are based around ClearSpeed's multi-threaded array processor (MTAP) architecture. This architecture has been developed to address the implementation issues of high-performance systems by providing unparalleled performance-per-watt.



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1 Description

The CSX700 comprises two multi-threaded array processor (MTAP) cores, two external DDR2 DRAM interfaces, a 16-lane PCI Express host interface, a high-speed chip-to-chip interface and embedded SRAM integrated onto a single chip. All subsystems on the chip are interconnected by a ClearConnect on-chip network (the ClearConnect bus).

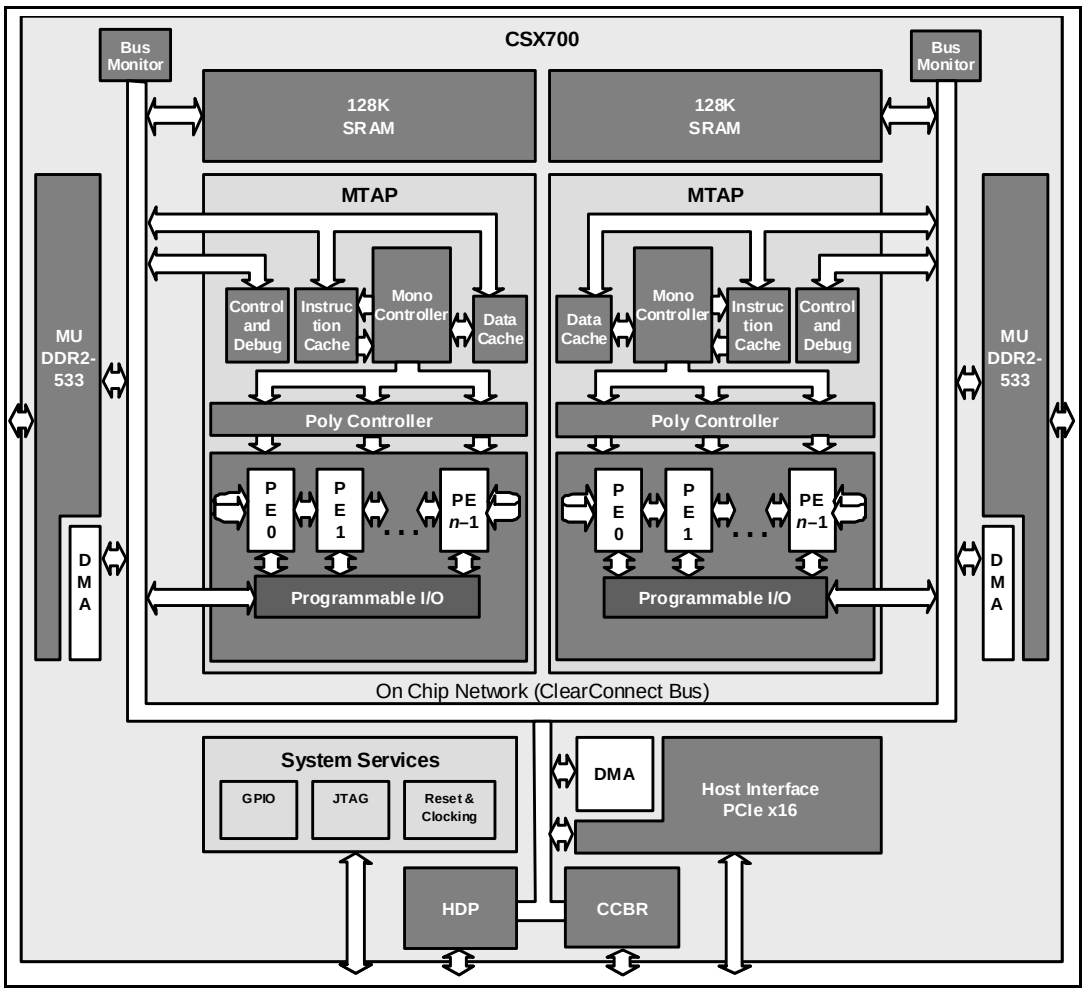

Figure 1: CSX700 block diagram

1.1 Multi-threaded array processor (MTAP) core

The MTAP architecture provides an exceptionally powerful and scalable processing solution, based on a SIMD array of processing elements (PEs). Each PE has its own local memory and I/O capability, making the architecture ideally suited for applications which have high processing and/or bandwidth requirements.

Each MTAP core contains an array of 96 PEs. The PEs include multiple processing units and have high level of internal instruction-level and data parallelism. Each PE also has its own local memory providing a high bandwidth access to frequently used data.

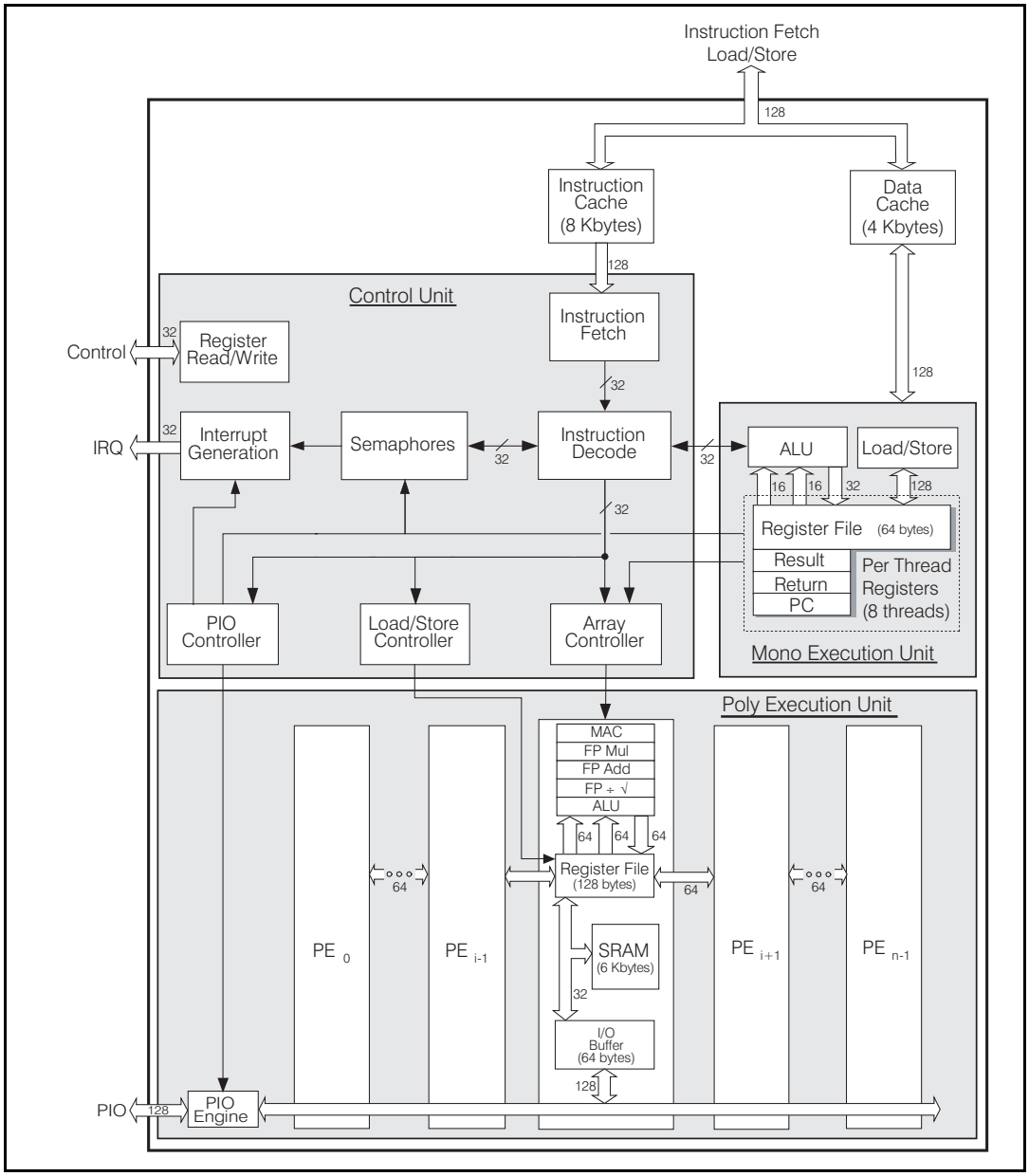

Figure 2: Block diagram of a single MTAP core

1.1.1 MTAP overview

The two MTAP cores are identical; a single MTAP core is shown in the block diagram (*Figure 2*).

The main components of the processor are:

- **Mono control unit:** fetches and decodes instructions. The single, unified instruction stream are fetched and decoded by the control unit. Mono instructions are despatched to the mono execution unit, poly instructions are sent to the poly controller;
- **Poly controller:** contains three parts:
  - The Programmed I/O (PIO) controller is responsible managing the transferring of data between external memory and the PEs.
  - Load/Store controller, which controls the transfer of data from the PE SRAM and the PIO buffer;
  - Array controller, responsible for the poly execution unit control.
- **Execution units**: consists of two main parts:
  - The mono execution unit which acts on mono (non-parallel) data and handles program flow control and I/O functions;
  - The poly execution unit which contains an array of Processing Elements (PEs) which act on poly (parallel) data.
- **Caches:** instruction and data caches to speed accesses to external code and data;
- **I/O:** in addition to loads and stores to local PE memory, there is a Programmed I/O (PIO) mechanism which allows the poly execution unit to perform loads and stores to external memory

It is the poly execution unit and its array of PEs that provide the processor's massive processing power and memory bandwidth. The mono and poly execution units have basically the same architecture and instruction set. The tightly integrated mono and poly execution units mean that the processor as a whole is efficient for simple sequential code, as well as when processing large amounts of data in parallel.

The various functional units within the execution units (for example, ALU, FPU, I/O) can operate concurrently.

The processor supports 64-bit addressing so that large data sets can be processed. The 64-bit address space is flexibly mapped into a 48-bit physical address space. For embedded systems and backward compatibility a simple 32-bit addressing mode is provided.

1.1.2 Mono controller

The instruction fetch and issue hardware supports multi-threaded execution. Thread switching is under software control and may be triggered in response to events such as the completion of an operation by one of the I/O engines. By providing support in hardware, the need for a real-time kernel for the MTAP processor is removed. The hardware supports 8 threads. Hardware semaphores are used to synchronize threads with other threads and with hardware units.

To optimize performance, the processor includes instruction and data caches.

Features

- hardware support for 8 threads,
- 128 8-bit semaphores,
- unified 32-bit instruction set,
- 8 Kbyte instruction cache, 4-way, 512 lines x 4 instructions, with manual and auto pre-fetching (configurable horizon),
- 4 Kbyte data cache, 4-way, 256 lines x 16 bytes,
- interrupt generation,
- debug support,
- event counters for PAPI (performance application programming interface) profiling support,
- ECC on all cache RAMs, FIFOs and other memories (including PE memory).

1.1.3 Mono execution unit

As well as handling mono data, the mono unit is responsible for program flow control (branching), thread switching and other control functions. The mono execution unit also has overall control of I/O operations. Results from these operations are returned to a register in the mono unit. The mono execution unit contains:

- ALU,
- 64-bit FPU,
- multiple 128-byte register files.

1.1.4 Poly execution unit

The MTAP core contains an array of 96 PEs. The array provides both compute power and high bandwidth storage. The PE array operates on a single-instruction multiple-data (SIMD) model, processing multiple data items in parallel. Each PE contains:

- 128-byte PE register file,
- 6 Kbytes of PE SRAM with ECC,
- 16-bit MAC with 64-bit accumulator,
- single and double precision floating point unit (FPU), with dual issue pipelined add and multiply,
- support for integer and floating point divide and square root.

1.1.5 Input-output

The MTAP processor supports a programmed I/O (PIO) channel designed for transferring variable amounts and types of data under software control. This is typically used to access external memory or peripherals. Key features are:

- 128-bit PIO data channel,
- transfer sizes of 8, 16, 32, 64 bytes per PE,
- addressing modes: (linear) addresses and strided,
- synchronized using semaphores.

1.2 PCI Express host interface (HIF)

The host interface contains a x16 2.5Gb/s rev 1.1 PCIe interface. This is capable of negotiating links of x16, x8, x4, x2 and x1 according to v1.1 of the PCIe Specification. It presents two PCIe BAR apertures, one for register control and the other for small data transfer. In addition, a dual-channel DMA unit allows high speed bi-directional data transfer at 3GB/s. It is possible to modify certain PCIe config space and PHY parameters prior to link negotiation using an external device connected to the HDP. The HIF also contains some host related system services (HRSS). These are functions, such as software reset and stopclock registers which must be accessible when the main part of the chip is in reset and/or not clocked.

1.3 Host debug port (HDP)

The HDP is the means by which the CSX700 is configured. It has full access to the register and memory space of the device.

The external interface is a low pin-count shared-bus interface that provides a low-cost access to a number of CSX700 devices on a board.

1.4 ClearConnect Bridge (CCBR)

The internal bus is made available at a port that can be interconnected with no glue logic to construct dual-chip systems. This enables system performance to be scaled to meet the requirements of the application. In addition, the CCBR allows the CSX700 to be used with an FPGA in embedded systems.

This full duplex port uses a double data rate interface to minimize the pin count.

1.5 Memory unit (MU)

External memory is connected through two 64-bit DDR2 DRAM interfaces. When used with a 72-bit wide DRAM array this provides error checking and correction (ECC). Each interface supports up to 8 Gbytes of local DRAM and can be accessed by both MTAP cores. The DRAM is accessible from any bus master in the system, including the host processor.

The DRAM controller runs asynchronously to the device core, from a clock generated by a dedicated internal PLL. The multiplication ratio from the reference clock input is programmed by control registers.

An attached programmable DMA engine permits data transfer to or from the external DRAM to occur in the background in parallel with the processor core executing other operations. The DMA unit may be programmed by either the host processor or the device processor core. DMA transfers can be chained together using transfer description records stored anywhere in system memory. DMA operation is integrated into the hardware semaphore mechanisms for inter-processor synchronization.

1.6 Interrupt and semaphore unit (ISU)

The ISU supports the synchronization between threads and with external events. Each MTAP has its own ISU, but can access both. Multiple processors may perform synchronization events, for example to assist in communication via shared memory, through

operations on the set of hardware semaphore elements contained in this block. Similarly, synchronization with a host processor may be performed via conversion of semaphore events to interrupt events. Both pin and message-signalled interrupts are supported for flexible support of multiple devices in various host environments.

1.7 SRAM

The CSX700 includes two 128 Kbyte blocks of on-chip SRAM which provide the processors with low latency access to code and data. Each memory is organized as 8K words of 16 bytes and can be ECC protected. Both blocks of SRAM can be accessed by both MTAP cores.

Typically, the SRAM is used to store items for which low-latency access from the processor core is important, such as instruction code and frequently used data. The SRAM is accessible from any bus master in the system, including the host processor.

1.8 System services

The system services blocks contains other control and utility signals such as reset controls and general purpose I/O (GPIO) signals.

The GPIO signals can be configured to be interrupt sources for systems integration use.

1.9 Bus monitor (BMON)

The bus monitors trap mis-addressed transactions. The details of these transactions can be extracted from the bus monitors to assist systems integration and software debug.

1.10 ClearConnect Bus (CCB)

The ClearConnect bus is a packet switched on-chip network; on the CSX700 it is configured as two independent channels. One of these is the main system bus, designed for high bandwidth data movements, the other is a peripheral bus, designed for read/write access to control registers and interrupt messages. Both system bus and peripheral bus are pipelined. The system bus is split transaction for maximum performance. Both busses support multiple concurrent transfers, thus providing extremely high aggregate bandwidth.

The system bus runs at core clock speed and can transfer up to 128 bytes in a single transaction. The peripheral bus can transfer 4 bytes in each transaction.

By means of the CCBR, the ClearConnect bus can be extended to a second CSX700 device and to system logic implemented in other devices such as FPGAs. All memory targets are then accessible by all masters on the global bus, using a 48-bit physical address. Master and target units are uniquely identified by means of device IDs that are assigned to individual devices at boot time, and internal node IDs that are fixed. The combination of device and node ID forms a geographic bus address that is unique to each unit. Part of the master’s logical address is used, by means of a programmable address aperture unit, to map logical addresses to physical addresses that reside on particular bus targets.

2 Interfaces

A set of interfaces allow the CSX700 to be used in different types of systems. All interfaces that carry data operate asynchronously to each other and to the processor core. This allows the clock frequency of the core and all interfaces to be optimized for the application.

The pin counts in the headings below include analog supplies and references but not core or I/O power and ground.

2.1 I/O signal types

The I/O pins of the CSX700 have different signalling standards according to their function. The I/O pins all have high-side and low-side clamping diodes, and so cannot tolerate applied voltages outside of their VDDIO to VSS range. In particular, this means that the SSTL pins are not 3.3V tolerant.

2.1.1 3.3V LVTTL

All configuration and control pins use 3.3V LVTTL I/Os. Some inputs include weak pull-up resistors; those that do not must not be left floating. The LVTTL outputs have a drive strength that self-series terminates into a 50Ω line, and do not require parallel termination. The GPIO pins are 20Ω terminated.

2.1.2 1.8V CMOS

A single pin, BIRQ_N pin in the CCBR, uses 1.8V CMOS. Usually BIRQ_N will be connected to the BIRQ_N pin on the CCBR interface of the connected device."

2.1.3 1.8V SSTL

The high bandwidth ports (CCBR, MU) of the device use SSTL I/O pins. The device contains programming registers that control whether the pin groups operate as SSTL class I or class II outputs. In point-to-point applications, class I is typically used. Some external termination is required on address and control lines for the memory unit.

The SSTL pads employ on-die termination (ODT) which is controlled either by register or dynamically by the device logic. This is in order to eliminate the need for external termination resistors.

A reference voltage is required for all SSTL input pins. There is approximately one VREF input for every nine inputs.

2.1.4 1.8V differential SSTL clock inputs

Many clock inputs on the CSX700 are differential SSTL inputs. These should be used with differential clock sources for lowest jitter and radiated emissions. They may also be used as single ended inputs by feeding a clock input to the CLK_P input and tying the CLK_N input to a reference voltage in the centre of the clock signal swing (typically VDDIO/2).

2.1.5 PCI Express

The PCI Express pins conform to PCI Express base Specification 1.1 standard.

2.2 Pin lists

The following tables give the pin descriptions and BGA locations. To assist with planning board layout, a spreadsheet detailing the specific pin locations and BGA trace lengths can be requested from ClearSpeed. The Type column has the following nomenclature:

	Type	Description
IO standard	Analog	The signal is analog not digital
	LVTTL	3.3V LVTTL
	CMOS	1.8V CMOS
	SSTL	1.8V SSTL. May be combined with Diff
	PCIe	PCI Express
Direction	I	Input
	O	Output
	IO	Input / output
Attributes	Diff	Differential
	PU	Pull up
	PD	Pull down
	OD	Pseudo open drain output. Driven to 1, or floats. May be combined with PD
	OS	Pseudo open source output. Driven to 0, or floats. May be combined with PU

Table 1. Pin types

Name	BGA	Type	Function
ExtRes_P, ExtRes_N	AM21 AN21	Analog	Connect a 2.05KΩ bias resistor with a tolerance of 0.1% and a low temperature coefficient between these two pins. This resistor must be as close to the package as possible, with less than 2Ω of trace resistance to either resistor leg.
PERP0, PERN0 PERP1, PERN1 PERP2, PERN2 PERP3, PERN3 PERP4, PERN4 PERP5, PERN5 PERP6, PERN6 PERP7, PERN7 PERP8, PERN8 PERP9, PERN9 PERP10, PERN10 PERP11, PERN11 PERP12, PERN12 PERP13, PERN13 PERP14, PERN14 PERP15, PERN15	AW22, AW23 AW24, AW25 AW26, AW27 AW28, AW29 AW30, AW31 AW32, AW33 AW34, AW35 AW36, AW37 AU39, AT39 AR39, AP39 AN39, AM39 AL39, AK39 AJ39, AH39 AG39, AF39 AE39, AD39 AC39, AB39	PCIe I Diff	Receive lane differential pairs.
PETP0, PETN0 PETP1, PETN1 PETP2, PETN2 PETP3, PETN3 PETP4, PETN4 PETP5, PETN5 PETP6, PETN6 PETP7, PETN7 PETP8, PETN8 PETP9, PETN9 PETP10, PETN10 PETP11, PETN11 PETP12, PETN12 PETP13, PETN13 PETP14, PETN14 PETP15, PETN15	AV22, AV23 AV24, AV25 AV26, AV27 AV28, AV29 AV30, AV31 AV32, AV33 AV34, AV35 AV36, AV37 AU38, AT38 AR38, AP38 AN38, AM38 AL38, AK38 AJ38, AH38 AG38, AF38 AE38, AD38 AC38, AB38	PCIe O Diff	Transmit lane differential pairs.
PREFCLK_P PREFCLK_N	AW19 AW20	I Diff	Differential 100MHz PCIe reference clock input.
PAVDD1 PAVDD2	AK20 AK22	1V8	PCIe PLL power
PAVSS1	AK21	GND	PCIe PLL ground
HSSAVDD0 HSSAVDD1 HSSAVDD2 HSSAVDD3	AK24 AK26 AK28 AK30	1V8	SerDes power

Table 2. PCI Express pins

Name	BGA	Type	Function
AVTT0 AVTT1 AVTT2 AVTT3 AVTT4 AVTT5 AVTT6 AVTT7	AU22 AU26 AU30 AU34 AT37 AM37 AH37 AD37	1V2	Transmit termination voltage
AVTR0 AVTR1 AVTR2 AVTR3	AP25 AP31 AL34 AF34	1V2	Receive termination voltage
V180P2	AF21	1V8	IO power

Table 2. PCI Express pins

Name	BGA	Type	Description
HIRQ_N	V37	IO, OS, LVTTL, PU	Active low interrupt request. Indicates that an HDP protocol error has occurred. Wired-OR output or input under register control.
HCLK	V32	I, LVTTL	Clock input for HDP
HREQ	V36	O, LVTTL	Arbitration: HDP requests bus
HGNT	V34	I, LVTTL	HDP grant in response to a HREQ, or to configure chip ID.
HRXSTP	W33	O, OD, LVTTL, PD	Flow control: HDP receiver requires the transmitter to pause
HRXD0 HRXD1 HRXD2 HRXD3 HRXD4 HRXD5 HRXD6 HRXD7	Y39 Y38 Y37 Y35 Y34 Y33 W37 W36	I, LVTTL	Receive data
HRXVAL	W34	IO, LVTTL	Receiver data valid
HRXEOP	W32	I, LVTTL	Receiver data end of packet
HTXD0 HTXD1 HTXD2 HTXD3 HTXD4 HTXD5 HTXD6 HTXD7	T39 T38 T37 T35 T34 T33 U38 U37	O, LVTTL	Transmit data
HTXVAL	U35	IO, LVTTL	Transmit data valid
HTXEOP	U33	OT, LVTTL	Transmit end of packet

Table 3. HDP interface signals

Name	BGA	Type	Description
HTXSTP	U34	I, LVTTL	Flow control: HDP transmitter should pause
VDDIO1	T36,U32,U39 V35,Y32,Y36, AA34	3V3	HDP LVTTL IO power

Table 3. HDP interface signals

Name	BGA	Type	Description
BREFCLK_P, BREFCLK_N	C39 D39	I, Diff, SSTL	CCBR reference clock input
BIRQ_N	F29	IO, CMOS	CCBR interrupt request Connects from second chip to first chip Direction is under register control, default is input Should have an external pull-up resistor
RX0D0 .. RX0D7, RX1D0 .. RX1D7, RX2D0 .. RX2D7, RX3D0 .. RX3D7, RX4D0 .. RX4D7, RX5D0 .. RX5D7, RX6D0 .. RX6D7, RX7D0 .. RX7D7, RX8D0 .. RX8D7	R32,R34,R35,P32,P33,N32,N34,N35 M32,M33,M34,L32,L34,K32,K33,K34 J32,J34,J35,H32,H33,G32,G34,G35 F32,F33,F34,E32,E34,D32,D33,D34 C32,C34,C35,B32,B33,A32,A34,A35 H28,G28,F28,H27,F27,H26,G26,F26 H25,F25,E25,H24,G24,H23,F23,E23 H22,G22,F22,H21,F21,H20,G20,F20 H19,F19,E19,H18,G18,H17,F17,E17	I, SSTL	CCBR receive data High speed DDR signal
RX0S .. RX8S	P34,L35,H34,E35,B34,E27,F24,E21, F18	I , SSTL	CCBR receive data strobe
RXSTP0 RXSTP1 RXSTP2	H31 H30 H29	O, SSTL	CCBR receive stop.
RXCLK	G30	I, SSTL	CCBR receive clock
RXVAL RXEOP RXODT	E31 F31 E29	I, SSTL	CCBR receive control.
TX0D0 .. TX0D7, TX1D0 .. TX1D7, TX2D0 .. TX2D7, TX3D0 .. TX3D7, TX4D0 .. TX4D7, TX5D0 .. TX5D7, TX6D0 .. TX6D7, TX7D0 .. TX7D7, TX8D0 .. TX8D7	A17,B17,D17,B18,C18,A19,B19,D19 B20,C20,D20,A21,B21,B22,C22,D22 A23,B23,D23,B24,C24,A25,B25,D25 B26,C26,D26,A27,B27,B28,C28,D28 A29,B29,D29,B30,C30,A31,B31,D31 D38,D37,D36,E39,E38,F38,F37,F36 G39,G38,G36,H38,H37,J39,J38,J36 K38,K37,K36,L39,L38,M38,M37,M36 N39,N38,N36,P38,P37,R39,R38,R36	O, SSTL	CCBR transmit data High speed DDR signal.
TX0S .. TX8S	D18,D21,D24,D27,D30,E36,H36,L36, P36	O, SSTL	CCBR transmit data strobe
TXSTP0 TXSTP1 TXSTP2	A38 B38 C38	I, SSTL	CCBR transmit stop.

Table 4. Bridge port interface signals

Name	BGA	Type	Description
TXCLK	B36	O, SSTL	CCBR transmit clock
TXVAL	A36	O, SSTL	CCBR transmit control, VAL: valid
TXEOP	A37	O, SSTL	CCBR transmit control, EOP: end of packet
TXODT	C36	O, SSTL	CCBR transmit control, ODT: on die termination
BVREF	U30,T30,R30,K26,K25,K24,K23,K22, K21,P30	Analog	CCBR SSTL input voltage reference
BAVDD1 BAVDD2	K30 M30	1V8	Power for CCBR TX and RX PLLs respectively
BAVSS1 BAVSS2	L30 N30	GND	Ground for CCBR TX and RX PLLs respectively
VDDIOC	A18,A22,A26,A30,B37,C19,C23,C27, C31,C33,D35,E20,E24,E28,E30,E37, F39,G17,G21,G25,G29,G33,H35,J37 ,K39,L33,M35,N37,P39,R33	1V8	CCBR SSTL IO power

Table 4. Bridge port interface signals

Name	BGA	Type	Description
M0_REFCLK_P M0_REFCLK_N	G1 F1	I, SSTL Diff	Reference clock input
M0_CLK0_P, M0_CLK0_N M0_CLK1_P, M0_CLK1_N M0_CLK2_P, M0_CLK2_N M0_CLK3_P, M0_CLK3_N M0_CLK4_P, M0_CLK4_N	R1,P1 K1,J1 A7,A6 A10,A9 A15,A14	O, SSTL Diff	Memory clock outputs
M0_A0 ... M0_A7 M0_A8 ... M0_A15	G7,G8,H9,H10,G10,H11,H12,G12 H13,H14,H7,G14,H15,J8,H16,G16	O SSTL	Memory address
M0_BA0 M0_BA1 M0_BA2	M8 L8 K8	O SSTL	Memory bank address
M0_RAS_N	R8	O, SSTL	Memory row address strobe
M0_CAS_N	M7	O, SSTL	Memory column address strobe
M0_WE_N	N8	O, SSTL	Memory write enable
M0_S0_N M0_S1_N	P7 P8	O, SSTL	Memory rank selects

Table 5. Memory unit 0 signals

Name	BGA	Type	Description
M0_CKE	K7	O, SSTL	Memory clock enable
M0_ODT0 M0_ODT1	T7 T8	O, SSTL	Memory on-die termination control
M0_DQ0 ... M0_DQ7 M0_DQ8 ... M0_DQ15 M0_DQ16 ... M0_DQ23 M0_DQ24 ... M0_DQ31 M0_DQ32 ... M0_DQ39 M0_DQ40 ... M0_DQ47 M0_DQ48 ... M0_DQ55 M0_DQ56 ... M0_DQ63	B16,C16,D16,D15,B15,C14,D14,B14 F14,B13,A13,E13,D13,D12,C12,B12 A11,D11,B11,D10,D9,C10,B9,B10 B8,D8,C8,E7,D7,C6,D6,E6 F5,F3,F4,G5,G4,H4,H3,H2 J4,J2,K2,K4,K3,L4,L1,L2 P6,N2,N4,N1,M3,M4,L6,M2 T4,T3,T2,R4,P3,R2,P2,P4	IO SSTL	Memory data bus
M0_CB0 . M0_CB7	B5,A4,A3,B3,C1,C2,D1,E2	IO, SSTL	Memory data check byte
M0_DM0 ... M0_DM8	F16,F13,E11,F9,G6,J5,N6,T6,C4	IO, SSTL	Memory data masks
M0_DQS0 ... M0_DQS8	E15,F12,F10,F8,H6,K6,N5,R5,D4	IO, SSTL	Memory data strobes
M0_DSQ0 ... M0_DSQ8	F15,F11,E9,F7,J6,L5,M6,R6,D3	IO, SSTL	Memory dummy strobe
M0_VREF	K18,K19,K17,K16,K14,K13,P10 R10,K15,K12,T10	I, Analog	Memory SSTL voltage reference inputs
M0_AVDD1	K10	1V8	Memory unit PLL power
M0_AVSS1	L10	GND	Memory unit PLL ground
VDDIOM0	A8,B2,B4,B6,C11,C15,C7,C9,D2 D5,E12,E16,E4,F6,G13,G3,G9,U5, H1,J7,K5,L3,M5,N7,R3,T1,T5,U3,U7	1V8	Memory unit SSTL IO power

Table 5. Memory unit 0 signals

Note: Pins M0_DSQ0 ... M0_DSQ8 should be implemented as NC (no connect). Connecting a load to these pins will affect the DDR interface timing.

Name	BGA	Type	Description
M1_REFCLK_P M1_REFCLK_N	AN1 AP1	I, SSTL Diff	Reference clock input
M1_CLK0_P, M1_CLK0_N M1_CLK1_P, M1_CLK1_N M1_CLK2_P, M1_CLK2_N M1_CLK3_P, M1_CLK3_N M1_CLK4_P, M1_CLK4_N	AE1,AF1 AK1,AL1 AW7,AW6 AW10,AW9 AW15,AW14	O, SSTL Diff	Memory clock outputs
M1_A0 ... M1_A3 M1_A4 ... M1_A7 M1_A8 ... M1_A11 M1_A12 ... M1_A15	AN7,AN8,AM9,AM10 AN10,AM11,AM12,AN12 AM13,AM14,AM7,AN14 AM15,AL8,AM16,AN16	O SSTL	Memory address

Table 6. Memory unit 1 signals

Name	BGA	Type	Description
M1_BA0 M1_BA1 M1_BA2	AH8 AJ8 AK8	O SSTL	Memory bank address
M1_RAS_N	AE8	O, SSTL	Memory row address strobe
M1_CAS_N	AH7	O, SSTL	Memory column address strobe
M1_WE_N	AG8	O, SSTL	Memory write enable
M1_S0_N M1_S1_N	AF7 AF8	O, SSTL	Memory rank selects
M1_CKE	AK7	O, SSTL	Memory clock enable
M1_ODT0 M1_ODT1	AD7 AD8	O, SSTL	Memory on-die termination control
M1_DQ0 ... M1_DQ7 M1_DQ8 ... M1_DQ15 M1_DQ16 ... M1_DQ23 M1_DQ24 ... M1_DQ31 M1_DQ32 ... M1_DQ39 M1_DQ40 ... M1_DQ47 M1_DQ48 ... M1_DQ55 M1_DQ56 ... M1_DQ63	AV16,AU16,AT16,AT15,AV15,AU14,AT14,AV14 AP14,AV13,AW13,AR13,AT13,AT12,AU12,AV1 2 AW11,AT11,AV11,AT10,AT9,AU10,AV9,AV10 AV8,AT8,AU8,AR7,AT7,AU6,AT6,AR6 AP5,AP3,AP4,AN5,AN4,AM4,AM3,AM2 AL4,AL2,AK2,AK4,AK3,AJ4,AJ1,AJ2 AF6,AG2,AG4,AG1,AH3,AH4,AJ6,AH2 AD4,AD3,AD2,AE4,AF3,AE2,AF2,AF4	IO SSTL	Memory data bus
M1_CB0 . M1_CB7	AV5,AW4,AW3,AV3,AU1,AU2,AT1,AR2	IO, SSTL	Memory data check byte
M1_DM0 ... M1_DM8	AP16,AP13,AR11,AP9,AN6,AL5,AG6,AD6,AU4	IO, SSTL	Memory data masks
M1_DQS0 ... M1_DQS8	AR15,AP12,AP10,AP8,AM6,AK6,AG5,AE5,AT4	IO, SSTL	Memory data strobes
M1_DSG0 ... M1_DSG8	AP15,AP11,AR9,AP7,AL6,AJ5,AH6,AE6,AT3	IO, SSTL	Memory dummy strobe
M1_VREF	AK18,AK19,AK17,AK16,AK14,AK13 AF10,AE10,AK15,AK12,AD10	I Analog	Memory SSTL voltage reference inputs
M1_AVDD1	AK10	1V8	Memory unit PLL power
M1_AVSS1	AJ10	GND	Memory unit PLL ground
VDDIOM1	AC3,AC7,AE3,AG7,AH5,AJ3,AK5,AL7,AM1 AN13,AN3,AN9,AP6,AR12,AR16,AR4,AT2 AT5,AU11,AU15,AU7,AU9,AV2,AV4,AV6 AW8,AD1,AD5,AC5	1V8	Memory unit SSTL IO power

Table 6. Memory unit 1 signals

Note: Pins M1_DSQ0 ... M1_DSQ8 should be implemented as NC (no connect). Connecting a load to these pins will affect the DDR interface timing.

Name	BGA	Type	Description
RST_OUT_N	AA35	O, LVTTL	Reset out to other chip.
BYPASS	AA32	I, LVTTL	Put the system PLL into bypass without glitch. Used for power management.
HIF_EN_N	AB32	I, LVTTL	Controls the enable state of the host interface.
IRQ_N	AC32	O, LVTTL	Interrupt request output.
SW_RST_IN_N	AA33	I, PU, LVTTL	Software controlled reset from the first chip.
GPIO0,GPIO1 GPIO2,GPIO3 GPIO4,GPIO5 GPIO6	AU18,AT17 AT19,AR17 AR18,AP17 AN18	IO, LVTTL	General purpose input output.
THDN1, THDP1 THDN2, THDP2	W1,V1 AW18,AW17	Analog	Thermal diode connection for diodes 1 and 2.
SREFCLK_P SREFCLK_N	V39 W39	I, Diff, SSTL	System PLL reference clock. Differential clock input.
CDI CCK CMS CRST_N	AB33 AB34 AC34 AC35	I , PU, LVTTL	CTAP control interface (conforms to IEEE 1149.1).
CDO	AB35	O, LVTTL	CTAP control interface (conforms to IEEE 1149.1).
TDI TCK TMS TRST_N	AP20 AR19 AN20 AP19	I, PU, LVTTL	JTAG interface (conforms to IEEE 1149.1).
TDO	AT20	O, LVTTL	JTAG interface (conforms to IEEE 1149.1).
SAVDD1	AA30	1V8	System PLL power
SAVSS1	Y30	GND	System PLL ground
VDDIO	AA34,Y32 AM17,AP18 AR20,AT18	3V3	LVTTL IO power
V180P1	AB28	1V8	SSTL IO power
PUP33	AC33	Analog	Needs 10KΩ pull up to 3V3
PUP18	C37	Analog	Needs 10KΩ pull up to 1V8
PDN	AP21	Analog	EFUSE pull down. Needs 10KΩ pull down to GND
MANUFACTURING TEST	K29,G2,F2 AN2,AP2 K28,AM20 AM19,AC30 AB30,W8		Used for manufacturing test. In applications, leave unconnected.

Table 7. System services signals

Name	BGA	Type	Description
MANUFACTURING TEST	AM24,AM26 AM28,AM30		Used for manufacturing test. In applications, leave unconnected.
MANUFACTURING TEST	AR21,AD32		Used for manufacturing test. In applications, leave unconnected.

Table 7. System services signals

Name	BGA	Type	Description
PERST_N	AV20	I, LVTTL	Primary chip reset. Requires a 10 kΩ external pull down resistor.
RST_INT_OUT_N	AU20	O, LVTTL	Internal reset monitor.
SW_RST_OUT_N	AV19	O, LVTTL	Software controlled reset to second chip.
STOP_CLK_OUT	AV17	O, LVTTL	Output from host accessed register to control the system clock.
STOP_CLK_IN	AV18	I, PD, LVTTL	Input to turn off the main system clock in a glitchless manner.
HIF_GPIO	AM18	IO, LVTTL	General purpose input output.

Table 8. Host related system services signals

Name	BGA	Type	Description
DMVDD1 DMVDD2	AA20 AG28	Analog	VDD on die power supply monitor
DMVSS1 DMVSS2	Y20 AG27	Analog	GND on die power supply monitor
IODVDD	M14	Analog	1V8 IO VDD on die power supply monitor (MU0)
IODVSS	M13	Analog	GND on die power supply monitor (MU0)

Table 9. Power supply

Name	BGA	Type	Description
CVDD	AA11,AA12,AA15,AA16,AA24,AA25,AA28,AA29,AB13, AB14,AB17,AB18,AB20,AB22,AB23,AB26,AB27,AC11, AC12,AC15,AC16,AC19,AC21,AC24,AC25,AC28,AC29, AD13,AD14,AD17,AD18,AD19,AD21,AD22,AD23,AD26, AD27,AE11,AE12,AE15,AE16,AE20,AE24,AE25,AE28, AE29,AF13,AF14,AF17,AF18,AF20,AF22,AF23,AF26, AF27,AG11,AG12,AG15,AG16,AG19,AG21,AG24,AG25, AG29,AH13,AH14,AH17,AH18,AH19,AH21,AH22,AH23, AH26,AH27,AJ11,AJ12,AJ15,AJ16,L11,L12,L15, L16,L19,L24,L25,L28,L29,M17,M18,M19,M21, M22,M23,M26,M27,N11,N12,N15,N16,N20,N24, N25,N28,N29,P13,P14,P17,P18,P20,P22,P23, P26,P27,R11,R12,R15,R16,R19,R21,R24,R25, R28,R29,T13,T14,T17,T18,T19,T21,T22,T23, T26,T27,U11,U12,U15,U16,U20,U24,U25,U28, U29,V13,V14,V17,V18,V20,V22,V23,V26,V27, W11,W12,W15,W16,W19,W21,W24,W25,W28,W29, Y13,Y14,Y17,Y18,Y19,Y21,Y22,Y23,Y26,Y27,L21	VDD	Core VDD power supply

Table 9. Power supply

Name	BGA	Type	Description
CVSS	AA13,AA14,AA17, AA18,AA19,AA21,AA22,AA23,AA26,AA27,AB11, AB12,AB15,AB16,AB19,AB21,AB24,AB25,AB29, AC13,AC14,AC17,AC18,AC20,AC22,AC23,AC26, AC27,AD11,AD12,AD15,AD16,AD20,AD24,AD25, AD28,AD29,AE13,AE14,AE17,AE18,AE19,AE21, AE22,AE23,AE26,AE27,AF11,AF12,AF15,AF16, AF19,AF24,AF25,AF28,AF29,AG13,AG14,AG17, AG18,AG20,AG22,AG23,AG26,AH11,AH12,AH15, AH16,AH20,AH24,AH25,AH28,AH29,AJ13,AJ14, AJ17,AJ18,AJ19,AJ20,AJ21,AJ22,AJ23,AJ24, AJ25,AJ26,AJ27,AJ28,AJ29,L13,L14,L17,L18, L22,L23,L26,L27,M11,M12,M15,M16,M20,M24,M25, M28,M29,N13,N14,N17,N18,N19,N21,N22,N23,N26, N27,P11,P12,P15,P16,P19,P21,P24,P25,P28,P29, R13,R14,R17,R18,R20,R22,R23,R26,R27,T11,T12, T15,T16,T20,T24,T25,T28,T29,U13,U14,U17,U18, U19,U21,U22,U23,U26,U27,V11,V12,V15,V16,V19, V21,V24,V25,V28,V29,W13,W14,W17,W18,W20,W22, W23,W26,W27,Y11,Y12,Y15,Y16,Y24,Y25,Y28,Y29,L20	GND	Common ground for Core VDD and all IO VDD

Table 9. Power supply

Name	BGA	Type	Description
IVSS	A2,A12,A16,A20,A24,A28, A33,A5,AA1,AA10,AA2,AA3,AA36,U4,AC4 AA37,AA38,AA39,AA4,AA5,AA6,AA7,AB1,AB10,AB2, AB3,AB36,AB37,AB4,AB5,AB6,AB7,AB8,AC1,AC10, AC2,AC36,AC37,AC6,AC8,AD30,AD33,AD34,AD35, AD36,AE30,AE32,AE33,AE34,AE35,AE36,AE37,AE7, AF30,AF32,AF33,AF35,AF36,AF37,AF5,AG10,AG3, AG30,AG32,AG33,AG34,AG35,AG36,AG37,AH1,AH10, AH30,AH32,AH33,AH34,AH35,AH36,AJ30,AJ32,AJ33, AJ34,AJ35,AJ36,AJ37,AJ7,AK11,AK23,AK25,AK27, AK29,AK32,AK33,AK34,AK35,AK36,AK37,AL3,AL32, AL33,AL35,AL36,AL37,AM22,AM23,AM25,AM27,AM29, AM31,AM32,AM33,AM34,AM35,AM36,AM5,AM8,AN11, AN15,AN17,AN19,AN22,AN23,AN24,AN25,AN26,AN27, AN28,AN29,AN30,AN31,AN32,AN33,AN34,AN35,AN36, AN37,AP22,AP23,AP24,AP26,AP27,AP28,AP29,AP30, AP32,AP33,AP34,AP35,AP36,AP37,AR1,AR10,AR14, AR22,AR23,AR24,AR25,AR26,AR27,AR28,AR29,AR3, AR30,AR31,AR32,AR33,AR34,AR35,AR36,AR37,AR5, AR8,AT21,AT22,AT23,AT24,AT25,AT26,AT27,AT28, AT29,AT30,AT31,AT32,AT33,AT34,AT35,AT36,AU13, AU17,AU19,AU21,AU23,AU24,AU25,AU27,AU28,AU29, AU3,AU31,AU32,AU33,AU35,AU36,AU37,AU5,AV1, AV21,AV38,AV39,AV7,AW12,AW16,AW2,AW21,AW38, AW5,B1,B35,B39,B7,C13,C17,C21,C25,C29,C3,C5, E1,E10,E14,E18,E22,E26,E3,E33,E5,E8,F30,F35, G11,G15,G19,G23,G27,G31,G37,H39,H5,H8,J3,J33, K11,K20,K27,K35,L37,L7,M1,M10,M39,N10,N3,N33, P35,P5,R37,R7,T32,U1,U10,U2,U36,U6,U8,V10,V2, V3,V30,V33,V38,V4,V5,V6,V7,V8,W10,W2,W3,W30, W35,W38,W4,W5,W6,W7,Y1,Y10,Y2,Y3,Y4,Y5,Y6,Y7	GND	Common ground for core VDD and all IO VDD

Table 9. Power supply

2.3 PCI Express

The PCI Express Interface is a 16 lane 2.5Gb/s serial standard used to connect to host motherboards and a variety of other systems.

The pins associated with PCI Express can be found in *Table 2.*

CSX700 can connect to a variety of host lane widths up to x16. It supports polarity reversal and limited lane reversal. The condition being that physical lane 0 must always be present in the final link configuration. The diagram below shows the supported and unsupported card and host slot configurations with respect to widths and lane reversal.

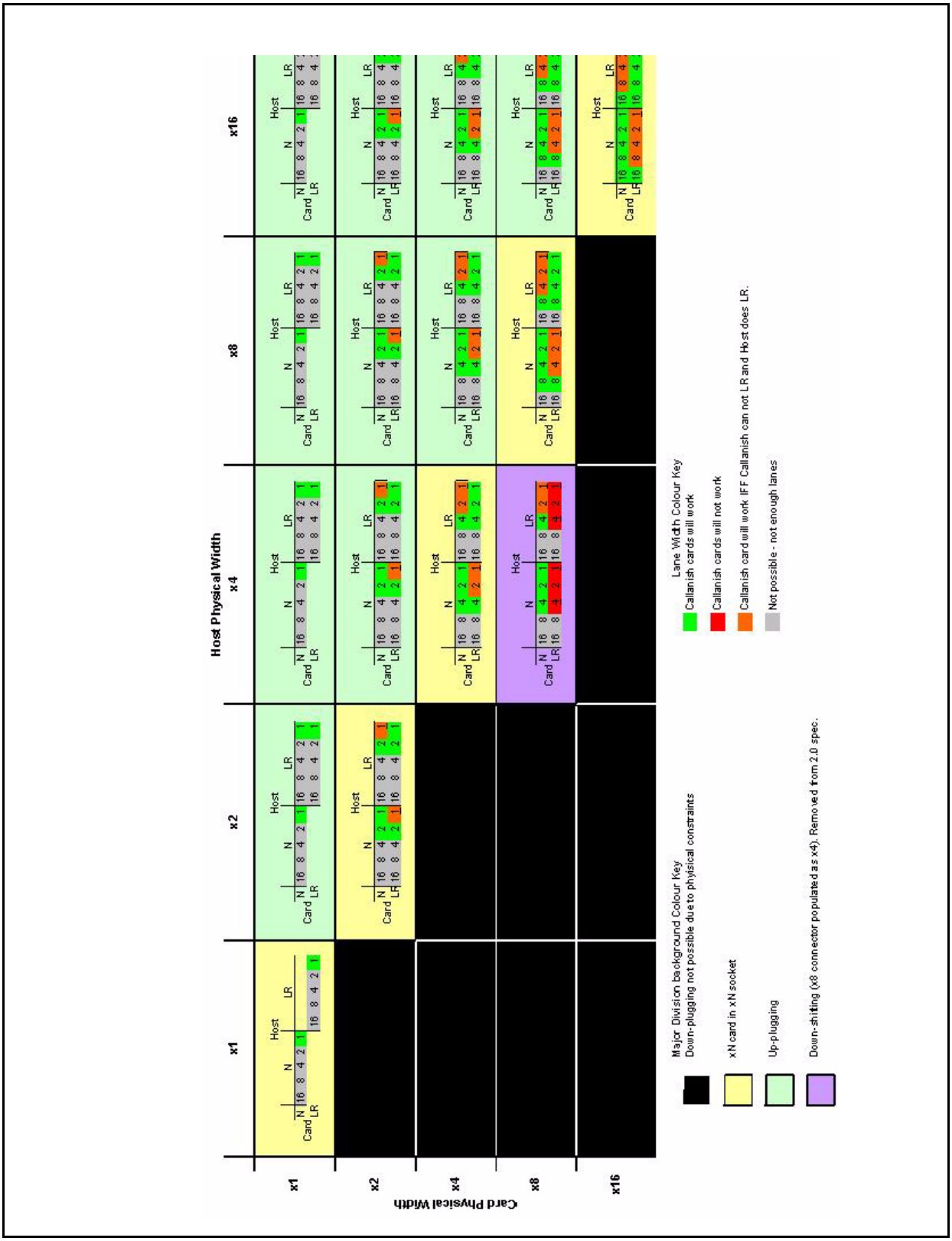

Figure 3: Permitted lane width and reversal

2.4 Host/debug port (HDP)

The HDP is used for booting the device. It also provides access to the processor debug features. It has byte-wide data ports, one each for input and output and uses a proprietary protocol. The ports are designed for multi-drop bus connections when more than one CSX700 device is used. The HDP is both a slave interface, for a host system to control the device, and a master interface, by which the device can access memory or other hardware functions that are part of host logic or associated with in-circuit debug hardware.

The pins associated with the HDP can be found in *Table 3.* The timing diagrams showing the protocol can be found in *Section 4.3*.

The HDP has its own clock input, which is typically run at a lower clock frequency than the device core. The HDP I/O pins are 3.3V LVTTL.

The HDP uses two byte-wide interfaces for input (the *downstream* interface) and output (the *upstream* interface), and both interfaces may operate simultaneously since they share no pins, other than the clock input **HCLK**. A media access control (MAC) layer allows provision for external multidrop connection so that connecting a host or debug adaptor to multiple CSX700 chips is straightforward. The only signals wired to individual devices of a multiple processor system are pins **HREQ** and **HGNT**, all others may be connected to a common bus.

Following reset, multiple interconnected CSX700 devices are enumerated by the boot system through their HDP interfaces. The boot system performs a special enumeration cycle to each device present by asserting **HGNT** while applying a device number to pins **HRX[7:0]**, which identifies its unique position on the multi-device network.

The HDP handles bus transactions transparently, one at a time. Each is treated as a stream of bytes, with header and data payload encoded according to the transaction type. The minimum length transaction encoding is 6 bytes. The data is transferred on **HTXDn** or **HRXDn** when the corresponding **HTXVAL** or **HRXVAL** is asserted The final byte in a transaction is marked with the assertion of the corresponding **HTX_EOP** or **HRXEOP** signal. Flow control is handled by **HTXSTP** and **HRXSTP**. The **HRXSTP** outputs are wired-OR from all the devices on the bus.

The HDP operates asynchronously to the device core from a dedicated clock input **HCLK**. All signals are synchronous to the rising edge of **HCLK**. The HDP contains buffering to match the slow byte-wide operation of its interfaces to the faster and wider internal bus.

HDP protocol errors are detected and indicated on the **HIRQ_N** output. This is a wired-NOR signal that can be connected to multiple devices on the HDP bus. One chip in a system, typically chip 0, has **HIRQ_N** configured as an input. It ORs its internal IRQ with the incoming IRQ and passes it on to the interrupt units. Further HDP and bus accesses may or may not be possible, depending on the nature of the error.

2.5 ClearConnect Bridge port

The ClearConnect Bridge port is a high speed port which enables data to be transferred to and from the device. The port is a full duplex 176-bit wide interface that uses DDR and clock forwarding to achieve high bandwidth. The port is a continuation of the internal ClearConnect bus, which can be *bridged* from one device to another to form a continuous packet switching network.

The pins associated with the CCBR can be found in *Table 4.*

Use of the bridge port is optional. If the bridge port is not used it can be disabled to reduce power consumption. Note that in this case the IO power supplies must still be connected.

The CCBR is software configurable for a variety of data rates. Once configured, it can be used for both AVCI (advanced virtual component interface) and PVCI (peripheral virtual component interface) traffic. Set up of the remote CCBR requires the use of the HDP.

The interface consists of 9 lanes of 9 signals; each lane being 8 data + 1 strobe. Data is transferred on both edges of the strobe. Signals within a lane must have their board traces closely skew matched at the higher operating speeds.

Pins in lanes 1 to 9 form a 72-bit bus which carries bus transactions in the form of header plus data payload with optional byte enables. The encoding of the header fields on to the device pins varies with transaction type.

The bridge ports transmit datapaths operate asynchronously from the device core, on clocks generated by a PLL whose reference is the differential input pin pair **BREFCLK_P** and **BREFCLK_N**. The input clock may be applied in single-ended mode by appropriate biasing of **BREFCLK_N**. Clock speeds are programmed through device registers. The receive data paths run at whatever frequency is applied as the forwarded clock from the transmit port of the device to which it is connected.

The PLLs can be bypassed by disconnecting the corresponding **AVDDn** supply.

Bridge port I/O pins

All pins, except **BIRQ_ N**, are bidirectional 1.8V SSTL (JEDEC standard JESD8-15a). Typically the pins are used in Class I mode although under register control they can be operated in Class II mode. When acting as receivers the pins have on-die termination and so external termination is not required. The on-die termination is either 75 Ω or 150 Ω and can be removed altogether under register control. All pads require a voltage reference input; there is one VREF pin (**BUREF0..9**) for each of the 10 groups of signal pins.

BIRQ_N is a bidirectional 1.8V LVCMOS pin which should have a pull-up resistor on the board.

2.6 Memory unit

The CSX700 uses DDR2-533 DRAM for its local memory. The data interface is 64 bits wide, with an additional 8 data bits for optional error correcting code (ECC). The CSX700 DRAM controller is software configurable for a variety of DDR2 DRAM types. The clock frequency is programmable through a PLL. The device supplies the clocks and all other signals required by the DRAMs.

Up to two ranks of devices are supported, with up to eight internal banks each, and an address width of up to sixteen bits. The interface may be operated with or without error correction, with memory width of 64 bits or 72 bits respectively. The DRAM array is operated with a DQ to DQS ratio of eight. Devices with a CAS latency of between 2 and 5 may be used.

The MU I/O pins are 1.8V SSTL operating in class I or class II, programmable using register bits for the different signal types. On-die termination is provided for all bidirectional signals; the termination is either 75 Ω or 150 Ω and can be removed altogether under register control.

The pins associated with the Memory Units can be found in *Table 5* and *Table 6*.

2.7 System services

A collection of device resources such as clocking and reset are collectively termed System Services. All signals are asynchronous. External pins are 3.3V CMOS except for **CLKIN_P** and **CLKIN_N** which are differential 1.8V SSTL. In addition, host related system service (HRSS) relates to those items that are controlled by the PCIe host but need to be accessible without traversing the CCB.

2.7.1 Reset

There are two separate reset sequences: system and PCIe. It is important that the system wide reset is removed before the final part of the PCIe reset. This is because the system bus may be required to alter configuration within the PCIe core. This is further complicated because it is possible to reset the system without resetting the PCIe subsystem. In addition it must be possible to run the device without having a PCIe host attached at all or with the host held in reset.

There is an asynchronous active low reset input pin. The entire device is held in reset whenever **PERST_N** is asserted (connected to **PERST_N** in a PCI Express system). During this reset, the PLL config for SYSPLL may be streamed in using CTAP). Once **SREFCLK_P / _N** are stable, **PERST_N** may be de-asserted. This starts two state machines which bring the system and PCIe PLLs out of reset, wait for them to lock and then removes reset from the logic.

The pin **HIF_EN_N** is used to control the configuration of the PICe. If PCIe is not used, **HIF_EN_N** should be held *high*. For system where PCIe is used, it should initially be held *low*. Once the main system reset has been removed internally, the HDP may be used to alter any PCIe configuration. The completion of this is signalled by putting **HIF_EN_N** *high* again. This allows the PCIe system to start link training.

A variety of software initiated resets are available. These are present on pins so they can be connected to another CSX700 and FPGA. The connectivity of these signals is shown in *Figure 4:*

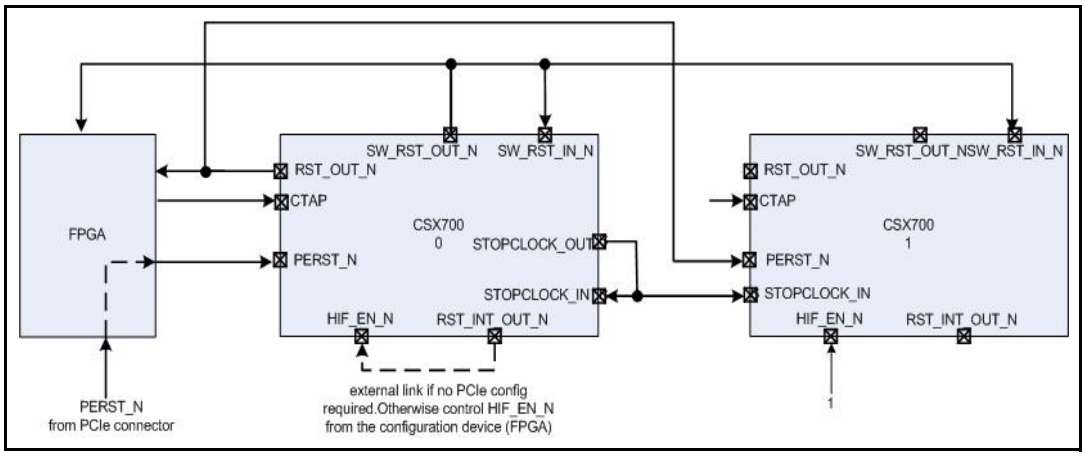

Figure 4: Reset in multiple device systems

2.7.2 Clocking

The main core clock, is generated by a PLL from an input reference of 33.33MHz to 100MHz (50MHz nominal). The PLL can be bypassed for test and debug purposes. The core clock is multiplied by a ratio that is programmed through the CTAP configuration interface.

The SYSPLL has a bypass input that can put the PLL into bypass and out again without causing any runt pulses on its output. This signal is available as a device pin **BYPASS**. This may be used to put the chip into a lower power mode. It can also be used to limit the overall power used by the board by providing a toggling signal. By varying the mark to space ratio, the amount of time the chip operates at full speed, and hence the power, can be controlled.

The SYSPLL also has the ability to glitchlessly stop the output clock. The clock can then be restarted glitch free. This is controlled by a pin **STOPCLOCK_IN**. Normally this is connected to **STOPCLOCK_OUT** of the chip with a working HIF, which is in turn under register control.

Differential inputs are provided for the PLL reference clocks to minimize jitter.

The HDP clock is input directly on the HCLK pin.

The CCBR, MU and PCIe clocks are generated within their blocks using PLLs from reference clock inputs.

2.7.3 GPIO

The general purpose I/O (GPIO) pins are 7 bidirectional I/Os that are controllable through PVCI registers. In addition there is a GPIO pin in the HRSS part of the HIF which is accessible from the host when the rest of the chip is not functioning due to CCB blocking, reset, clock or other hardware problems.

Each pin can be individually controlled and used as:

- input: data can be read by PVCI,
- output data (0,1): data can be written by PVCI,
- pseudo open drain output (0,Z): data can be written by PVCI,
- pseudo open source output data (1, Z): data can be written by PVCI,
- input interrupt with programmable polarity. These are fed into the interrupt unit and then masked as usual. Optionally, the input can go via a sticky bit.

The input is resynchronized to the core clock before being applied to the input register or interrupts.

2.7.4 Configuration TAP controller

There are a number areas where configuration or control is required prior to taking the device out of reset. To achieve this, a serial interface is provided. This interface, the Configuration TAP controller (CTAP), conforms to the JTAG test specification.

This five-pin interface uses the same signalling protocol as an IEEE 1149.1 compliant JTAG port, and drives an IEEE 1149.1 compliant state machine. It is, however, important to note that the CTAP system as a whole is **not** IEEE 1149.1 compliant.

2.7.4.1 Supported instructions

The CTAP interface contains a JTAG-like instruction register that is 4 bits long and supports the four instructions listed in *Table 10*.

Instruction	Opcode	Selected data register	Length
BYPASS	1111	Bypass register	1
PLLCTRL	1001	PLL control register	156
RESETCTRL	1010	Reset control	9
CLKCTRL	1011	Clock control register	30

Table 10. CTAP Instructions

Whenever the CTAP is reset using the **CRST_N** input pin, or by placing the CTAP state machine into Test-Logic-Reset, the BYPASS instruction is automatically loaded and the **PLLCTRL**, **RESETCTRL**, and **CLKCTRL** registers are reset to the all-zeros state. *Figure 5* shows the register structure.

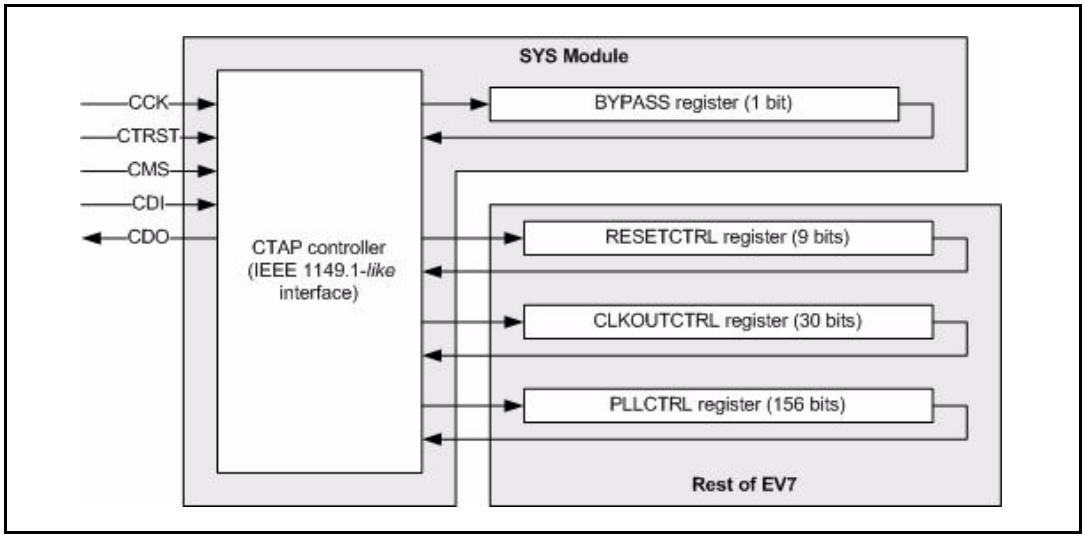

Figure 5: CTAP register structure

2.7.4.2 PLL control register

The PLL control register is used to configure the SYSPLL.

Note that bit 0 is nearest **CDO** and is shifted into **CDI** first.

Bit range	Width	Function
131:0	-	These bits should always be written with 0.
139:132	8	MULT[a]
149:140	10	TUNE[a]
153:150	4	RANGE[a]

Table 11. CTAP PLL control register

Bit range	Width	Function
154	1	No effect
155	1	PLL override - When '1', allows CTAP override of PLL settings
a: See PLL settings below.		

Table 11. CTAP PLL control register

The SYSPLL settings set during CTAP config depend on the required core clock frequency and reference clock frequency. Other output and reference clock frequencies are possible. Consult ClearSpeed for details.

Reference frequency (MHz)	Frequency (MHz)	Range (hex, 4 bits)	MULT (hex, 8 bits)	TUNE (hex, 10 bits)
50	100	6	d8	341
	125	C	74	340
	150	C	96	341
	200	E	d8	341
	250	4	bb	390

Table 12. PLL configuration settings

2.7.4.3 Reset control register

The reset control register allows control of the SYS PLL reset.

*Note: Bit 0 is nearest **CDO** and is shifted into **CDI** first.*

Bit									Description
8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	Normal operation
1	1	0	0	0	1	0	0	0	SYS PLL in reset - HIF enabled
1	1	0	1	1	0	1	1	1	SYS PLL in reset - HIF disabled
Others									Undefined

Table 13. CTAP reset control register

2.7.4.4 Clock control register

The clock control register is used for controlling the termination on the reference clock inputs. There are five reference clock inputs on the device (**SYS**, **HIF**, **MU0**, **MU1** and **CCBR**), so the CLKCTRL register is split into five sections with spaces in between as shown in *Table 14*.

Note that bit 0 is nearest **CDO** and is shifted into **CDI** first.

Bit range	Width	Function
3:0	4	Write 0000
4	1	PCI Express reference clock termination select: 0: CMOS/LVDS 1: LVPECL (default)
5	1	Write 0
9:6	4	Write 0000
11:10	2	Memory unit 1 reference clock termination select: 00: none 10: 75 Ω (default) 11: 150 Ω
15:12	4	Write 0000
17:16	2	Memory unit 0 reference clock termination select (as above)
21:18	4	Write 0000
23:22	2	CCBR reference clock termination select (as above)
27:24	4	Write 0000
29:28	2	SYS reference clock termination select (as above)

Table 14. CTAP PLL control register

2.7.5 Thermal monitor

The CSX700 die incorporates two thermal diodes. Access to the thermal monitor diodes is provided by two pairs of dedicated pins, **THDN1/THDP1** and **THDN2/THDP2**. By connecting an appropriate device, such as the National Instruments LM86, they enable measurement of die temperature during operation.

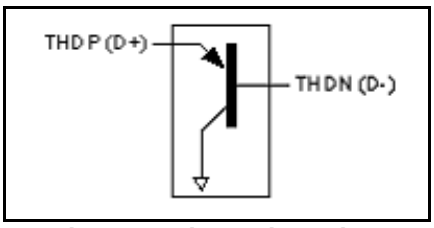

Figure 6: Thermal monitor

2.8 JTAG boundary scan test access port (TAP)

The TAP conforms to IEEE 1149.1 and supports full EXTEST on all pins (except analog functions).

All TAP input pins are 3.3V LVTTL with weak pull-ups.

2.8.1 TAP instructions

There are two registers which are accessed through the TAP controller:

- identification (read only),
- external boundary scan (I/O pads).

The available TAP instructions are shown in *Table 15*.

<table>
<tr><th>Instruction</th><th>Instruction code</th><th>Description</th><th>Length</th></tr>
<tr><td>BYPASS</td><td>1111</td><td></td><td>1</td></tr>
<tr><td>EXTEST</td><td>0000</td><td>Used for test of device connectivity in assembled system.
Contact ClearSpeed for details of the boundary scan chain.</td><td></td></tr>
<tr><td>SAMPLE</td><td>0001</td><td></td><td></td></tr>
<tr><td>IDCODE</td><td>0010</td><td>Used to identify device as part of a chain: 0x1000 73EB
<table>
<tr><th>Version
(4 bits)</th><th>Part number
(16 bits)</th><th>Manufacturer
(11 bits)</th><th>LSB</th></tr>
<tr><td>0001</td><td>0000 0000 0000 0111</td><td>0011 1110 101</td><td>1</td></tr>
</table></td><td>32</td></tr>
<tr><td>USERCODE</td><td>0100</td><td>CSX700 user code register: 0x0000 7000</td><td>32</td></tr>
</table>

Table 15. TAP instructions

3 DC and thermal characteristics

3.1 Recommended operating conditions

Parameter		Min.	Typ. (1)	Max.	Units
CVDD	Core supply voltage	0.90	1.0	1.32	V
V180P1, V180P2, VDDIOC, VDDIOM0, VDDIOM1	External (I/O) supply voltages	1.65	1.8	1.95	V
VDDIO1, VDDIO	External (I/O) supply voltages	3.0	3.3	3.6	V
BAVDD1, BAVDD2, M0_AVDD1, M1_AVDD1, SAVDD1	PLL analog supply voltage	1.65	1.8	1.95	V
PAVDD1 PAVDD2	PCIe PLL analog supply voltage	1.65	1.8	2.75	V
HSSAVDD	PCIe SerDes analog supply voltage	1.65	1.8	2.75	V
AVTT	PCIe transmit termination	1.1 or VDD	1.2	1.95	V
AVTR	PCIe receive termination	0.9 or VDD	1.2	1.95	
BVREF, M0_VREF, M1_VREF	SSTL voltage reference	0.825	0.9	0.975	V
PAVDD1, 2	PCIe analog supply current			94	mA
HSSAVDD per pin	PCIe SerDes analog supply current			16	mA
AVTT per pair of pins	PCIe transmit termination current		106	141	mA
AVTR per pin	PCIe receive termination current			0	mA
BVREF, M0_VREF, M1_VREF per interface	SSTL voltage reference current			2	mA
VDDIOC	CCBR I/O supply current		671	1790	mA
VDDIOMn	MU I/O supply current		615	1640	mA
SAVDD1, BAVDD1, BAVDD2, M0AVDD1, M1_AVDD1 per supply	PLL analog supply current			34	mA
VDDIO, VDDIO1 combined	I/O supply current		9	616	mA

Table 16. Recommended operating conditions

Parameter		Min.	Typ. (1)	Max.	Units
V180P1, V180P2 combined	I/O supply current			6.7	mA
CVDD(2)		1	8	20	A
CALRES	External resistor	2050 -0.1%	2050	2050 +0.1%	Ω
Wiring to CALRES external resistor		0	1	2	Ω
T_{case}	Case temperature	0		70	°C
T_J	Junction temperature	0		100	°C
θ_{JC}	Junction to case thermal resistance (cold plate method)		0.171		°C/W
$\theta_{JB, JEDEC test board}$	Junction to board thermal resistance		2.14		°C/W
$\theta_{JB, JEDEC application board 14 layers}$	Junction to board thermal resistance		2.12		°C/W
Ψ_{JT}	Junction to top of package JESD51-2		0.142		°C/W
Ψ_{JB}	Junction to board JESD51-6		0.67		°C/W

Table 16. Recommended operating conditions

1. Typical means running a typical power intensive application at a typical voltage (such as DGEMM).
2. CVDD: min is powered but non operational, typical is running a typical power intensive application at typical voltage (such as DGEMM) and max is this same application at maximum voltage. Other applications will generally be lower.

All thermal parameters are based on thermal simulation. A Flomerics Flotherm package model is available on request.

3.1.1 Supply sequencing

The voltage applied to **VDD** must never exceed the voltage applied to any of the **VDDIO** supplies. Particular care should be taken to ensure that **VDD** is never driven higher than **VDDIO** during power-up and power-down.

To avoid the possibility of damage to I/O pads, no I/O signal should have voltages applied outside of their corresponding **VDDIO** supply. Particular care should be taken at power-up not to apply signals to I/O pins before **VDDIO** is applied. The applied I/O voltage may track the rise of **VDDIO**, as long as the Absolute Maximum ratings are observed. **AVTT** and **AVTR** must never be lower than **VDD**.

PERST_N must be active (low) during power up.

3.2 Handling and assembly

The CSX700 meets JEDEC MSL (Moisture Sensitivity Level) 4. Once removed from the moisture-proof packaging, the components have a floor life of 72 hours (at or below 30°C / 60% relative humidity). After this they will require re-baking at 125°C for 24 hours.

Warning: **ESD (electrostatic discharge) sensitive device. Electrostatic charges of up to several thousand volts can accumulate on test equipment and the human body, and can discharge without detection. Although the CSX700 includes ESD protection circuitry, permanent damage may be caused to devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid damage and loss of functionality.**

3.3 Absolute maximum and minimum ratings

Parameter	Minimum	Maximum	Units
Core supply voltage (**VDD**)	-0.3V	+1.6	V
1.8V CMOS Input voltage[a]	-0.60	2.4	V
3.3V LVTTL Input voltage[a]	-0.60	3.9	V
IOVDD180	TBD		V
IOVDD330	TBD		V
PCIe RXxIN, RXxIP voltage	-0.5	AVTR	
PLL AVDD	TBD		V
PAVDD1, PAVDD2	-0.5	2.75	V
HSSAVDD	-0.5	2.75	V
AVTT[b]	-0.5	1.95	V
AVTR[b]	-0.5	1.95	V
T_J Operating die temperature	-20	125	°C
Soldering temperature[c]		250	°C
Storage temperature[d]	-55	125	°C

a. Over and undershoot only
b. AVTT and AVTR must never be lower than VDD
c. For lead-free e1 parts using SnAgCu BGA balls
d. For loose devices

Table 17. Absolute maximum ratings

Note: *These are stress ratings only. Conditions beyond those listed above may cause permanent damage to the device. Functional operation at these or any other conditions outside the normal operating range is not implied. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.*

3.4 Termination and reference voltages

3.4.1 CCBR

CCBR pins are 1.8V SSTL signals. The receivers have on-die termination and so in most applications external termination is not required. Because of this all pads require a voltage reference input of 1/2 **VDDIOC**; there is one **BVREF** pin for each of the 10 groups of signal pins. **BVREF** signals must be decoupled at the pin, and the signal kept away from sources of interference.

In applications where the CCBR is unused, the reference clock and **BIRQ_N** should be pulled inactive, data and control pins left unconnected and **BVREF** pins tied to ground. **VDDIOC** must still be applied, but **BAVDD** must be tied to ground.

3.4.2 PCI Express

The **PREFCLK_P** and **PREFCLK_N** pins must be externally terminated as shown in *Figure 7*. The internal termination mode must be set to LVDS using CTAP (see *Section 2.7.4.4*)

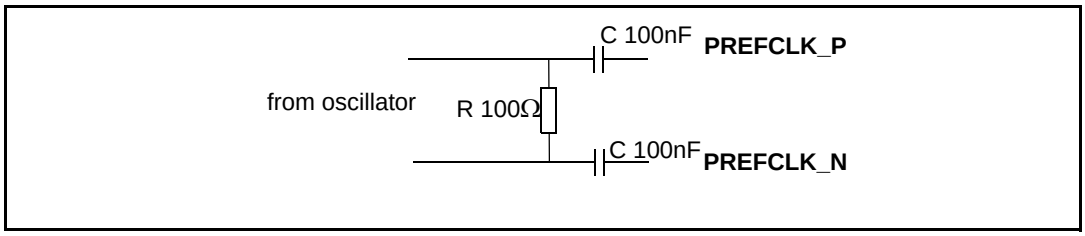

Figure 7: PCI Express reference clock termination

When unused, **PREFCLK_P/N** should be left in the default PECL mode and left unconnected.

Unused PCIe lanes should be left unconnected.

3.4.3 MU

MU pins are 1.8V bidirectional SSTL signals. When acting as receivers the pins have on-die termination and so in most applications external termination is not required. The memory reference voltage, **M*n*_VREF**, requires a voltage level of 1/2 **VDDIO**. **M*n*_VREF** signals must be decoupled at the pin, and the signal kept away from sources of interference.

In applications where the MU is unused, the reference clock should be held inactive, data and control pins left unconnected and **M*n*_VREF** pins tied to ground. **VDDIOM*n*** must still be applied, but **BAVDD** must be tied to ground.

3.4.4 Analog supplies

The analog supplies on the chip require low noise supplies to avoid clock jitter. This is achieved by a combination of supply filters and decoupling. *Table 18* below shows what is required on each pin whether it is used or unused. Type A and B filters refer to the component values. The circuit is as shown in *Figure 8*. Type A filters are required per power pin, whereas only one type B filters is required. Decoupling is per pin. When PCI Express is

used with less than all 16 lanes available, only a subset of the power supplies need filtering. The mapping between lane width and usage is shown in *Table 19*.

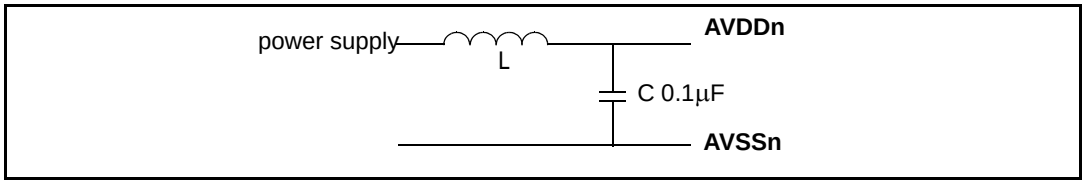

Figure 8: Analog supply filter

	Supply filter		Decoupling	
	used	**unused**	**used**	**unused**
SAVDD1 M0_AVDD1 M1_AVDD1 BAVDD1 BAVDD2	A	Direct to ground	N/A	N/A
PAVDD1, PAVDD2	A	Direct to ground	N/A	N/A
HSSAVDD0 ... HSSAVDD3	A	Direct to 1.8V supply	N/A	N/A
AVTT0 ... AVTT7	B	Direct to 1.2V supply[1]	100nF	No
AVTR0 ... AVTR3	B	Direct to 1.2V supply[1]	100nF	No
1. If all of the PCIe is unused, and 1.2V is unavailable, 1.8V supply may be used.				

Table 18. Analog supply filter and decoupling

AVTT*i*	0	1	2	3	4	5	6	7
AVTR*i*	0		1		2		3	
HSSAVDD*i*	0		1		2		3	
PCIe unused	unused							
x1	used		unused					
x2	used		unused					
x4	used		unused					
x8	used				unused			
x16	used							

Table 19. PCI Express power supply usage vs lane width

Example type A filter is:

- L: Murata BLM15BB221SN1
- C: 2.2uF Murata GRM155R60J225ME15
- Power supply: 1.8V

Example type B filter is:

- L: Murata BLM31PG121SN1
- C: 10uF Murata GRM21BR61A106KE19K
- Power supply: 1.2V

Used PCIe lanes should have a 100nF capacitor in series with each PCB trace placed close to the connector.

3.5 1.8V CMOS DC characteristics

Parameter		Min.	Typ.	Max.	Units
VIH	High level input voltage	0.65 * **V180P*n***		1.95	V
VIL	Low level input voltage	0		0.35 * **V180P*n***	V
VOH	High level output voltage	**V180P*n*** - 0.45		1.95	V
VOL	Low level output voltage	0		0.45	V
IOH	High level drive current (VOH=1.2V)[a]	12.0			mA
IOL	Low level drive current (VOL=0.45V)[a]	9.0			mA
a. **V180P*n*** = 1.65V, 100°C					

Table 20. DC characteristics for 1.8V CMOS pins

3.6 3.3V LVTTL characteristics

Parameter		Min.	Typ.	Max.	Units
VIH	High level input voltage	2.0		3.6	V
VIL	Low level input voltage	0		0.8	V
VOH	High level output voltage	2.4		3.6	V
VOL	Low level output voltage	0		0.4	V
IOH	High level drive current (VOH=2.4V)[a]	11.08			mA
IOL	Low level drive current (VOL=0.4V)[a]	7.37			mA
IOH_{GPIO}	High level drive current (VOH=2.4V)[a]	29.25			mA
IOL_{GPIO}	Low level drive current (VOL=0.4V)[a]	19.47			mA
a. VDDIOx (being either VDDIO or VDDIO1)= 3.0V, 100°C					

Table 21. DC characteristics for 3.3V LVTTL pins

3.7 SSTL DC characteristics

Parameter		Min.	Typ.	Max.	Units
VIH	High level input voltage	VREF+0.125		VDD+0.3	V
VIL	Low level input voltage	-0.3		VREF-0.125	V
VIN_{DIFF}	Input signal voltage (differential pins)	-0.3		VDDIOx+0.3	
VID_{DIFF}	Input differential voltage (differential pins)	0.25		VDDIOx(1)+0.6	
VTT	Termination voltage	VREF-0.04	VREF	VREF+0.04	V
VREF	Differential input reference	0.833	0.9	0.969	V
IOH	High level drive current (VOH=1.42V)[a]	-13.4			mA
IOL	Low level drive current (VOL=0.28V)[a]	13.4			mA
ODT75	Termination resistance at 75Ω setting	61.6	75	90	Ω
ODT150	Termination resistance at 150Ω setting	123	150	180	Ω

Table 22. DC characteristics for SSTL pins

1. Where VDDIOx is either VDDIOC, VDDIOM0 or VDDIO1.

4 AC characteristics

4.1 Test conditions

Output timings are measured with the following loads:

- HDP, JTAG, CTAP: 30pF
- CCBR: 10pF
- MU: 3pF

All designs should be simulated using IBIS models and meet all other HDK requirements.

4.2 PCI Express interface

Transmit slew, amplitude and de-emphasis, and receiver equalization can be configured prior to link bringup.

Description	Min.	Typ.	Max.	Units
Duty cycle at PREFCLK_P / _N	45	50	55	%
Rise/Fall time at PREFCLK_P / _N			1	ns
Frequency range at PREFCLK_P / _N		100		MHz
Peak - Peak at PREFCLK_P / _N	500		800	mV

Table 23. PCI Express reference clock parameters

Parameter	Description	Min.	Typ.	Max.	Units
UI_{TX}	Unit interval		400		ps
$V_{TX\text{-}DIFFp\text{-}p}$	Differential peak to peak output voltage	0.800		1.2	V
$V_{TX\_DE\_RATIO}$	De-emphasized differential output voltage ratio	-3.0	-3.5	-4.0	dB
T_{TX_EYE}	Minimum TX eye width	0.75			UI
$T_{TX\_EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125	UI
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- TX output rise fall time	0.125			UI
$V_{TX\text{-}CM\text{-}ACp}$	RMS AC peak common mode output voltage			20	mV
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0		100	mV
$V_{TX\_CM\_DC\_LINE\_DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0		25	mV

Table 24. PCI Express transmit parameters

Parameter	Description	Min.	Typ.	Max.	Units
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0		20	mV
$T_{L-TX-SKEW}$	Lane to lane output skew			500+2UI	ps

Table 24. PCI Express transmit parameters

Parameter	Description	Min.	Typ.	Max.	Units
UI_{RX}	Unit interval		400		ps
$V_{RX-DIFFp-p}$	Differential input peak to peak voltage	0.175		1.2	V
T_{RX-EYE}	Minimum receive eye width	0.4			UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and the maximum deviation from the median			0.3	UI
$V_{RX-CM-ACp}$	AC peak common mode in out voltage			150	mV
$L_{RX-SKEW}$	Total skew			20	ns

Table 25. PCIe receive parameters

4.3 HDP

All HDP timings are relative to the rising edge of input clock **HCLK**.

Name	Min.	Max.	Comment	Units
tHCK	10		Period, clock input **HCLK**	ns
tHSU	2		Setup, input to **HCLK**	ns
tHH	1.1		Hold, input from **HCLK**	ns
tHCO	0.5	5.5	Delay, **HCLK** to any output	ns

Table 26. HDP timing parameters

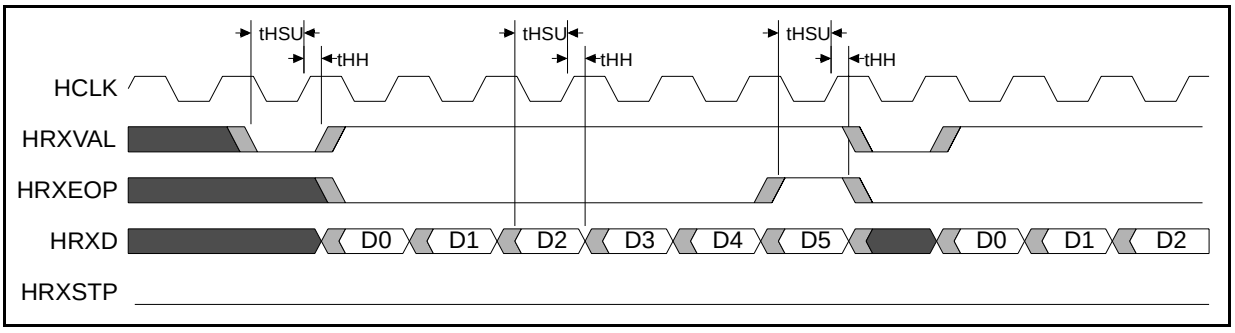

Figure 9: HDP packet

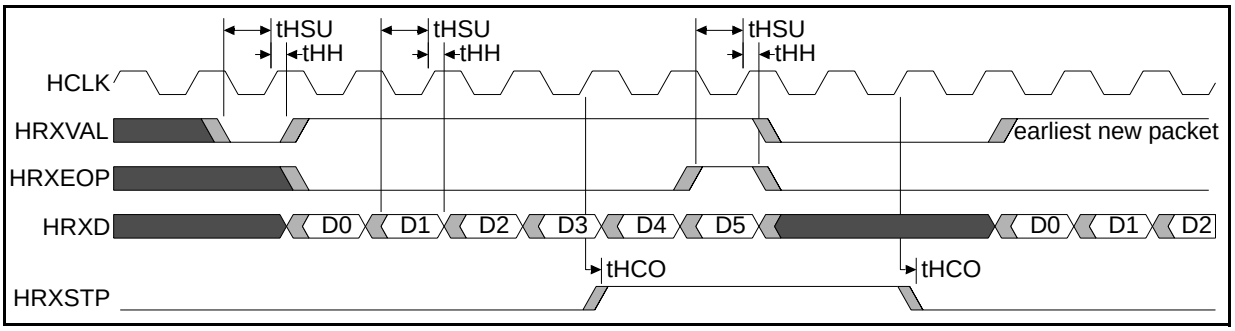

Figure 10: HDP packet receive flow control

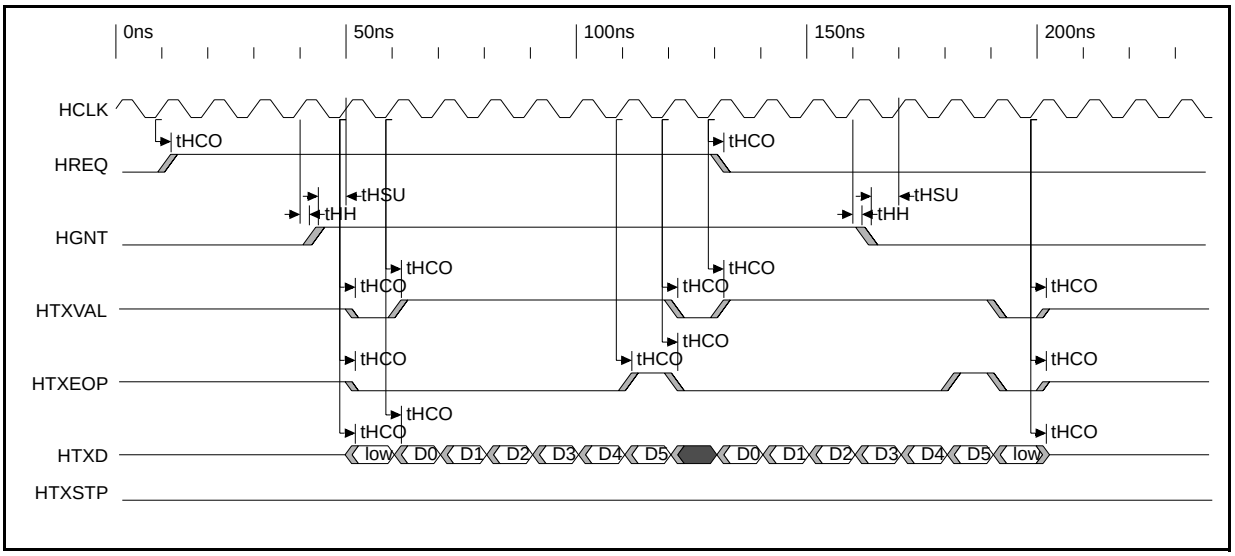

Figure 11: HDP packet transmit

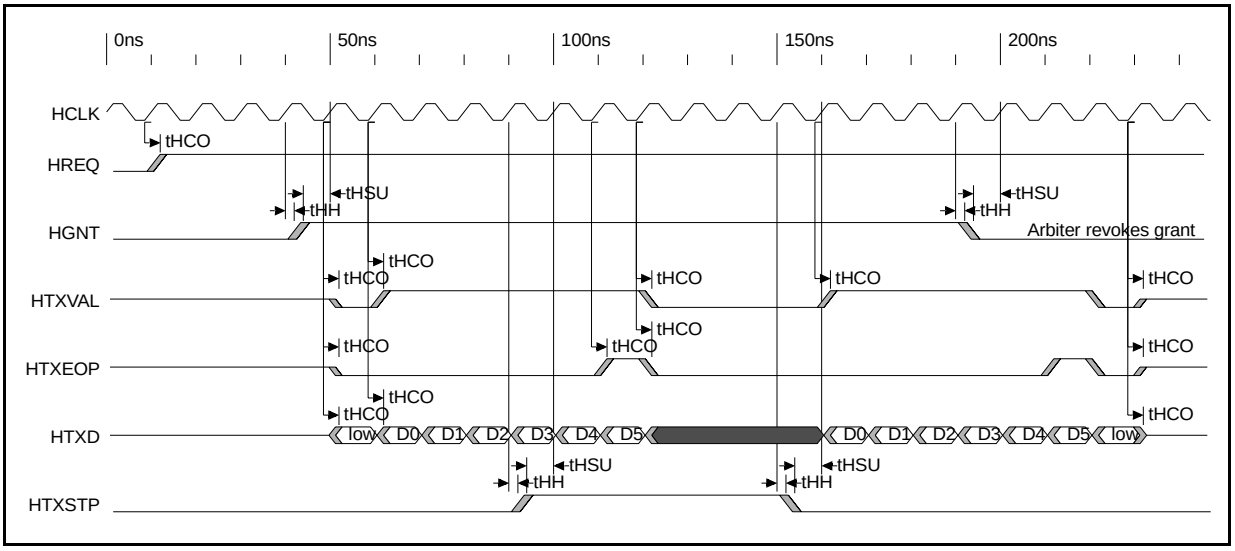

Figure 12: HDP packet transmit with flow control and grant revocation

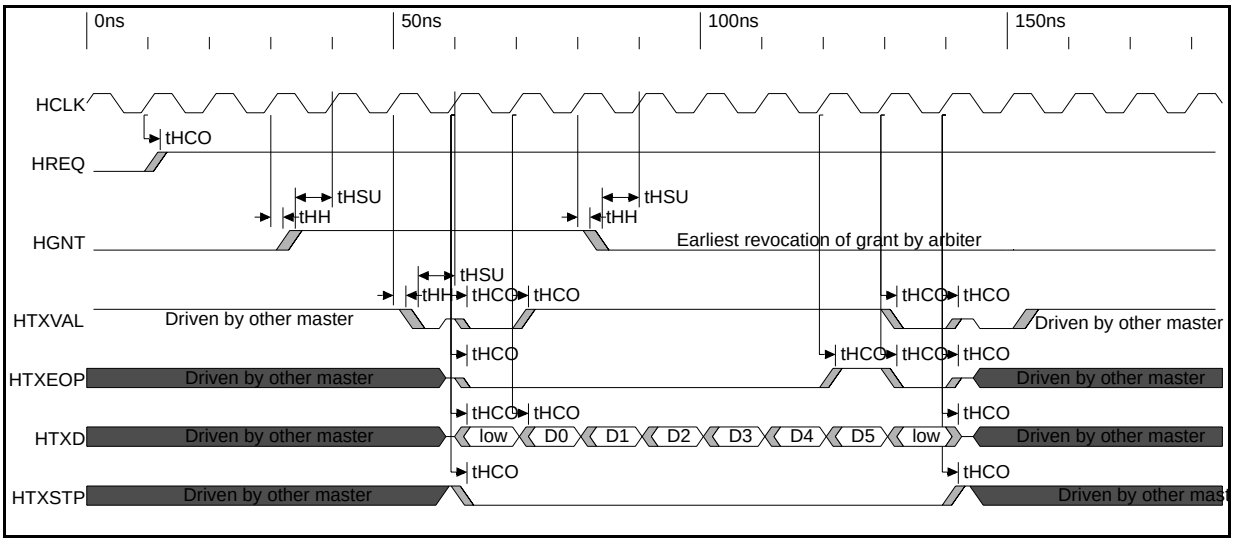

Figure 13: HDP transmit arbitration

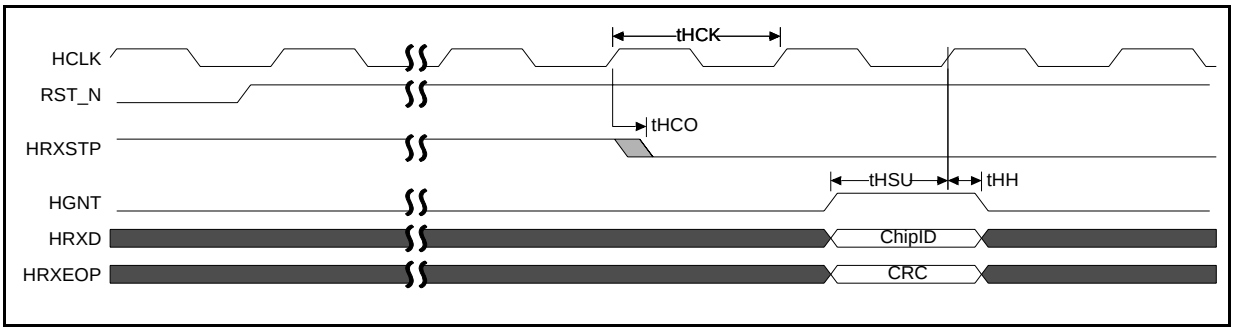

Figure 14: HDP initialization

4.4 CCBR

Name	Min.	Max.	Comment	Units
tBCK	10	30	Period bridge port transmit reference clock **BREFCLK_P, BREFCLK_N**	ns
tBCKH	3		Pulse width high, bridge port transmit reference clock **BREFCLK_P, BREFCLK_N**	ns
tBCKL	3		Pulse width low, bridge port transmit reference clock **BREFCLK_P, BREFCLK_N**	ns
ref clock jitter		100	Cycle-cycle jitter, bridge port transmit reference clock **BREFCLK_P, BREFCLK_N**	ps
tBP	2		Transmit data bit period.(1)	ns
tBCSO	-0.25	0.25	Output skew, transmit clock to any transmit strobe.	ns
tBDSO	0.5		Delay, transmit data out to strobe out rising/falling, same lane.(2)	ns

Table 27. CCBR timing parameters

Name	Min.	Max.	Comment	Units
tBSDO	0.5		Delay, strobe out rising/falling to transmit data out, same lane.	ns
tBCKI	4		Period, receive clock in.	ns
tBCSI	-1.0	1.0	Input skew, receive clock to any receive strobe.	ns
tBSU	0.25		Setup, input data valid to input strobe rising/falling, same lane.	ns
tBH	0.25		Hold, input strobe rising/falling to input data invalid, same lane.	ns

Table 27. CCBR timing parameters

1. tPP is defined by the program**ming of the Bridge Port clock generator PLL, and the input clock frequency on** BREFCLK_P, BREFCLK_N.
2. At minimum tPP.

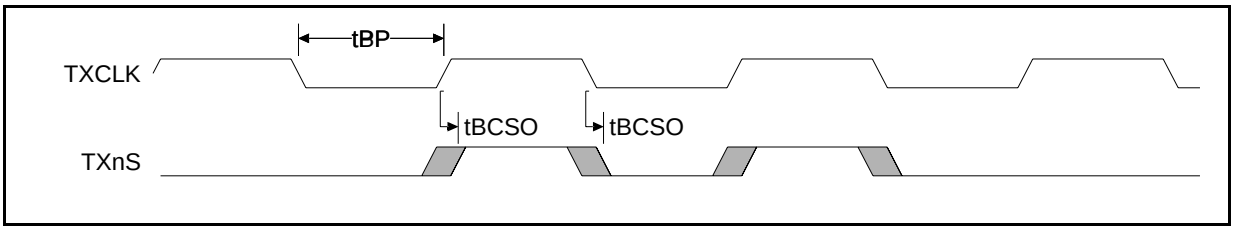

Figure 15: CCBR transmit clock and transmit strobes

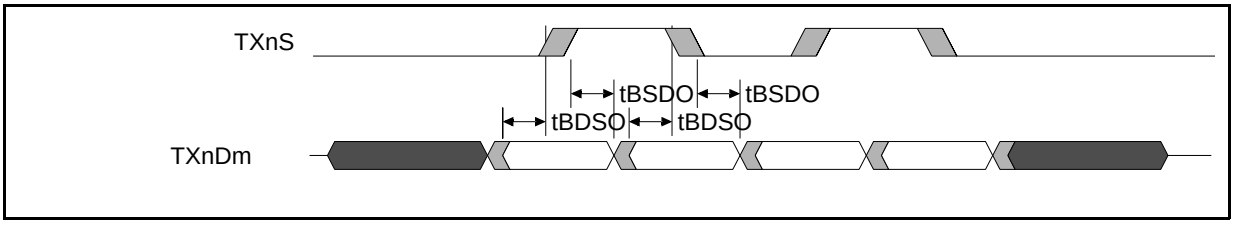

Figure 16: CCBR transmit data and strobe (same lane)

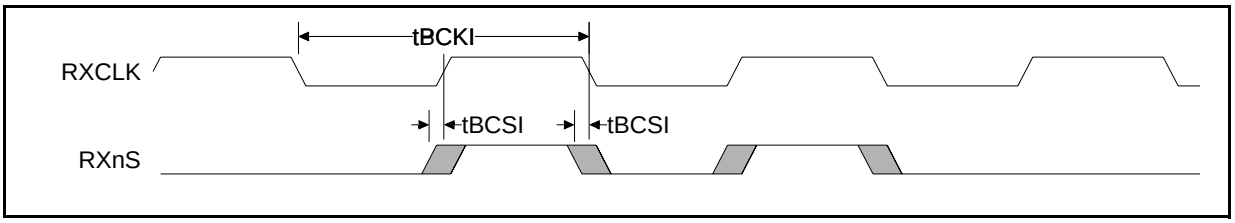

Figure 17: CCBR receive clock and receive strobe

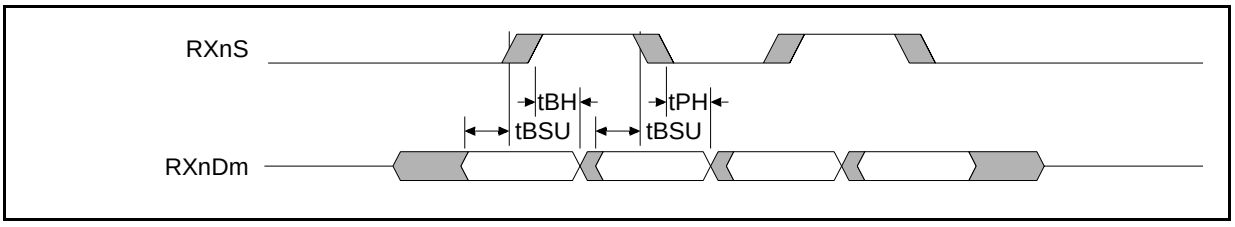

Figure 18: CCBR receive data and strobe (same lane)

4.5 Memory unit

Both memory units have the same timing parameters. The diagrams below refer to M0, but apply to M1 as well.

Correct DDR2 design requires careful PCB layout to match skew between clocks, strobes and their respective data groups. Timing between clocks, strobes and data are controllable using internal registers. For the correct settings and further board layout details, see the Hardware Development Kit.

Name	Min.	Typ.	Max.	Comment	Units
tMCK	10		30	Period, memory unit reference clock Mn_CLK_P, Mn_CLK_N	ns
tMCKH	3			Pulse high width, memory unit reference clock Mn_CLK_P, Mn_CLK_N	ns
tMCKL	3			Pulse low width, memory unti reference clock Mn_CLK_P, Mn_CLK_N	ns
tMOCK	3.75		7.5	Clock output period	ns
tMOCKH	1.8		1.95	Clock output high time (tMCK=3.75ns)	ns
tMOCKL	1.8		1.95	Clock output low time (tMCK=3.75ns)	ns
tMCKSK			50	Skew between any of the clock outputs	ps
tMDIW	400			Allowable input data window	ps
tMDQSOSK			100	Skew between output strobes	ps
tMDOW	1.5			Output data window	ns
tMCAOSU	0.9			Delay from control/address edge to following clock rising edge	ns
tMCAOH	0.9			Delay from clock rising edge to control/address edge	ns
tBPSU	0.25			Packet control (RXVAL, RXEOP) to rising RXCLK setup	ns
tBPHD	0.25			Packet control (RXVAL, RXEOP) to rising RXCLK hold	ns
tBPCO	1.0			Packet control (TXVAL, TXEOP) to rising TXCLK output	ns
tBCPO	1.0			Rising TXCLK output to packet control (TXVAL, TXEOP)	ns

Table 28. MU timing parameters

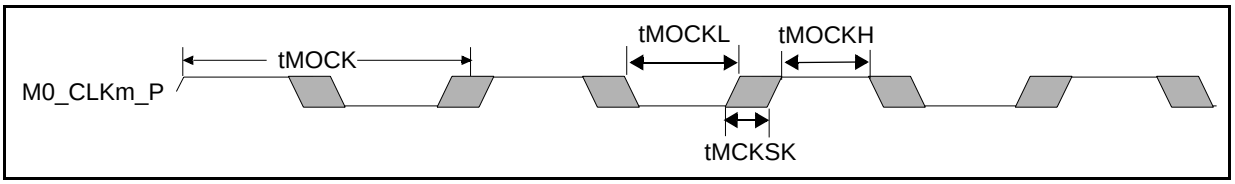

Figure 19: MU memory clock

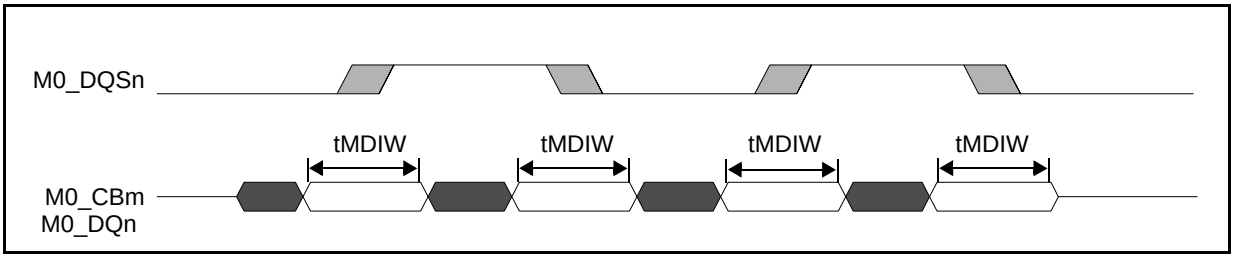

Figure 20: MU read

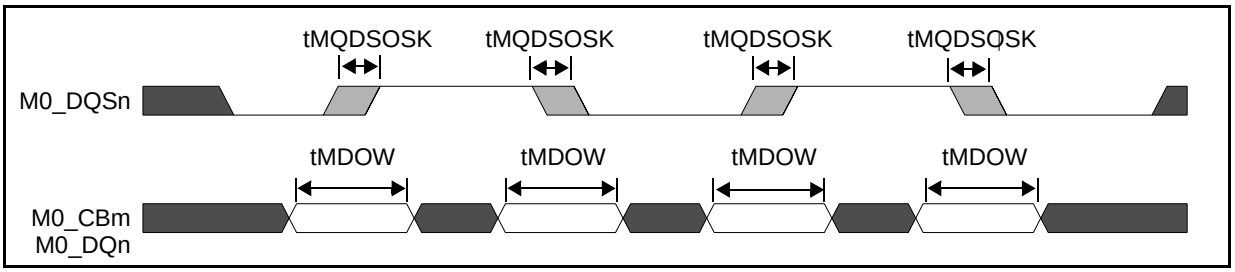

Figure 21: MU write

4.6 System service

The signals **RST_OUT_N, BYPASS, HIF_EN_N, IRQ_N, SW_RST_IN_N, GPIOn, HIF_GPIO, RST_INT_OUT_N, SW_RST_OUT_N, STOP_CLK_IN**, and **STOP_CLK_OUT** are all asynchronous to any clock.

Name	Min.	Max.	Comment	Units
fSYS(1)		250	Internal system clock frequency	MHz
tSCK	10	30(2)	Period, core reference clock **SREFCLK_P, SREFCLK_N**	ns
tSCKH	3		Pulse width high, core reference clock **SREFCLK_P, SREFCLK_N**	ns
tSCKL	3		Pulse width low, core reference clock **SREFCLK_P, SREFCLK_N**	ns
jitter		100	Cycle-cycle jitter, core reference clock **SREFCLK_P, SREFCLK_N**	ps
tRST	100		**PERST_N** assertion pulse width	ns

Table 29. SYS timing parameters

1. Internal clock frequency is set by the reference clock and internal PLL settings that can be altered using CTAP.
2. Maximum period is only relevant when using SYSPLL. BYPASS mode can tolerate any maximum period.

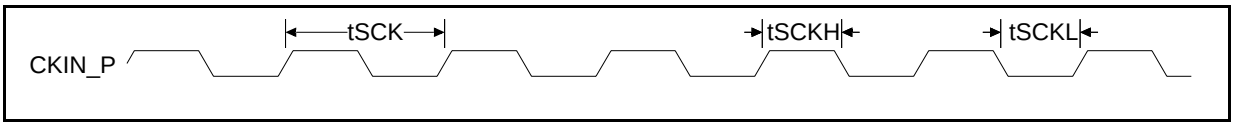

Figure 22: System reference clock

4.6.1 JTAG and CTAP

The operation of the IEEE1149.1 JTAG port and CTAP are independent of the other device interfaces. They both have the same timing parameters.

Name	Min.	Max.	Comment	Units
tTRST	50		**TRST_N** assertion pulse width	ns
tTSDC	10		**TMS**, **TDI** setup before **TCK** rising	ns
tTHCD	25		**TMS**, **TDI** hold after **TCK** rising	ns
tTCCYC	50		**TCK** period rising to rising	ns
tTCPW	25		**TCK** high or low pulse width	ns
tTCO	0	15	**TCK** falling to **TDO** valid delay	ns

Table 30. Test access port timing parameters

5 Bootstrap sequence

The usual initialization and bootstrap sequence is summarized below.

1. Power-up and wait for power to stabilize with **PERST_N** asserted.
2. Stabilize system and PCIe reference clocks.
3. Change system PLL configuration using CTAP if required.
4. De-assert **PERST_N**, with **HIF_EN_N** held low.
5. Wait until **RST_INT_OUT_N** is deasserted, indicating PLL lock and main system has come out of reset.
6. Configure chip ID using HDP if required.
7. Configure PCIe parameters using HDP is required.
8. Put **HIF_EN_N** high to allow PCIe to start link training.
9. Host processor programs CCB threshold registers in SYS_SRV using HIF.
10. Host processor programs other system registers.
11. Host processor initializes MU and CCBR.
12. Host processor boots MTAP.

Note: Further information is available from the Hardware Programming Manual.

6 Mechanical data

The CSX700 is available in a 1,429 pin thermally-enhanced Ball Grid Array (BGA) package. Mechanical details are shown in *Figure 23* and *Figure 24*.

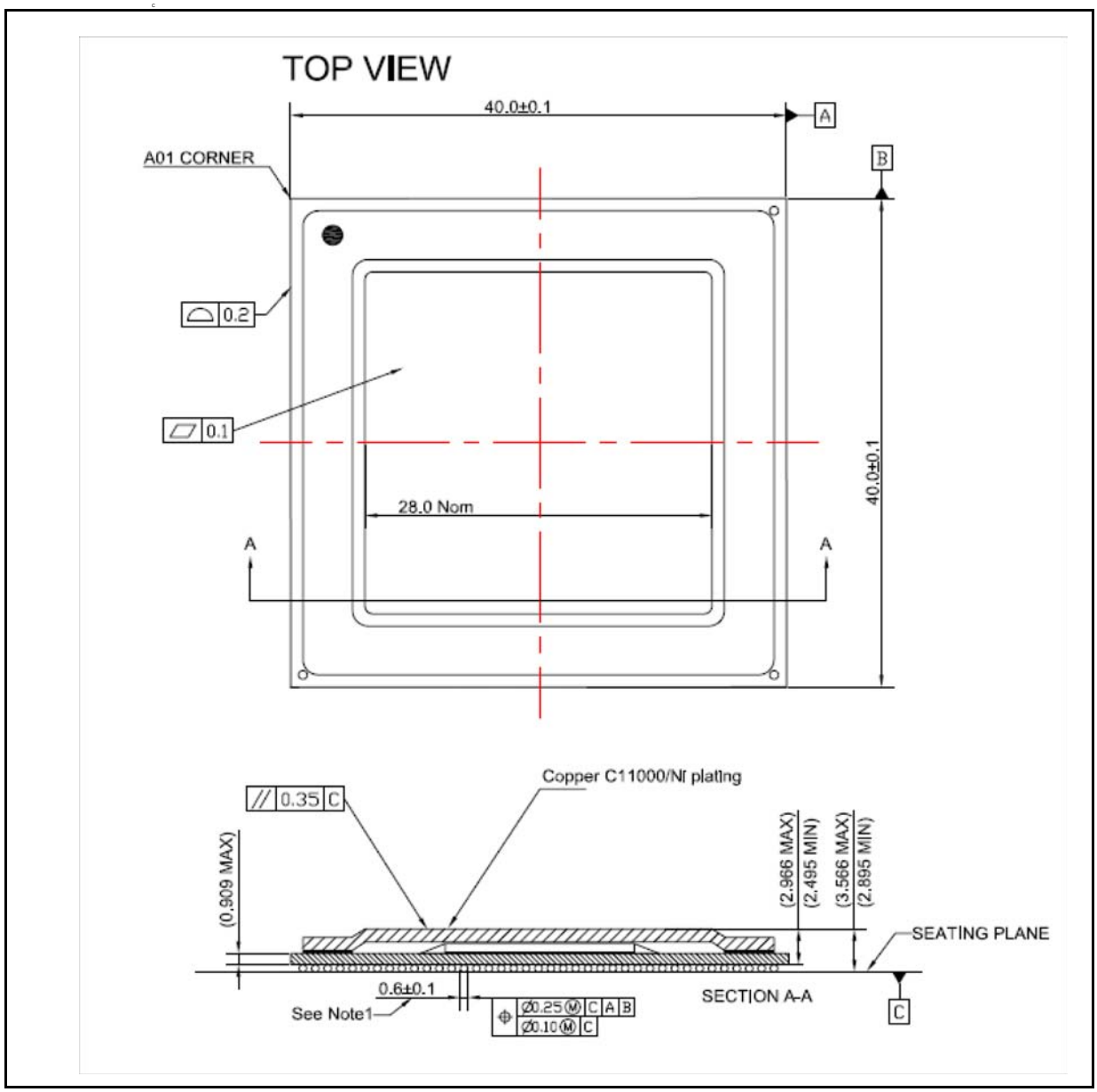

Figure 23: Mechanical data - top view

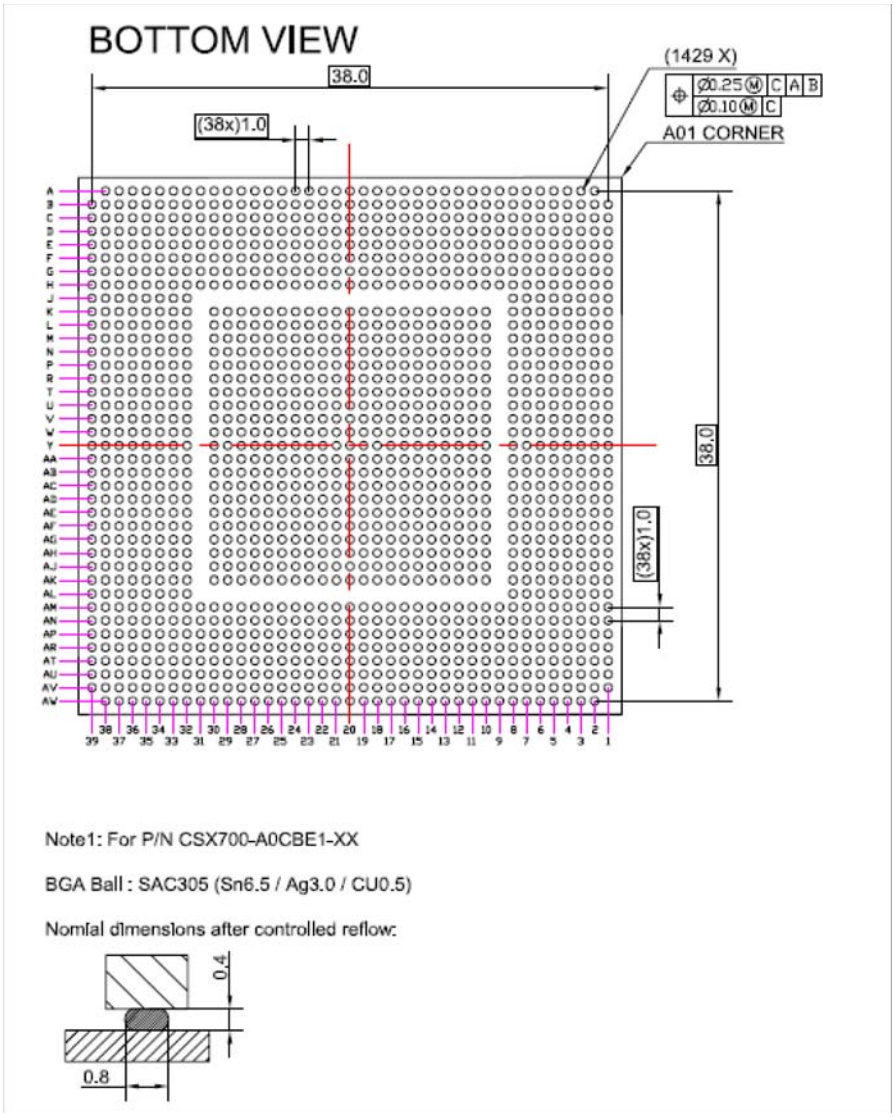

Figure 24: Mechanical data - bottom view

7 Ordering information

The available products are shown in the table below. These are the products planned for volume production. Contact your ClearSpeed representative to confirm availability of specific products and to check on new releases.

ClearSpeed order code	Device marking	Description
	CSX700-A0CBEI-ES	Engineering samples
	CSX700-A0CBEI	Production devices

The device marking is made up of the following elements.

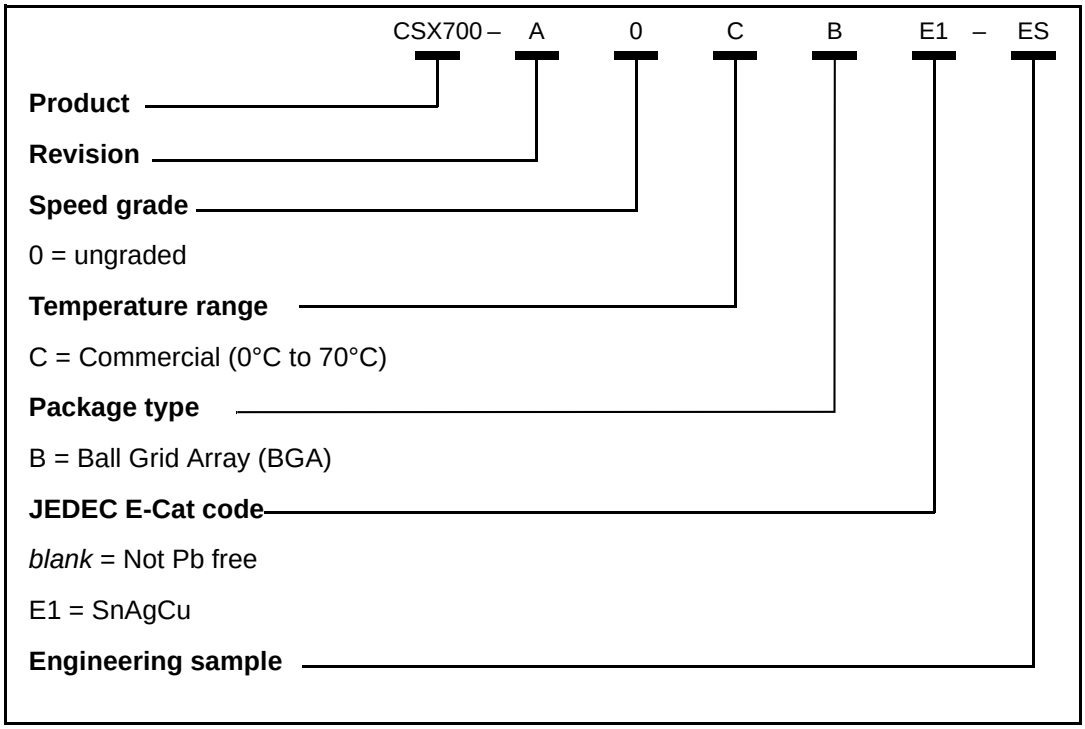

Figure 25: Marking elements

Revision history

Date	Revision	Changes
August 2008	A	Initial released version.
August 2009	B	Updated Company Information
August 2010	C	Updated Company Information
September 2010	D	Updated Company Information
January 2011	E	Updated Company Information

Table 31. Document revision history

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