219-0008; Rev 1; 3/12

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

General Description

The DS28E02 combines 1024 bits of EEPROM with challenge-and-response authentication security implemented with the FIPS 180-3 Secure Hash Algorithm (SHA-1). The 1024-bit EEPROM array is configured as four pages of 256 bits with a 64-bit scratchpad to perform write operations. All memory pages can be write protected, and one page can be put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. Each DS28E02 has its own guaranteed unique 64-bit ROM registration number that is factory installed into the chip. The DS28E02 communicates over the single-contact 1-Wire® bus. The communication follows the standard 1-Wire protocol with the registration number acting as the node address in the case of a multidevice 1-Wire network.

Applications

Reference Design License Management

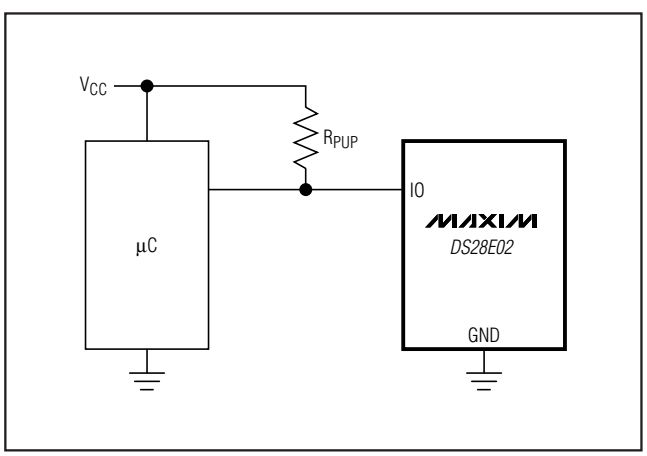
System Intellectual Property Protection

Sensor/Accessory Authentication and Calibration

Medical Consumable Authentication

Printer Cartridge Configuration and Monitoring

Typical Operating Circuit



Features

- **1024 Bits of EEPROM Memory Partitioned Into Four Pages of 256 Bits**
- **On-Chip 512-Bit SHA-1 Engine to Compute 160-Bit Message Authentication Codes (MACs) and to Generate Secrets**
- **Write Access Requires Knowledge of the Secret and the Capability of Computing and Transmitting a 160-Bit MAC as Authorization**
- **User-Programmable Page Write Protection for Page 0, Page 3, or All Four Pages Together**
- **User-Programmable OTP EPROM Emulation Mode for Page 1 (“Write to 0”)**
- **Communicates to Host with a Single Digital Signal at 12.5kbps or 35.7kbps Using 1-Wire Protocol**
- **Switchpoint Hysteresis and Filtering to Optimize Communication Performance in the Presence of Noise**
- **Reads and Writes Over 1.75V to 3.65V Voltage Range from -20°C to +85°C**
- **6-Lead TSOC and TDFN Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS28E02P+	-20°C to +85°C	6 TSOC
DS28E02P+T&R	-20°C to +85°C	6 TSOC
DS28E02Q+T&R	-20°C to +85°C	6 TDFN-EP* (2.5k pcs)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim’s website at www.maxim-ic.com.

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

ABSOLUTE MAXIMUM RATINGS

IO Voltage Range to GND .....-0.5V to +4V
IO Sink Current 20mA
Operating Temperature Range .....-20°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -20°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 2)	1.75		3.65	V
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)	300		750	Ω
Input Capacitance	C_{IO}	(Notes 4, 5)		1500		pF
Input Load Current	I_L	IO pin at V_{PUP}	0.05		5	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6, 7)	0.4		V_{PUP} – 0.89	V
Input Low Voltage	V_{IL}	(Notes 2, 8)			0.30	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 6, 9)	0.74		V_{PUP} – 0.49	V
Switching Hysteresis	V_{HY}	(Notes 5, 6, 10)	0.26		1.02	V
Output Low Voltage	V_{OL}	At 4mA current load (Note 11)			0.4	V
Recovery Time (Notes 2, 12)	t_{REC}	Standard speed, RPUP = 750Ω	20			µs
		Overdrive speed	20			
Time Slot Duration (Notes 2, 13)	t_{SLOT}	Standard speed	80			µs
		Overdrive speed	28			
IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE						
Reset Low Time (Note 2)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	50		80	
Reset High Time (Note 14)	t_{RSTH}	Standard speed	480			µs
		Overdrive speed	48			
Presence-Detect Sample Time (Notes 2, 15)	t_{MSP}	Standard speed	60		72	µs
		Overdrive speed	7		10	
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Notes 2, 16)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	8		15.5	
Write-One Low Time (Notes 2, 16)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	1		2	
IO PIN: 1-Wire READ						
Read Low Time (Notes 2, 17)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read Sample Time (Notes 2, 17)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
EEPROM						
Programming Current (Notes 5, 18)	I_{PROG}	IO voltage < 3.65V			3.5	mA
		IO voltage < 2.95V			2.5	
		IO voltage = 1.75V			1.0	

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -20°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Programming Time	t_{PROG}	(Note 19)			25	ms
Write/Erase Cycles (Endurance) (Notes 20, 21)	N_{CY}	At +25°C	200,000			—
		At +85°C	50,000			
Data Retention (Notes 22, 23, 24)	t_{DR}	At +85°C	40			Years
SHA-1 ENGINE						
Computation Current	I_{LCSHA}	(Notes 5, 18)	Refer to full data sheet			mA
Computation Time (Notes 5, 25)	t_{CSHA}					ms

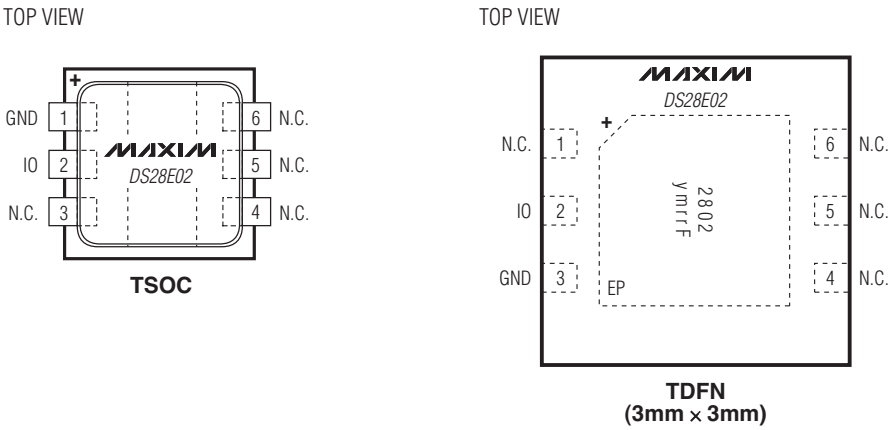
Note 1: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.
Note 2: System requirement.
Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.
Note 4: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
Note 5: Guaranteed by design, characterization, and/or simulation only. Not production tested.
Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 7: Voltage below which, during a falling edge on IO, a logic 0 is detected.
Note 8: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic 0 level.
Note 9: Voltage above which, during a rising edge on IO, a logic 1 is detected.
Note 10: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic 0.
Note 11: The I-V characteristic is linear for voltages less than 1V.
Note 12: Applies to a single device attached to a 1-Wire line.
Note 13: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.
Note 14: An additional reset or communication sequence cannot begin until the reset high time has expired.
Note 15: Interval after t_{RSTL} during which a bus master can read a logic 0 on IO if there is a DS28E02 present. The power-up presence detect pulse could be outside this interval but will be complete within 2ms after power-up.
Note 16: ε in Figure 12 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.
Note 17: δ in Figure 12 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.
Note 18: Current drawn from IO during the EEPROM programming interval or SHA-1 computation.

Note 19: Refer to full data sheet for this note.

Note 20: Write-cycle endurance is degraded as T_A increases.
Note 21: Not 100% production tested; guaranteed by reliability monitor sampling.
Note 22: Data retention is degraded as T_A increases.
Note 23: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.
Note 24: EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended; the device can lose its write capability after 10 years at +125°C or 40 years at +85°C.
Note 25: Refer to full data sheet for this note.

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

Pin Configurations



Pin Description

PIN		NAME	FUNCTION
TSOC	TDFN-EP		
1	3	GND	Ground Reference
2	2	IO	1-Wire Bus Interface. Open-drain signal that requires an external pullup resistor.
3, 4, 5, 6	1, 4, 5, 6	N.C.	Not Connected
—	—	EP	Exposed Pad (TDFN Only). Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.

Detailed Description

The DS28E02 combines 1024 bits of EEPROM organized as four 256-bit pages, a 64-bit secret, a register page, a 512-bit SHA-1 engine, and a 64-bit ROM registration number in a single chip. Data is transferred serially through the 1-Wire protocol, which requires only a single data lead and a ground return. The DS28E02 has an additional memory area called the scratchpad that acts as a buffer when writing to the memory, the register page, or when installing a new secret. Data is first written to the scratchpad from where it can be read back. After the data has been verified, a copy scratchpad command transfers the data to its final memory location, provided that the DS28E02 receives a matching 160-bit MAC. The computation of the MAC involves the secret and additional data stored in the DS28E02 including the device's registration number. The DS28E02 understands a unique command "Refresh Scratchpad." Proper use of a refresh sequence after a copy scratchpad operation reduces the number of weak bit failures if the device is used in a touch environment (see the *Writing with Verification* section). The refresh sequence also provides a means to restore functionality in a device with bits in a weak state.

In addition to its important use as a unique data value in cryptographic SHA-1 computations, the device's 64-bit ROM ID guarantees unique identification and can be used to electronically identify the equipment in which it is used. The ROM ID is also used to address the device for the case of a multidrop 1-Wire network environment, where multiple devices reside on a common 1-Wire bus and operate independently of each other. Applications of the DS28E02 include reference design license management, system intellectual property protection, accessory

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

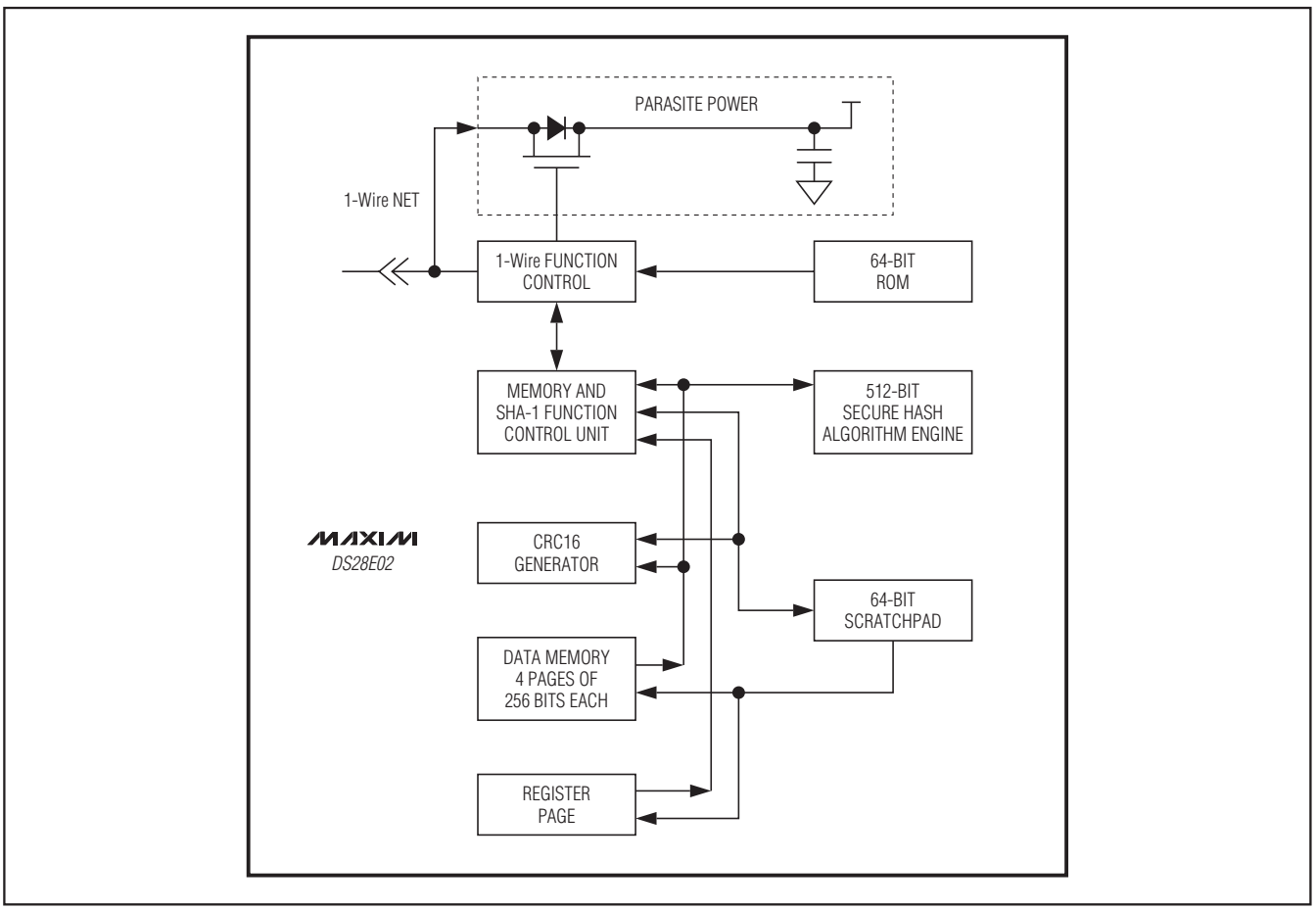


Figure 1. Block Diagram

or consumable authentication and calibration, and printer cartridge configuration and monitoring.

Overview

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS28E02. The DS28E02 has six main data components: 64-bit ROM, 64-bit scratchpad, four 256-bit pages of EEPROM, register page, and a 512-bit SHA-1 engine. Figure 2 shows the hierarchic structure of the 1-Wire protocol. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, Resume Communication, Overdrive-Skip ROM, or Overdrive-Match ROM. Upon completion of an Overdrive-Skip ROM or Overdrive-Match ROM command executed at standard speed, the device enters overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 10. After a ROM function command is successfully executed, the memory and SHA-1 functions become accessible and the master can provide any one of the 9 available function commands. The function protocols are described in Figure 8. **All data is read and written least significant bit first.**

64-Bit ROM

Each DS28E02 contains a unique ROM registration number that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in Application Note

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

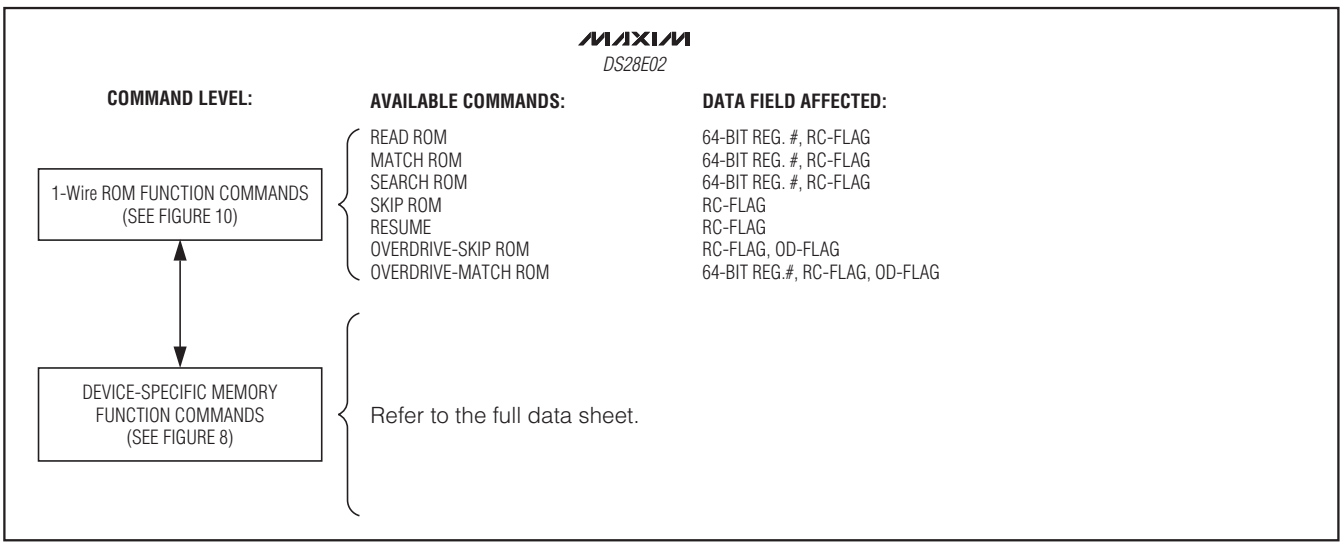


Figure 2. Hierarchic Structure for 1-Wire Protocol

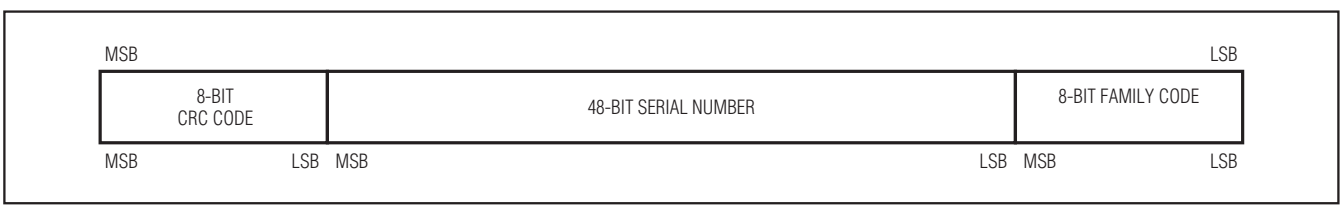


Figure 3. 64-Bit ROM

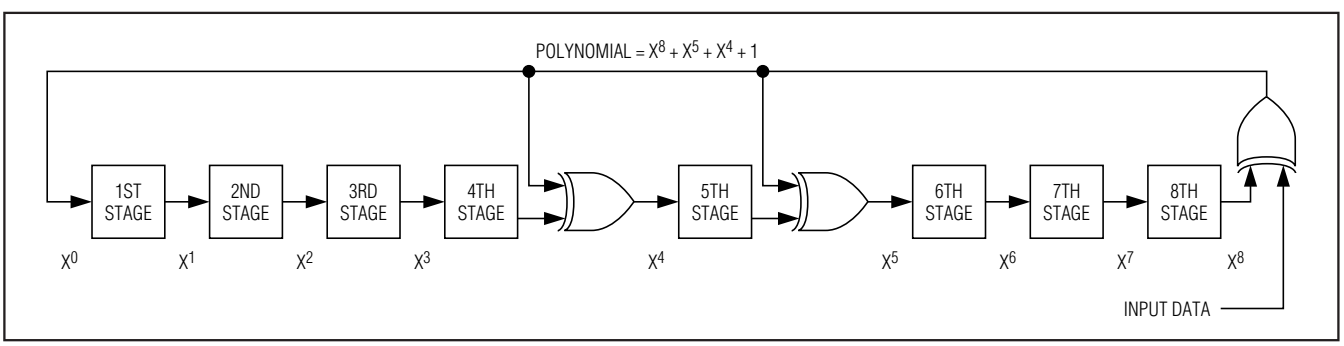


Figure 4. 1-Wire CRC Generator

27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products*.

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

Memory Access

The DS28E02 has four memory areas: data memory, secrets memory, register page with special function registers and user bytes, and a volatile scratchpad. The data memory is organized as four pages of 32 bytes.

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

Refer to the full data sheet.

Figure 5. Memory Map

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

Refer to the full data sheet.

Figure 6. Memory Protection Matrix

BIT #	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2 (0)	T1 (0)	T0 (0)
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	1	PF	1	1	E2 (1)	E1 (1)	E0 (1)

Figure 7. Address Registers

Address Registers and Transfer Status

The DS28E02 employs three address registers: TA1, TA2, and E/S (Figure 7). These registers are common to many other 1-Wire devices, but operate slightly differently with the DS28E02. Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is read. Register E/S is a read-only transfer-status register used to verify data integrity with write commands. Since the scratchpad of the DS28E02 is designed to accept data in blocks of 8 bytes only, the lower 3 bits of TA1 are forced to 0 and

the lower 3 bits of the E/S register (ending offset) always read 1. This indicates that all the data in the scratchpad is used for a subsequent copying into main memory or secret. Bit 5 of the E/S register, called PF or partial byte flag, is a logic 1 if the number of data bits sent by the master is not an integer multiple of eight or if the data in the scratchpad is not valid due to a loss of power. A valid write to the scratchpad clears the PF bit. Bits 3, 4, and 6 have no function; they always read 1. The partial flag supports the master checking the data integrity after a write command. The highest valued bit of the E/S register, called authorization accepted (AA), acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

Writing with Verification

To write data to the DS28E02, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command, which specifies the desired target address and the data to be written to the scratchpad. Note that writes to data memory must be performed on 8-byte boundaries with the three LSBs of the target address T[2:0] equal to 000b. Therefore, if T[2:0] are sent with nonzero values, the device sets these bits to 0 and uses the modified address as the target address. The master should always send eight complete data bytes. After the 8 bytes of data have been transmitted, the master can elect to receive an inverted CRC-16 of the Write Scratchpad command, the address as sent by the master, and the data as sent by the master. The master can compare the CRC to the value it has calculated itself to determine if the communication was successful. After the scratchpad has been written, the master should always perform a read scratchpad to verify that the intended data was in fact written. During a read scratchpad, the DS28E02 repeats the target address TA1 and TA2 and sends the contents of the E/S register. The partial flag (bit 5 of the E/S register) is set to 1 if the last data byte the DS28E02 received during a write scratchpad or refresh scratchpad command was incomplete, or if there was a loss of power since data was last written to the scratchpad. The authorization-accepted (AA) flag (bit 7 of the E/S register) is normally cleared by a write scratchpad or refresh scratchpad; therefore, if it is set to 1, it indicates that the DS28E02 did not understand the proceeding write (or refresh) scratchpad command. In either of these cases, the master should rewrite the scratchpad. After the master receives the E/S register, the scratchpad data is received. The descriptions of write scratchpad and refresh scratchpad provide clarification of what changes can occur to the scratchpad data under certain conditions. An inverted CRC of the read scratchpad command, target address, E/S register, and scratchpad data follows the scratchpad data. As with the write scratchpad command, this CRC can be compared to the value the master has calculated to determine if the communication was successful. After the master has verified the data, it can send the copy scratchpad to copy the scratchpad to memory.

Refer to the full data sheet.

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

Memory and SHA-1 Function Commands

This section describes the commands and flowcharts needed to use the memory and SHA-1 engine of the device. **Refer to the full data sheet for more information.**

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS28E02 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

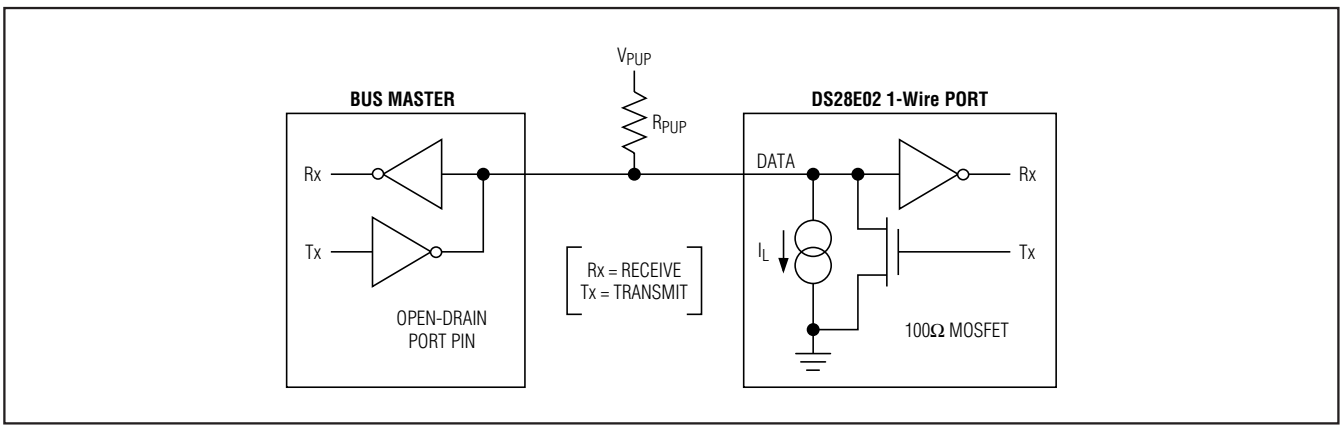


Figure 9. Hardware Configuration

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E02 is open drain with an internal circuit equivalent to that shown in Figure 9.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E02 supports both a standard and overdrive communication speed of 12.5kbps (max) and 35.7kbps (max), respectively. Note that legacy 1-Wire products support a standard communication speed of 16.3kbps and overdrive of 142kbps. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E02 requires a pullup resistor of 750Ω (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **must** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E02 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory/SHA Function Command
- Transaction/Data

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E02 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28E02 supports. All ROM function commands are 8 bits long. A list of these commands follows (see the flowchart in Figure 10).

Read ROM [33h]

The Read ROM command allows the bus master to read the DS28E02's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit device registration number, allows the bus master to address a specific DS28E02 on a multidrop bus. Only the DS28E02 that exactly matches the 64-bit registration number responds to the subsequent memory or SHA-1 function command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the search tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit registration number. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

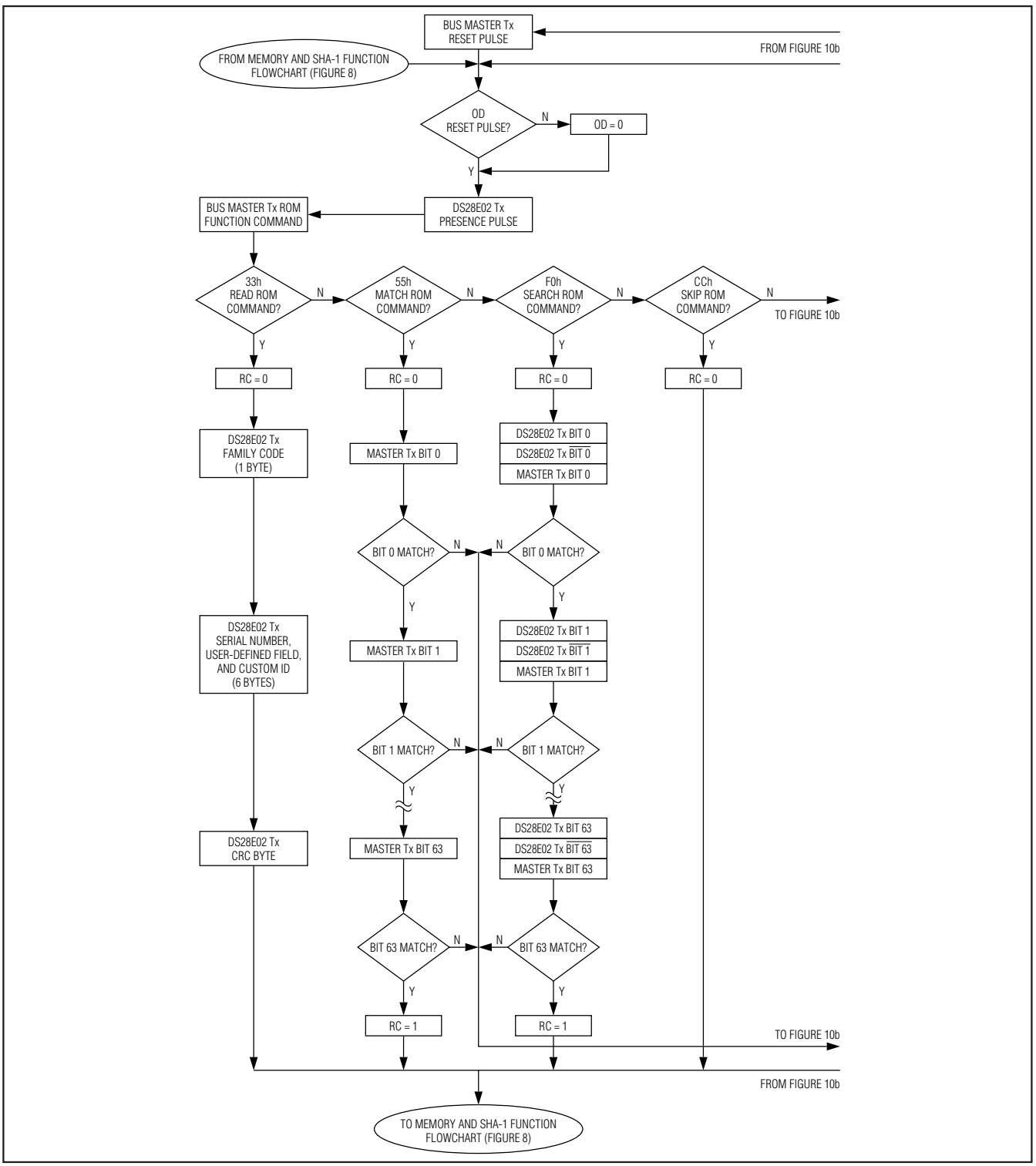
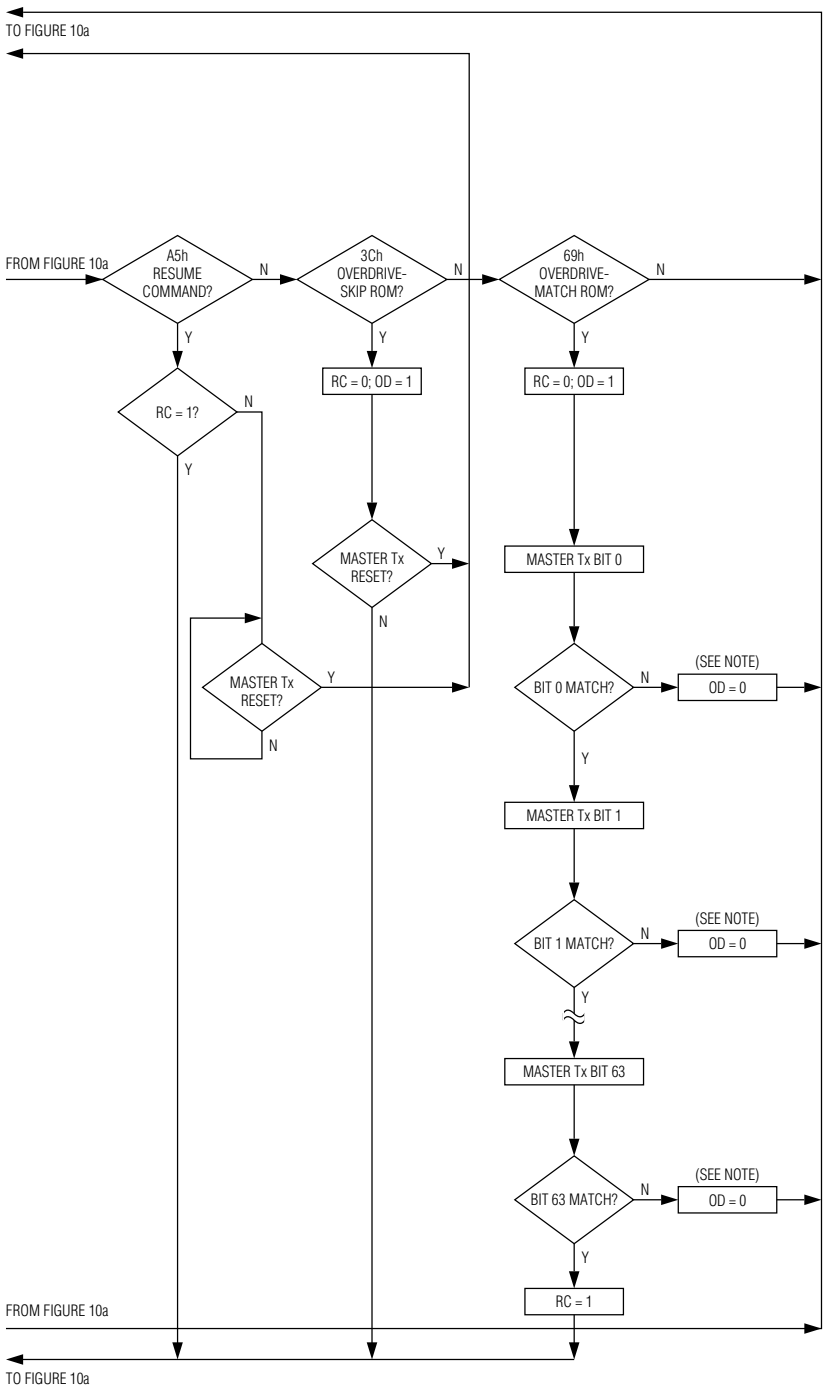


Figure 10a. ROM Functions Flowchart



NOTE: THE OD FLAG REMAINS AT 1 IF THE DEVICE WAS ALREADY AT OVERDRIVE SPEED BEFORE THE OVERDRIVE-MATCH ROM COMMAND WAS ISSUED.

Figure 10b. ROM Functions Flowchart

1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the memory and SHA-1 function commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit registration number. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS28E02 into the overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480Ìs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit registration number transmitted at overdrive speed allows the bus master to address a specific DS28E02 on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS28E02 that exactly matches the 64-bit number responds to the subsequent memory or SHA-1 function command. Slaves already in overdrive mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in overdrive mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive-Match ROM command can be used with a single device or multiple devices on the bus.

1-Wire Signaling

The DS28E02 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS28E02 can communicate at at two different speeds: standard speed and overdrive speed. If not explicitly set into the overdrive mode, the DS28E02 communicates at standard speed. While in overdrive mode, the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 11 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28E02 when determining a logical level, not triggering any events.

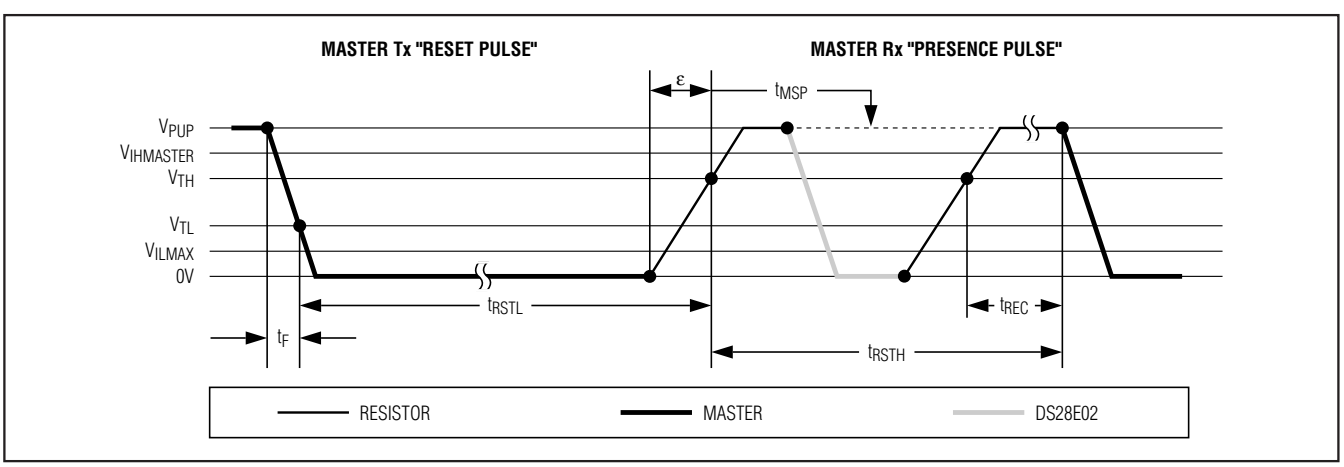


Figure 11. Initialization Procedure: Reset and Presence Pulse

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Figure 11 shows the initialization sequence required to begin any communication with the DS28E02. A reset pulse followed by a presence pulse indicates that the DS28E02 is ready to receive data, given the correct ROM and memory and SHA-1 function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the overdrive mode, returning the device to standard speed. If the DS28E02 is in overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in overdrive mode. If the device is in overdrive mode and t_{RSTL} is between 80µs and 480µs, the device resets, but the communication speed is undetermined.

After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor. When the threshold V_{TH} is crossed, the DS28E02 waits and then transmits a presence pulse by pulling the line low. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

Read/Write Time Slots

Data communication with the DS28E02 takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. Figure 12 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28E02 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28E02 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E02 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E02 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of $t_{RL} + \delta$ (rise time) on one side and the internal timing generator of the DS28E02 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}), in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E02 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E02 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance.

Improved Network Behavior (Switchpoint Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28E02 uses a new 1-Wire front-end, which makes it less sensitive to noise.

The DS28E02's 1-Wire front-end differs from traditional slave devices in two characteristics.

1) There is additional lowpass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
2) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below $V_{TH} - V_{HY}$, it is not recognized (Figure 13). The hysteresis is effective at any 1-Wire speed.

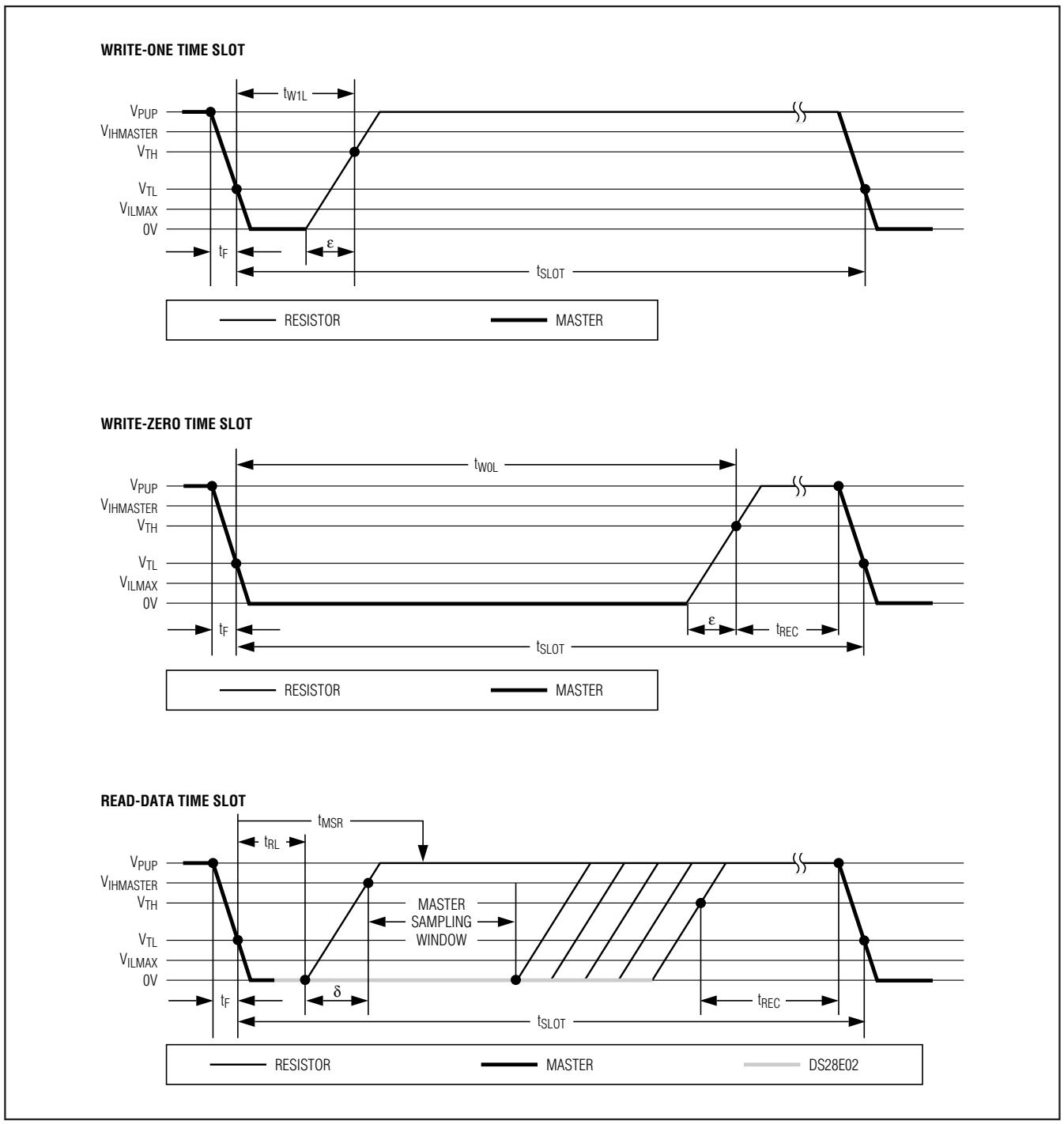

Figure 12. Read/Write Timing Diagrams

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CRC Generation

The DS28E02 uses two different types of CRCs. One CRC is an 8-bit type that is computed at the factory and is stored in the most significant byte of the 64-bit registration number. The bus master can compute a CRC value from the first 56 bits of the 64-bit registration number and compare it to the value read from the DS28E02 to determine if the registration number has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form.

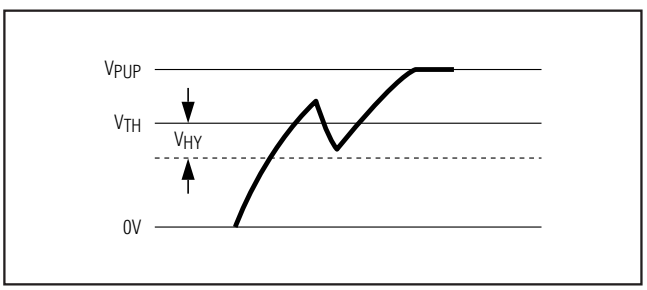

Figure 13. Noise Suppression Scheme

The other CRC is a 16-bit type, which is used for error detection with memory and SHA-1 commands. **For details, refer to the full data sheet.**

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Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 TSOC	D6+1	21-0382	90-0321
6 TDFN-EP	T633+2	21-0137	90-0058

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—
1	3/12	Revised the *Electrical Characteristics* table notes 1, 4, 15; added the land pattern numbers to the *Package Information* table	3, 33

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