AT7910E

SpW-10X SpaceWire Router

DATASHEET

Features

- SpaceWire Router
  - Logical to Physical addressing translation
  - Priority Management
  - Header Deletion Capability
- Eight Bidirectional SpaceWire links
  - Full duplex communication
  - Data rate from 2 up to 200 Mbit/s in each direction
- Two External Interfaces
  - Dedicated Input and Output FIFOs
  - 9-bit wide Interface
- Configuration Port
  - Read/Write Accesses to internal registers
  - Accessible from both the spacewire links (8 channels) and the external interfaces
  - Remote Memory Access Protocol (RMAP) support
- Time Code Interface
  - Master/Slave Capability
  - Error/Status Interface
- Operating range
  - Voltages 3V to 3.6V
  - Temperature - 55°C to +125°C
- Maximum Power consumption
  - All spacewire links active at 200Mbit/s : 4W
- Radiation Performance
  - Total dose tested successfully up to 300 Krad (Si)
  - No single event latchup below a LET of 80 MeV/mg/cm2
- ESD better than 2000V
- Quality Grades
  - QML-Q or V with SMD
- Package: 196pins MQFPF
- Mass: 12grams

Description

The SpW-10X SpaceWire routing switch is capable of connecting many nodes, providing a means of routing packets between the nodes connected to it. It comprises eight SpaceWire link interfaces and a routing matrix. The routing matrix enables packets arriving at one link interface to be transferred to and sent out of another link interface on the routing switch.

The AT7910E was designed by Austrian Aerospace (Austria) and the University of Dundee (Scotland). It is manufactured using the SEU hardened cell library from Atmel MH1RT CMOS 0.35µm radiation hardened sea of gates technology.

For any technical question relative to the functionality of the AT7910E please contact Atmel technical support at **assp-applab.hotline@nto.atmel.com**.

This document must be read in conjunction with the University of Dundee "***SpaceWire Router SpW-10X User Manual***" available at **www.atmel.com**.

Table of Contents

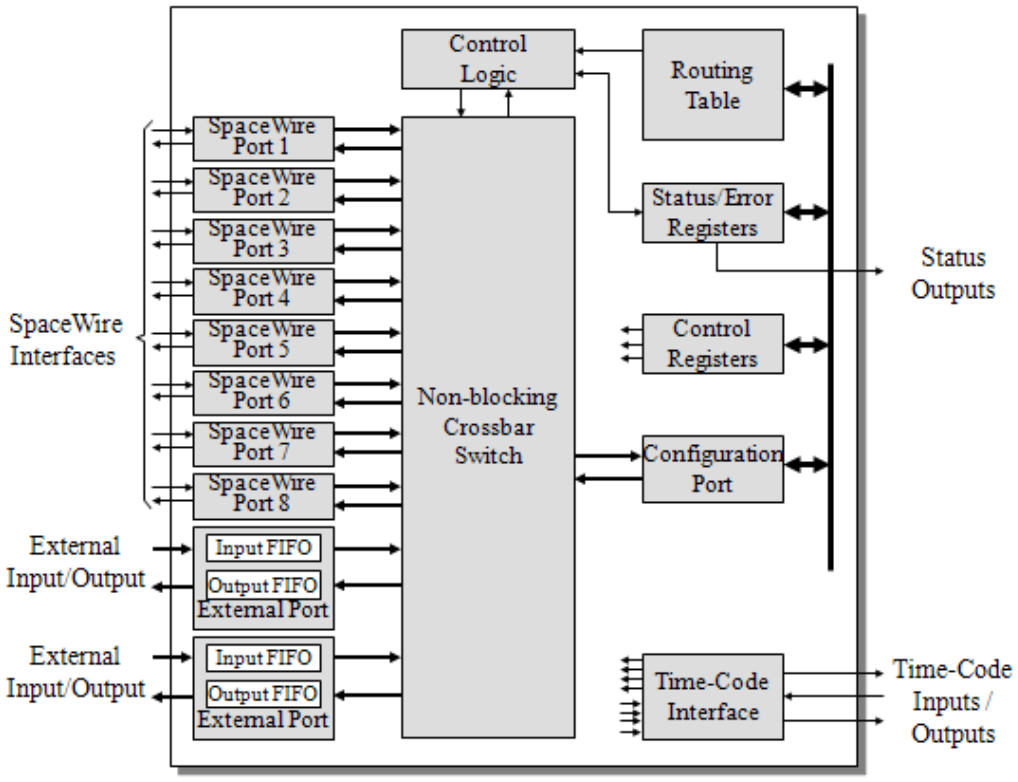
1. Functional Description

The SpaceWire router comprises the following functional logic blocks:

- Eight SpaceWire bi-directional serial ports.
- Two external parallel input/output ports each comprising an input FIFO and an output FIFO.
- A non-blocking crossbar switch connecting any input port to any output port.
- An internal configuration port accessible via the crossbar switch from the external parallel input/output port or the SpaceWire input/output ports.
- A routing table accessible via the configuration port which holds the logical address to output port mapping.
- Control logic to control the operation of the switch, performing arbitration and group adaptive routing.
- Control registers than can be written and read by the configuration port and which hold control information e.g. link operating speed.
- An external time-code interface comprising tick_in, tick_out and current tick count value
- Internal status/error registers accessible via the configuration port
- External status/error signals

A block diagram of the routing switch is given in the following figure:

Figure 1. SpaceWire Router Block Diagram



The AT7910E provides a routing capability between eight SpaceWire links according to the SpaceWire Standard ECSS-E-50-12A. In addition for use as a node interface, the AT7910E integrates other interfaces such as:

- External ports
- Configuration port
- Time-code interface
- Control/Status interface

1.1 SpaceWire Ports

The SpaceWire router has eight bi-directional SpaceWire links each compliant with the SpaceWire standard ECSS-E-50-12A.

Each SpaceWire link is controlled by an associated link register and routing control logic. Packets received on SpaceWire links are routed by the routing control logic to the configuration port, other SpaceWire link ports or the external FIFO ports depending on the packet address.

Packets with invalid addresses are discarded by the SpaceWire router. The SpaceWire link status is recorded in the associated link register and error status is held by the router until cleared by a configuration command.

1.2 External Ports

The SpaceWire router has two bi-directional parallel FIFO interfaces that can be used to connect the router to an external host system. The external port FIFO is two data characters deep.

Each FIFO is written to or read from synchronously with the 30MHz system clock.
An eight-bit data interface and an extra control bit for end of packet markers are provided by each external port FIFO. Packets received by the external port are routed by the routing control logic to the configuration port, SpaceWire link ports or the other external port depending on the packet address.

Packets with invalid addresses are discarded by the SpaceWire router.

1.3 Configuration Port

The SpaceWire router has one configuration port which performs read and write operations to internal router registers.

Packets are routed to the configuration port when a packet with a leading address byte equal to zero is received. The Remote Memory Access Protocol (RMAP) is used to access the configuration port.

If an invalid command packet is received then the error is flagged to an associated status register and the packet is discarded.

1.4 Routing table

The SpaceWire router routing table is set by the router command packets to assign logical addresses to physical destination ports on the router.

A group of destination ports can be set, in each routing table location, to enable group adaptive routing. When a packet is received with a logical address the routing table is checked by the routing control logic and the packet is routed to the destination port when the port is ready. Routing table locations are set to invalid at power on or at reset.

The routing table logical addresses can also be set to support high priority and header deletion. High priority packets are routed before low priority packets and header deletion of logical addresses can be used to support regional logical addressing.

An invalid routing address will cause the packet to be spilled by the control logic.

1.5 Routing control logic and crossbar

The routing control logic is responsible for arbitration of output ports, group adaptive routing and the crossbar switching. Arbitration is performed when two or more source ports are requesting to use the same destination port.

A priority based arbitration scheme with two priority levels, high and low, is used where high priority packets are routed before low priority packets. Fair arbitration is performed on packets which have the same priority levels to ensure each packet gets equal access to the output port.

Group adaptive routing control selects one of a number of output ports for sending out the source packet.

1.6 Time Code Processing

An internal time-code register is used in the router to allow the router to be a time-code master or a time-code slave.

In master mode the time-code interface is used to provide a tick-in to the SpaceWire routing causing time-codes to be propagated through the network. Two modes of time master operation are supported, an automatic mode where a time-code is propagated on each external tick-in and a normal mode where the time-code is propagated dependent on the external time-in signal.

In time-code slave mode a valid received time-code, one plus the value of the router time-code register, causes a tick-out to be sent to the SpaceWire links and the external time-code interface. The time-code is propagated to all time-code ports except the port on which the time-code was received. If the time-code received is not one plus the value of the time-code register then the time-code register is updated but the tick-out is not performed. In this way, circular network paths do not cause a constant stream of time-codes to be sent in a loop.

1.7 Control/Status Registers

The control and status registers in the SpaceWire router provide the means to control the operation of the router, set the router configuration and parameters or monitor the status of the device. The registers are accessed using RMAP command packets received by the configuration port.

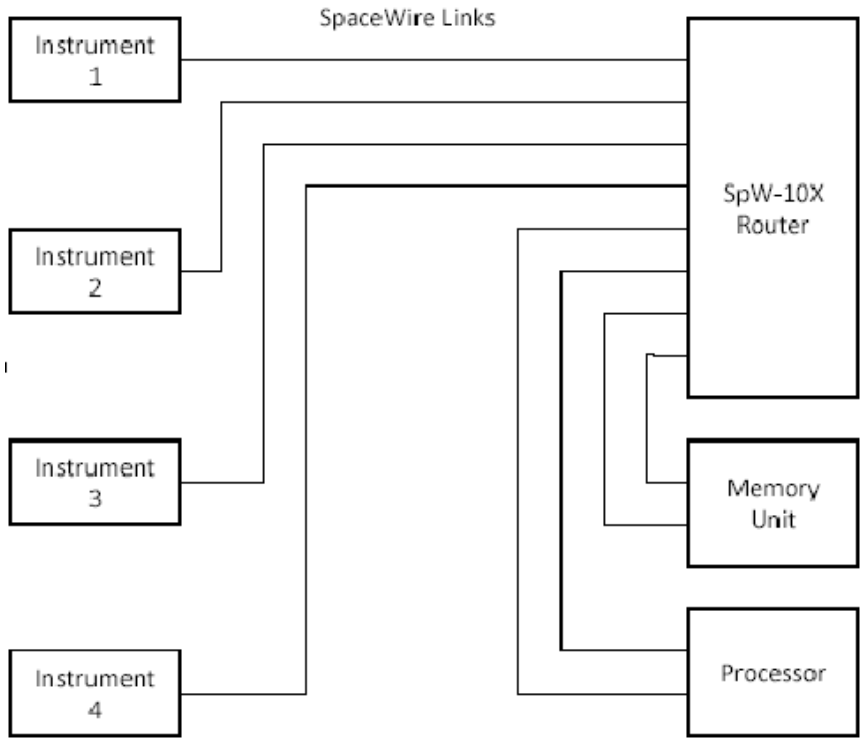
2. Typical Applications

The AT7910E SpaceWire router is perfectly suited for development of applications requiring a standalone router, a terminal node with SpaceWire interface or a mixed configuration of the two previous ones.

2.1 Stand-alone router

The AT7910E SpaceWire Router may be used as a stand-alone router with up to eight SpaceWire links connected to it. Configuration of the routing tables etc. may be done by sending SpaceWire packets containing configuration commands to the router.

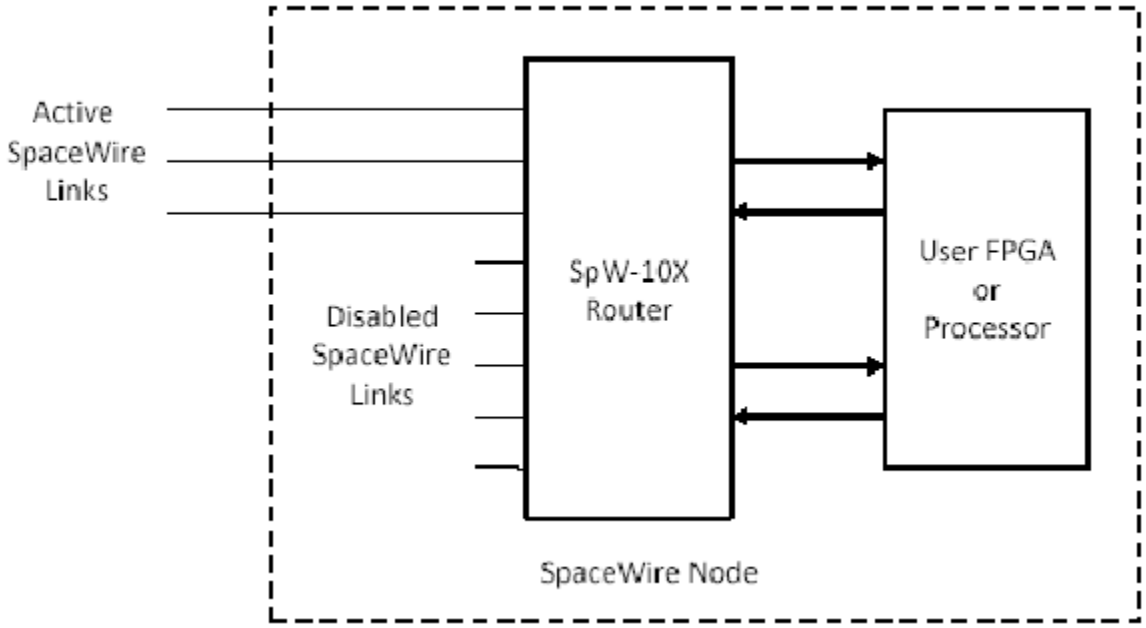
Figure 2-1. AT7910E as SpaceWire router



2.2 Node interface

The SpaceWire Router has two external ports which enable the device to be used as a node interface. The equipment to be connected to the SpaceWire network is attached to one or both external ports. One or more SpaceWire ports are used to provide the connection into the SpaceWire network. Unused SpaceWire ports may be disabled and their outputs tri-stated to save power. In this arrangement configuration of the routing tables and other parameters may be done by sending configuration packets from the local host via an external port or from a remote network manager via a SpaceWire port.

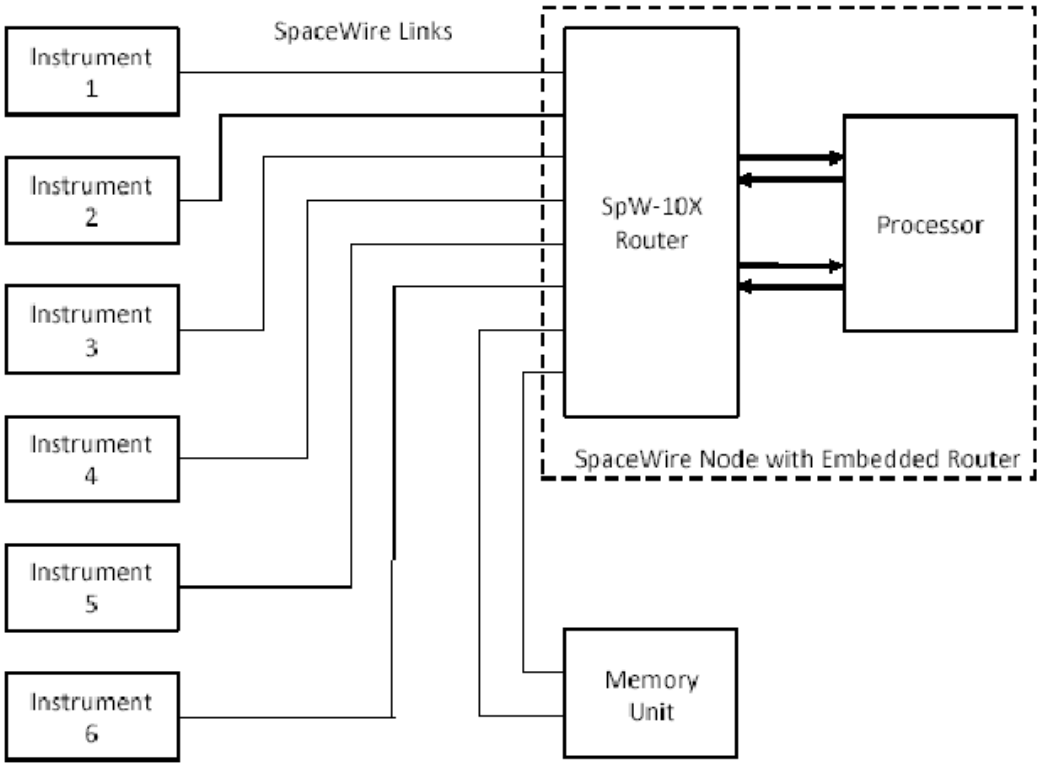
Figure 2-2. AT7910E as SpaceWire node interface



2.3 Embedded router

The SpaceWire Router device can also be used to provide a node with an embedded router. In this case the external ports are used to provide the local connections to the node and the SpaceWire ports are used to make connections to other ports in the network.

Figure 2-3. AT7910E as Embedded Router



3. PLL Filter

The AT7910E uses an internal PLL to provide the base transmit clock signal for the SpaceWire interfaces. External components are required to implement the PLL loop filter and to provide a bias for the PLL VCO.

Note that RVCO, C and C0 are all connected to a quiet common ground track.

Dedicated decoupling capacitors are also required for the PLL power supply.

Figure 3-1. PLL filter and decoupling capacitors

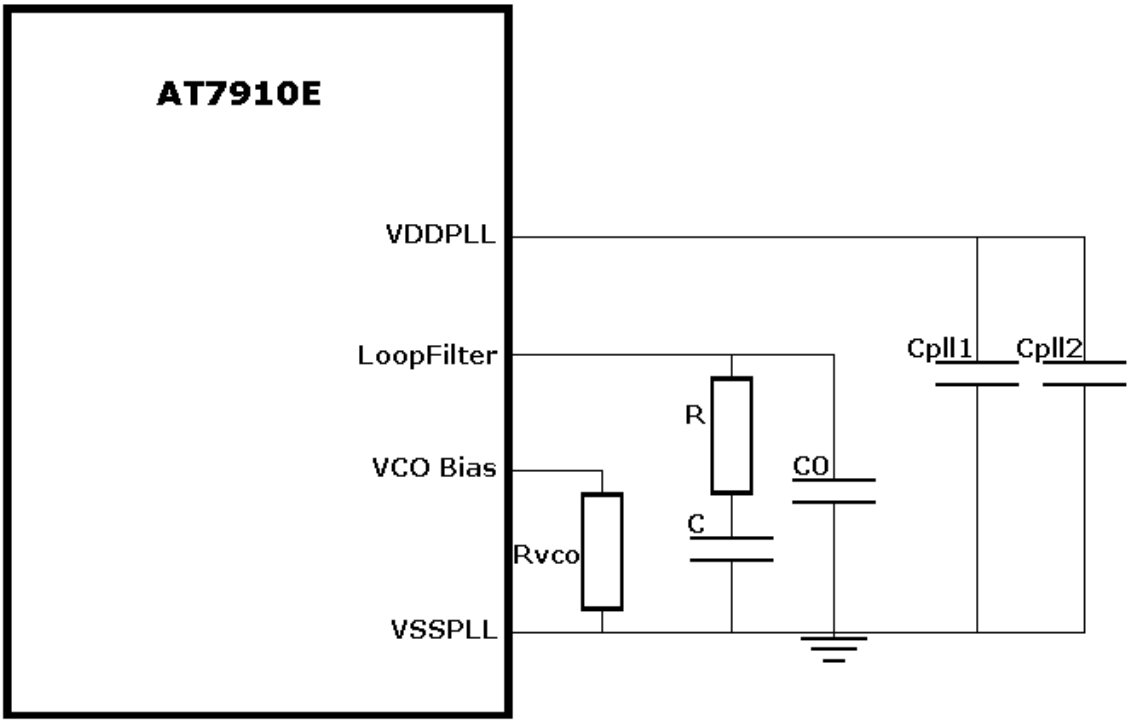


Table 3-1. PLL filter recommended components

Component	Value
R	10kW ± 5%, ¼W
C	120pF, ± 5%
C0	3.3pF, ± 5%
RVCO	4.7kW for 100-150MHz operation
	1.8kW for 150-200MHz operation

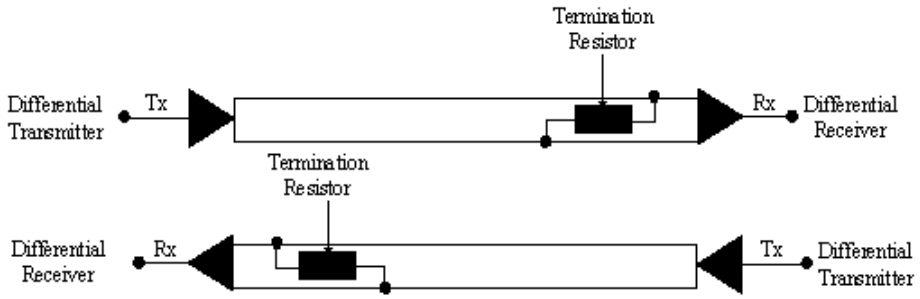
Table 3-2. PLL decoupling capacitors

Component	Value
Cpll1	100nF, ± 5%
Cpll2	10µF, ± 5%

4. LVDS Interface

The AT7910E provides 8 SpaceWire link based on LVDS IOs that should comply with the **EIA-644 standard requirements**.
The basic LVDS interface consists in a single differential link interconnected between a transmiter and a receiver.
Such a link requires a termination resistor on the receiver side to allow high frequency transfer usage. The nominal resistor value for the termination resistor 100 ohms. LVDS bidirectional communication principle

Figure 4-1. LVDS interface principle



Caution: The AT7910E doesn't embed the termination resistors on the receivers.

4.1 AT7910E Limitation

Due to MH1RT technology limitation, the electrical parameters of the **EIA-644 standard** can not all be met on the transmitters of the AT7910E

Figure 4-2. Output electrical characteristics

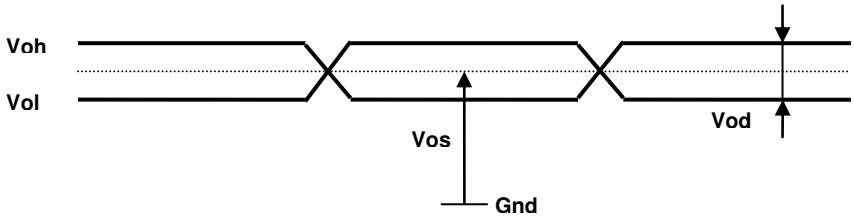


Table 4-1. AT7910E LVDS TX feature

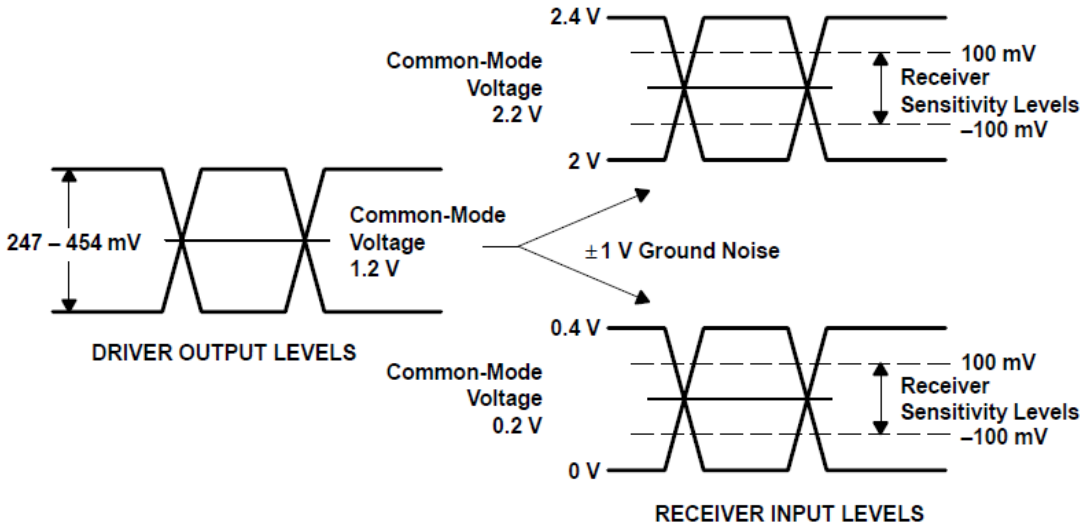
Parameter	TIA/EIA Standard	AT7910E	Unit
VOS min	1125	**800**	mV
VOS max	1375	**1568**	mV
VOD Min	247	**247**	mV
VOD Max	454	**550**	mV
DeltaVOD	50	**50**	mV
DeltaVOS (dynamic)	150	**200**	mV

4.2 AT7910E Compatibility with LVDS receiver Standards

The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247mV to 550mV with a typical offset voltage of 1.2V relative to ground.

The recommended voltage applied to the LVDS receiver is between ground and 2.4 V with a common mode range of 0.05V to 2.35V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state. The LVDS interconnecting media must be matched with the 100ohm termination resistor located at the inputs of the receiver.

Figure 4-3. Transmitter to Receiver electrical characteristics



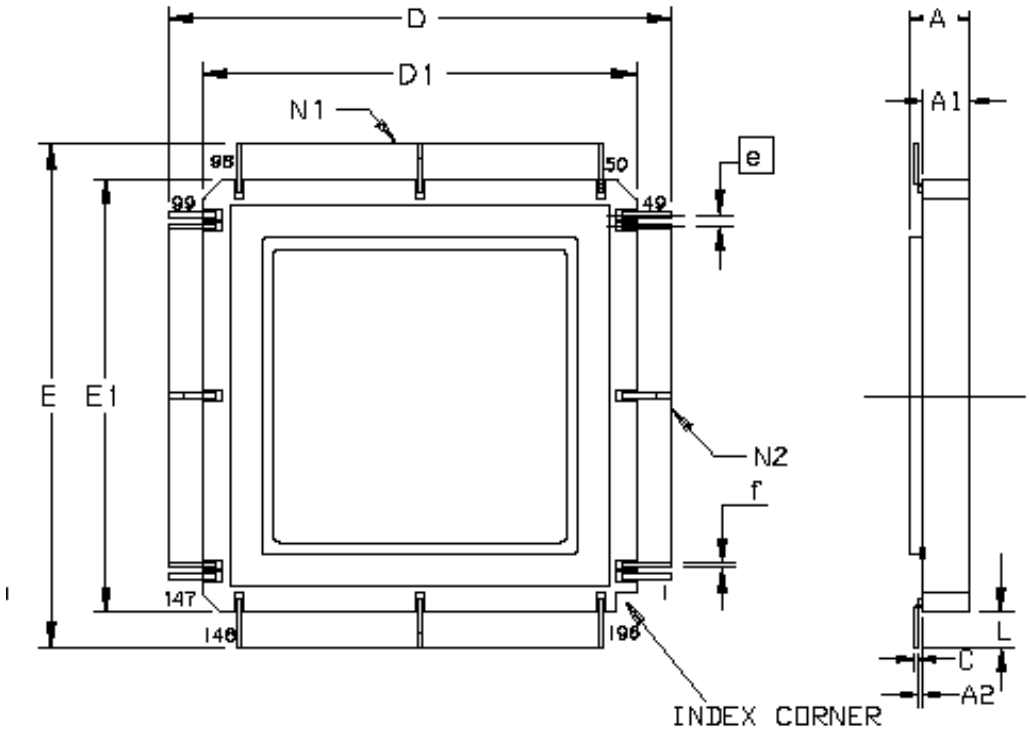
5. Package Information

5.1 Package Outline

5.1.1 MQFPF 196

Here is a presentation of the mechanical outline of the 196 pins Ceramic Quad Flat Pack (CQFP 196) package used for the AT7910E.

Figure 5-1. MQFPF 196 package



	Min	Max	Min	Max
A	2.13	2.65	.084	.104
A1	1.83	2.24	.072	.088
A2	0.203 REF		.008 REF	
C	0.102	0.203	.004	.008
D/E	46.73	47.94	1.840	1.887
D1/E1	34.03	34.54	1.340	1.360
e	0.635 BSC		.025 BSC	
f	0.20 REF		.008 REF	
L	6.35	6.70	.250	.264
N1	49		49	
N2	49		49	

Lid connected to ground

Table 5-1. Pin Assignment

Pin Assignment									
Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
1	VDDB	41	VSSB	81	SIN-7	121	EXTINDATA9_6	161	EXTTIMEIN2
2	CLK	42	VSSA	82	SOUT-7	122	EXTINDATA9_7	162	EXTTIMEIN3
3	RST	43	VDDA	83	SOUT+7	123	EXTINDATA9_8	163	EXTTIMEIN4
4	TESTIOE	44	VDDB	84	VSSB	124	EXTINFULL9	164	EXTTIMEIN5
5	TESTE	45	DOUT-3	85	VDDB	125	VSSB	165	EXTTIMEIN6
6	FEEDBDIV0	46	DOUT+3	86	DOUT-7	126	VDDB	166	EXTTIMEIN7
7	VSSA	47	DIN+4	87	DOUT+7	127	EXTINWRITE9	167	SELEXTTIME
8	VDDA	48	DIN-4	88	DIN+8	128	EXTOUTDATA10_0	168	TIMECTRRST
9	FEEDBDIV1	49	LVDS_REF	89	DIN-8	129	EXTOUTDATA10_1	169	EXTTICKOUT
10	FEEDBDIV2	50	SIN+4	90	SIN+8	130	EXTOUTDATA10_2	170	EXTTIMEOUT0
11	VSSB	51	SIN-4	91	VSSA	131	EXTOUTDATA10_3	171	EXTTIMEOUT1
12	VDDPLL	52	SOUT-4	92	VDDA	132	EXTOUTDATA10_4	172	EXTTIMEOUT2
13	VCOBias	53	SOUT+4	93	SIN-8	133	EXTOUTDATA10_5	173	EXTTIMEOUT3
14	LOOPFILTER	54	DOUT-4	94	SOUT-8	134	VSSB	174	VSSB
15	VSSPLL	55	DOUT+4	95	SOUT+8	135	VDDB	175	VDDB
16	VDDB	56	VSSA	96	DOUT-8	136	EXTOUTDATA10_6	176	EXTTIMEOUT4
17	DIN+1	57	VDDA	97	DOUT+8	137	EXTOUTDATA10_7	177	EXTTIMEOUT5
18	DIN-1	58	VSSB	98	VSSB	138	EXTOUTDATA10_8	178	EXTTIMEOUT6
19	SIN+1	59	VDDB	99	VDDB	139	EXTOUTEMPTY10	179	EXTTIMEOUT7
20	SIN-1	60	DIN+5	100	EXTOUTDATA9_0	140	VSSA	180	STATMUXADDR0
21	SOUT-1	61	DIN-5	101	EXTOUTDATA9_1	141	VDDA	181	STATMUXADDR1
22	SOUT+1	62	SIN+5	102	EXTOUTDATA9_2	142	EXTOUTREAD10	182	STATMUXADDR2
23	DOUT-1	63	SIN-5	103	EXTOUTDATA9_3	143	EXTINDATA10_0	183	STATMUXADDR3
24	DOUT+1	64	SOUT-5	104	EXTOUTDATA9_4	144	EXTINDATA10_1	184	VSSB
25	DIN+2	65	SOUT+5	105	VSSA	145	EXTINDATA10_2	185	VDDB
26	DIN-2	66	DOUT-5	106	VDDA	146	EXTINDATA10_3	186	STATMUXOUT0
27	SIN+2	67	DOUT+5	107	EXTOUTDATA9_5	147	EXTINDATA10_4	187	STATMUXOUT1
28	SIN-2	68	DIN+6	108	VSSB	148	EXTINDATA10_5	188	STATMUXOUT2
29	VSSB	69	DIN-6	109	VDDB	149	EXTINDATA10_6	189	VSSA
30	VDDB	70	SIN+6	110	EXTOUTDATA9_6	150	EXTINDATA10_7	190	VDDA
31	SOUT-2	71	SIN-6	111	EXTOUTDATA9_7	151	EXTINDATA10_8	191	STATMUXOUT3
32	SOUT+2	72	VSSB	112	EXTOUTDATA9_8	152	EXTINFULL10	192	STATMUXOUT4
33	DOUT-2	73	VDDB	113	EXTOUTEMPTY9	153	EXTINWRITE10	193	STATMUXOUT5
34	DOUT+2	74	SOUT-6	114	EXTOUTREAD9	154	VSSA	194	STATMUXOUT6
35	DIN+3	75	SOUT+6	115	EXTINDATA9_0	155	VDDA	195	STATMUXOUT7
36	DIN-3	76	DOUT-6	116	EXTINDATA9_1	156	VSSB	196	VSSB
37	SIN+3	77	DOUT+6	117	EXTINDATA9_2	157	VDDB		
38	SIN-3	78	DIN+7	118	EXTINDATA9_3	158	EXTTICKIN		
39	SOUT-3	79	DIN-7	119	EXTINDATA9_4	159	EXTTIMEIN0		
40	SOUT+3	80	SIN+7	120	EXTINDATA9_5	160	EXTTIMEIN1		

5.2 Pin Description

Table 5-2. Pin Description

Signal Name(1)(3)	Type(2)	Function	Buffer type
VDDA VDDB VDDPLL		3.3V Power for the device	POWER
VSSA VSSB VSSPLL		Ground for the device	POWER
LVDSRef		LVDS Power reference for the device	POWER
VCOBias		Bias for the PLL VCO (Rvco)	
LoopFilter		Internal PLL filter	
CLK	I	System Clock - Provides the reference clock for all the AT7910E modules except the SpaceWire interface receivers	CMOS3V3
RST*	I	Asynchronous active low system reset	CMOS3V3
FEEDBDIV[2:0]	I	PLL feedback divider configuration - Set the internal PLL output clock rate	CMOS3V3
DOUT+[1:8] DOUT-[1:8]	O	Differential output pair - Data part of Data-Strobe SpaceWire link 1 to 8.	LVDS+ LVDS-
SOUT+[1:8] SOUT-[1:8]	O	Differential output pair - Strobe part of Data-Strobe SpaceWire link 1 to 8.	LVDS+ LVDS-
DIN+[1:8] DIN-[1:8]	I	Differential input pair - Data part of Data-Strobe SpaceWire link 1 to 8.	LVDS+ LVDS-
SIN+[1:8] SIN-[1:8]	I	Differential input pair - Strobe part of Data-Strobe SpaceWire link 1 to 8.	LVDS+ LVDS-
EXTOUTDATA9[8:0]	O	Output data from external port zero FIFO. Bit eight determines the data type data, EOP or EEP	CMOS3V3
EXTINDATA9[8:0]	I	Input data from external port zero FIFO. Bit eight determines the data type data, EOP or EEP	CMOS3V3
EXTOUTEMPTY9*	O	FIFO ready signal for external output port zero. When high the FIFO has data. When low the FIFO is empty	CMOS3V3
EXTOUTREAD9*	I	Asserted Low to read from the external output port zero FIFO.	CMOS3V3
EXTINFULL9*	O	FIFO ready signal for external input port zero. When high there is space in the FIFO so it can be written to. When low the FIFO is full.	CMOS3V3
EXTINWRITE9*	I	Asserted Low to write to the external input port zero FIFO.	CMOS3V3
EXTOUTDATA10[8:0]	O	Output data from external port one FIFO. Bit eight determines the data type data, EOP or EEP	CMOS3V3
EXTINDATA10[8:0]	I	Input data from external port one FIFO. Bit eight determines the data type data, EOP or EEP	CMOS3V3
EXTOUTEMPTY10*	O	FIFO ready signal for external output port one. When high the FIFO has data. When low the FIFO is empty	CMOS3V3

Signal Name(1)(3)	Type(2)	Function	Buffer type
EXTOUTREAD10*	I	Asserted Low to read from the external output port one FIFO.	CMOS3V3
EXTINFULL10*	O	FIFO ready signal for external input port one. When high there is space in the FIFO so it can be written to. When low the FIFO is full.	CMOS3V3
EXTINWRITE10*	I	Asserted Low to write to the external input port one FIFO.	CMOS3V3
EXTTICKIN	I	The rising edge of the EXT_TICK_IN signal is used to indicate when a time- code is to be sent	CMOS3V3
EXTTIMEIN[7:0]	I	EXT_TIME_IN(7:0) provides the value of the time-code to be distributed by the router	CMOS3V3
SELEXTTIME	I	If SEL_EXT_TIME is high on the rising edge of EXT_TICK_IN the value on EXT_TIME_IN(7:0) is loaded into the internal time-code register and propagated by the router.	CMOS3V3
TIMECTRRST	I	This signal causes the internal time-code counter to be reset to zero.	CMOS3V3
EXTTICKOUT	O	The falling edge of EXT_TICK_OUT is used to indicated the reception of a time-code.	CMOS3V3
EXTTIMEOUT[7:0]	O	Received time-code value which is valid when EXT_TICK_OUT is asserted.	CMOS3V3
STATMUXADDR[3:0]	I	Select the error indication status signals to be output on STAT_MUX_OUT	CMOS3V3
STATMUXOUT[7:0]	I/O	After reset the STAT_MUX_OUT pins are inputs which define the power on configuration status of the router. After the power on reset configuration of the router has been read from STAT_MUX_OUT the pins are driven as outputs by the router.	CMOS3V3
TESTEN	I	Shall be tied to ground	CMOS3V3
TESTIOEN	I	Shall be tied to ground	CMOS3V3

Notes:

1. Groups of pins represent busses where the highest number is the MSB.
2. O = Output; I = Input; I/O = Input/Output
3. XXX* = active low signal

5.3 Electrical Characteristics

5.4 Absolute Maximum Ratings

Table: Absolute rating ltside

Supply Voltage (VCC)……..... -0.5V to +4V

I/O Voltage…….…..-0.5V to VCC+0.5V

Storage Temperature (Tstg).....-65°C to +150°C

Junction Temperature (Tj)…….……...175°C

Junction to Case Thermal resistance (RThjc) .....5°C /W

*Notice: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

5.5 DC Electrical Characteristics

Table 5-3. 3.3V operating range DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature		-55	125	□C	
Operating Voltage	VCC	3.0	3.6	V	
Input HIGH Voltage	VIH	2.0		V	
Input LOW Voltage	VIL		0.8	V	
Output HIGH Voltage	VOH	2.4		V	IOL = 3, 6, 12mA / VCC = VCC(min)
Output LOW Voltage	VOL		0.4	V	IOH = 3, 6, 12mA / VCC = VCC(min)
Output Short circuit current	IOS		23 13	mA mA	VOUT = VCC VOUT = GND

5.6 Power consumption

Maximum power consumption figures at Vcc = 3.6V are presented in the following table.

Table 5-4. 3.3V Power Consumption

Operation Mode	Power consumption [W]
ICCSB(1) - Standby	1.8
ICCOP(2) - SpaceWire links On	2.6

Notes:

1. Dynamic power with all interfaces active including external ports.
2. Clock Frequency @ 3.12MHz, all SpW links active @3.12Mbps, no data transfert.

5.7 AC Electrical Characteristics

The following table gives the worst case timings measured by Atmel on the 3.0V to 3.6V operating range

Table 5-5. 3.3V operating range timings[1]

Parameter	Symbol	Min.	Max.	Unit
Propagation delay CLK Low to DOUT0 High	Tp0		16	ns
Propagation delay CLK Low to DOUT1 High	Tp1		16	ns
Propagation delay CLK Low to DOUT2 High	Tp2		16	ns
Propagation delay CLK Low to DOUT3 High	Tp3		16	ns
Propagation delay CLK Low to DOUT4 High	Tp4		16	ns
Propagation delay CLK Low to DOUT5 High	Tp5		16	ns
Propagation delay CLK Low to DOUT6 High	Tp6		16	ns
Propagation delay CLK Low to DOUT7 High	Tp7		16	ns
Propagation delay CLK Low to DOUT0 Low	Tp8		16	ns
Propagation delay CLK Low to DOUT1 Low	Tp9		16	ns
Propagation delay CLK Low to DOUT2 Low	Tp10		16	ns
Propagation delay CLK Low to DOUT3 Low	Tp11		16	ns
Propagation delay CLK Low to DOUT4 Low	Tp12		16	ns
Propagation delay CLK Low to DOUT5 Low	Tp13		16	ns
Propagation delay CLK Low to DOUT6 Low	Tp14		16	ns
Propagation delay CLK Low to DOUT7 Low	Tp15		16	ns
Propagation delay CLK Low to SOUT0 High	Tp16		16	ns
Propagation delay CLK Low to SOUT1 High	Tp17		16	ns
Propagation delay CLK Low to SOUT2 High	Tp18		16	ns
Propagation delay CLK Low to SOUT3 High	Tp19		16	ns
Propagation delay CLK Low to SOUT4 High	Tp20		16	ns
Propagation delay CLK Low to SOUT5 High	Tp21		16	ns
Propagation delay CLK Low to SOUT6 High	Tp22		16	ns
Propagation delay CLK Low to SOUT7 High	Tp23		16	ns
Propagation delay CLK Low to SOUT0 Low	Tp24		16	ns
Propagation delay CLK Low to SOUT1 Low	Tp25		16	ns
Propagation delay CLK Low to SOUT2 Low	Tp26		16	ns
Propagation delay CLK Low to SOUT3 Low	Tp27		16	ns
Propagation delay CLK Low to SOUT4 Low	Tp28		16	ns
Propagation delay CLK Low to SOUT5 Low	Tp29		16	ns
Propagation delay CLK Low to SOUT6 Low	Tp30		16	ns
Propagation delay CLK Low to SOUT7 Low	Tp31		16	ns

Note:

1. The timing parameters presented in the above table are measured under production configuration (PLL bypassed and test mode enabled). During normal operation (PLL active and test mode disabled) the propagation delay is directly linked to the PLL . Then, the timing figures are not applicable under application conditions.

For guaranteed timings refer to the “**Switching Characteristics**” section of the ‘**SpW-10X SpaceWire Router User Manual**’.

6. Ordering Information

6.1 AT7910E Ordering Codes

Atmel Ordering Code	Package Type	Temperature Range	Quality Level
AT7910EKB-E	MQFPF196	25°C	Engineering sample
5962-09A0301QXC	MQFPF196	-55°C to +125°C	QML_Q
5962-09A0301VXC	MQFPF196	-55°C to +125°C	QML_V
5962R09A0301VXC	MQFPF196	-55°C to +125°C	QMLV-RHA

(*) according to Atmel Quality flow document 4288, see Atmel web site

7. Revision History

Doc. Rev.	Date	Comments
B	02-2009	Corrected pinout error: pin 190 is VDDA and not VSSB. See Table 1 on page 6.
C	06-2009	Corrected ICCop Value.See Table 7-3 on page 14
D	07-2009	Removing untested ICCop Value.See Table 7-3 on page 14
E	07-2009	SMD Part numbers added.
F	08-2009	Remove Atmel Part numbers.
G	02-2013	Template update Addition of VOS min/max Addition of VOD min/max

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