SY02-PLL2

Date: December 12, 2003

• INTRODUCTION

The SY02-PLL2 is a crystal-based PLL synchronizer designed as a module level subsystem for easy incorporation into telecommunication equipment.

• FEATURES

- Low jitter output from intrinsically low jitter VCXO;
- Two references inputs, user selects the frequencies;
- Alarms and status;
- Buffered reference output;
- Tri-state (high impedance) reference and oscillators outputs;
- Provides free running clock output of ±20ppm;
- The unit changes timing modes in response to external events;
- J-TAG service port for re-programming and servicing;

• APPLICATIONS

- Line Cards
- ATM
- SDH
- PDH
- SONET
- Other telecommunication equipment.

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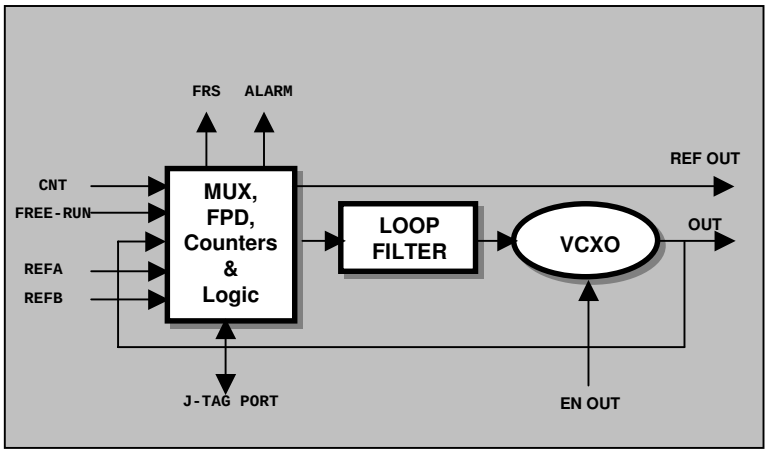


- **DESCRIPTION**

The SY02-PLL2 is a Phase Lock Loop has been designed as a module level subsystem for easy incorporation into telecommunication equipment. The module generates the output from a low jitter VCXO and provides recovered signal as secondary output. The SY02-PLL2 has two reference inputs with frequencies that can be selected by user from 8 to 77.76MHz. The input reference selection pin (CNT) selects which reference will be used. The loop bandwidth is optimized according to used VCXO and wanted output performance. The ALARM output signal monitors the status of the phase loop in case of Loss of Lock (LOL) and Loss of Reference (LOR) both internal signals. The two control inputs provides module to go into free-run regardless of the reference (FREE_RUN) and to the tri-state high impedance output (OUT EN). The SMD package dimensions are 19.4 x 20.3 mm and power supply is 3.3V.

- INPUT REFERENCE SELECTION

CNT	Reference selected
0	REF A
1	REF B

- OUTPUT PROGRAMMING

EN OUT	FREE-RUN	FRS output	OUTPUT
0	0	0	Locked to Reference
1	X	0	Hi-Z Tri-State
0	1	1	Free-Run

- ALARM STATES

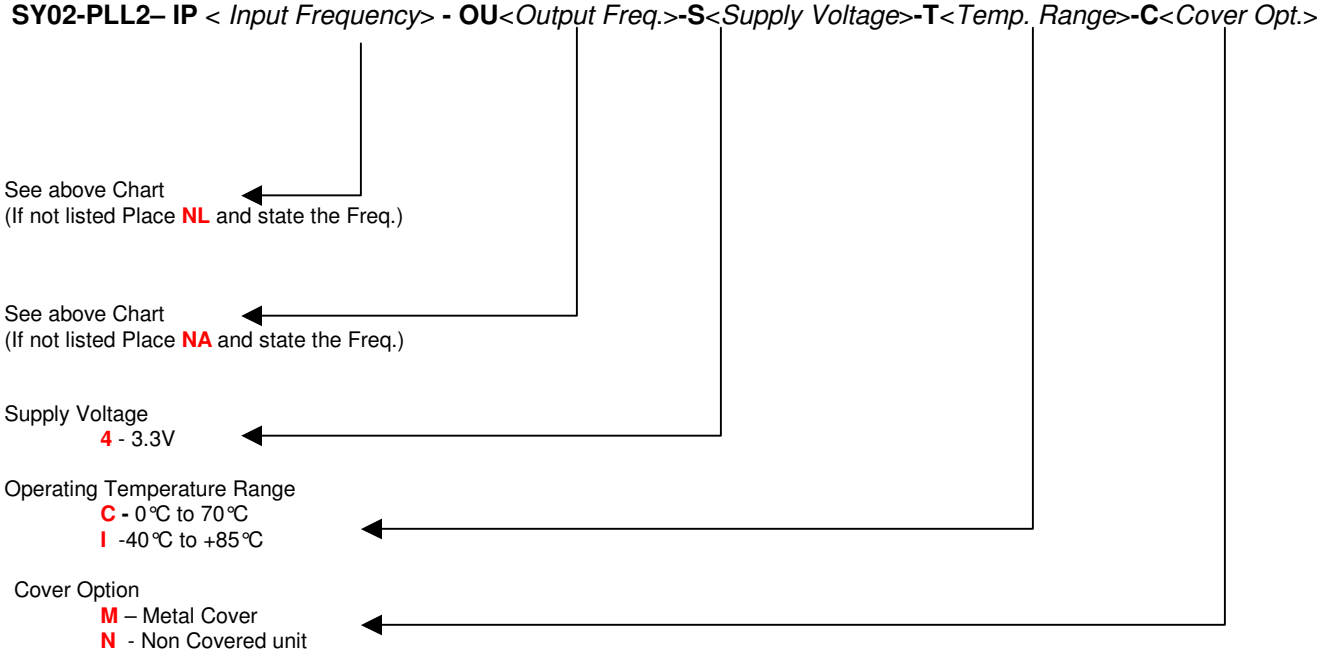
LOL	LOR	ALARM
0	0	0 -No alarm
1	0	1- Loss of Lock
0	1	1-Loss of Reference

- **PIN DESCRIPTION**

Pin #	Name	Description
1	REF OUT	Reference Output -> The recovered signal from reference.
2	TCK	J-TAG port for factory usage – TCK
3	TMS	J-TAG port for factory usage – TMS
4	GND	Ground
5	FREE-RUN	Free-Run -> Control input to force unit to run as free running oscillator
6	ALARM	Alarm output -> Output signal presents if LOL or LOR
7	REF B IN	Reference B Input -> Reference input signal
8	REF A IN	Reference A Input -> Reference input signal
9	OUT	Oscillator Output -> Output of the module
10	FRS	Free Run Status Output -> Status of free run mode.
11	Vcc	Positive supply voltage
12	TDO	J-TAG port for factory usage – TDO
13	OUT EN	Output Enable -> Control input to enable/disable the module output
14	CNT	Control Input -> Select one of the reference input

- **ORDERING INFORMATION**

SY02-PLL2– IP < *Input Frequency*> **- OU**<*Output Freq.*>**-S**<*Supply Voltage*>**-T**<*Temp. Range*>**-C**<*Cover Opt.*>



- INPUT/OUTPUT FREQUENCIES AVAILABLE:

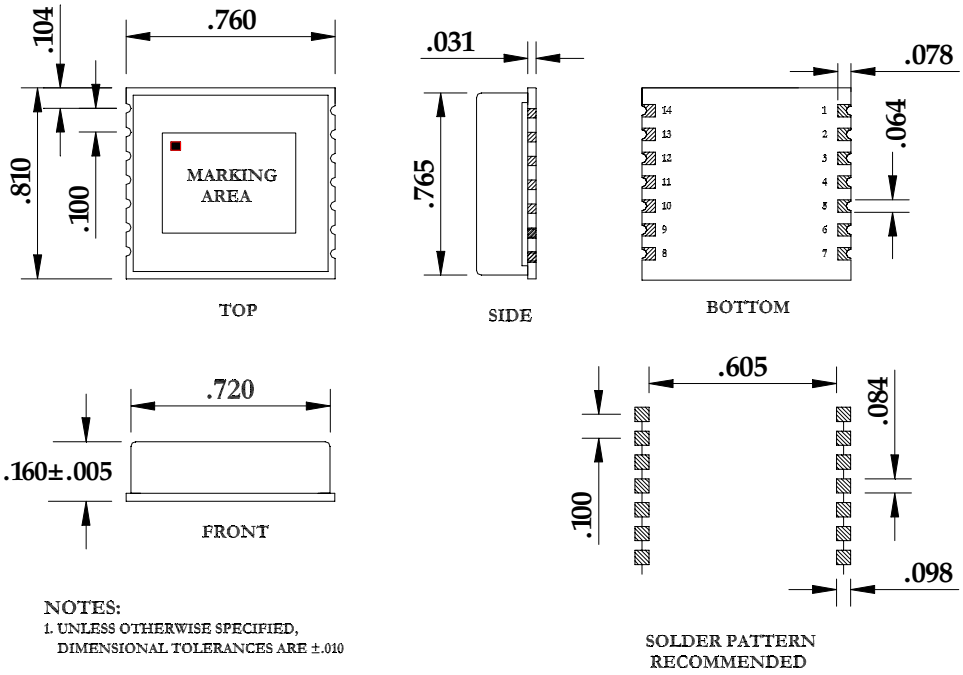
Frequency	Suffix	Frequency	Suffix
8KHz	F8	20.000MHz	M1
1.024MHz	E0	20.4800MHz	A4
1.544MHz	T1	26.0000MHz	G2
2.048MHz	E1	27.0000MHz	A6
4.096MHz	E2	32.768MHz	E4
6.1760MHz	T2	34.560MHz	A8
6.480MHz	D1	37.0560MHz	A9
8.192MHz	E3	38.880MHz	O2
10.000MHz	A1	44.7360MHz	T3
12.800MHz	S1	51.8400MHz	D1
13.000MHz	G1	61.4400MHz	U1
15.000MHz	A2	62.5000MHz	G1
16.384MHz	E4	65.5360MHz	B2
19.440MHz	O1	77.7600MHz	O3

- *For other frequencies contact the factory!*
- *Add to P/N "EXT" for extended operating temperature (*-40° to 85℃)

- **SPECIFICATION**

General Specifications	Mechanical	19.4 x 20.3 mm	SMT Module FR4 14pins dual-in-line
	Power Environment Internal Oscillators	3.3VDC, <100mA Operating Temperature Storage Temperature Humidity Voltage Controlled Crystal Oscillator (VCXO) and Crystal Oscillator (XO)	Regulated 0℃ to 70℃ (Extended Temp. available -40° to 85℃) -40° to 85℃ 5% to 95% non-condensing
Input Signals	Number of Reference Inputs	2	
	Input reference frequency Signal Level	See the table LVCMOS/LVTTL Compatible	Select by external pins
Output Signals	Number of Outputs	2	
	Output 1	See the table	User defined
	Output 1 Signal Level	LVCMOS	
	Output 2	Recovered REF IN	
	Output 2 Signal Level	LVCMOS	
	Tracking/Capture Range	±25ppm min	
Signal Quality Performance	Jitter generation	<0.001UI RMS	
	Jitter tolerance	2 μs, 10 Hz (0.05 UI @ 8KHz)	
Frequency Output Performance	Free run accuracy	±20ppm max. 0℃ to 70℃	No reference signal

- **OUTLINE DRAWING**



NOTES:
1. UNLESS OTHERWISE SPECIFIED, DIMENSIONAL TOLERANCES ARE ±.010