

# **F81485**

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## **5V Low Power RS-485 Interface Transceiver**

**Release Date: March, 2013**

**Version: V0.14P**

## F81485 Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2011/12	-	Preliminary
V0.11P	2012/01	-	Made Clarification and Correction Update Top Marking Specification Update Differential Input Threshold Spec.
V0.12P	2012/02	-	Made Clarification and Correction. Update Operating Temperature
V0.13P	2012/03	-	Made Clarification and Correction. Update Electrical Characteristics (Add Symbol, Testing Figures, spec...)
V0.14P	2013/03	-	Made Clarification and Correction. Update ESD spec. to $\pm 15\text{KV}$ Contact

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### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Fintek for any damages resulting from such improper use or sales.

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## 1 General Description

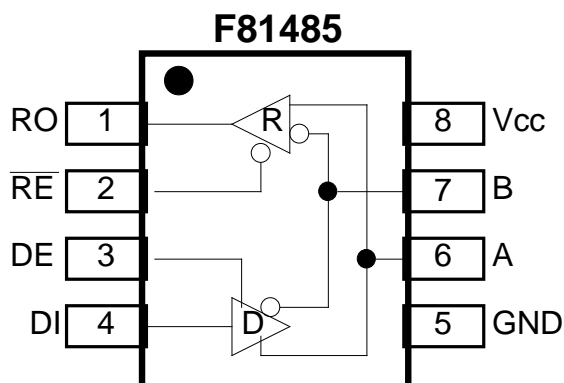
The F81485 is a CMOS design, features with single 5 V power supply, and low power differential bus/line transceiver suitable for the multipoint data transmission EIA standard RS485 and RS422 applications. The extended common-mode range is  $-7\text{ V}$  to  $+12\text{ V}$ . Both the driver and the receiver can be enabled independently. The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by the bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state. The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating). Up to 32 transceivers can be connected simultaneously on a bus, but only one driver should be enabled at any time. The F81485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at data rates up to 10 Mbps while low skew minimizes EMI interference. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

## 2 Feature List

- Single 5V Supply
- Meets EIA RS-485 Standard
- High Speed, Low Power CMOS
- $-7\text{V}$  to  $12\text{V}$  Bus Common-Mode Range Permits
- $\pm 7\text{V}$  Ground Difference Between Devices on the Bus
- ESD IEC 61000-4-2  $\pm 15\text{KV}$  [Contact](#) Discharge Testing
- 70mV Typical Input Hysteresis
- Driver propagation delay: 40 ns typical
- Receiver propagation delay: 70 ns typical
- High-Z outputs with power off
- 8 Pin SOP Packaging

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## 3 Pin Configuration



## 4 Pin Description

IN <sub>t</sub>	- TTL level input pin.
O <sub>4</sub>	- Output pin with 4mA driver.
P	- Power.

### 4.1. Power Pin

Pin	Pin Name	Type	Description
5	GND	P	GND.
8	VCC	P	4.75V < VCC < 5.25V power supply voltage input.

### 4.2. Transceiver

Pin	Pin Name	Type	Description
1	RO	O <sub>4</sub>	Receiver Output. When enabled (RE# is low), then if A > B by 200 mV, RO is high. A < B by 200 mV, RO is low.
2	RE#	IN <sub>t</sub>	Active Low Receiver Output Enable pin. A low level enables the receiver output, RO. A high level places it in a high impedance state.
3	DE	IN <sub>t</sub>	Active High Driver Output Enable. A high level enables the driver differential outputs, A and B. The chip will function as a line driver. A low level places it in a high impedance state.
4	DI	IN <sub>t</sub>	Driver Input. When the driver is enabled (DE is high), a logic low on DI forces A low and B high, while a logic high on DI forces A high and B low.
6	A	I/O	Non-inverting Receiver Input A/Driver Output A.
7	B	I/O	Inverting Receiver Input B/Driver Output B.

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## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

PARAMETER		RATING	UNIT
V <sub>CC</sub>		6	V
Input Voltage	Logic	-0.3 to V <sub>CC</sub> +0.5	V
	Drivers	-0.3 to V <sub>CC</sub> +0.5	V
	Receivers	±15	
Output Voltage	Logic	-0.3 to V <sub>CC</sub> +0.5	V
	Drivers	±15	V
	Receivers	-0.3 to V <sub>CC</sub> +0.5	
Storage Temperature		-65 to +150	°C
Lead Temperature (soldering, 10s)		+300	°C
Power Dissipation		500	mW

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

Test condition: V<sub>CC</sub> = 5V

PARAMETER	SYMBOL	MIN.	TYP.	MAX	UNIT	CONDITIONS
Supply Voltage	V <sub>CC</sub>	4.75		5.25	V	
Supply Current	I <sub>CC</sub>		900		μA	No Load
Operating Temperature (1)	T	-40		85	°C	

Note (1): Design Guarantee -40 °C ≤ T ≤ 85 °C

### 5.2 Driver Section

Test condition: V<sub>CC</sub> = 5V

PARAMETER	SYMBOL	MIN.	TYP.	MAX	UNIT	CONDITIONS
<b>DC Characteristics</b>						
Differential Output Voltage (See Figure 1)	V <sub>OD</sub>	GND		V <sub>CC</sub>	V	Unloaded, R = ∞
		2		V <sub>CC</sub>	V	With load, R = 50Ω (RS422)
		1.5		V <sub>CC</sub>	V	With load, R = 27Ω (RS485)
Differential Output Voltage for Complimentary States (See Figure 1)	Δ V <sub>OD</sub>			0.2	V	R = 27Ω or R = 50Ω
Driver Common-Mode Output Voltage (See Figure 1)	V <sub>OC</sub>			3	V	R = 27Ω or R = 50Ω
Input High Voltage	V <sub>INH</sub>	2.0			V	Applies to DE, DI, RE#
Input Low Voltage	V <sub>INL</sub>			0.8	V	Applies to DE, DI, RE#
Input Current	I <sub>IN</sub>			±10	μA	Applies to DE, DI, RE#
Driver Short Current	I <sub>DSC</sub>	35		250	mA	V <sub>OUT</sub> = High, -7V ≤ V <sub>O</sub> ≤ +12V
		35		250	mA	V <sub>OUT</sub> = Low, -7V ≤ V <sub>O</sub> ≤ +12V

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PARAMETER	SYMBOL	MIN.	TYP.	MAX	UNIT	CONDITIONS
<b>AC Characteristics</b>						
Maximum Data Rate	-	10			Mbps	RE# = 5V, DE = 5V
Driver Input to Output (See Figure 3)	$t_{DPLH}, t_{DPHL}$	20	40	60	ns	$t_{PLH}; R_{DIFF} = 54\Omega, C_{L1} = C_{L2} = 100pF$
	$t_{DPLH}, t_{DPHL}$	20	40	60	ns	$t_{PHL}; R_{DIFF} = 54\Omega, C_{L1} = C_{L2} = 100pF$
Driver Skew	$ t_{DPLH} - t_{DPHL} $		5	10	ns	$t_{SKEW} =  t_{DPLH} - t_{DPHL} $
Driver Rise or Fall Time	$t_R, t_F$	3	15	40	ns	10% to 90%, $R_{DIFF} = 54\Omega, C_{L1} = C_{L2} = 100pF$
Driver Enable to Output High (See Figure 4)	$t_{DZH}$		40	70	ns	$C_{L1} = 100pF$
Driver Enable to Output Low (See Figure 4)	$t_{DZL}$		40	70	ns	$C_{L1} = 100pF$
Driver Disable Time from Low (See Figure 4)	$t_{DLZ}$		40	70	ns	$C_{L1} = 100pF$
Driver Disable Time from High (See Figure 4)	$t_{DHZ}$		40	70	ns	$C_{L1} = 100pF$

## 5.3 Receiver Section

Test condition: VCC = 5V

PARAMETER	SYMBOL	MIN.	TYP.	MAX	UNIT	CONDITIONS
<b>DC Characteristics</b>						
Differential Input Threshold	$V_{TH}$	-300		+0	mV	$-7V \leq V_{CM} \leq +12V$
Input Hysteresis	$\Delta V_{TH}$		70		mV	$V_{CM} = 0V$
Output Voltage High	$V_{OH}$	3.5			V	$I_o = -4mA, V_{ID} = +200mV$
Output Voltage Low	$V_{OL}$			0.4	V	$I_o = +4mA, V_{ID} = -200mV$
Output Current	$I_{CC}$			$\pm 1$	$\mu A$	$0.4V \leq V_o \leq 2.4V, RE\# = -5V$
Input Resistance	$R_{IN}$	12	15		K $\Omega$	$-7V \leq V_{CM} \leq +12V$
Input Current (A,B), $V_{IN} = 12V$	$I_{IN}$			+1.0	mA	DE = 0V, $V_{cc} = 0V$ or 5.25V, $V_{IN} = 12V$
Input Current (A,B), $V_{IN} = -7V$	$I_{IN}$			-0.8	mA	DE = 0V, $V_{cc} = 0V$ or 5.25V, $V_{IN} = -7V$
Short Circuit Current	$I_{SCC}$	7		95	mA	$0V \leq V_{CM} \leq V_{cc}$

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PARAMETER	SYMBOL	MIN.	TYP.	MAX	UNIT	CONDITIONS
<b>AC Characteristics</b>						
Maximum Data Rate	-	10			Mbps	RE# = 0V, DE = 0V
Receiver Input to Output (See Figure 3)	$t_{PHL}, t_{PLH}$	60	70	200	ns	$t_{PLH}; R_{DIFF} = 54\Omega, C_{L1} = C_{L2} = 100pF$
	$t_{PHL}, t_{PLH}$	60	70	200	ns	$t_{PHL}; R_{DIFF} = 54\Omega, C_{L1} = C_{L2} = 100pF$
Receiver Skew	$ t_{PHL} - t_{PLH} $		15		ns	$t_{SKEW} =  t_{DPLH} - t_{DPLH} $
Receiver Enable to Output Low	$t_{ZL}$		20	50	ns	$C_{RL} = 15pF$ , See Figure 2
Receiver Enable to Output High	$t_{ZH}$		20	50	ns	$C_{RL} = 15pF$ , See Figure 2
Receiver Disable Time from Low	$t_{LZ}$		20	50	ns	$C_{RL} = 15pF$ , See Figure 2
Receiver Disable Time from High	$t_{HZ}$		20	50	ns	$C_{RL} = 15pF$ , See Figure 2

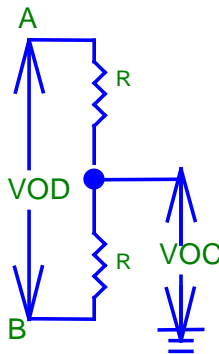


Figure 1: RS-485 Driver Test Load Circuit

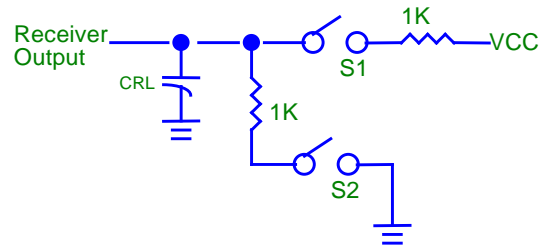


Figure 2: Receiver Timing Test Load Circuit

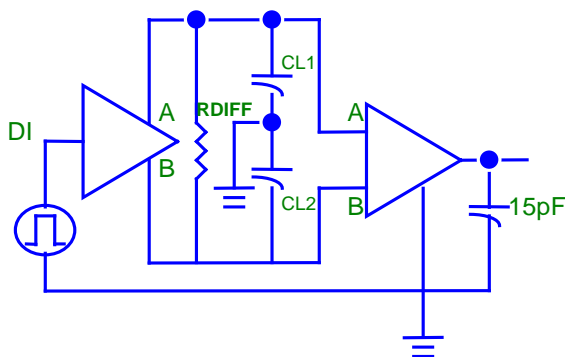


Figure 3: RS-485 Driver/Receiver Timing Test Circuit

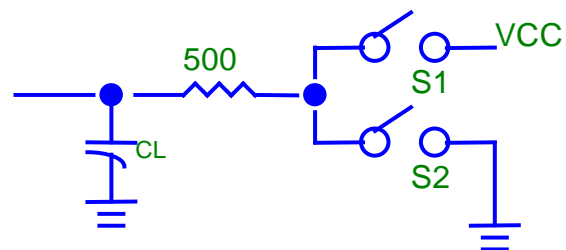


Figure 4: RS-485 Driver Timing Test Load Circuit



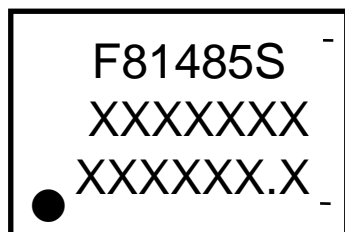
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## 6 Ordering Information

Part Number	Package Type
F81485S	8-SOP Green Package

## 7 Top Marking Specification

The version identification is shown as the bold red characters. Please refer to below for detail:



1<sup>st</sup> Line: Fintek Logo

2<sup>nd</sup> Line: Device Name → **F81485S**, where S means 8-SOP package

2<sup>nd</sup> Line: Assembly Plant Code (X) + Assembled Year Code (X) + Week Code (XX) + Fintek Internal Code (XX) + IC Version (X) where A means version A, B means version B, ...

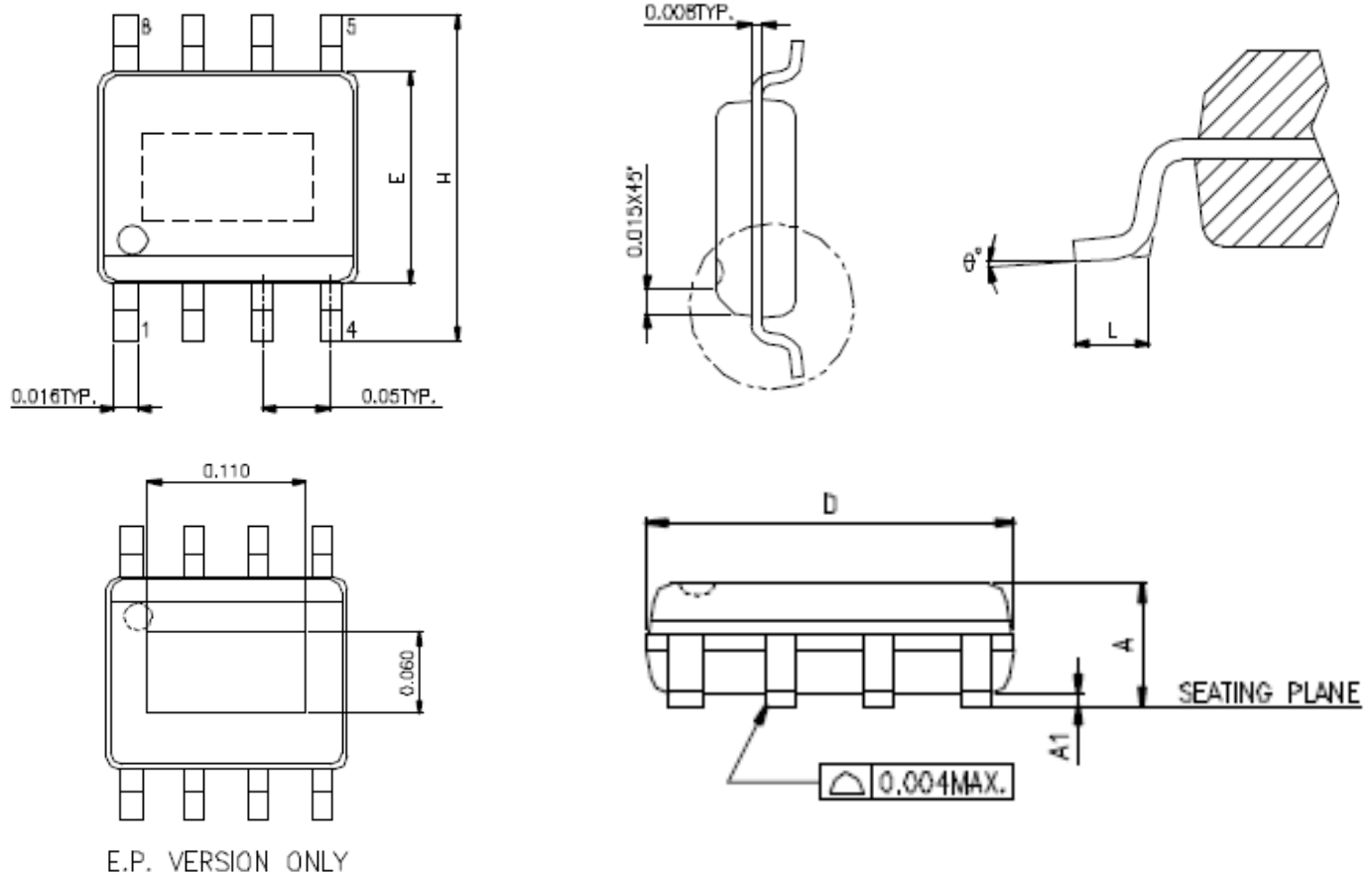
3<sup>rd</sup> Line: Wafer Fab Code (XXXX...XX)

● : Pin 1 Identifier

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## 8 Package Spec.

### 8-SOP Package



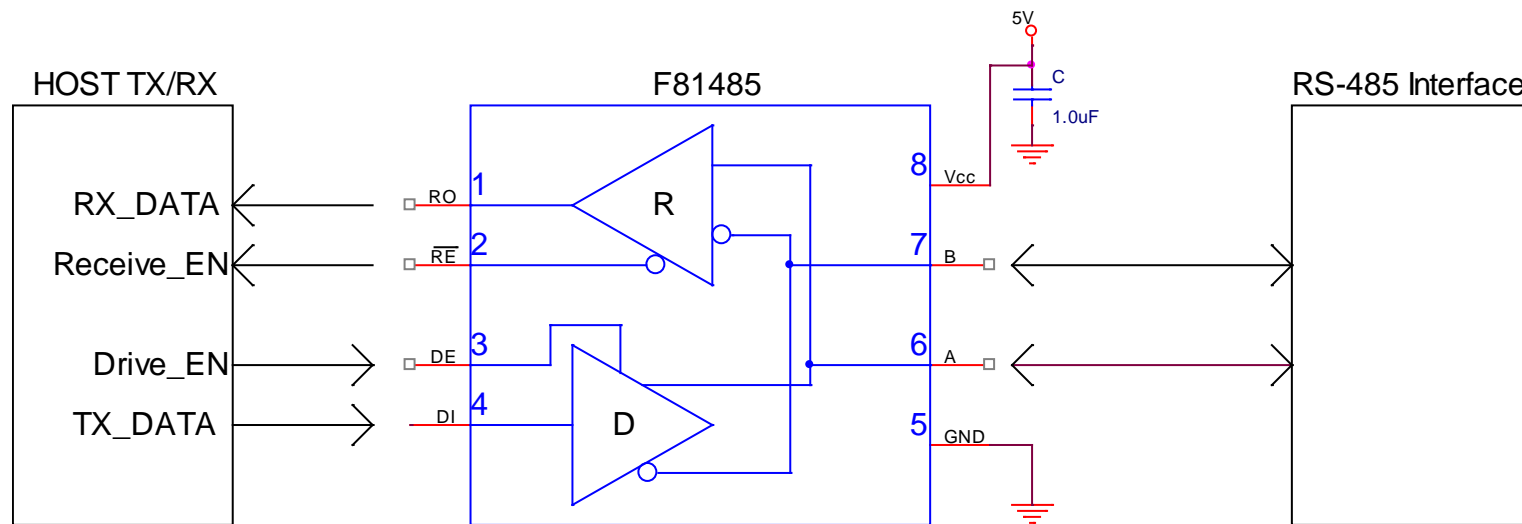
SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
$\theta^\circ$	0	8

UNIT : INCH

#### NOTES:

1. JEDEC OUTLINE : MS-012 AA / E.P. VERSION : N/A
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

## 9 Application Circuit



### MODE SELECTION

/RE	DE	MODE
0	0	RS485 Recieve
1	1	RS485 Drive
0	1	RS485 LoopBack
1	0	Dis_RS485

Title		
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