# F85226AF

## LPC to ISA Bridge



**Release Date: July, 2008**
**Revision: V0.20P**

# F85226AF Datasheet Revision History

| Version | Date | Page | Revision History |
|---|---|---|---|
| V0.20P | 2008/7/24 | - | Release Version |
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# Table of Contents

# 1. General Description

The F85226AF is a LPC to ISA Bridge IC for new generation chipset which is no support for ISA bus and slots. However the demand of ISA devices still exists. Therefore LPC to ISA Bridge IC is necessary to be used for new chipset system. The F85226AF is the best selection even though there is the PCI to ISA Bridge for supporting ISA device, because the issue of package size is critical for layout requirement. Follows the point at these issues, the F85226AF is optimal solution for the non-ISA chipset, the package of F85226AF will be the best chosen for economic solution and save the layout size of Motherboard.

The F85226AF absolutely meets LPC spec. 1.1 and supports fully ISA interface. Provides multi-ISA compatible slots without buffering and supports ISA parallel IRQ transfer to serial IRQ by IRQ Serialier. The F85226AF also provides programmable general purpose I/O pins for user. It is completely LPC to ISA bridge specialized chip.



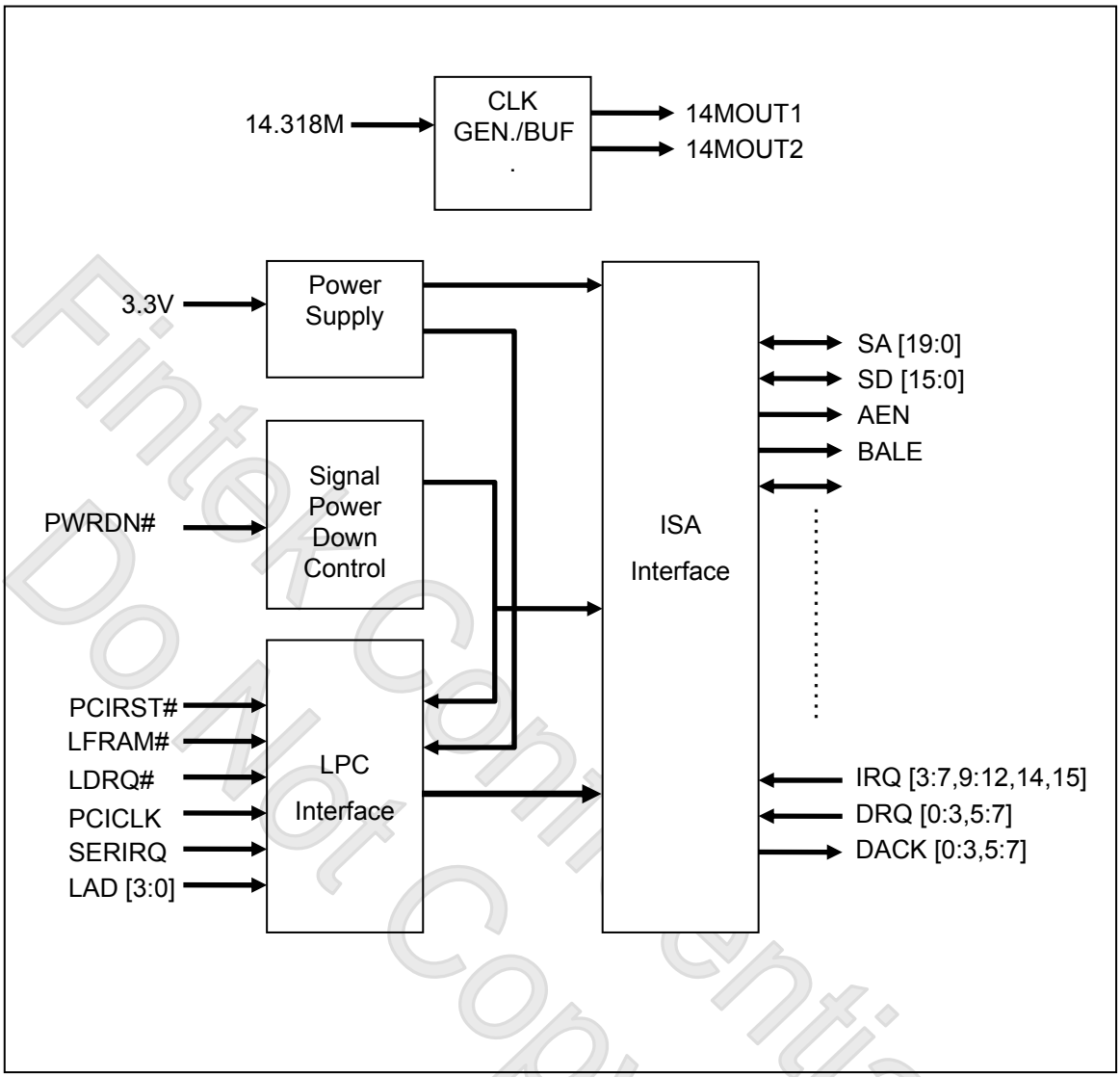
# 2. Features

- Meets LPC spec. 1.1
- Supports LDRQ#(LPC DMA), SERIRQ(Serial IRQ)
- Fully ISA bridge support except bus master(By conditions)
- Supports 8/16bit I/O and memory R/W
- All software transparent
- All ISA signals can be isolate
- ISA parallel IRQ transfer to serial IRQ by IRQ Serialier
- Supports multi-slots without buffering
- Supports the PCI clock to divide by 3 or 4 for ISA bus
- Supports to generate two 14.318MHz buffer out from one 14.318MHz in
- 4 sets of address decoder supported
- Supports programmable general purpose I/O pins
- Powered by 3Vcc (Signal 5V tolerance)
- 128pin PQFP package

# 3. Key Specifications

- Supply Voltage 3.0v to 3.6v
- Operating Supply current 4mA typ.

# 4. Block Diagram



## 5. Pin Configuration

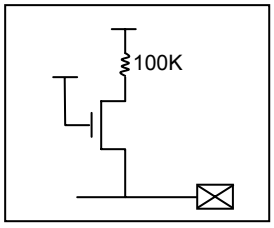

## 6. Pin Descriptions

$I/O_{24ts}$ - TTL level bi-directional pin and Schmitt trigger with 24 mA source-sink capability.

$I/OD_{24ts\_u100k}$ - TTL level input pin and Schmitt trigger, Open-drain output with 24 mA sink capability, internal pull-up 100KΩ connected with 3.3V to protect electric leakage.

$I/O_{24ts\_u100k}$ - TTL level input pin and Schmitt trigger, Output pin with 24 mA sink capability, internal pull-up 100KΩ connected with 3.3V to protect electric leakage.

$O_{24\_u100k}$ - Output pin with 24 mA source-sink capability, internal pull-up 100KΩ connected with 3.3V to protect electric leakage.




$O_{24}$ - Output pin with 24 mA source-sink capability.

$O_{20}$ - Output pin with 20 mA source-sink capability.

$IN_t$ - TTL level input pin.

$IN_{ts}$ - TTL level input pin and schmitt trigger.

P - Power.

## 6.1 Power Pin

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 5, 20, 25, 45, 55, 70, 85, 105, 120 | VDD3V | P | Standard Power Supply Voltage Input with 3.3V. |
| 15, 30, 50, 60, 80, 95, 110, 125 | GND | P | Ground. |

## 6.2 Power on strapping signal

| Pin No | Pin Name | Type | PWR | Description |
|---|---|---|---|---|
| 36 | 80PCS#/KBEN# | $I/OD_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Power-on strapping with external pulled-down resistor 10k will enable K/B and mouse functions. When it is set, pin 38, 39 and 40 will execute IRQ1, KBCS# and MCCS# signals. |
| 37 | ROMCS#/ROM_EN | $I/O_{24ts}$ (5V-tolerance) | VDD3v | Power-on strapping without internal resister, need external pulled-up resistor to enable CR03h (BIOS_ROM_EN bit) If there is a boot-ROM (BIOS). Else if without boot-ROM, please use external pulled-down 10K resister to disable this BIOS_ROM_EN. |
| 126 | DACK7#/RTCEN# | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Power-on strapping with external pulled-down 10k resistor will enable RTC functions. When it is set, pin 64 and 65 will do IRQ8 and RTCCS# signals. |
| 128 | DACK6#/HEFRAS | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Set this function will change the port that is used to access configuration registers. Default setting is 4Eh, but by power-on strapping with a external pulled-down 10k resister change to 2Eh. |
| 2 | DACK5#/EN_GP2X | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Power-on strapping with external pulled-down 10k resistor. Then it will disable LA [19:17] function and pin108~pin111, pin29 use as GPIO2X function. |

## 6.3 LPC interface

| Pin No. | Pin Name | Type | PWR | Description |
|---|---|---|---|---|
| 16-19 | LAD[3:0] | $I/O_{24ts}$ | VDD3v | Multiplexed command, address bi-directional data and cycle status. Through the LPC bus between a host and a peripheral. |
| 13 | LFRAME# | $IN_{ts}$ | VDD3v | Low pulse indicates start of a new cycle or termination of broken cycle. |
| 21 | PCICLK | $IN_t$ | VDD3v | PCI clock used for the LPC bus. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew. |

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| 14 | PCIRST# | $IN_{ts}$ | VDD3v | PCI system reset used for the LPC bus. The Reset signal line can be connected to PCIRST# signal on the host. |
| 23 | SERIRQ | $I/O_{24ts}$ | VDD3v | Serial IRQ Input/Output. |
| 22 | LDRQ# | $O_{24}$ | VDD3v | Encoded DMA Request signal. |
| 24 | PWRDN# | $IN_{ts}$ | VDD3v | Power Down. The signal is active low according to CR 44 Bit 7and wake-up enable by hardware setting. There are eight different power-down states (Power down Mode 3). |

## 6.4 ISA interface

| Pin No. | Pin Name | Type | PWR | Description |
|---|---|---|---|---|
| 58-56 | SA[19:17] | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | System Address Bus. These are the upper addresses that define the ISA's byte address space (up to 1 M byte). The SA [19:17] are at tri-states during PCIRST#. |
| 54-51<br>49-46<br>44-41<br>35-31 | SA[16:0] | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | System Address Bus. These define the ISA's byte address space (up to 128K byte). The SD [16:0] are at tri-states during PCIRST#. |
| 122-121<br>119-114<br>75-71<br>69-67 | SD[15:0] | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | System Data Bus. These provide 16-bit data for devices to reside on the ISA Bus. The SD [15:0] are at tri-states during PCIRST#. |
| 59 | AEN | $O_{24}$ (5V-tolerance) | VDD3v | Address Enable. AEN is asserted during DMA cycles, driven high during F85226AF initiated refresh cycles, driven low upon PCIRST#. |
| 86 | IOR# | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | I/O Read. IOR# is asserted to request an ISA I/O slave to drive data onto the data bus. |
| 84 | IOW# | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | I/O Write. IOW# is asserted to request an ISA I/O slave to accept data from the data bus. |
| 61 | IOCHRDY | $I/O_{24ts}$ (5V-tolerance) | VDD3v | I/O Channel Ready. IOCHDRY asserted indicates that an ISA slave requires additional wait states. When the F85226AF is an ISA slave, IOCHRDY is an output indicating additional wait states are required. |
| 92 | SYSCLK | $O_{24}$ | VDD3v | ISA System Clock. SYSCLK offers the reference clock to the ISA bus. The frequency is generated from dividing PCICLK by 3 or 4 (select by CR06 bit7). |
| 77 | RSTDRV | $O_{24}$ | VDD3v | Reset Drive. RSTDRV asserted indicates to reset devices that reside on the ISA Bus while the PCIRST# has been asserted. |

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| 11 | IOCS16# | $I/O_{24ts}$ (5V-tolerance) | VDD3v | 16-bit I/O Chip Select. IOCS16# is asserted by 16-bit ISA I/O devices to indicate that they support 16-bit I/O bus cycles. |
| 12 | MEMCS16# | $I/O_{24ts}$ (5V-tolerance) | VDD3v | Memory Chip Select 16. MEMCS16# is asserted by 16-bit ISA memory devices to indicate that the memory slave supports 16-bit accesses. |
| 76 | IOCHCK# | $IN_{ts}$ (5V-tolerance) | VDD3v | I/O Channel Check. Asserted by an ISA device indicating an error condition. |
| 81 | OWS# | $IN_{ts}$ (5V-tolerance) | VDD3v | Zero Wait States. An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be executed as an ISA zero wait state cycle. ZEROWS# has no effect during 16-bit I/O cycles. |
| 103-104 106-107 | LA[23:20] | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Unlatched Address. The LA [23:20] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA [23:20] are outputs when the F85226AF owns the ISA Bus. |
| 108-109 111 | LA[19:17] | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Unlatched Address. The LA [19:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA [19:17] are outputs when the F85226AF owns the ISA Bus. |
| | GP23, GP22, GP21 | | | General purpose I/O pin. |
| 82 | SMEMW# | $O_{24}$ (5V-tolerance) | VDD3v | Standard (system) Memory Write. SMEMW# is asserted for memory write accesses below 1MB. |
| 83 | SMEMR# | $O_{24}$ (5V-tolerance) | VDD3v | Standard (system) Memory Read. SMEMR# is asserted for memory read accesses below 1 MB. |
| 91 | REFRESH# | $O_{24\_u100k}$ (5V-tolerance) | VDD3v | Refresh Cycle indicator. REFRESH# asserted indicates that a refresh cycle is in progress, or ISA master requests F85226AF to generate a refresh cycle. The signal is at tri-stated upon PCIRST#. |
| 101 | BALE | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Bus Address Latch Enable. BALE asserted indicates when the address (SA[19:0], LA[23:17]) and SBHE# are valid. The LA [23:17] address lines are latched on the trailing edge of BALE. BALE is driven by low upon PCIRST#. |
| 102 | SBHE# | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | System Byte High Enable. SBHE# asserted indicates that SD[15:8] will be used to transfer a byte. SBHE# is at an unknown state upon PCIRST#. |
| 112 | MEMR# | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Memory Read. MEMR# asserted indicates the current ISA bus cycle is a memory read. |
| 113 | MEMW# | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | Memory Write. MEMW# asserted indicates the current ISA bus cycle is a memory write. |

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| 123 | MASTER# | $IN_{ts}$ (5V-tolerance) | VDD3v | The MASTER# input asserted indicates an ISA bus master is driving the ISA bus. This signal is executed with DREQ line by an ISA master to gain control of the ISA Bus. |
| 98 | IRQ3 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 3. |
| 97 | IRQ4 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 4. |
| 96 | IRQ5 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 5. |
| 94 | IRQ6 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 6. |
| 93 | IRQ7 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 7. |
| 78 | IRQ9 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 9. |
| 10 | IRQ10 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 10. |
| 9 | IRQ11 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 11. |
| 8 | IRQ12 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 12. |
| 6 | IRQ14 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 14. |
| 7 | IRQ15 | $IN_{ts}$ (5V-tolerance) | VDD3v | Parallel Interrupt Requested Input 15. |
| 3 | DRQ0 | $IN_{ts}$ (5V-tolerance) | VDD3v | DMA Request input 0. The DREQ asserted indicates that either a slave DMA device is requesting DMA services or an ISA bus master is requesting to use the ISA bus. |
| 90 | DRQ1 | $IN_{ts}$ (5V-tolerance) | VDD3v | DMA Request input 1. |
| 79 | DRQ2 | $IN_{ts}$ (5V-tolerance) | VDD3v | DMA Request input 2. |
| 88 | DRQ3 | $IN_{ts}$ (5V-tolerance) | VDD3v | DMA Request input 3. |
| 1 | DRQ5 | $IN_{ts}$ (5V-tolerance) | VDD3v | DMA Request input 5. |

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|---|---|---|---|---|
| 127 | DRQ6 | $IN_{ts}$ (5V-tolerance) | VDD3v | DMA Request input 6. |
| 124 | DRQ7 | $IN_{ts}$ (5V-tolerance) | VDD3v | DMA Request input 7. |
| 4 | DACK0# | $O_{24}$ (5V-tolerance) | VDD3v | DMA Acknowledge channel 0. The DACK# outputs asserted indicates that either a DMA channel or an ISA bus master has been granted the ISA bus. |
| 89 | DACK1# | $O_{24}$ (5V-tolerance) | VDD3v | DMA Acknowledge channel 1. |
| 99 | DACK2# | $O_{24}$ (5V-tolerance) | VDD3v | DMA Acknowledge channel 2. |
| 87 | DACK3# | $O_{24}$ (5V-tolerance) | VDD3v | DMA Acknowledge channel 3. |
| 2 | DACK5#<br>EN_GP2X | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | DMA Acknowledge channel 5.<br>During power-on strapping with external pulled-down 10k resistor. Then it will disable LA [19:17] function and pin108~pin111, pin29 use as GPIO2X function. |
| 128 | DACK6#<br>HERFRA | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | DMA Acknowledge channel 6.<br>During power-on reset, this pin is pulled-up internally(Select 4Eh) ,and is defined as HEFRAS which provides the power-on value for CR3 bit4 .A 10k ohm is recommended if intends to pull down .(Select 2Eh) |
| 126 | DACK7#<br>RTCEN# | $I/O_{24ts\_u100k}$ (5V-tolerance) | VDD3v | DMA Acknowledge channel 7.<br>RTC Function Enable. The pin applies a pull-down resistor (4.7K ohm) to enable RTC functions (RTCCS#, and IRQ8) |
| 100 | TC | $O_{24}$ (5V-tolerance) | VDD3v | Terminal Count. TC signals the final data transfer of a DMA transfer. |
| 36 | 80PCS#<br>KBEN# | $I/OD_{24ts\_u100k}$ (5V-tolerance) | VDD3v | 80h PORT Chip Select.(Default)<br>Only decode IO address port 80h and must apply with IOW#.<br>K/B Functions Enable. During power-on reset this pin is weak pulled-up internally. The pin applied a pull-down resistor (10K ohm) to enable K/B functions. (IRQ1,KBCS#,and MCCS#) |
| 37 | ROMCS# | $I/O_{24ts}$ (5V-tolerance) | VDD3v | ROMCS#, this pin enable positive decoder of BIOS address range. |

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|---|---|---|---|---|
| | ROM_EN | | | Power-on strapping with internal pulled-up resistor will enable CR03h (BIOS_ROM_EN, BIOS_WR_EN bit). If there is a boot-ROM (BIOS), else if without boot-ROM, please use external pulled-down 10K resister to disable this ROM_EN and WR_EN. |
| 38 | GPIO0<br>IRQ1 | $I/O_{24ts}$ (5V-tolerance) | VDD3v | General purpose I/O pin 0.<br>Parallel Interrupt Requested Input 1. This pin is used for specific K/B functions. |
| 39 | GPIO1<br>KBCS# | $I/O_{24t}$ (5V-tolerance) | VDD3v | General purpose I/O pin 1.<br>Decode address 60h and 64h to generate chip selected signal. Enable by KBEN# power-on setting. |
| 40 | GPIO2<br>MCCS# | $I/O_{24ts}$ (5V-tolerance) | VDD3v | General purpose I/O pin 2.<br>Decode address 62h and 66h to generate chip selected signal. Enable by KBEN# power-on setting. |
| 62 | GPIO3<br>IRQIN | $I/O_{24ts}$ (5V-tolerance) | VDD3v | General purpose I/O pin 3.<br>It is programmable to transfer parallel IRQ input to serial IRQ, Enable by KBEN# power-on setting. |
| 63 | GPIO4<br>PLED | $I/O_{24ts}$ (5V-tolerance) | VDD3v | General purpose I/O pin 4.<br>Power LED output, the signal is at low state after system reset. |
| 64 | GPIO5<br>IRQ8 | $I/O_{24ts}$ (5V-tolerance) | VDD3v | General purpose I/O pin 5.<br>Parallel Interrupt Requested Input 8. This interrupt request is used for specific RTC functions. Enable by RTCEN# power-on setting. |
| 65 | GPIO6<br>RTCCS# | $I/O_{24ts}$ (5V-tolerance) | VDD3v | General purpose I/O pin 6.<br>Decode address 70h and 71h to generate chip selected signal. Enable by RTCEN# power-on setting. |
| 66 | GPIO7<br>IOHCS# | $I/O_{24ts}$ (5V-tolerance) | VDD3v | General purpose I/O pin 7.<br>Decode SA [15-11] all are at “0” state initially and setting by CR04 Bit 7. |
| 26 | 14.318M | $IN_{ts}$ (5V-tolerance) | VDD3v | 14.318 MHz Clock Input. |
| 27 | 14MOUT 1 | $O_{20}$ | VDD3v | 14.318 MHz Buffer Output 1. |
| 28 | 14MOUT 2 | $O_{20}$ | VDD3v | 14.318 MHz Buffer Output 2. |
| 29 | GP20<br>PLED | $I/O_{24ts}$ (5V-tolerance) | VDD3v | General purpose I/O pin.<br>Power LED output, the signal is at low state after system reset. |

# 7. Function Description

## 7.1 LPC interface:

The F85226AF implemented full functions that described in the LPC I/F 1.1 specification and transfers all subtractive cycles from LPC bus to ISA interface for more ISA compatibility. The F85226AF built in 16-bit IO/ Memory enhances transaction. Peripheral or Master devices can assert cycles that are not defined in positive decode ranges of LPC Interface. All LPC bus signals use PCI electrical characteristics. The following cycle types are supported by F85226AF.

- IO read write (8 / 16 bit)
- Memory read write (8 / 16 bit)
- DMA read write (8/ 16 / 32 bit)
- Firmware memory read write (only support size 8 or 16 bit).

**eCycles**:

S: Start Cycle

C: Command Type Cycle

| Cycle Types | Encoding | Remark |
|---|---|---|
| IO Read | S: 0x0h;<br>C: 0x0h | Size: 8 bit and 16 bit in Enhanced mode, for LPC peripheral. |
| IO Write | S: 0x0h;<br>C: 0x2h | Size: 8 bit and 16 bit in Enhanced mode, for LPC peripheral. |
| Memory Read | S: 0x0h;<br>C: 0x4h | Size: 8 bit and 16 bit in Enhanced mode, for LPC peripheral and host. |
| Memory Write | S: 0x0h;<br>C: 0x6h | Size: 8 bit and 16 bit in Enhanced mode, for LPC peripheral and host. |
| DMA Read | S: 0x0h;<br>C: 0x8h | Size: 8, 16 and 32 bit, for LPC peripheral. |
| DMA Write | S: 0x0h;<br>C: 0xAh | Size: 8, 16 and 32 bit, for LPC peripheral. |
| Booting Memory Read | S: 0xDh; | Size: 8, 16, 32 and 1024 bit, for LPC peripheral. |
| Booting Memory Write | S: 0xEh; | Size: 8, 16, and 32 bit, for LPC peripheral. |

**Start:**

The cycle indicates the beginning or abort of a transaction. When LFRAME# is asserted low and monitors LAD[3:0] that determine frame type to enter a valid Start.

**Cycle Type and Direction:**

LPC host will issue the transaction cycle and direction by LAD[3:1] and LAD0 is always ignored.

### Size:

LPC host on DMA or bus master on memory transaction issue data size that will be transferred by LAD[1:0] and LAD[3:2] must be driven 0x00b.

### Turn-Around:

LPC host or peripheral will issue two clock wide cycles after turning control over to peripheral or turning back from peripheral to host. LAD[3:0] should be driven to high level on first cycle and release to tri-state on next one.

### Address:

While doing IO transaction, this duration is four clock wide that indicates 16-bit address, on Memory cycles there are eight clocks that indicates 32-bit address will be asserted by LPC host or Master. The duration is not asserted on DMA transaction.

### Channel and Terminal count:

Only on DMA transferring, LAD[2:0] signals indicate granted channel in one clock cycle. LAD[3] indicates Terminal count down.

### Data:

Each frame can carry one byte (8 bit), first nibble is Data[7;4] and next is Data[3:0].

### SYNC:

LPC host or peripheral can add wait state, response error and ready to accept a frame by LAD[3:0].

0x0h: Ready
0x5h: Short Wait, maximum number of SYNC is 8 clocks.
0x6h: Long Wait, no maximum number.
0x9h: Ready More on DMA transaction.
0xAh: Error, it relates to IOCHK# on ISA interface.
Others: Reserved.
STA : Start Cycle
CT : Cycle Type and Direction
H_TAR: Host Turn-Around
P_TAR: Peripheral Turn-Around

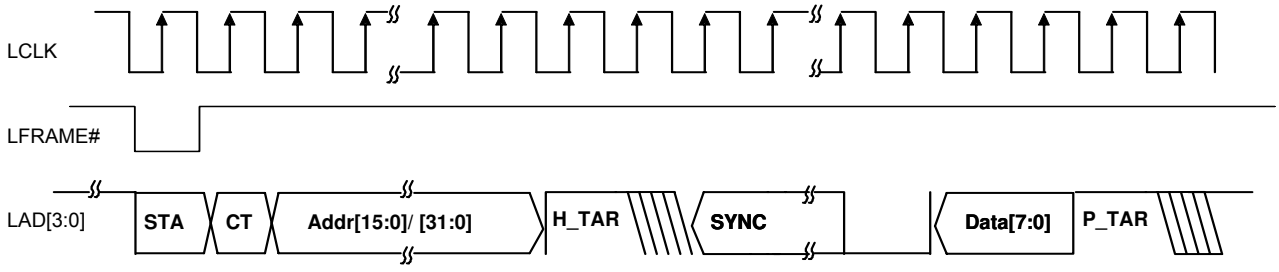


Figure: Read Cycles

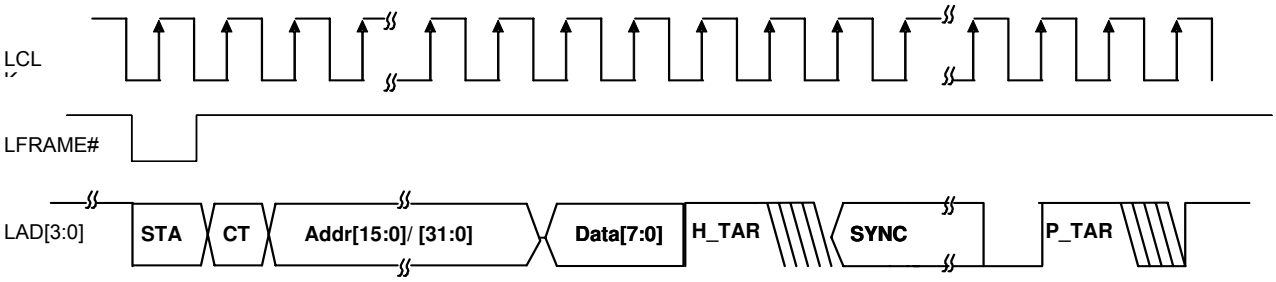


Figure: Write Cycles

### 7.1.1 IO/Memory Read and Write Cycles

When LPC interface Bridge issues IO cycles that meet subtractive decode, F85226AF will assert corresponded IOR#, IOW# , MEMR# ,SMEMR# , MEMW# and SMEMW# then respond by inserting wait cycles (long wait SYNC). After finishing ISA transaction and there isn't any valid ISA Wait state inserted, it responds Ready-state and terminates the cycles. If the host issues 16 bit transfer, F85226AF will active enhance 16-bit transferring function automatically.

### 7.1.2 DMA Read and Write Cycles

The read transactions transfer data from main memory to peripheral and write cycles transfer data from peripheral to main memory. DMA requests form ISA interface are delivered by LDRQ# to DMA controller (like 8237) and the acknowledge responds from LAD [3:0] encoding message. Terminal count is depended on the counter programmed in DMA controller, when reach the counter threshold, TC is related to LAD3 and asserted when DMA controller plan to terminal DMA transaction.

### 7.1.3 Booting Memory Read and Write Cycles

The ISA interface of F85226AF can communicate to ISA ROM (System BIOS) with ROMCS#, MEMER# and MEMW#, BIOS booting cycles of PC system may assert through different cycle type ( like Memory Read and Firmware Memory Read) , F85226AF can perform a positive decoder on specified memory range included legacy BIOS , extended legacy BIOS and user defined High Memory address.