F81865

Super IO with 6 UARTs

Release Date: May, 2010
Version: V0.28P

F81865 Datasheet Revision History

Version	Date	Page	Revision History
V0.20P	2008/10/9	-	Release Version
V0.21P	2008/10/23	92	Add GPIO Base Address Register
V0.22P	2008/10/30	130	Update Application Circuit
V0.23P	2008/12/17	-	1. Pin 82 PWR Type Update to VBAT 2. Update UART Clock Register 3. Revise UART Name From UART0~5 to UART1~6 4. Add IR & Part of UART 6 Function at Pin 9, 10, 11 5. Add Bypass Mode at ACPI control register. 6. Add Electrical Characteristics 7. Checking Typing
V0.24P	2008/12/25		Made Correction & Clarification
V0.25P	2009/6/17		● Made Correction & Clarification ● Revise index 96h bit 3-0 ● Update Application Circuit
V0.26P	2009/9/17		Made Correction & Clarification Modify Electrical Characteristics
V0.27P	2009/12/07		Made Correction & Clarification Modify Application Circuit (sheet 4)
V0.28P	2010/5/24		Made Correction & Clarification Add OVT# SMI mode to index 2h bit 5-4 & figure 7.3 Enhanced Fan Description & Count (Section 7.6.1 fan) Modify RS485 Enable Register for COM 1~6—Index F0h, bit 4

Table of Content

1. General Description

The F81865 is the featured IO chip for Industrial PC system. Equipped with one IEEE 1284 parallel port, 6 UART ports with 9-bit protocol, KBC, Serial Peripheral Interface (SPI), SIR and one FDC. The F81865 integrated with hardware monitor, 7 sets of voltage sensor, 2 sets of creative auto-controlling fans and 2 temperature sensor pins for the accurate dual current type temperature measurement for CPU thermal diode or external transistors 2N3906.

The F81865 provides flexible features for multi-directional application. For instance, supports 53 GPIO pins, IRQ sharing function designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature, the F81865 also integrated SPI interface. The SPI interface is for BIOS usage including bridge function. Others, the F81865 supports newest Intel PECI interfaces for new generational CPU temperature use. Furthermore, F81865 provides independent RTC function.

These features as above description will help you more and improve product value. Finally, the F81865 is powered by 3.3V voltage, with the LPC interface in the package of 128-PQFP.

2. Feature List

- **General Functions**
  - Comply with LPC 1.1
  - Support ACPI 3.0
  - Provides one FDC, KBC and Parallel Port
  - Provide 6 fully functional UART and 1 SIR
  - 9-bit Protocol for UARTs
  - Support IRQ Sharing function.
  - H/W monitor functions
  - SPI interface for BIOS
  - RTC function
  - Support PECI 1.0 interface
  - 53 GPIO Pins for flexible application
  - 24/48 MHz clock input
  - Packaged in 128-PQFP and powered by 3.3VCC

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and under run conditions
- Built-in address mark detection circuit to simplify the read electronics
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate

UART

- Provide 6 fully functional UART
- 6 high-speed 16C550 compatible UART with 16-byte FIFOs
- Fully programmable serial-interface characteristics
- Baud rate supports 115.2K, max. up to 1.5M
- Support IRQ 3,4,5,6,7,8,9,10,11 sharing
- Provide 9-bits Function for Gaming Machine
- Support IrDA version 1.0 SIR protocol

Parallel Port

- One PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284
- Enhanced printer port back-drive current protection

Keyboard Controller

- compatibility with the 8042
- Support PS/2 mouse
- Support both interrupt and polling modes
- Hardware Gate A20 and Hardware Keyboard Reset

Hardware Monitor Functions

- 2 dual current type (±3℃) thermal inputs for CPU thermal diode and 2N3906 transistors
- Temperature range -40℃~127℃
- 7 sets voltage monitoring (4 external and 3 internal powers)
- High limit signal (PME#) for Vcore level

- 2 fan speed monitoring inputs
- 2 fan speed PWM/DC control outputs(support 3 wire and 4 wire fans)
- Issue PME# and OVT# hardware signals output
- Case intrusion detection circuit
- WATCHDOG# comparison of all monitored values
- Integrate Intel PECI 1.0 Interface

Serial Peripheral Interface Compatible

- Support SPI bridge function for BIOS use

RTC function

- RTC for time synchronizing.
- Provide 256 bytes RAM for CMOS setting save.
- 32.768K Crystal input
- Stand alone VBAT power input requirement

GPIO Function

- Total 53 pins GPIO
- Interrupt status support
- All GPIO can be programmed.
- All GPIO pins default mode are OD level input.
- Supports High/Low Level/Pulse, Open Drain/Push Pull function selection

Package

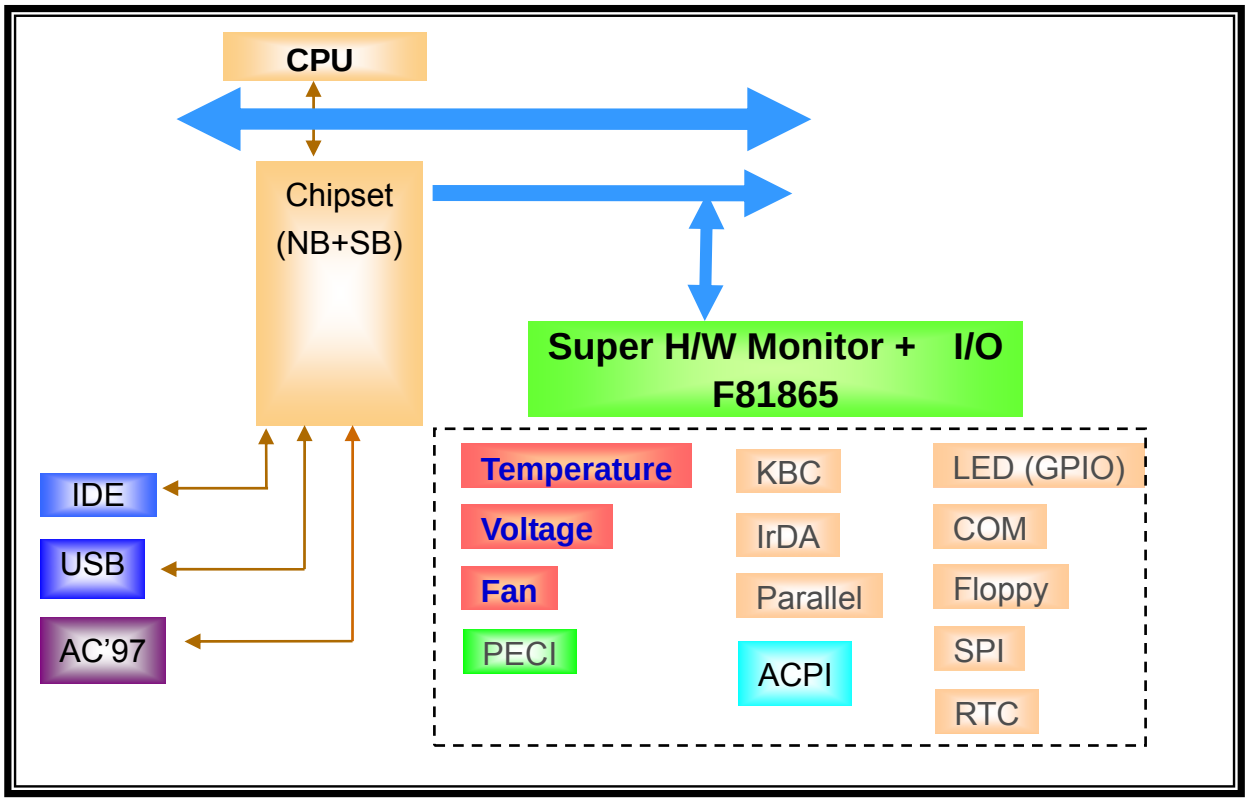
- 128-pin PQFP Green Package

Noted: Patented TW207103 TW207104 TW220442 US6788131 B1 TWI235231 TW237183 TWI263778

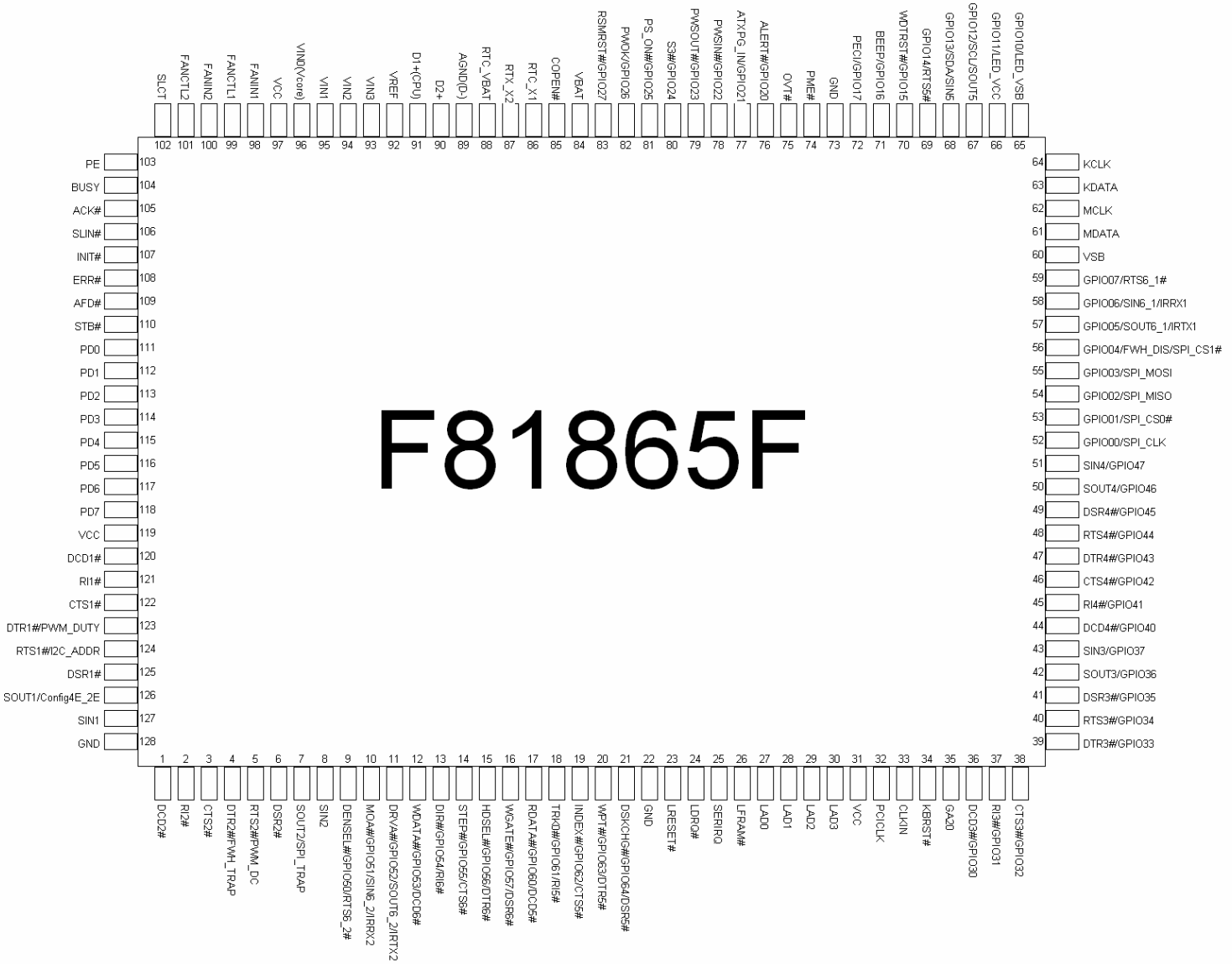
3. Key Specification

Supply Voltage	3.0V to 3.6V
Operating Supply Current	10 mA typ.

4. Block Diagram



5. Pin Configuration



$I/O_{12st,5V}$ - TTL level bi-directional pin and schmitt trigger, 12 mA sink capability, 5V tolerance.
I/OOD_{12t} - TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability.
I/OOD_{14} - TTL level bi-directional pin, can select to OD or OUT by register, with 14 mA source-sink capability.
I/OOD_{8} - TTL level bi-directional pin, can select to OD or OUT by register, with 8 mA source-sink capability.
$I/OD_{16t,5v}$ - TTL level bi-directional pin,Open-drain output with 16 mA source-sink capability, 5V tolerance.
$OD_{16,u10,5v}$ - Open-drain output pin with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.
$I/OD_{12st,5v}$ - TTL level bi-directional pin and schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.
$O_{8,u47,5v}$ - Open-drain pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.
O_{8} - Output pin with 8 mA source-sink capability.
O_{12} - Output pin with 12 mA source-sink capability.
AOUT - Output pin(Analog).
$OD_{12,5v}$ - Open-drain output pin with 12 mA sink capability, 5V tolerance.
OD_{14} - Open-drain output pin with 14 mA sink capability.
OD_{24} - Open-drain output pin with 24 mA sink capability.
I/O_{24t} - TTL level bi-directional pin, 24mA sink capability.
I/O_{8t} - TTL level bi-directional pin, 8 mA sink capability.
$IN_{t,5v}$ - TTL level input pin,5V tolerance.
IN_{st} - TTL level input pin and schmitt trigger.
$IN_{st,5v}$ - TTL level input pin and schmitt trigger, 5V tolerance.
AIN - Input pin(Analog).
P - Power.

6. Pin Description

6.1 Power Pin

Pin No.	Pin Name	Type	Description
31, 119	VCC	P	Power supply voltage input with 3.3V
60	VSB	P	Stand-by power supply voltage input 3.3V
84	VBAT	P	Battery voltage input
88	RTC_VBAT	P	Battery voltage input for RTC
97	AVCC	P	Analog Power with 3.3V
89	AGND(D-)	P	Analog GND
22, 73, 128	GND	P	Digital GND

6.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
23	LRESET#	$IN_{st,5v}$	VCC	Reset signal. It can connect to PCIRST# signal on the host.
24	LDRQ#	O_{12}	VCC	Encoded DMA Request signal.
25	SERIRQ	I/O_{24t}	VCC	Serial IRQ input/Output.
26	LFRAME#	IN_{st}	VCC	Indicates start of a new cycle or termination of a broken cycle.
27-30	LAD[0:3]	I/O_{24t}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
32	PCICLK	IN_{st}	VCC	33MHz PCI clock input.
33	CLKIN	IN_{st}	VCC	System clock input. According to the input frequency 24/48MHz.

6.3 FDC

Pin No.	Pin Name	Type	PWR	Description
9	DENSEL#	OD_{14}	VCC	Drive Density Select. Set to 1 – High data rate.(500Kbps, 1Mbps) Set to 0 – Low data rate. (250Kbps, 300Kbps)
	GPIO50	I/OOD_{14}		General Purpose IO.
	RTS6_2#	O_{14}		UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
10	MOA#	OD_{14}	VCC	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
	GPIO51	I/OOD_{14}		General Purpose IO.
	SIN6_2	$IN_{t,5v}$		UART Serial Input. Used to receive serial data through the communication link.
	IRRX_2	$IN_{t,5v}$		Infrared Receiver input.
11	DRVA#	OD_{14}	VCC	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
	GPIO52	I/OOD_{14}		General Purpose IO.
	SOUT6_2	O_{14}		UART Serial Output. Used to transmit serial data out to the communication link.
	IRTX_2	O_{14}		Infrared Transmitter Output.
12	WDATA#	OD_{14}	VCC	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
	GPIO53	I/OOD_{14}		General Purpose IO.
	DCD6#	$IN_{t,5v}$		Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.

13	DIR#	OD_{14}	VCC	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
	GPIO54	I/OOD_{14}		General Purpose IO.
	RI6#	$IN_{t,5v}$		Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
14	STEP#	OD_{14}	VCC	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
	GPIO55	I/OOD_{14}		General Purpose IO.
	CTS6#	$IN_{t,5v}$		Clear To Send is the modem control input.
15	HDSEL#	OD_{14}	VCC	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
	GPIO56	I/OOD_{14}		General Purpose IO.
	DTR6#	O_{14}		UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
16	WGATE#	OD_{14}	VCC	Write enable. An open drain output.
	GPIO57	I/OOD_{14}		General Purpose IO.
	DSR6#	$IN_{t,5v}$		Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
17	RDATA#	IN_{ts5v}	VCC	The read data input signal from the FDD.
	GPIO60	I/OOD_{12}		General Purpose IO.
	DCD5#	$IN_{t,5v}$		Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
18	TRK0#	$IN_{t,5v}$	VCC	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
	GPIO61	I/OOD_{12}		General Purpose IO.
	RI5#	$IN_{t,5v}$		Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
19	INDEX#	$IN_{st,5v}$	VCC	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
	GPIO62	I/OOD_{12}		General Purpose IO.
	CTS5#	$IN_{t,5v}$		Clear To Send is the modem control input.
20	WPT#	$IN_{st,5v}$	VCC	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
	GPIO63	I/OOD_{12}		General Purpose IO.
	DTR5#	O_{12}		UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.

21	DSKCHG#	$IN_{t,s5v}$	VCC	Diskette change. This signal is active low at power on and whenever the diskette is removed.
	GPIO64	I/OOD_{12}		General Purpose IO.
	DSR5#	$IN_{t,5v}$		Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.

6.4 UART

Pin No.	Pin Name	Type	PWR	Description
120	DCD1#	$IN_{t,5v}$	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
121	RI1#	$IN_{t,5v}$	VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
122	CTS1#	$IN_{t,5v}$	VCC	Clear To Send is the modem control input.
123	DTR1#	$O_{8,u47,5v}$	VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	PWM_DUTY_TRAP	$IN_{t,5v}$	VCC	Power on strapping pin: 1(Default): (Internal pull high) Power on fan speed default duty is 60%.(PWM) 0: (External pull down) Power on fan speed default duty is 100%.(PWM)
124	RTS1#	$O_{8,u47,5v}$	VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
	I2C_ADDR_TRAP	$IN_{t,5v}$	VCC	Power on strapping pin: 1: (internal pull high, default) Power on I2C slave address is 8'h5C. 0: (external pull down) Power on I2C slave address is 8'h5A.
125	DSR1#	$IN_{t,5v}$	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
126	SOUT1	$O_{8,u47,5v}$	VCC	UART Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	Config4E_2E	$IN_{t,5v}$		Power on strapping: 1(Default)Configuration register:4E/4F 0 Configuration register:2E/2F
127	SIN1	$IN_{t,5v}$	VCC	UART Serial Input. Used to receive serial data through the communication link.

1	DCD2#	$IN_{t,5v}$	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
2	RI2#	IN_{t5v}	VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
3	CTS2#	IN_{t5v}	VCC	Clear To Send is the modem control input.
4	DTR2#	$O_{8,u47,5v}$	VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	FWH_TRAP	$IN_{t,5v}$	VCC	Power on strapping pin: 1(Default): (Internal pull high) FWH is enabled. 0: (External pull down) FWH is disabled.
5	RTS2#	$O_{8,u47,5v}$	VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
	PWM_DC	IN_{t5v}	VCC	Power on strapping pin: 1: (internal pull high, default) Fan control is PWM mode. 0: (external pull down) Fan control is linear mode (DAC output).
6	DSR2#	$IN_{t,5v}$	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
7	SOUT2	$O_{8,u47,5v}$	VCC	UART Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	SPI_TRAP	$IN_{t,5v}$		Power on strapping: 1(Default internal pull high) SPI is disabled. 0 (external pull down) SPI is enabled.
8	SIN2	$IN_{t,5v}$	VCC	UART Serial Input. Used to receive serial data through the communication link.
36	DCD3#	$IN_{t,5v}$	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
	GPIO30	I/OOD_8		General Purpose IO.
37	RI3#	IN_{t5v}	VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	GPIO31	I/OOD_8		General Purpose IO.
38	CTS3#	$IN_{t,5v}$	VCC	Clear To Send is the modem control input.
	GPIO32	I/OOD_8		General Purpose IO.
39	DTR3#	O_8	VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to

				communicate.
	GPIO33	I/OOD_8		General Purpose IO.
40	RTS3#	O_8	VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	GPIO34	I/OOD_8		General Purpose IO.
41	DSR3#	$IN_{t,5v}$	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
	GPIO35	I/OOD_8		General Purpose IO.
42	SOUT3	O_8	VCC	UART Serial Output. Used to transmit serial data out to the communication link.
	GPIO36	I/OOD_8		General Purpose IO.
43	SIN3	$IN_{t,5v}$	VCC	UART Serial Input. Used to receive serial data through the communication link.
	GPIO37	I/OOD_8		General Purpose IO.
44	DCD4#	$IN_{t,5v}$	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
	GPIO40	I/OOD_8		General Purpose IO.
45	RI4#	$IN_{t,5v}$	VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	GPIO41	I/OOD_8		General Purpose IO.
46	CTS4#	$IN_{t,5v}$	VCC	Clear To Send is the modem control input.
	GPIO42	I/OOD_8		General Purpose IO.
47	DTR4#	O_8	VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	GPIO43	I/OOD_8		General Purpose IO.
48	RTS4#	$O_{8,u47,5v}$	VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
	GPIO44	I/OOD_8		General Purpose IO.
49	DSR4#	$IN_{t,5v}$	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
	GPIO45	I/OOD_8		General Purpose IO.
50	SOUT4	O_8	VCC	UART Serial Output. Used to transmit serial data out to the communication link.
	GPIO46	I/OOD_8		General Purpose IO.
51	SIN4	$IN_{t,5v}$	VCC	UART Serial Input. Used to receive serial data through the communication link.
	GPIO47	I/OOD_8		General Purpose IO.

6.5 Parallel Port

Pin No.	Pin Name	Type	PWR	Description
102	SLCT	$IN_{st,5v}$	VCC	An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
103	PE	$IN_{st,5v}$	VCC	An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
104	BUSY	$IN_{st,5v}$	VCC	An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
105	ACK#	$IN_{st,5v}$	VCC	An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
106	SLIN#	$OD_{12,5v}$	VCC	Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
107	INIT#	$OD_{12,5v}$	VCC	Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
108	ERR#	$IN_{st,5v}$	VCC	An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
109	AFD#	$OD_{12,5v}$	VCC	An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
110	STB#	$OD_{12,5v}$	VCC	An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
111	PD0	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
112	PD1	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 1.
113	PD2	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 2.
114	PD3	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 3.
115	PD4	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 4.
116	PD5	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 5.
117	PD6	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 6.
118	PD7	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 7.

6.6 Hardware Monitor

Pin No.	Pin Name	Type	PWR	Description
93	VIN3	AIN	AVCC	Voltage Input 3.
94	VIN2	AIN	AVCC	Voltage Input 2.
95	VIN1	AIN	AVCC	Voltage Input 1.
96	VIN0 (Vcore)	AIN	AVCC	Voltage Input for Vcore.
98	FANIN1	$IN_{st,5v}$	VCC	Fan 1 tachometer input.
99	FANCTL1	$OD_{12,5v}$ AOUT	VCC	Fan 1 control output. This pin provides PWM duty-cycle output or a voltage output.
100	FANIN2	$IN_{st,5v}$	VCC	Fan 2 tachometer input.
101	FANCTL2	$OD_{12,5v}$ AOUT	VCC	Fan 2 control output. This pin provides PWM duty-cycle output or a voltage output.
90	D2+	AIN	AVCC	Thermal diode/transistor temperature sensor input.
91	D1+(CPU)	AIN	AVCC	CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.
92	VREF	AOUT	AVCC	Voltage reference output.
71	BEEP	OD_{24}	VSB	Beep pin.
	GPIO16	I/OOD_{12t}		General purpose IO.
72	PECI	I/O_{8t}	VSB	PECI interface pin.
	GPIO17	I/OOD_{12t}		General purpose IO.
75	OVT#	$OD_{12,5v}$	VSB	Over temperature signal output.
85	COPEN#	$IN_{st,5v}$	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss.

6.7 SPI, GPIO, SIR

Pin No.	Pin Name	Type	PWR	Description
52	GPIO00	I/OOD_{12t}	VSB	General purpose IO.
	SPI_CLK	O_{12}		Serial clock output pin for SPI device.
53	GPIO01	I/OOD_{12t}	VSB	General purpose IO.
	SPI_CS0#	OD_{12}		Connect this pin to primary BIOS chip select pin.
54	GPIO02	I/OOD_{12t}	VSB	General purpose IO.
	SPI_MISO	$IN_{t,5v}$		SPI master in/slave out pin.
55	GPIO03	I/OOD_{12t}	VSB	General purpose IO.
	SPI_MOSI	O_{12}		SPI master out/slave in pin.
56	GPIO04	I/OOD_{12t}	VSB	General purpose IO.
	FWH_DIS	O_{12}		Firmware hub disable
57	GPIO05	I/OOD_{12t}	VSB	General purpose IO.
	SOUT6_1	O_{12}		UART Serial Output. Used to transmit serial data out to the communication link.

	IRTX_1	O_{12}		Infrared Transmitter Output.
58	GPIO06	I/OOD_{12t}	VSB	General purpose IO.
	SIN6_1	$IN_{t,5v}$		UART Serial Input. Used to receive serial data through the communication link.
	IRRX_1	$IN_{t,5v}$		Infrared Receiver input.
59	GPIO07	I/OOD_{12t}	VSB	General purpose IO.
	RTS6_1#	O_{12}		UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
65	GPIO10	I/OOD_{12t}	VSB	General purpose IO.
	LED_VSB	OD_{12}		Power LED for VSB.
66	GPIO11	I/OOD_{12t}	VSB	General purpose IO.
	LED_VCC	OD_{12}		Power LED for VCC.
67	GPIO12	I/OOD_{12t}	VSB	General purpose IO.
	SCL	I/OOD_{12t}		SMBus Clock.
	SOUT5	O_{12}		UART Serial Output. Used to transmit serial data out to the communication link.
68	GPIO13	I/OOD_{12t}	VSB	General purpose IO.
	SDA	I/OOD_{12t}		SMBus Data.
	SIN5	$IN_{t,5v}$		UART Serial Output. Used to transmit serial data out to the communication link.
69	GPIO14	I/OOD_{12t}	VSB	General purpose IO.
	RTS5#	O_{12}		UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.

6.8 ACPI Function Pins

Pin No.	Pin Name	Type	PWR	Description
70	WDTRST#	$OD_{12,5v}$	VSB	Watch dog timer signal output.
	GPIO15	I/OOD_{12t}		General purpose IO.
76	ALERT#	OD_{12}	VSB	Alert a signal when temperature over limit setting.
	GPIO20	I/OOD_{12t}		General purpose IO.
74	PME#	$OD_{12,5v}$	VSB	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up.
77	ATXPG_IN	$IN_{st,5v}$	VSB	ATX Power Good input.
	GPIO21	I/OOD_{12t}		General purpose IO.
78	PWSIN#	$IN_{st,5v}$	VSB	Main power switch button input.
	GPIO22	I/OOD_{12t}		General purpose IO.
79	PWSOUT#	OD_{12}	VSB	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
	GPIO23	I/OOD_{12t}		General purpose IO.
80	S3#	$IN_{st,5v}$	VSB	S3# Input is Main power on-off switch input.
	GPIO24	I/OOD_{12t}		General purpose IO.

81	PS_ON#	$OD_{12\text{-}5v}$	VSB	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
	GPIO25	I/OOD_{12t}		General purpose IO.
82	PWROK	OD_{12}	VBAT	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V.
	GPIO26	I/OOD_{12t}		General purpose IO.
83	RSMRST#	OD_{12}	VBAT	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 2.8V.
	GPIO27	I/OOD_{12t}		General purpose IO.

6.9 KBC Function

Pin No.	Pin Name	Type	PWR	Description
34	KBRST#	$OD_{16,u10,5V}$	VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms.
35	GA20	$OD_{16,u10,5V}$	VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms.
63	KDATA	$I/OD_{16t,5V}$	VSB	PS/2 Keyboard Data.
64	KCLK	$I/OD_{16t,5V}$	VSB	PS/2 Keyboard Clock.
61	MDATA	$I/OD_{16t,5V}$	VSB	PS/2 Mouse Data.
62	MCLK	$I/OD_{16t,5V}$	VSB	PS/2 Mouse Clock.

6.10 RTC Function

Pin No.	Pin Name	Type	PWR	Description
86	RTC_X1	AIN	RTC_VBAT	RTC 32.768KHz crystal input.
87	RTC_X2	AOUT	RTC_VBAT	RTC 32.768KHz crystal output.

7. Function Description

7.1. Power on Strapping Option

The F81865 provides six pins for power on hardware strapping to select required functions. See below table for the detail:

Pin No.	Symbol	Value	Description
4	FWH_TRAP	1	FWH as a primary BIOS
		0	SPI as a primary BIOS
123	PWM_Duty	1	Power on fan speed default duty is 60%. (Default)
		0	Power on fan speed default duty is 100%.
7	SPI_TRAP	1	SPI function disable(Default)
		0	SPI function enable
124	I2C_ADDR	1	The I2C slave address is 8'h5C (Default)
		0	The I2C slave address is 8'h5A
126	Config4E_2E	1	Configuration Register I/O port is 4E/4F. (Default)
		0	Configuration Register I/O port is 2E/2F.
5	PWM_DC	1	Fan control mode: PWM mode. (Default)
		0	Fan control mode: DAC mode.

7.2. FDC

The Floppy Disk Controller provides the interface between a host processor and one floppy disk drive. It integrates a controller and a digital data separator with write pre-compensation, data rate selection logic, microprocessor interface, and a set of registers. The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, 1 Mbps and 2 Mbps. It operates in PC/AT mode.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD. The controller manages data transfers using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution, and Result. Not all commands utilize all these three phases.

The below content is about the FDC device register descriptions. All the registers are for software porting reference.

Status Register A (PS/2 mode) — Base + 0

Bit	Name	R/W	Default	Description
7	INTPEND	R	0	This bit indicates the state of the interrupt output.
6	DRV2_N	R	-	0: a second drive has been installed. 1: a second drive has not been installed.

5	STEP	R	0	This bit indicates the complement of STEP# disk interface output.
4	TRK0_N	R	-	This bit indicates the state of TRK0# disk interface input.
3	HDSEL	R	0	This bit indicates the complement of HDSEL# disk interface output. 0: side 0. 1: side 1.
2	INDEX_N	R	-	This bit indicates the state of INDEX# disk interface input.
1	WPT_N	R	-	This bit indicates the state of WPT# disk interface input. 0: disk is write-protected. 1: disk is not write-protected.
0	DIR	R	0	This bit indicates the complement of DIR# disk interface output.

Status Register A (Model 30 mode) — Base + 0

Bit	Name	R/W	Default	Description
7	INTPEND	R	0	This bit indicates the state of the interrupt output.
6	DRQ	R	0	This bit indicates the state of the DRQ signal.
5	STEP_FF	R	0	This bit indicates the complement of latched STEP# disk interface output.
4	TRK0	R	-	This bit indicates the complement of TRK0# disk interface input.
3	HDSEL_N	R	1	This bit indicates the state of HDSEL# disk interface output. 0: side 0. 1: side 1.
2	INDEX	R	-	This bit indicates the complement of INDEX# disk interface input.
1	WPT	R	-	This bit indicates the complement of WPT# disk interface input. 0: disk is write-protected. 1: disk is not write-protected.
0	DIR_N	R	1	This bit indicates the state of DIR# disk interface output. 0: head moves in inward direction. 1: head moves in outward direction.

Status Register B (PS/2 Mode) — Base + 1

Bit	Name	R/W	Default	Description
7-6	Reserved	R	11	Reserved. Return 11b when read.
5	DR0	R	0	Drive select 0. This bit reflects the bit0 of Digital Output Register.
4	WDATA	R	0	This bit changes state at every rising edge of WDATA#.
3	RDATA	R	0	This bit changes state at every rising edge of RDATA#.
2	WGATE	R	0	This bit indicates the complement of WGATE# disk interface output.
1	MOTEN1	R	0	This bit indicates the complement of MOB# disk interface output. Not support in this design.
0	MOTEN0	R	0	This bit indicates the complement of MOA# disk interface output.

Status Register B (Model 30 Mode) — Base + 1

Bit	Name	R/W	Default	Description
7	DRV2_N	R	-	0: a second drive has been installed. 1: a second drive has not been installed.

6	DSB_N	R	1	This bit indicates the state of DRVB# disk interface output. Not support in this design.
5	DSA_N	R	1	This bit indicates the state of DRVA# disk interface output.
4	WDATA_FF	R	0	This bit is latched at the rising edge of WDATA# and is cleared by a read from the Digital Input Register.
3	RDATA_FF	R	0	This bit is latched at the rising edge of RDATA# and is cleared by a read form the Digital Input Register.
2	WGATE_FF	R	0	This bit is latched at the falling edge of WGATE# and is cleared by a read from the Digital Input Register.
1	DSD_N	R	1	This bit indicates the complement of DRVD# disk interface output. Not support in this design.
0	DSC_N	R	1	This bit indicates the complement of DRVC# disk interface output. Not support in this design.

Digital Output Register — Base + 2

Bit	Name	R/W	Default	Description
7	MOTEN3	R	0	Motor enable 3. Not support in this design.
6	MOTEN2	R	0	Motor enable 2. Not support in this design.
5	MOTEN1	R/W	0	Motor enable 1. Used to control MOB#. MOB# is not support in this design.
4	MOTEN0	R/W	0	Motor enable 0. Used to control MOA#.
3	DAMEN	R/W	0	DMA enable. This bit has two mode of operation. PC-AT and Model 30 mode: write 1 will enable DMA and IRQ, write 0 will disable DMA and IRQ. PS/2 mode: This bit is reserved. DMA and IRQ are always enabled in PS/2 mode.
2	RESET	R	0	Write 0 to this bit will reset the controller. I will remain in reset condition until a 1 is written.
1	DSD_N	R	1	This bit indicates the complement of DRVD# disk interface output. Not support in this design.
0	DSC_N	R	1	This bit indicates the complement of DRVC# disk interface output. Not support in this design.

Tape Drive Register — Base + 3

Bit	Name	R/W	Default	Description
7-6	Reserved	R	00	Reserved. Return 00b when read.
5-4	TYPEID	R	11	Reserved in normal function, return 11b when read. If 3 mode FDD function is enabled. These bits indicate the drive type ID.
3-2	Reserved	R	11	Reserved. Return 11b when read in normal function. Return 00b when read in 3 mode FDD function.
1-0	TAPESEL	R/W	0	These bits assign a logical drive number to be a tape drive.

Main Status Register — Base + 4

Bit	Name	R/W	Default	Description
7	RQM	R	0	Request for Master indicates that the controller is ready to send or receive data from the uP through the FIFO.

6	DIO	R	0	Data I/O (direction): 0: the controller is expecting a byte to be written to the Data Register. 1: the controller is expecting a byte to be read from the Data Register.
5	NON_DMA	R	0	Non DMA Mode: 0: the controller is in DAM mode. 1: the controller is interrupt or software polling mode.
4	FDC_BUSY	R	0	This bit indicate that a read or write command is in process.
3	DRV3_BUSY	R	0	FDD number 3 is in seek or calibration condition. FDD number 3 is not support in this design.
2	DRV2_BUSY	R	0	FDD number 2 is in seek or calibration condition. FDD number 2 is not support in this design.
1	DRV1_BUSY	R	0	FDD number 1 is in seek or calibration condition. FDD number 1 is not support in this design.
0	DRV0_BUSY	R	0	FDD number 0 is in seek or calibration condition.

Data Rate Select Register — Base + 4

Bit	Name	R/W	Default	Description
7	SOFTRST	W	0	A 1 written to this bit will software reset the controller. Auto clear after reset.
6	PWRDOWN	W	0	A 1 to this bit will put the controller into low power mode which will turn off the oscillator and data separator circuits.
5	Reserved	-	-	Return 0 when read.
4-2	PRECOMP	W	000	Select the value of write precompensation: 250K-1Mbps / 2Mbps 000: default delays / default delays 001: 41.67ns / 20.8ns 010: 83.34ns / 41.17ns 011: 125.00ns / 62.5ns 100: 166.67ns / 83.3ns 101: 208.33ns / 104.2ns 110: 250.00ns / 125.00ns 111: 0.00ns (disabled) / 0.00ns (disabled) The default value of corresponding data rate: 250Kbps: 125ns 300Kbps: 125ns 500Kbps: 125ns 1Mbps: 41.67ns 2Mbps: 20.8ns
1-0	DRATE	W	10	Data rate select: MFM / FM 00: 500Kbps / 250Kbps 01: 300Kbps / 150Kbps 10: 250Kbps / 125Kbps 11: 1Mbps / illegal

Data (FIFO) Register — Base + 5

Bit	Name	R/W	Default	Description
7-0	DATA	R/W	00h	The FIFO is used to transfer all commands, data and status between controller and the system. The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. The FIFO is default disabled and could be enabled via the CONFIGURE command.

Status Registers 0

Bit	Name	R/W	Default	Description
7-6	IC	R	-	Interrupt code : 00: Normal termination of command. 01: Abnormal termination of command. 10: Invalid command. 11: Abnormal termination caused by poling.
5	SE	R	-	Seek end. Set when a SEEK or RECALIBRATE or a READ or WRITE with implied seek command is completed.
4	EC	R	-	Equipment check. 0: No error 1: When a fault signal is received form the FDD or the TRK0# signal fails to occur after 77 step pulses.
3	NR	R	-	Not ready. 0: Drive is ready 1: Drive is not ready.
2	HD	R	-	Head address. The current head address.
1-0	DS	R	-	Drive select. 00: Drive A selected. 01: Drive B selected. 10: Drive C selected. 11: Drive D selected.

Status Registers 1

Bit	Name	R/W	Default	Description
7	EN	R	-	End of Track. Set when the FDC tries to access a sector beyond the final sector of a cylinder.
6	DE	R	-	Data Error. The FDC detect a CRC error in either the ID field or the data field of a sector.
4	OR	R	-	Overrun/Underrun. Set when the FDC is not serviced by the host system within a certain time interval during data transfer.
3	Reserved	-	-	Unused. This bit is always “0”
2	ND	R	-	No Data. Set when the following conditions occurred: 1. The specified sector is not found during any read command. 2. The ID field cannot be read without errors during a READ ID command. 3. The proper sector sequence cannot be found during a READ TRACK command.
1	NW	R	-	No Writable Set when WPT# is active during execution of write commands.

0	MA	R	-	Missing Address Mark. Set when the following conditions occurred: 1. Cannot detect an ID address mark at the specified track after encountering the index pulse form the INDEX# pin twice. 2. Cannot detect a data address mark or a deleted data address mark on the specified track.

Status Registers 2

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Unused. This bit is always “0”.
6	CM	R	-	Control Mark. Set when following conditions occurred: 1. Encounters a deleted data address mark during a READ DATA command. 2. Encounters a data address mark during a READ DELETED DATA command.
5	DD	R	-	Data Error in Data Field. The FDC detects a CRC error in the data field.
4	WC	R	-	Wrong Cylinder. Set when the track address from the sector ID field is different from the track address maintained inside the FDC.
3	SE	R	-	Scan Equal. Set if the equal condition is satisfied during execution of the SCAN command.
2	SN	R	-	Scan Not Satisfied. Set when the FDC cannot find a sector on the track which meets the desired condition during any scan command.
1	BC	R	-	Bad Cylinder. The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FFh which indicates a bad track.
0	MD	R	-	Missing Data Address Mark. Set when the FDC cannot detect a data address mark or a deleted data address mark.

Status Registers 3

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Unused. This bit is always “0”.
6	WP	R	-	Write Protect. Indicates the status of WPT# pin.
5	Reserved	R	-	Unused. This bit is always “1”.
4	T0	R	-	Track 0. Indicates the status of the TRK0# pin.
3	Reserved.	R	-	Unused. This bit is always “1”.
2	HD	R	-	Head Address. Indicates the status of the HDSEL# pin.
1	DS1	R	-	Drive Select. These two bits indicate the DS1, DS0 bits in the command phase.
0	DS0	R	-	

Digital Input Register (PC-AT Mode) — Base + 7

Bit	Name	R/W	Default	Description
7	DSKCHG	R	-	This bit indicates the complement of DSKCHG# disk interface input.
6-0	Reserved	R	-	Reserved.

Digital Input Register (PS/2 Mode) — Base + 7

Bit	Name	R/W	Default	Description
7	DSKCHG	R	-	This bit indicates the complement of DSKCHG# disk interface input.
6-3	Reserved	-	-	Reserved.
2-1	DRATE	R	10	These bits indicate the status of the DRATE programmed through the Data Rate Select Register or Configuration Control Register.
0	HIGHDEN_N	R	1	0: 1Mbps or 500Kbps data rate is chosen. 1: 300Kbps or 250Kbps data rate is chosen.

Digital Input Register (Model 30 Mode) — Base + 7

Bit	Name	R/W	Default	Description
7	DSKCHG_N	R	-	This bit indicates the state of DSKCHG# disk interface input.
6-4	Reserved	-	-	Reserved.
3	DMAEN	R	0	This bit reflects the DMA bit in Digital Output Register.
2	NOPRE	R	0	This bit reflects the NOPRE bit in Configuration Control Register.
1-0	DRATE	R	10	These bits indicate the status of DRATE programmed through the Data Rate Select Register or Configuration Control Register.

Configuration Control Register (PC-AT and PS/2 Mode) — Base + 7

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	DRATE	W	10	These bit determine the data rate of the floppy controller. See DRATE bits in Data Rate Select Register.

Configuration Control Register (Model 30 Mode) — Base + 7

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved.
2	NOPRE	W	0	This bit could be programmed through Configuration Control Register and be read through the bit 2 in Digital Input Register in Model 30 Mode. But it has no functionality.
1-0	DRATE	W	10	These bits determine the data rate of the floppy controller. See DRATE bits in Data Rate Select Register.

FDC Commands

Terminology:

C	Cylinder Number 0 -256
D	Data Pattern
DIR	Step Direction 0: step out 1: step in
DS0	Drive Select 0
DS1	Drive Select 1
DTL	Data Length
EC	Enable Count
EOT	End of Track
EFIFO	Enable FIFO 0: FIFO is enabled. 1: FIFO is disabled.
EIS	Enable Implied Seek
FIFOTHR	FIFO Threshold
GAP	Alters Gap Length
GPL	Gap Length
H/HDS	Head Address
HLT	Head Load Time
HUT	Head Unload Time
LOCK	Lock EFIFO, FIFOTHR, PTRTRK bits. Prevent these bits from being affected by software reset.
MFM	MFM or FM mode 0: FM 1: MFM
MT	Multi-Track
N	Sector Size Code. All values up to 07h are allowable. 00: 128 bytes 01: 256 bytes .. .. 07 16 Kbytes
NCN	New Cylinder Number
ND	Non-DMA Mode
OW	Overwritten
PCN	Present Cylinder Number
POLL	Polling disable 0: polling is enabled. 1: polling is disabled.
PRETRK	Precompensation Start Track Number
R	Sector address
RCN	Relative Cylinder Number
SC	Sector per Cylinder
SK	Skip deleted data address mark
SRT	Step Rate Time
ST0	Status Register 0
ST1	Status Register 1
ST2	Status Register 2
ST3	Status Register 3
WGATE	Write Gate alters timing of WE.

Read Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	SK	0	0	1	1	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution.
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

Read Deleted Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	SK	0	1	1	0	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								

	R	---------- C ----------	Sector ID information after command execution.
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

Read A Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	MFM	0	0	0	0	1	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system. FDD reads contents of all cylinders from index hole to EOT.
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution.
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

Read ID

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	MFM	0	0	1	0	1	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register.
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								

	R	---------- C ----------	Disk status after the command has been completed.
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

Verify

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	SK	1	0	1	1	0	Command code
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL/SC ----------								
Execution										No data transfer
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution.
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

Version

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

Write Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	0	0	0	1	0	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command
	W	---------- H ----------								

	W	---------- R ----------	execution
	W	---------- N ----------	
	W	---------- EOT ----------	
	W	---------- GPL ----------	
	W	---------- DTL ----------	
Execution			Data transfer between the FDD and system.
Result	R	---------- ST0 ----------	Status information after command execution.
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- C ----------	Sector ID information after command execution.
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

Write Deleted Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	0	0	1	0	0	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system.
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution.
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

Format A Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	MFM	0	0	1	1	0	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes/Sector
	W	---------- SC ----------								Sectors/Cylinder
	W	---------- GPL ----------								Gap 3 Length
	W	---------- D ----------								Data Pattern
Execution for each sector (repeat)	W	---------- C ----------								Input sector parameter.
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								

Recalibrate

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	0	1	1	1	Command code
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to track 0

Sense Interrupt Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								
	R	---------- PCN ----------								

Specify

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	0	0	1	1	Command code
	W	|---------- SRT ----------|				|---------- HUT ----------|			
	W	|---------- SRT ----------|							ND	

Seek

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	1	1	1	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution										Head positioned over proper cylinder on diskette

Configure

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	1	0	0	1	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	0	EIS	EFIFO	POLL	|---------- FIFOTHR ----------|				
	W	---------- PRETRK ----------								
Execution										Internal registers written

Relative Seek

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	1	DIR	0	0	1	1	1	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- RCN ----------								

Perpendicular Mode

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	1	0	0	1	0	Command code
	W	OW	0	D3	D2	D1	D0	GAP	WGATE	

Lock

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	LOCK	0	0	1	0	1	0	0	Command code
Result	R	0	0	0	LOCK	0	0	0	0	

Dumpreg

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	1	1	1	0	Command code
Result	R	---------- PCN (Drive 0) ----------								
	R	---------- PCN (Drive 0) ----------								

	R	---------- PCN (Drive 0) ----------	
	R	---------- PCN (Drive 0) ----------	
	R	|---------- SRT ----------| |---------- HUT ----------|	
	R	|---------- SRT ----------| ND	
	R	---------- SC/EOT ----------	
	R	LOCK 0 D3 D2 D1 D0 GAP WGATE	
	R	0 EIS EFIFO POLL |---------- FIFOTHR ----------|	
	R	---------- PRETRK ----------	

Sense Drive Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	0	1	0	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information abut disk drive

Invalid

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	---------- Invalid Codes ----------								FDC goes to standby state.
Result	R	---------- ST0----------								ST0 = 80h

7.3. UART

The F81865 provides up to 6 UART ports and supports IRQ sharing for system application. The UARTs are used to convert data between parallel format and serial format. They convert parallel data into serial format on transmission and serial format into parallel data on receiver side. The serial format is formed by one start bit, followed by five to eight data bits, a parity bit if programmed and one (1.5 or 2) stop bits. The UARTs include complete modem control capability and an interrupt system that may be software trailed to the computing time required to handle the communication link. They have FIFO mode to reduce the number of interrupts presented to the host. Both receiver and transmitter have a 16-byte FIFO.

The below content is about the UARTs device register descriptions. All the registers are for software porting reference.

Receiver Buffer Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	RBR	R	00h	The data received. Read only when LCR[7] is 0

Transmitter Holding Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	THR	W	00h	Data to be transmitted. Write only when LCR[7] is 0

Divisor Latch (LSB) — Base + 0

Bit	Name	R/W	Default	Description
7-0	DLL	R/W	01h	Baud generator divisor low byte. Access only when LCR[7] is 1.

Divisor Latch (MSB) — Base + 1

Bit	Name	R/W	Default	Description
7-0	DLM	R/W	00h	Baud generator divisor high byte. Access only when LCR[7] is 1.

Interrupt Enable Register (IER) — Base + 1

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	SM2	R/WC	0	This bit is used only in 9-bit mode and always returns “0” when 9-bit mode is disabled. 0: The receiver could receive data byte. 1: The receiver could only receive address byte and issue an interrupt when the address is received.
3	EDSSI	R/W	0	Enable Modem Status Interrupt. Access only when LCR[7] is 0.
2	ELSI	R/W	0	Enable Line Status Error Interrupt. Access only when LCR[7] is 0.
1	ETBFI	R/W	0	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR[7] is 0.
0	ERBFI	R/W	0	Enable Received Data Available Interrupt. Access only when LCR[7] is 0.

Interrupt Identification Register (IIR) — Base + 2

Bit	Name	R/W	Default	Description
7	FIFO_EN	R	0	0: FIFO is disabled 1: FIFO is enabled.
6	FIFO_EN	R	0	0: FIFO is disabled 1: FIFO is enabled.
5-4	Reserved	-	-	Reserved.
3-1	IRQ_ID	R	00	000: Interrupt is caused by Modem Status 001: Interrupt is caused by Transmitter Holding Register Empty 010: Interrupt is caused by Received Data Available. 110: Interrupt is caused by Character Timeout 011: Interrupt is caused by Line Status.
0	IRQ_PENDN	R	1	1: Interrupt is not pending. 0: Interrupt is pending.

FIFO Control Register — Base + 2

Bit	Name	R/W	Default	Description
7-6	RCV_TRIG	W	00	00: Receiver FIFO trigger level is 1. 01: Receiver FIFO trigger level is 4. 10: Receiver FIFO trigger level is 8. 11: Receiver FIFO trigger level is 14.
5-3	Reserved	-	-	Reserved.
2	CLRTX	R	0	Reset the transmitter FIFO.
1	CLRRX	R	0	Reset the receiver FIFO.
0	FIFO_EN	R	0	0: Disable FIFO. 1: Enable FIFO.

Line Control Register (LCR) — Base + 3

Bit	Name	R/W	Default	Description
7	DLAB	R/W	0	0: Divisor Latch can't be accessed. 1: Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	0	0: Transmitter is in normal condition. 1: Transmit a break condition.
5	STKPAR	R/W	0	XX0: Parity Bit is disable 001: Parity Bit is odd. 011: Parity Bit is even 101: Parity Bit is logic 1 111: Parity Bit is logic 0
4	EPS	R/W	0	
3	PEN	R/W	0	
2	STB	R/W	0	0: Stop bit is one bit 1: When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit
1-0	WLS	R/W	00	00: Word length is 5 bit 01: Word length is 6 bit 10: Word length is 7 bit 11: Word length is 8 bit

MODEM Control Register (MCR) — Base + 4

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	LOOP	R/W	0	0: UART in normal condition. 1: UART is internal loop back
3	OUT2	R/W	0	0: All interrupt is disabled. 1: Interrupt is enabled (disabled) by IER.
2	OUT1	R/W	0	Read from MSR[6] while in loop back mode
1	RTS	R/W	0	0: RTS# is forced to logic 1 1: RTS# is forced to logic 0
0	DTR	R/W	0	0: DTR# is forced to logic 1 1: DTR# is forced to logic 0

Line Status Register (LSR) — Base + 5

Bit	Name	R/W	Default	Description
7	RCR_ERR	R	0	0: No error in the FIFO when FIFO is enabled 1: Error in the FIFO when FIFO is enabled.

6	TEMT	R	1	0: Transmitter is in transmitting. 1: Transmitter is empty.
5	THRE	R	1	0: Transmitter Holding Register is not empty. 1: Transmitter Holding Register is empty.
4	BI	R	0	0: No break condition detected. 1: A break condition is detected.
3	FE	R	0	0: Data received has no frame error. 1: Data received has frame error.
2	PE	R	0	0: Data received has no parity error. 1: Data received has parity error.
1	OE	R	0	0: No overrun condition occurred. 1: An overrun condition occurred.
0	DR	R	0	0: No data is ready for read. 1: Data is received.

MODEM Status Register (MSR) — Base + 6

Bit	Name	R/W	Default	Description
7	DCD	R	-	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	-	Complement of RI# input. In loop back mode , this bit is equivalent to OUT1 in MCR
5	DSR	R	-	Complement of DSR# input. In loop back mode , this bit is equivalent to DTR in MCR
4	CTS	R	-	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR
3	DDCD	R	0	0: No state changed at DCD#. 1: State changed at DCD#.
2	TERI	R	0	0: No Trailing edge at RI#. 1: A low to high transition at RI#.
1	DDSR	R	1	0: No state changed at DSR#. 1: State changed at DSR#.
0	DCTS	R	1	0: No state changed at CTS#. 1: State changed at CTS#.

Scratch Register — Base + 7

Bit	Name	R/W	Default	Description
7-0	SCR	R/W	00h	Scratch register.

7.4. Parallel Port

The parallel port in F81865 supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP) mode. Refer to the configuration registers for more information on selecting the mode of operation.

The below content is about the Parallel Port device register descriptions. All the registers are for software porting reference.

Parallel Port Data Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	DATA	R/W	00h	The output data to drive the parallel port data lines.

ECP Address FIFO Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	ECP_AFIFO	R/W	00h	Access only in ECP Parallel Port Mode and the ECP_MODE programmed in the Extended Control Register is 011. The data written to this register is placed in the FIFO and tagged as an Address/RLE. It is auto transmitted by the hardware. The operation is only defined for forward direction. It divide into two parts : Bit 7 : 0: bits 6-0 are run length, indicating how many times the next byte to appear (0 = 1time, 1 = 2times, 2 = 3times and so on). 1: bits 6-0 are ECP address. Bit 6-0 : Address or RLE depends on bit 7.

Device Status Register — Base + 1

Bit	Name	R/W	Default	Description
7	BUSY_N	R	-	Inverted version of parallel port signal BUSY.
6	ACK_N	R	-	Version of parallel port signal ACK#.
5	PERROR	R	-	Version of parallel port signal PE.
4	SELECT	R	-	Version of parallel port signal SLCT.
3	ERR_N	R	-	Version of parallel port signal ERR#.
2-1	Reserved	R	11	Reserved. Return 11b when read.
0	TMOUT	R	-	This bit is valid only in EPP mode. Return 1 when in other modes. It indicates that a 10uS time out has occurred on the EPP bus. 0: no time out error. 1: time out error occurred, write 1 to clear.

Device Control Register — Base + 2

Bit	Name	R/W	Default	Description
7-6	Reserved	-	11	Reserved. Return 11b when read.
5	DIR	R/W	0	0: the parallel port is in output mode. 1: the parallel port is in input mode. It is auto reset to 1 when in SPP mode.
4	ACKIRQ_EN	R/W	0	Enable an interrupt at the rising edge of ACK#.
3	SLIN	R/W	0	Inverted and then drives the parallel port signal SLIN#. When read, the status of inverted SLIN# is return.
2	INIT_N	R/W	0	Drives the parallel port signal INIT#. When read, the status of INIT# is return.
1	AFD	R/W	0	Inverted and then drives the parallel port signal AFD#. When read, the status of inverted AFD# is return.

0	STB	R/W	0	Inverted and then drives the parallel port signal STB#. When read, the status of inverted STB# is return.

EPP Address Register — Base + 3

Bit	Name	R/W	Default	Description
7-0	EPP_ADDR	R/W	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Address Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Address Read protocol.

EPP Data Register — Base + 4 – Base + 7

Bit	Name	R/W	Default	Description
7-0	EPP_DATA	R/W	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Data Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Data Read protocol.

Parallel Port Data FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	C_FIFO	R/W	00h	Data written to this FIFO is auto transmitted by the hardware to the device by using standard parallel port protocol. It is only valid in ECP and the ECP_MODE is 010b.The operation is only for forward direction.

ECP Data FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	ECP_DFIFO	R/W	00h	Data written to this FIFO when DIR is 0 is auto transmitted by the hardware to the device by using ECP parallel port protocol. Data is auto read from device into the FIFO when DIR is 1 by the hardware by using ECP parallel port protocol. Read the FIFO will return the content to the system. It is only valid in ECP and the ECP_MODE is 011b.

ECP Test FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	T_FIFO	R/W	00h	Data may be read, written from system to the FIFO in any Direction. But no hardware handshake occurred on the parallel port lines. It could be used to test the empty, full and threshold of the FIFO. It is only valid in ECP and the ECP_MODE is 110b.

ECP Configuration Register A — Base + 400h

Bit	Name	R/W	Default	Description
7	IRQ_MODE	R	0	0: interrupt is ISA pulse. 1: interrupt is ISA level. Only valid in ECP and ECP_MODE is 111b.

6-4	IMPID	R	001	000: the design is 16-bit implementation. 001: the design is 8-bit implementation (default). 010: the design is 32-bit implementation. 011-111: Reserved. Only valid in ECP and ECP_MODE is 111b.
3	Reserved	-	-	Reserved.
2	BYTETRAN_N	R	1	0: when transmitting there is 1 byte waiting in the transceiver that does not affect the FIFO full condition. 1: when transmitting the state of the full bit includes the byte being transmitted. Only valid in ECP and ECP_MODE is 111b.
1-0	Reserved	R	00	Return 00 when read. Only valid in ECP and ECP_MODE is 111b.

ECP Configuration Register B — Base + 401h

Bit	Name	R/W	Default	Description
7	COMP	R	0	0: only send uncompressed data. 1: compress data before sending. Only valid in ECP and ECP_MODE is 111b.
6	Reserved	R	1	Reserved. Return 1 when read. Only valid in ECP and ECP_MODE is 111b.
5-3	ECP_IRQ_CH	R	001	000: the interrupt selected with jumper. 001: select IRQ 7 (default). 010: select IRQ 9. 011: select IRQ 10. 100: select IRQ 11 101: select IRQ 14. 110: select IRQ 15. 111: select IRQ 5. Only valid in ECP and ECP_MODE is 111b.
2-0	ECP_DMA_CH	R	011	Return the DMA channel of ECP parallel port. Only valid in ECP and ECP_MODE is 111b.

Extended Control Register — Base + 402h

Bit	Name	R/W	Default	Description
7-5	ECP_MODE	R/W	000	000: SPP Mode. 001: PS/2 Parallel Port Mode. 010: Parallel Port Data FIFO Mode. 011: ECP Parallel Port Mode. 100: EPP Mode. 101: Reserved. 110: Test Mode. 111: Configuration Mode. Only valid in ECP.
4	ERRINTR_EN	R/W	0	0: disable the interrupt generated on the falling edge of ERR#. 1: enable the interrupt generated on the falling edge of ERR#.
3	DAMEN	R/W	0	0: disable DMA. 1: enable DMA. DMA starts when SERVICEINTR is 0.

2	SERVICEINTR	R/W	1	0: enable the following case of interrupt. DMAEN = 1: DMA mode. DMAEN = 0, DIR = 0: set to 1 whenever there are writeIntrThreshold or more bytes are free in the FIFO. DMAEN = 0, DIR = 0: set to 1 whenever there are readIntrThreshold or more bytes are valid to be read in the FIFO.
1	FIFOFULL	R	0	0: The FIFO has at least 1 free byte. 1: The FIFO is completely full.
0	FIFOEMPTY	R	0	0: The FIFO contains at least 1 byte. 1: The FIFO is completely empty.

7.5. Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60h. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system.

Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60h or 64h. Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is “0”.

Status Register

The status register is an 8-bit read-only register at I/O address 64h that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset.

3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Mouse Output Buffer	0: Muse output buffer empty 1: Mouse output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
<tr><td>AAh</td><td>Self-test
Return 55h if self test succeeds</td></tr>
<tr><td>ABh</td><td>keyboard Interface Test
8’h00: indicate keyboard interface is ok.
8’h01: indicate keyboard clock is low.
8’h02: indicate keyboard clock is high
8’h03: indicate keyboard data is low
8’h04: indicate keyboard data is high</td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
</table>

AEh	Enable Keyboard Interface
C0h	Read Input Port(P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into STATUS register
C2h	Continuously puts the upper four bits of Port1 into STATUS register
CAh	Read the data written by CBh command.
CBh	Written a scratch data. This byte could be read by CAh command.
D0h	Send Port2 value to the system
D1h	Only set/reset GateA20 line based on the system data bit 1
D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Low pulse on KBRST# about 6μS

KBC Command Description

PS/2 wakeup function

The KBC supports keyboard and mouse wakeup function. KBC will assert PME or PSOUT# signal. Those wakeup conditions are controlled by configuration register.

7.6. Hardware Monitor

7.6.1 General Description

Voltage

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.04V. Therefore the voltage under 2.04V (ex:1.5V) can be directly connected to these analog inputs. The voltage higher than 2.04V should be reduced by a factor with external resistors so as to obtain the input range. Only 3Vcc is an exception for it is main power of the F81865. Therefore 3Vcc can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F81865 and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V (See figure 7-1).

There are four voltage inputs in the F81865 and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ where V_{+12V} is the analog input voltage, for example.

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

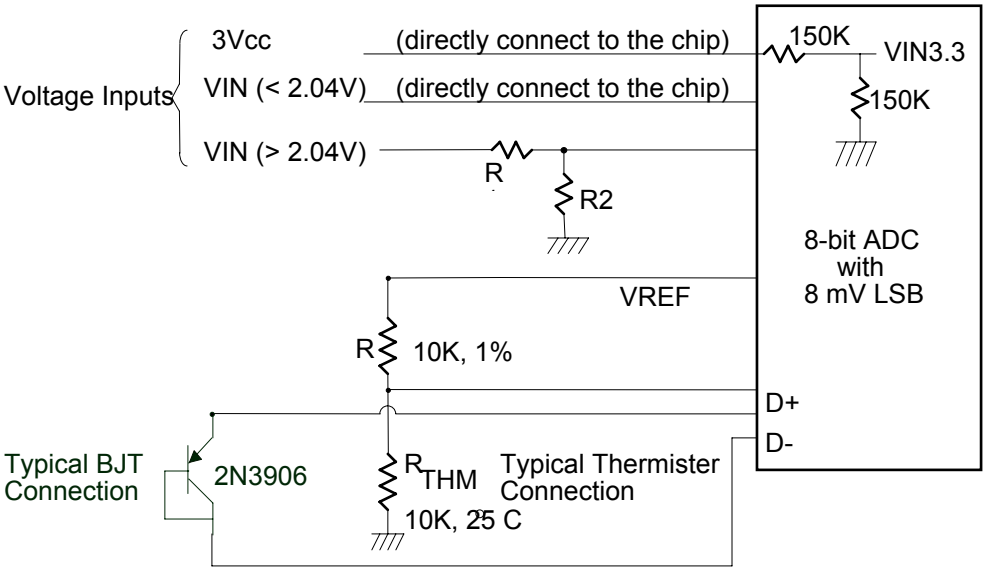


Fig 7-1

PME# interrupt for voltage is shown as figure 7-2. Voltage exceeding or going below high limit will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.

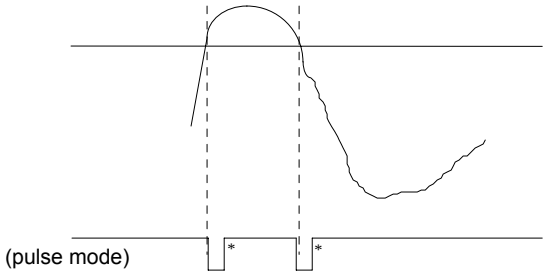


Fig 7-2

Temperature Sensor

The F81865 monitors two remote temperature sensors. These sensors can be measured from -40°C to 127°C (for thermal diode) & 0°C to 127°C (for thermistor). More detail please refer to the register description.

Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

(1) Monitor Temperature from "thermistor"

The F81865 can connect two thermistors to measure environment temperature or remote

temperature. The specification of thermistor should be considered to (1) β value is 3435K (2) resistor value is 10K ohm at 25°C. In the Figure 7-1, the thermistor is connected by a serial resistor with 10K ohm, then connected to VREF.

(2) Monitor Temperature from "thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F81865 is capable to these situations. The build-in reference table is for PNP 2N3906 transistor. In the Figure 7-1, the transistor is directly connected into temperature pins.

ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF or 3300pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

Over Temperature Signal (OVT#)

OVT# alert for temperature is shown as figure 7-3. When monitored temperature exceeds the over-temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.

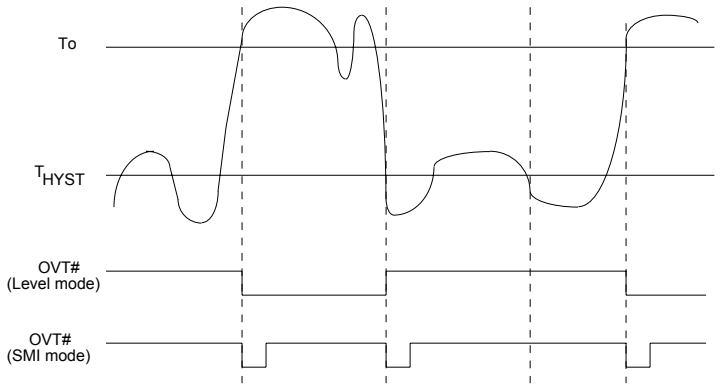
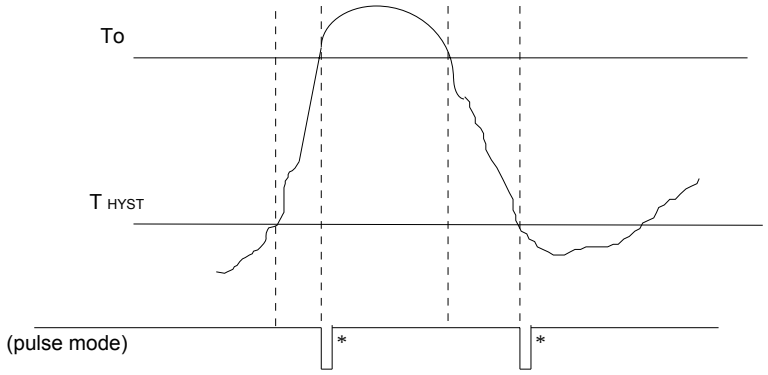


Fig 7-3

Temperature PME#

PME# interrupt for temperature is shown as figure 7-4. Temperature exceeding high limit or going below hysteresis will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

Fig 7-4

Fan

Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to:

$$\text{Count} = \frac{1.5 \times 10^6}{\text{RPM}}$$

In other words, the fan speed counter (12 bit resolution) has been read from register, the fan speed can be evaluated by the following equation.

$$\text{RPM} = \frac{1.5 \times 10^6}{\text{Count}}$$

As for fan, it would be best to use 2 pulses (4 phases fan) tachometer output per round. So the parameter “Count” under 5 bit filter is 4096~64 and RPM is 366~23438 based on the above equation. If using 8 phases fan, RPM would be from 183~11719.

Fan speed control

The F81865 provides 2 fan speed control methods:

1. DAC FAN CONTROL 2. PWM DUTY CYCLE

DAC Fan Control

The range of DC output is 0~VCC, controlled by 8-bit register. 1 LSB is about 0.013V (VCC=3.3V). The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = \text{VCC} \times \frac{\text{Programmed 8bit Register Value}}{256}$$

And the suggested application circuit for linear fan control would be:

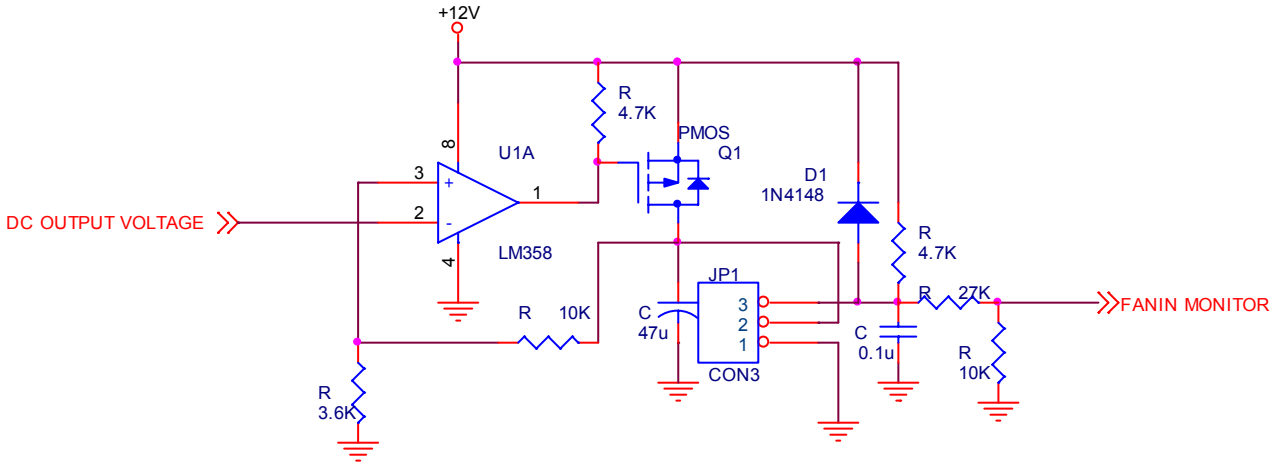


Fig 7-5

PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle(\%)} = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

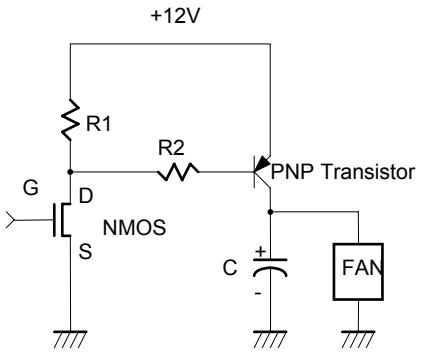


Fig 7-6

Fan speed control mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2.Stage auto mode, 3. Linear auto mode. More detail, please refer the description of registers.

Manual mode

For manual mode, it generally acts as software fan speed control.

Stage auto mode

At this mode, the F81865 provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F81865 can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take figure 7-7 as example. When temperature boundaries are set as 45, 55, 65, and 75°C and there are five intervals (each interval is 10° C). The related desired fan speed counts for each interval are 0500h, 0400h, 0300h, 0200h and 0100h. When the temperature is within 55~65°C, the fan speed count 300h will be load into FAN EXPECT COUNT that define in registers. Then, the F81865 will adjust PWMOUT duty-cycle to meet the expected value. It can be said that the fan will be turned on with a specific speed set by BIOS and automatically controlled with the temperature variation. The F81865 will take charge of all the fan speed control and need no for software support.

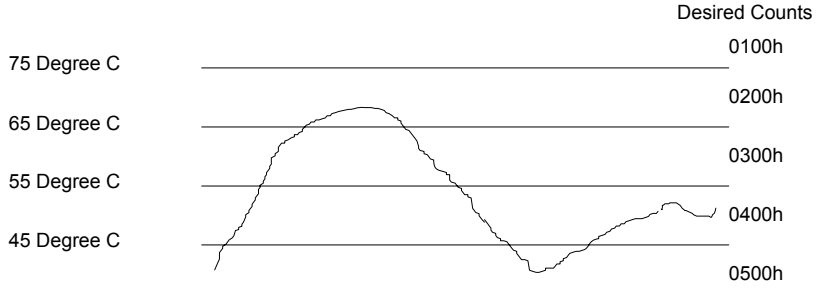
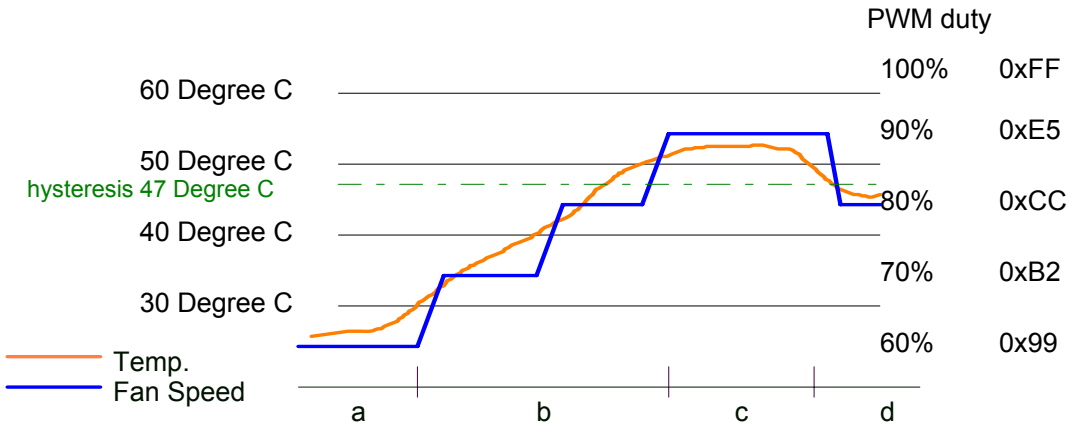


Figure 7-7

There are some examples as below:

A. Stage auto mode (PWM Duty)

Set temperature as 60°C, 50°C, 40°C, 30°C and Duty as 100%, 90%, 80%, 70%, 60%



a. Once temp. is under 30°C, the lowest fan speed keeps 60% PWM duty

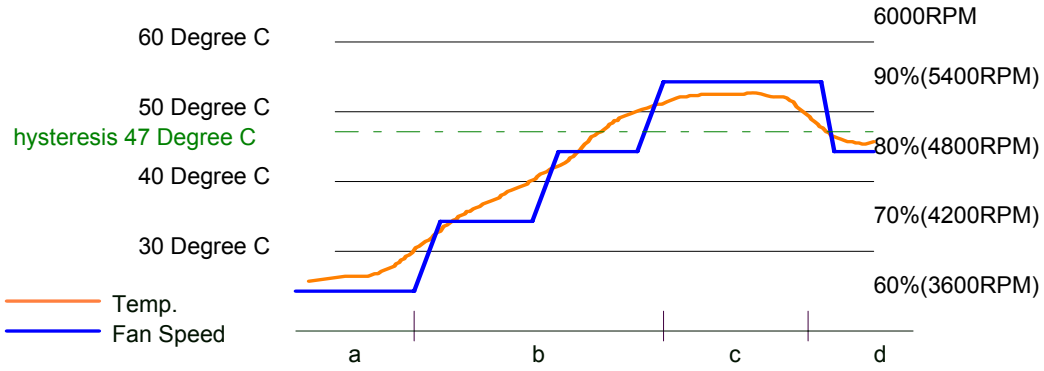
b. Once temp. is over 30°C,40°C,50°C, the fan speed will vary from 60% to 90% PWM duty and increase with temp. level.

c. Once temp. keeps in 55°C, fan speed keeps in 90% PWM duty

If set the hysteresis as 3°C (default 4°C), once temp reduces under 47°C, fan speed reduces to 80% PWM duty and stays there.

B. Stage auto mode (RPM%)

Set temperature as 60°C, 50°C, 40°C, 30°C and assume the Full Speed is 6000 RPM, set 90% of full speed RPM(5400 RPM), 80%(4800 RPM), 70%(4200 RPM), 60%(3600 RPM) of full speed RPM



a. Once temp. is under 30°C, the lowest fan speed keeps 60% of full speed (3600RPM).

b. Once temp. is over 30°C,40°C,50°C, the fan speed will vary from 3600RPM to 5400RPM and increase with temp. level.

c. Once temp. keeps in 55°C, fan speed keeps in 90% of full speed (5400RPM)

d. If set the hysteresis as 3°C (default 4°C), once temp reduces under 47°C, fan speed reduces to 4800RPM and stays there.

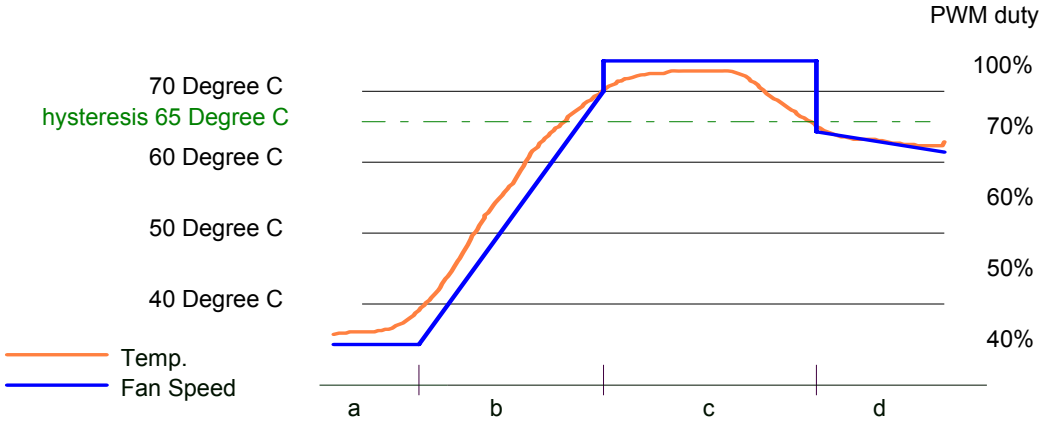
.

Linear auto mode

Furthermore, F81865 also supports linear auto mode. Below two examples describe this mode. More detail, please refer to the register description.

A. Linear auto mode (PWM Duty I)

Set temperature as 70°C, 60°C, 50°C, 40°C and Duty as 100%, 70%, 60%, 50%, 40%



a. Once temp. is under 40°C, the lowest fan speed keeps 40% PWM duty

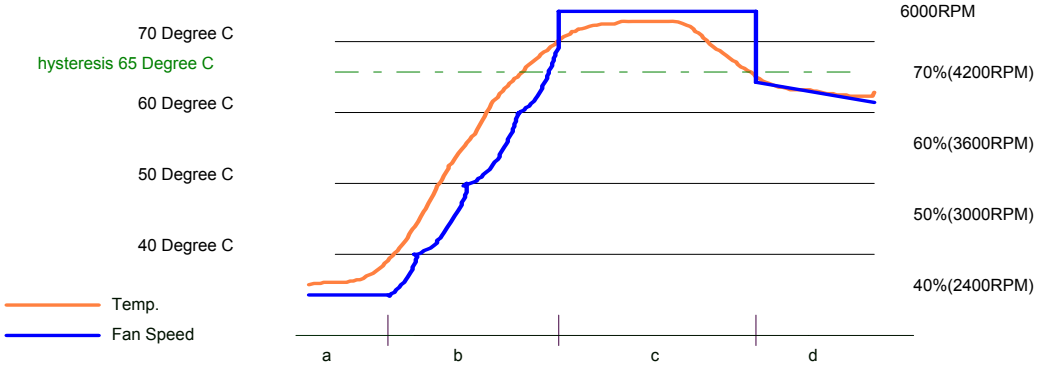
b. Once temp. is over 40°C,50°C,60°C, the fan speed will vary from 40% to 70% PWM duty and linearly increase with temp. variation. The temp.-fan speed monitoring and flash interval is 1sec.

c. Once temp. goes over 70°C, fan speed will directly increase to 100% PWM duty (full speed)

d. If set the hysteresis as 5°C(default is 4°C), once temp reduces under 65°C (not 70°C), fan speed reduces from 100% PWM duty and decrease linearly with temp..

B. Linear auto mode (RPM%)

Set temperature as 70°C, 60°C, 50°C, 40°C and if full speed is 6000RPM, setting 100%, 70%, 60%, 50%, 40% of full speed.



a. Once temp. is under 40°C, the lowest fan speed keeps 40% of full speed (2400RPM)

b. Once temp. is over 40°C,50°C,60°C, the fan speed will vary from 40% to 70% of full speed and almost linearly increase with temp. variation. The temp.-fan speed monitoring and flash interval is 1sec.

c. Once temp. goes over 70°C, fan speed will directly increase to full speed 6000RPM.

d. If set the hysteresis as 5°C, once temp reduces under 65°C (not 70°C), fan speed reduces from full speed and decrease linearly with temp..

PWMOUT Duty-cycle operating process

In both "Manual RPM" and "Temperature RPM" modes, the F81865 adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

1. When expected count is 0xFFF, PWMOUT duty-cycle will be set to 0x00 to turn off fan.
2. When expected count is 0x000, PWMOUT duty-cycle will be set to 0xFF to turn on fan with full speed.
3. If both (1) and (2) are not true,
   When PWMOUT duty-cycle decrease to MIN_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, the F81865 will keep duty-cycle at 00h for 1.6 seconds. After that, the F81865 starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the period, the F81865 will ignore it.

Fig 7-8

FAN_FAULT#

Fan_Fault# will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count on time. (Figure 7-9)

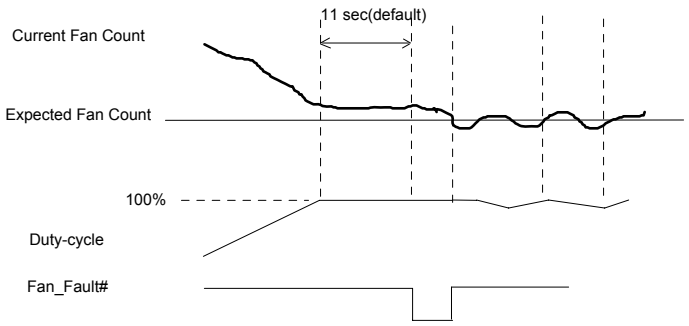


Fig 7-9

(2). After the period of detecting fan full speed, when PWM_Duty > Min. Duty, and fan count is still in 0xFFF.

7.6.2 Hardware Monitor Device Registers

Before the device registers, the following is a register map order which shows a summary of all registers. Please refer each register if you want more detail information.

Register CR01 ~ CR0E → Configuration Registers
Register CR10 ~ CR32 → Voltage Setting Register
Register CR60 ~ CR8F → Temperature Setting Register
Register CR90 ~ CRBF → Fan Control Setting Register
→Fan1 Detail Setting CRA0 ~ CRAF
→Fan2 Detail Setting CRB0 ~ CRBF

7.6.2.1Configuration Setting

Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7-3	Reserved	0h	0	Reserved
2	POWER_DOWN	R/W	0	Hardware monitor function power down.
1	FAN_START	R/W	1	Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.
0	V_T_START	R/W	1	Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.

Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7	DUMMY_REG	R/W	0	Dummy register.
6	CASE_BEEP_EN	R/W	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.
5-4	OVT_MODE	R/W	0	00: The OVT# will be level mode. 01: The OVT# will be 500us pulse mode (SMI). 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	DUMMY_REG	R/W	0	Dummy register.
2	CASE_PME_EN	R/W	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

Configuration Register — Index 03h

Bit	Name	R/W	Default	Description
7-1	Reserved	R/W	0	Reserved
0	CASE_STS	R/W	0	Case open event status, write 1 to clear if case open event cleared.

CPU Temperature Measure Method Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-6	Reserved	R/W	0	Reserved.
5	T1_IIR_EN	R/W	0	Set one to enable the IIR filter when CPU measure mode is PECI

4	Reserved	R/W	0	Reserved.
3-2	VTT_SEL	R/W	0	This register is used to select the output voltage for PECI. 00: 1.23V 01: 1.13V 10: Reserved. 11: 1.00V
1-0	MEAS_TYPE	R/W	0	This register selects the method for measuring the CPU temperature. 00: normal diode. 01: PECI 10: Reserved. 11: Reserved.

CPU Select Register — Index 0Bh

Bit	Name	R/W	Default	Description
7-4	CPU_SEL	R/W	0	Each bit indicates one CPU. Set only one bit at a time.
3-1	Reserved	R/W	0	Reserved.
0	DOMAIN	R/W	0	Set one to enable getting dual core CPU temperature.

TCC Temperature Register — Index 0Ch

Bit	Name	R/W	Default	Description
0	TCC_TEMP	R/W	0x55	This indicates the TCC temperature for the PECI. The absolute temperature is achieved by adding the reading from PECI to this register.

PECI Slope Control Register — Index 0Eh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	PECI_ADD	R/W	0	Refer to PECI_SCALE.
2-0	PECI_SCALE	R/W	0	This register accompany with PECI_ADD defines the PECI reading slope. (PECI_READ indicates the reading for host, PECI_TMP indicates the reading from PECI in the following description) When PECI_ADD is 0: 000: PECI_READ = PECI_TMP. 001: PECI_READ = PECI_TMP - 1/2* (PECI_TMP). 010: PECI_READ = PECI_TMP - 1/4* (PECI_TMP). 011: PECI_READ = PECI_TMP - 1/8* (PECI_TMP). 100: PECI_READ = PECI_TMP - 1/16* (PECI_TMP). 101: PECI_READ = PECI_TMP - 1/32* (PECI_TMP). 110: PECI_READ = PECI_TMP - 1/64* (PECI_TMP). 111: PECI_READ = PECI_TMP - 1/128* (PECI_TMP). When PECI_ADD is 1: 000: PECI_READ = PECI_TMP. 001: PECI_READ = PECI_TMP + 1/2* (PECI_TMP). 010: PECI_READ = PECI_TMP + 1/4* (PECI_TMP). 011: PECI_READ = PECI_TMP + 1/8* (PECI_TMP). 100: PECI_READ = PECI_TMP + 1/16* (PECI_TMP). 101: PECI_READ = PECI_TMP + 1/32* (PECI_TMP). 110: PECI_READ = PECI_TMP + 1/64* (PECI_TMP). 111: PECI_READ = PECI_TMP + 1/128* (PECI_TMP).

7.6.2.2 Voltage Setting

Voltage PME Enable Register — Index 10h

Bit	Name	R/W	Default	Description
7-2	Reserved	R/W	0	Reserved.
1	VIN0_PME_EN	R/W	0	0: disable VIN0 PME. 1: enable VIN0 PME. See VIN0_EXC_STS for detail.
0	Reserved	R/W	0	Reserved.

Voltage Exceed Status Register — Index 11h

Bit	Name	R/W	Default	Description
7-2	Reserved	R/W	0	Reserved.
1	VIN0_EXC_STS	R/W	0	This bit records the change of VIN0 real time exceeding status. When VIN0 exceeds VIN0_HIGH_LIMIT or VIN0 returns to the normal range, this bit will be set to “1”. Write “1” to clear this bit.
0	Reserved	R/W	0	Return 0 when read.

Voltage Real Time Exceed Status Register — Index 12h

Bit	Name	R/W	Default	Description
7-2	Reserved	R/W	0	Reserved.
1	VIN0_EXC	R/W	0	0: VIN0 is less or equal than VIN0_HIGH_LIMIT. 1: VIN0 is great than VIN0_HIGH_LIMIT.
0	Reserved	R/W	0	Return 0 when read.

Voltage BEEP Enable Register — Index 13h

Bit	Name	R/W	Default	Description
7-2	Reserved	R/W	0	Reserved.
1	VIN0_BEEP_EN	R/W	0	0: disable VIN0 BEEP. 1: enable VIN0 BEEP. See VIN0_EXC for detail.
0	Reserved	R/W	0	Reserved.

Voltage reading and limit— Index 20h- 2Fh

Address	Attribute	Default Value	Description
20h	RO	--	VCC3V reading. The unit of reading is 16mV.
21h	RO	--	VIN0 (Vcore) reading. The unit of reading is 8mV.
22h	RO	--	VIN1 reading. The unit of reading is 8mV.
23h	RO	--	VIN2 reading. The unit of reading is 8mV.
24h	RO	--	VIN3 reading. The unit of reading is 8mV.
25h	RO	--	VSB3V reading. The unit of reading is 16mV.
26h	RO	--	VBAT reading. The unit of reading is 16mV.
29~2Fh	RO	FF	Reserved

Voltage VIN0 High Limit Register — Index 32h

Bit	Name	R/W	Default	Description
7-0	VIN1_HIGH_LIMIT	R/W	ffh	This defines the VIN1 voltage high limit.

7.6.2.3 Temperature Setting

Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	EN_ T2_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	Reserved	R/W	0	Reserved
3	Reserved	R/W	0	Reserved
2	EN_ T2_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R/W	0	Reserved

Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	T2_OVT _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
5	T1_OVT _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
4	Reserved	-	-	Reserved
3	Reserved	-	-	Reserved
2	T2_EXC _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
1	T1_EXC _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
0	Reserved	-	-	Reserved

Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	T2_OVT	R/W	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	Reserved	-	-	Reserved
3	Reserved	-	-	Reserved
2	T2_EXC	R/W	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	Reserved	-	-	Reserved

Temperature BEEP Enable Register — Index 63h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	EN_ T2_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	Reserved	R/W	0	Reserved
3	Reserved	R/W	0	Reserved
2	EN_ T2_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R/W	0	Reserved

OVT Output Enable Register 1 — Index 66h

Bit	Name	R/W	Default	Description
7	Reserved	R	0h	Reserved.
6	EN_T2_ALERT	R/W	0	Enable temperature alert (ALERT) mechanism of temperature2.
5	EN_T1_ALERT	R/W	1	Enable temperature alert (ALERT) mechanism of temperature1.
4	Reserved	R	0h	Reserved.
3	Reserved	R	0h	Reserved.
2	EN_T2_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	1	Enable over temperature (OVT) mechanism of temperature1.
0	Reserved	R	0h	Reserved.

Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Default	Description
7-4	Reserved	RO	0	--
3	Reserved	R	0h	--
2	T2_MODE	R/W	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	R	0h	--

TEMP1 Limit Hystersis Select Register -- Index 6Ch

Bit	Name	R/W	Default	Description
7-4	TEMP1_HYS	R/W	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	Reserved	R	0h	--

TEMP2 Limit Hystersis Select Register -- Index 6Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	R	0h	--
3-0	TEMP2_HYS	R/W	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

DIODE OPEN Status Register -- Index 6Fh

Bit	Name	R/W	Default	Description
7-4	Reserved	RO	0h	Reserved
3	Reserved	RO	0h	Reserved
2	T2_DIODE_OPEN	RO	0h	External diode 2 is open
1	T1_DIODE_OPEN	RO	0h	External diode 1 is open
0	Reserved	R	0h	--

Temperature — Index 70h- 8Fh

Address	Attribute	Default Value	Description
70h	Reserved	--	Reserved
71h	Reserved	--	Reserved
72h	RO	--	Temperature 1 reading (TEMP1). The unit of reading is 1°C.At the moment of reading this register.
73h	Reserved	--	Reserved
74h	RO	--	Temperature 2 reading (TEMP2). The unit of reading is 1°C.At the moment of reading this register.
75h	Reserved	--	Reserved
76h	Reserved	--	Reserved
77-7Bh	Reserved	--	Reserved
7C-7Fh	Reserved	--	Reserved
80h	Reserved	--	Reserved
81h	Reserved	--	Reserved
82h	R/W	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	55h	Temperature sensor 2 high limit. The unit is 1°C.
86h	Reserved	--	Reserved
87h	Reserved	--	Reserved
88-8Bh	Reserved	--	Reserved
8C~8Fh	Reserved	--	Reserved

7.6.2.4 Fan Control Setting

FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-2	Reserved	RO	0h	Reserved
1	EN_FAN2_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.

0	EN_FAN1_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Default	Description
7-2	Reserved	RO	0	Reserved
1	FAN2_STS	R/W	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
1	FAN2_EXC	RO	--	This bit set to high mean that fan2 count can't meet expect count over than PME time(CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	RO	--	This bit set to high mean that fan1 count can't meet expect count over than PME time(CR9F) or when duty not zero but fan stop over then 3 sec.

FAN BEEP# Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	FULL_WITH_T2_EN	R/W	0	Set this bit to one will trig all fans to full speed when T2 is over the high limit.
5	FULL_WITH_T1_EN	R/W	0	Set this bit to one will trig all fans to full speed when T1 is over the high limit.
4	Reserved	R/W	0	Reserverd
3	Reserved	RO	0	Reserved
2	Reserved	RO	0	Reserved
1	EN_FAN2_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.
0	EN_FAN1_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.

Fan Type Select Register -- Index 94h

Bit	Name	R/W	Default	Description
7-6	Reserved	--	--	Reserved.
5-4	Reserved	--	--	Reserved
3-2	FAN2_TYPE	R/W	2'b 0S	00: Output PWM mode (pushpull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved.
1-0	FAN1_TYPE	R/W	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved.

S: Register default values are decided by trapping.

Fan mode Select Register -- Index 96h

Bit	Name	R/W	Default	Description
7-6	Reserved	--	--	Reserved

5-4	Reserved	--	--	Reserved
3-2	FAN2_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xB6-0xBE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** (voltage) that defined in 0xB6-0xBE. 10: Manual mode fan control, user can write expect **RPM** count to 0xB2-0xB3, and F81865 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, it will output that value duty or voltage to controlled fan speed.
1-0	FAN1_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xA6-0xAE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expect **RPM** count to 0xA2-0xA3, and F81865 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, it will output that value duty or voltage to control fan speed.

Auto Fan1 and Fan2 Boundary Hystersis Select Register -- Index 98h

Bit	Name	R/W	Default	Description
7-4	FAN2_HYS	R/W	4h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	4h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Auto Fan1 and Fan2 Update Rate Select Register -- Index 9Bh

Bit	Name	R/W	Default	Description
7-6	Reserved	--	--	Reserved
5-4	Reserved	--	--	Reserved
3-2	FAN2_RATE_SEL	R/W	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_RATE_SEL	R/W	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Default	Description
7-4	FAN2_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

3-0	FAN1_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

Fan Fault Time Register -- Index 9Fh

Bit	Name	R/W	Default	Description
7-5	Reserved	--	--	Reserved.
4	START_DUTY_SEL	R/W	--	0: The power on fan speed is 100% 1: The power on fan speed is 60%. This bit is power on trap by FAN_100_60. Default is 60%.
3-0	FAN_PME_TIME	R/W	0Ah	This is the time value in second for the fan fault mechanism. If the duty is 100% in RPM mode and the fan speed can't exceed the expected value. After the time set by this byte, the fan fault will asserts if it is enabled.

Fan1 Index A0h- AFh

Address	Attribute	Default Value	Description
A0h	RO	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	8'hff	FAN1 count reading (LSB).
A2h~ A3h	Reserved	--	See index 96h
A4h	R/W	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	8'hff	FAN1 full speed count reading (LSB).

T1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Reserved
6-0	BOUND1TMP1	R/W	3Ch (60^oC)	The 1st BOUNDARY temperature for VT1 in temperature mode. When T1 temperature **exceeds** this boundary, FAN1 expect value will be in full speed. When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load the value calculated from segment2 index ABh.

T1 BOUNDARY 2 TEMPERATURE – Index A7

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Reserved
6-0	BOUND2TMP1	R/W	32h (50^oC)	The 2nd BOUNDARY temperature for VT1 in temperature mode. When T1 temperature exceeds this boundary, FAN1 expect value will load from segment 2 register (index ABh). When T1 temperature is below this boundary – hysteresis, FAN1 expect value will load from segment 3 register (index ACh).

T1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Reserved.

6-0	BOUND3TMP1	R/W	28h ($40^{o}C$)	The 3rd BOUNDARY temperature for VT1 in temperature mode. When T1 temperature exceeds this boundary, FAN1 expect value will load from segment 3 register (index ACh). When T1 temperature is below this boundary – hysteresis, FAN1 expect value will load from segment 4 register (index ADh).

T1 BOUNDARY 4 TEMPERATURE – Index A9

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Reserved.
6-0	BOUND4TMP1	R/W	1Eh ($30^{o}C$)	The 4th BOUNDARY temperature for VT1 in temperature mode. When T1 temperature **exceeds** this boundary, FAN1 expect value will load the value calculated from segment 4 (index ADh). When T1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **5** register (index AEh).

FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Default	Description
7-0	SEG1SPEED1	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Default	Description
7-0	SEG2SPEED1	R/W	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 3 SPEED COUNT – Index ACh

Bit	Name	R/W	Default	Description
7-0	SEG3SPEED1	R/W	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 4 SPEED COUNT – Index ADh

Bit	Name	R/W	Default	Description
7-0	SEG4SPEED1	R/W	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 5 SPEED COUNT – Index AEh

Bit	Name	R/W	Default	Description
7-0	SEG5SPEED1	R/W	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0	Reserved
5	FAN1_UP_T_EN	R/W	0	0: Fan1 speed still follows the T1. 1: Fan1 will load the full speed when any temperature exceeds its high limit.
4	FAN1_INTERPOLATION_EN	R/W	1	0: When T1 is in the range between BOUND1TMP1 and BOUND4TMP1, the fan expect is SEG2SPEED1. 1: When T1 is in the range between BOUND1TMP1 and BOUND4TMP1, the fan expect is calculated by the equation: fan expect = [(current TEMP – BOUND4TMP1)/(BOUDN1TMP1 – BOUND4TMP1)]*(SEG2SPEED1 – SEG5SPEED1) + SEG5SPEED1.
3	FAN1_JUMP_HIGH_EN	R/W	1	0: When T1 is over BOUND1TMP1, the duty cycle will increase one by one. 1: When T1 is over BOUND1TMP1, the duty cycle will directly jump to full speed.
2	FAN1_JUMP_LOW_EN	R/W	1	0: When T1 is over BOUND1TMP1, the duty cycle will decrease one by one. 1: When T1 is over BOUND1TMP1, the duty cycle will directly jump to the expect value.
1-0	Fan1_temp_sel	R/W	1	0: reserved. 1: fan1 follow temperature 1. 2: fan1 follow temperature 2. 3: reserved.

Fan2 Index B0h- BFh

Address	Attribute	Default Value	Description
B0h	RO	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	8'hff	FAN2 count reading (LSB).
B2h~B3h	Reserved	--	See index 96h
B4h	R/W	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	8'hff	FAN2 full speed count reading (LSB).

T2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND1TMP2	R/W	3Ch (60°C)	The 1st BOUNDARY temperature for VT2 in temperature mode. When T1 temperature **exceeds** this boundary, FAN2 expect value will be in full speed. When T2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load the value calculated from segment2 (index BBh).

T2 BOUNDARY 2 TEMPERATURE – Index B7

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND2TMP2	R/W	32 ($50^{o}C$)	The 2nd BOUNDARY temperature for VT2 in temperature mode. When T2 temperature exceeds this boundary, FAN2 expect value will load from segment 2 register (index BBh). When T2 temperature is below this boundary – hysteresis, FAN2 expect value will load from segment 3 register (index BCh).

T2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND3TMP2	R/W	28h ($40^{o}C$)	The 3rd BOUNDARY temperature for VT2 in temperature mode. When T2 temperature exceeds this boundary, FAN2 expect value will load from segment 3 register (index BCh). When T2 temperature is below this boundary – hysteresis, FAN2 expect value will load from segment 4 register (index BDh).

T2 BOUNDARY 4 TEMPERATURE – Index B9

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND4TMP2	R/W	1Eh ($30^{o}C$)	The 4^{th} BOUNDARY temperature for VT2 in temperature mode. When T2 temperature **exceeds** this boundary, FAN2 expect value will load the value calculated from segment2 (index BDh). When T2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **5** register (index BEh).

FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Default	Description
7-0	SEG1SPEED2	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%: full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Default	Description
7-0	SEG2SPEED2	R/W	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 3 SPEED COUNT – Index BCh

Bit	Name	R/W	Default	Description
7-0	SEG3SPEED2	R/W	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 4 SPEED COUNT – Index BDh

Bit	Name	R/W	Default	Description
7-0	SEG4SPEED2	R/W	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 5 SPEED COUNT – Index BEh

Bit	Name	R/W	Default	Description
7-0	SEG5SPEED2	R/W	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0	Reserved
5	FAN2_UP_T_EN	R/W	0	0: Fan2 speed still follows the T2. 1: Fan2 will load the full speed when any temperature exceeds its high limit.
4	FAN2_INTERPOLATION_EN	R/W	1	0: When T2 is in the range between BOUND1TMP2 and BOUND4TMP2, the fan expect is SEG2SPEED2. 1: When T2 is in the range between BOUND1TMP2 and BOUND4TMP2, the fan expect is calculated by the equation: fan expect = [(current TEMP – BOUND4TMP2)/(BOUDN1TMP2 – BOUND4TMP2)]*(SEG2SPEED2 – SEG5SPEED2) + SEG5SPEED2.
3	FAN2_JUMP_HIGH_EN	R/W	1	0: When T2 is over BOUND1TMP2, the duty cycle will increase one by one. 1: When T2 is over BOUND1TMP2, the duty cycle will directly jump to full speed.
2	FAN2_JUMP_LOW_EN	R/W	1	0: When T2 is over BOUND1TMP2, the duty cycle will decrease one by one. 1: When T2 is over BOUND1TMP2, the duty cycle will directly jump to the expect value.
1-0	Fan2_temp_sel	R/W	2	0: reserved. 1: fan1 follow temperature 1. 2: fan1 follow temperature 2. 3: reserved.

7.7. SPI Interface

Communication between the two devices is handling via the serial peripheral interface (SPI). Every SPI system consist of one master and one or more slaves, where a master provides the SPI clock and slave receives clock from the master.

This design is only master function, for basic signal, master-out/slave-in (MOSI), master-in/slave-out (MISO), serial clock (SCK), and 2 slaves select (SS), are needed for SPI interface. Each of slave select supports from 512kbits to 8Mbits flash is decided by configuration register. Serial clock (SCK) signal frequency is varied from 1.7MHz to 33MHz. The serial data (MOSI) for SPI interface translates to depend on SCK rising edge or falling edge is decided by

configuration register.

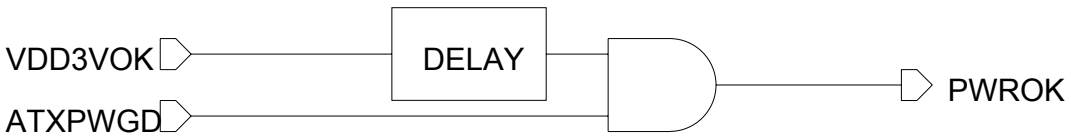
7.8. ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

There are 4 modes under power loss state via setting ACPI control register. The always on, always off, keep last state & bypass mode.. In keep last state mode, one register will latch the status before power loss. If it is power on before power loss, it will automatically power on when power is resumed. If it is power off before power loss, it will remain power off when power is resumed.

PWROK Signals



PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed via register (100ms ~ 400ms).

7.9. Watchdog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal is depend on register setting.

The time unit has two ways from 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Others, please refer the device register description as below.

Watchdog Timer Configuration Register 1— base address + 05h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.

5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

Watchdog Timer Configuration Register 2 — base address + 06h

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	Time of watchdog timer

Watchdog PME Control Register — base address + 0Ah

Bit	Name	R/W	Default	Description
7	WDT_PME	R	--	The PME Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5-1	Reserved	--	--	Reserved.
0	WDOUT_EN	R/W	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.

7.10. RTC Function

The RTC function is a full binary-coded decimal (BCD) low-power real time clock and calendar chip which provides seconds, minutes, hours, day, date, month, and year information. Functions can be upgraded flexibly for special MB system. More detail description and setting, please refer to the device register as below.

Seconds Register — Index 00h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6-0	SEC	R/W	00h	Seconds (SEC). To write this SEC, “SET” bit (CR0B[7]) must be set to 1.

Seconds Alarm Register — Index 01h

Bit	Name	R/W	Default	Description
7	SEC_ALARM_EN	R/W	0	Seconds Alarm Enable (SEC_ALARM_EN). To compare SEC_ALARM with SEC, this bit must be set to 1. If this bit is not set to 1, it means that you don’t care about second alarm.
6-0	SEC_ALARM	R/W	00h	Seconds Alarm (SEC_ALARM).

Minutes Register — Index 02h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6-0	MIN	R/W	00h	Minutes (MIN). To write MIN, “SET” bit (CR0B[7]) must be set to 1.

Minutes Alarm Register — Index 03h

Bit	Name	R/W	Default	Description
7	MIN_ALARM_EN	R/W	0	Minutes Alarm Enable. To compare MIN_ALARM with MIN, this bit must be set to 1. If this bit is not set to 1, it means that you don't care about minutes alarm.
6-0	MIN_ALARM	R/W	00h	Minutes Alarm (MIN_ALARM).

Hours Register — Index 04h

Bit	Name	R/W	Default	Description
7	PM_FLAG	R/W	0	PM Flag (PM_FLAG) This bit is used to indicate that hour is at AM or PM. It only makes sense when "M24" bit (CR0C[1]) is set to 0. To write this bit, "SET" bit (CR0C[7]) must be set to 1. 0: AM 1: PM
6	Reserved	R	0	Reserved
5-0	HRS	R/W	12h	Hours (HRS). To write HRS, "SET" bit (CR0C[7]) must be set to 1.

Hours Alarm Register — Index 05h

Bit	Name	R/W	Default	Description
7	HRS_ALARM_EN	R/W	0	Hours Alarm Enable (HRS_ALARM_EN) To compare HRS_ALARM/PM_ALARM with HRS/PM_FLAG, this bit must be set to 1. If this bit is not set to 1, it means that you don't care about hours alarm.
6	PM_ALARM	R/W	0	PM Flag Alarm (PM_ALARM)
5-0	HRS_ALARM	R/W	00h	Hours Alarm (HRS_ALARM).

Day of Week Register — Index 06h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	0	Reserved
2-0	WEEK	R/W	001b	Day of Week (WEEK). To write WEEK, "SET" bit (CR0C[7]) must be set to 1. 001: Sunday 010: Monday 011: Tuesday 100: Wednesday 101: Thursday 110: Friday 111: Saturday

Date of Month Register — Index 07h

Bit	Name	R/W	Default	Description
7-6	Reserved	R	0	Reserved
5-0	DOM	R/W	01h	Date of Month (DOM). To write DOM, "SET" bit (CR0C[7]) must be set to 1.

Month Register — Index 08h

Bit	Name	R/W	Default	Description
7-5	Reserved	R	0	Reserved
4-0	MTH	R/W	01h	Month (MTH). To write MTH, "SET" bit (CR0C[7]) must be set to 1.

Year Register — Index 09h

Bit	Name	R/W	Default	Description
7-0	YEAR	R/W	07h	Year (YEAR) To write YEAR, "SET" bit (CR0C[7]) must be set to 1.

Control Register 1 — Index 0Ah

Bit	Name	R/W	Default	Description
7	UIP	R	0	Update Cycle In Progress (UIP). UIP is cleared in the end of an update cycle and when "SET" (CR0C[7]) is 1.
6-4	Reserved	R/W	010b	Reserved
3-0	PIR	R/W	0000b	Periodic Interrupt Rate (PIR) 0000: NONE 0001: 16 kHz 0010: 8 kHz 0011: 4 kHz 0100: 2 kHz 0101: 1 kHz 0110: 512 Hz 0111: 256 Hz 1000: 128 Hz 1001: 64 Hz 1010: 32 Hz 1011: 16 Hz 1100: 8 Hz 1101: 4 Hz 1110: 2 Hz 1111: 1 Hz

Control Register 2 — Index 0Bh

Bit	Name	R/W	Default	Description
7	SET	R/W	0	Set Calendar Registers (SET) This bit must be set to 1 to enable writing calendar registers. When this bit is set, the calendar update process will be stop.
6	PIE	R/W	0	Periodic Interrupt Enable (PIE) The bit is set to 1 to enable the generation of interrupt by PF (CR0E[6]).
5	AIE	R/W	0	Alarm Interrupt Enable (AIE) This bit is set to 1 to enable the generation of interrupt by UF (CR0E[5]).
4	UIE	R/W	0	Update-Ended Interrupt Enable (UIE) This bit is set to 1 to enable the generation of interrupt by UF (CR0E[4])
3	Reserved	R	0	Reserved
2	DM	R/W	0	Data Mode (DM) 0: Binary Coded Decimal Mode (BCD mode) 1: Binary Mode
1	M24	R/W	0	24/12 Hours Mode (M24) 0: AM/PM 12 Hours Mode 1: 24 Hours Mode
0	DSE	R/W	0	Daylight Saving Enable (DSE) 0: Disable Special Updates 1: Enable Special Updates: (a) The last Sunday of April, the time increases from AM 01:59:59 to AM 03:00:00. (b) The last Sunday of October, the time decreases from AM 01:59:59 to AM 01:00:00

Status Register — Index 0Ch

Bit	Name	R/W	Default	Description
7	RTC_INT_N	R	1	RTC Interrupt Request Flag (RTC_INT_N). The interrupt request flag is set to 0 if one of the following cases are true: FP*PIE = "1" AF*AIE = "1" UF*UIE = "1"
6	PF	R	0	Periodic Interrupt Flag (PF) This bit is set to 1 when a rising edge is detected on the selected PIR clock. PF is set to 1 regardless of the state of PIE bit. This bit is cleared after CR0E is read.
5	AF	R	0	Alarm Interrupt Flag (AF) This bit is set to 1 when the current time has reached the alarm time. AF is set to 1 regardless of the state of AIE bit. This bit is cleared after CR0E is read.
4	UF	R	0	Update-Ended Interrupt Flag (UF) This bit is set to 1 after the end of each update cycle. UF is set to 1 regardless of the state of UIE bit. This bit is cleared after CR0E is read.
3-0	Reserved	R	0	Reserved

Data Valid Register — Index 0Dh

Bit	Name	R/W	Default	Description
7	DATA_VALID	R	1	Data Valid Flag (DATA_VALID) Read this bit in LSH0051A will always return 1.
6	DOM_ALARM_EN	R/W	0	Date of Month Alarm Enable (DOM_ALARM_EN). To compare DOM_ALARM with DOM, this bit must be set to 1. If this bit is not set to 1, it means that you don't care about date of month alarm.
5-0	DOM_ALARM	R/W	00h	Date of Month Alarm (DOM_ALARM).

RAM Data Register — Index 0Eh ~ IndexFFh (Total 242 Bytes)

8. Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87

-o 4e 87 (enable configuration)

-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer to each device chapter if you want more detail information.

Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
02	Software Reset Register	-	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register	0	0	0	0	0	1	1	1
21	Chip ID Register	0	0	0	0	0	1	0	0
23	Vender ID Register	0	0	0	1	1	0	0	1
24	Vender ID Register	0	0	1	1	0	1	0	0
25	I2C Address Select Register	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
26	Clock Select Register	0	-	-	0	-	-	-	0
27	ROM Address Select Register	0	0/1	1/0	1/0	0/1	0/1	0/1	0
28	GPIO4 Enable Register	0	0	0	0	0	0	0	0
29	GPIO3 Enable Register	0	0	0	0	0	0	0	0
2A-1	LED Mode Select Register	0	0	0	0	0	0	0	0
2A-2	Full UR5 UR6 Select	-	-	-	-	0	0	0	0
2B	GPIO1 Enable Register	0	0	0	1	1	1	1	1
2C	GPIO2 Enable Register	0	0	0	0	0	0	0	0
2D	Wakeup Control Register	0	-	-	-	1	0	0	0

Device Configuration Registers

"-" Reserved or Tri-State

FDC Device Configuration Registers (LDN CR00)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	FDC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	0
74	DMA Channel Select Register	-	-	-	-	-	0	1	0
F0	FDD Mode Register	-	-	-	0	1	1	1	0
F2	FDD Drive Type Register	-	-	-	-	-	-	1	1
F4	FDD Selection Register	-	-	-	0	0	-	0	0
Parallel Port Device Configuration Registers (LDN CR03)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB

30	Parallel Port Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	0	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	1
74	DMA Channel Select Register	-	-	-	0	-	0	1	1
F0	PRT Mode Select Register	-	1	0	0	0	0	1	0

Hardware Monitor Device Configuration Registers (LDN CR04)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

KBC Device Configuration Registers (LDN CR05)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	0
72	Mouse IRQ Channel Select Register	-	-	-	-	0	0	0	0
FE	PS/2 Swap Register	0	-	-	0	0	0	0	1
F0	User Wakeup Code	0	1	1	1	0	0	0	1

GPIO Device Configuration Registers (LDN CR06)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0
F1	GPIO0 Output Data Register	0	0	0	0	0	0	0	0
F2	GPIO0 Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO0 Drive Enable Register	0	0	0	0	0	0	0	0
F4	GPIO0 Mode Select 1 Register	0	0	0	0	0	0	0	0
F5	GPIO0 Mode Select 2 Register	0	0	0	0	0	0	0	0
F6	GPIO0 Pulse Width Select 1 Register	0	0	0	0	0	0	0	0
F7	GPIO0 Pulse Width Select 2 Register	0	0	0	0	0	0	0	0
F8	GPIO0 Interrupt Enable Register	0	0	0	0	0	0	0	0

F9	GPIO0 Interrupt Status Register	0	0	0	0	0	0	0	0
E0	GPIO1 Output Enable Register	0	0	0	0	0	0	0	0
E1	GPIO1 Output Data Register	1	1	1	1	1	1	1	1
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	0	0	0	0	0	0	0	0
EF	LED Mode Register	0	-	-	-	0	0	0	0
D0	GPIO2 Output Enable Register	0	0	0	0	0	0	0	0
D1	GPIO2 Output Data Register	1	1	1	1	1	1	1	1
D2	GPIO2 Pin Status Register	-	-	-	-	-	-	-	-
D3	GPIO2 Drive Enable Register	0	0	0	0	0	0	0	0
C0	GPIO3 Output Enable Register	0	0	0	0	0	0	0	0
C1	GPIO3 Output Data Register	1	1	1	1	1	1	1	1
C2	GPIO3 Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3 Drive Enable Register	0	0	0	0	0	0	0	0
B0	GPIO4 Output Enable Register	0	0	0	0	0	0	0	0
B1	GPIO4 Output Data Register	1	1	1	1	1	1	1	1
B2	GPIO4 Pin Status Register	-	-	-	-	-	-	-	-
B3	GPIO4 Drive Enable Register	0	0	0	0	0	0	0	0
A0	GPIO5 Output Enable Register	0	0	0	0	0	0	0	0
A1	GPIO5 Output Data Register	1	1	1	1	1	1	1	1
A2	GPIO5 Pin Status Register	-	-	-	-	-	-	-	-
A3	GPIO5 Drive Enable Register	0	0	0	0	0	0	0	0
90	GPIO6 Output Enable Register	-	-	-	0	0	0	0	0
91	GPIO6 Output Data Register	-	-	-	1	1	1	1	1
92	GPIO6 Pin Status Register	-	-	-	-	-	-	-	-
93	GPIO6 Drive Enable Register	-	-	-	0	0	0	0	0

WDT Device Configuration Registers (LDN CR07)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	WDT Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F5	WDT Control Register	0	0	0	0	0	0	0	0
F6	WDT Timer Register	0	0	0	0	0	0	0	0
FA	WDT PME Enable Register	0	0	-	-	-	-	-	0

SPI Device Configuration Registers (LDN CR08)

Register 0x[HEX]	Register Name	Default Value MSB							LSB

F0	SPI Control Register	0	0	0	1	0	0	0	0
F1	SPI Timeout Value Register	0	0	0	0	0	1	0	0
F2	SPI Baud Rate Divisor Register	-	-	-	-	-	0	0	1
F3	SPI Status Register	0	-	-	-	0	-	-	-
F4	SPI High Byte Data Register	0	0	0	0	0	0	0	0
F5	SPI Command Data Register	0	0	0	0	0	0	0	0
F6	SPI Chip Select Register	-	-	-	-	0	0	0	0
F7	SPI Memory Mapping Register	-	-	-	-	-	-	-	-
F8	SPI Operate Register	0	0	0	0	0	0	0	0
FA	SPI Low Byte Data Register	0	0	0	0	0	0	0	0
FB	SPI Address High Byte Register	0	0	0	0	0	0	0	0
FC	SPI Address Medium Byte Register	0	0	0	0	0	0	0	0
FD	SPI Address Low Byte Register	0	0	0	0	0	0	0	0
FE	SPI Program Byte Register	0	0	0	0	0	0	0	0
FF	SPI Write Data Register	0	0	0	0	0	0	0	0

PME and ACPI Device Configuration Registers (LDN CR0A)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	RTC Device Enable Register	-	-	-	-	-	-	-	0
F0	PME Event Enable 1 Register	-	0	0	0	0	0	0	0
F1	PME Event Enable 2 Register	-	-	0	0	0	0	0	0
F2	PME Event Status 1 Register	-	-	-	-	-	-	-	-
F3	PME Event Status 2 Register	-	-	-	-	-	-	-	-
F4	ACPI Control Register	0	0	0	0	0	1	1	0
F5	ACPI Control Register	-	0	0	1	1	1	0	0
F6	ACPI Control Register	0	0	0	0	0	0	0	0

RTC Device Configuration Registers (LDN CR0B)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	RTC Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

UART1 Device Configuration Registers (LDN CR10)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1

61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	Control Register	0	0	0	0	-	-	0	0
F2	Clock Select Register	-	-	-	-	-	-	0	0
F4	Slave Address Register	0	0	0	0	0	0	0	0
F5	Slave Address Enable Register	0	0	0	0	0	0	0	0

UART2 Device Configuration Registers (LDN CR11)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	Control Register	0	0	0	0	-	-	0	0
F2	Clock Select Register	-	-	-	-	-	-	0	0
F4	Slave Address Register	0	0	0	0	0	0	0	0
F5	Slave Address Enable Register	0	0	0	0	0	0	0	0

UART3 Device Configuration Registers (LDN CR12)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	0	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	Control Register	0	0	0	0	-	-	0	0
F2	Clock Select Register	-	-	-	-	-	-	0	0
F4	Slave Address Register	0	0	0	0	0	0	0	0
F5	Slave Address Enable Register	0	0	0	0	0	0	0	0

UART4 Device Configuration Registers (LDN CR13)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	0	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	Control Register	0	0	0	0	-	-	0	0
F2	Clock Select Register	-	-	-	-	-	-	0	0
F4	Slave Address Register	0	0	0	0	0	0	0	0

F5	Slave Address Enable Register	0	0	0	0	0	0	0	0

UART5 Device Configuration Registers (LDN CR14)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	Control Register	0	0	0	0	-	-	0	0
F2	Clock Select Register	-	-	-	-	-	-	0	0
F4	Slave Address Register	0	0	0	0	0	0	0	0
F5	Slave Address Enable Register	0	0	0	0	0	0	0	0

UART6 Device Configuration Registers (LDN CR15)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	Control Register	0	0	0	0	0	0	0	0
F1	IR Mode Register	-	-	-	0	0	0	0	0
F2	Clock Select Register	-	-	-	-	-	-	0	0
F4	Slave Address Register	0	0	0	0	0	0	0	0
F5	Slave Address Enable Register	0	0	0	0	0	0	0	0

8.1 Global Control Registers

8.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (VCC).

8.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 08h: Select SPI device configuration registers. 0Ah: Select PME & ACPI device configuration registers. 0Bh: Select RTC device configuration registers. 10h: Select UR1 device configuration registers. 11h: Select UR2 device configuration registers. 12h: Select UR3 device configuration registers. 13h: Select UR4 device configuration registers. 14h: Select UR5 device configuration registers. 15h: Select UR6 device configuration registers.

8.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	07h	Chip ID 1.

8.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	04h	Chip ID2.

8.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID 1.

8.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID 2.

8.1.7 I2C Address Select Register — Index 25h

Bit	Name	R/W	Default	Description
7-1	I2C_ADDR	R/W	-	The default value is determined by power on trap pin RTS1#. The default I2C address is 0x5C and 0x5A for pull-up and pull-down respective. By writing 0x07, 0x04 and then new I2C_ADDR, programmer could change the default I2C address. Write the same value again will disable the programmed I2C_ADDR and return to the default address. Caution: during the enable sequence, the EN_ARA_MODE will be also changed. User should program the correct value of EN_ARA_MODE after changing I2C_ADDR.

0	EN_ARA_MODE	R/W	0	0: disable I2C ARA. 1: enable I2C ARA.

8.1.8 Clock Select Register — Index 26h

Bit	Name	R/W	Default	Description
7	CLK24M_SEL	R/W	0	0: the CLKIN is 48MHz. 1: the CLKIN is 24MHz.
6-5	Reserved	-	-	Reserved.
4	SPI_TM_RST_SEL	R/W	0	SPI time out status reset source select: 0: reset by internal VDD3VOK. 1: reset by internal VSBOK. This bit is powered by VBAT.
3-1	Reserved	-	-	Reserved.
0	UR_GP_PROG_EN	R/W	0	This bit is used to select the Index 2Ah. 0: Index 2Ah is the LED Mode Select Register. 1: Index 2Ah is the Full UR5 UR6 Select Register.

8.1.9 ROM Address Select Register — Index 27h

Bit	Name	R/W	Default	Description
7	ROM_WR_EN	R/W	0	0: disable the memory write cycle, the memory write cycle will be ignored. 1: enable the memory write cycle.
6	SPI_EN	R/W	-	SPI enable: 0: the SPI is disabled. 1: the SPI is enabled. The default value is determined by the power on trap pin SOUT2. Pull down this pin to enable SPI. This bit is powered by VSB3V.
5	FWH_EN	R/W	-	FWH enable: 0: the FWH is disabled. 1: the FWH is enabled. The default value is determined by the power on trap pin DTR2#. Pull up this pin to enable FWH. Accompany with SPI_EN. BIOS system as below list:
4	PORT_4E_EN	R/W	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by SOUT1. Pull down to select port 2E/2F.

FWH_EN	SPI_EN	Description
1	x	This architecture uses FWH as primary BIOS
0	1	This architecture doesn't implement FWH and uses SPI as primary BIOS.

3	SEG_000E_EN	R/W	-	Memory address 0x000E_0000 to 0x000E_FFFF decode enable. 0: disable this range. 1: enable this range. The default value is determined by power on trap pin SOUT2. Pull down to enable this bit.
2	SEG_FFF8_EN	R/W	-	Memory address 0xFFF8_0000 to 0xFFFF_FFFF and 0x000F_0000 to 0x000F_FFFF decode enable. 0: disable these ranges. 1: enable these ranges. The default value is determined by power on trap pin SOUT2. Pull down to enable this bit.
1	SEG_FFEF_EN	R/W	-	Memory address 0xFFEE_0000 to 0xFFEF_FFFF decode enable. 0: disable this range. 1: enable this range. The default value is determined by power on trap pin SOUT2. Pull down to enable this bit.
0	SEG_FFF0_EN	R/W	0	Memory address 0xFFF0_0000 to 0xFFF7_FFFF decode enable. 0: disable this range. 1: enable this range.

8.1.10 GPIO4 Enable Register — Index 28h

Bit	Name	R/W	Default	Description
7	GPIO47_SEL	R/W	0	0: the function of SIN4/GPIO47 is SIN4. 1: the function of SIN4/GPIO47 is GPIO47.
6	GPIO46_SEL	R/W	0	0: the function of SOUT4/GPIO46 is SOUT4. 1: the function of SOUT4/GPIO47 is GPIO46.
5	GPIO45_SEL	R/W	0	0: the function of DSR4#/GPIO45 is DSR4#. 1: the function of DSR4#/GPIO45 is GPIO45.
4	GPIO44_SEL	R/W	0	0: the function of RTS4#/GPIO44 is RTS4#. 1: the function of RTS4#/GPIO44 is GPIO44.
3	GPIO43_SEL	R/W	0	0: the function of DTR4#/GPIO43 is DTR4#. 1: the function of DTR4#/GPIO43 is GPIO43.
2	GPIO42_SEL	R/W	0	0: the function of CTS4#/GPIO42 is CTS4#. 1: the function of CTS4#/GPIO42 is GPIO42.
1	GPIO41_SEL	R/W	0	0: the function of RI4#/GPIO41 is RI4#. 1: the function of RI4#/GPIO41 is GPIO41.
0	GPIO40_SEL	R/W	0	0: the function of DCD4#/GPIO40 is DCD4#. 1: the function of DCD4#/GPIO40 is GPIO40.

8.1.11 GPIO3 Enable Register — Index 29h

Bit	Name	R/W	Default	Description
7	GPIO37_SEL	R/W	0	0: the function of SIN3/GPIO37 is SIN3. 1: the function of SIN3/GPIO37 is GPIO37.

6	GPIO36_SEL	R/W	0	0: the function of SOUT3/GPIO36 is SOUT3. 1: the function of SOUT3/GPIO37 is GPIO36.
5	GPIO35_SEL	R/W	0	0: the function of DSR3#/GPIO35 is DSR3#. 1: the function of DSR3#/GPIO35 is GPIO35.
4	GPIO34_SEL	R/W	0	0: the function of RTS3#/GPIO34 is RTS3#. 1: the function of RTS3#/GPIO34 is GPIO34.
3	GPIO33_SEL	R/W	0	0: the function of DTR3#/GPIO33 is DTR3#. 1: the function of DTR3#/GPIO33 is GPIO33.
2	GPIO32_SEL	R/W	0	0: the function of CTS3#/GPIO32 is CTS3#. 1: the function of CTS3#/GPIO32 is GPIO32.
1	GPIO31_SEL	R/W	0	0: the function of RI3#/GPIO31 is RI3#. 1: the function of RI3#/GPIO31 is GPIO31.
0	GPIO30_SEL	R/W	0	0: the function of DCD3#/GPIO30 is DCD3#. 1: the function of DCD3#/GPIO30 is GPIO30.

8.1.12 LED Mode Select Register (UR_GP_PROG_EN = 0)— Index 2Ah (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7-6	VSBLED_SEL	R/W	2'b00	VSBLED function select. 00: VSBLED drives low. 01: VSBLED is tri-state. 10: VSBLED drives a 0.5HZ clock. 11: VSBLED drives a 1HZ clock. (Clock output is inversed with VCCLED clock output).
5-4	VCCLED_SEL	R/W	2'b00	VCCLED function select. 00: VCCLED drives low. 01: VCCLED is tri-state. 10: VCCLED drives a 0.5HZ clock. 11: VCCLED drives a 1HZ clock. (Clock output is inversed with VSBLED clock output).

<table>
<tr><td>3</td><td>FDC_GP_EN</td><td>R/W</td><td>0</td><td>FDC_GP_EN, UR6_FULL_EN, UR5_FULL_EN, UR6_ALT_EN, IR_ALT_EN and RTS6_ALT_EN will determine the functions of pin 9 to pin 21.
Pin 17 to pin 21
<table>
<tr><th>FDC_GP_EN</th><th>UR5_FULL_EN</th><th>UR6_FULL_EN</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>FDC inputs</td></tr>
<tr><td>X</td><td>1</td><td>X</td><td>UR5 Modem Control</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>GPIO60 ~ GPIO64</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>GPIO60 ~ GPIO64</td></tr>
</table>
Pin 12 to pin 16
<table>
<tr><th>FDC_GP_EN</th><th>UR5_FULL_EN</th><th>UR6_FULL_EN</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>FDC outputs</td></tr>
<tr><td>X</td><td>X</td><td>1</td><td>UR6 Modem Control</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>GPIO53 ~ GPIO57</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>GPIO53 ~ GPIO57</td></tr>
</table>
Pin 10 to pin 11
<table>
<tr><th>FDC_GP_EN</th><th>UR6_ALT_EN</th><th>IR_ALT_EN</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>FDC outputs*</td></tr>
<tr><td>X</td><td>1</td><td>X</td><td>SIN6_2/SOUT6_2</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>IRRX_2/IRTX_2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>GPIO51 ~ GPIO52</td></tr>
</table>
Pin 9
<table>
<tr><th>FDC_GP_EN</th><th>RTS6_ALT_EN</th><th></th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td></td><td>FDC outputs*</td></tr>
<tr><td>X</td><td>1</td><td></td><td>RTS6_2#</td></tr>
<tr><td>1</td><td>0</td><td></td><td>GPIO50</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
</table>
*When UR5_FULL_EN or UR6_FULL_EN is set to “1”, the pin function will become GPIOs.</td></tr>
<tr><td>2</td><td>UR6_GP_EN</td><td>R/W</td><td>0</td><td>This bit accompanying with IR_GP_EN will determine the function of GPIO05/SOUT6/IRTX and GPIO06/SIN6/IRRX.
<table>
<tr><th>UR6_GP_EN</th><th>IR_GP_EN</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>GPIO05/GPIO06</td></tr>
<tr><td>1</td><td>x</td><td>SOUT6_1/SIN6_1</td></tr>
<tr><td>0</td><td>1</td><td>IRTX_1/IRRX_1</td></tr>
</table></td></tr>
<tr><td>1</td><td>UR5_GP_EN</td><td>R/W</td><td>0</td><td>UR5 enable. (This bit affects the pin function only when GPIO12_SEL and GPIO13_SEL is “0”).
0: the function of GPIO12/SCL/SOUT5 and GPIO13/SDA/SIN5 will be determined by GPIO12_SEL and GPIO13_SEL.
1: the function of GPIO12/SCL/SOUT5 and GPIO13/SDA/SIN5 will be SOUT5 and SIN5 respectively if GPIO12_SEL and GPIO13_SEL is “0”.</td></tr>
<tr><td>0</td><td>IR_GP_EN</td><td>R/W</td><td>0</td><td>See UR6_GP_EN for detail.</td></tr>
</table>

8.1.13 Full UR5 UR6 Select Register (UR_GP_PROG_EN = 1) — Index 2Ah (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.

6	RTS6_2_ALT_EN	R/W	0	0: Set this bit "1" will enable RTS6_2# output from DENSEL#/GPIO50/RTS6_2#.
5	UR6_ALT_EN	R/W	0	0: Pin 10, Pin 11 will function as MOA#/GPIO51/IRRX_2 and DRVA#/GPIO52/IRTX_2 respectively. 1: Pin 10, Pin 11 will function as SIN6_2 and SOUT6_2 respectively.
4	IR_ALT_EN	R/W	0	This bit only has effect if UR6_ALT_EN is "0" 0: Pin 10, Pin 11 will function as MOA#/GPIO51 and DRVA#/GPIO52 respectively. 1: Pin 10, Pin 11 will function as IRRX_2 and IRTX_2 respectively. If IR_ALT_EN is set "1", the IR receiver input is determined by IRRX2_2.
3	UR6_FULL_EN	R/W	0	Set this bit will disable FDC and change the following pins to UR6 Modem control pins: WDATA# → DCD6# DIR# → RI6# STEP# → CTS6# HDSEL# → DTR6# WGATE# → DSR6# GPIO07 → RTS6# See FDC_GP_EN for other FDC pins' function.
2	RTS6_EN	R/W	0	Set this bit will enable RTS6# function. 0: GPIO07/RTS6# functions as GPIO07 1: GPIO07/RTS6# functions as RTS6#.
1	UR5_FULL_EN	R/W	0	Set this bit will disable FDC and change the following pins to UR5 Modem control pins: RDATA# → DCD5# TRK0# → RI5# INDEX# → CTS5# WPT# → DTR5# DSKCHG# → DSR5# GPIO14 → RTS5# See FDC_GP_EN for other FDC pins' function.
0	RTS5_EN	R/W	0	Set this bit will enable RTS5# function. 0: GPIO14/RTS5# functions as GPIO14 1: GPIO14/RTS5# functions as RTS5#.

8.1.14 GPIO1 Enable Register — Index 2Bh (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO17_SEL	R/W	0	0: the function of PECI/GPIO17 is PECI. 1: the function of PECI/GPIO17 is GPIO17.
6	GPIO16_SEL	R/W	0	0: the function of BEEP/GPIO16 is BEEP. 1: the function of BEEP/GPIO17 is GPIO16.
5	GPIO15_SEL	R/W	0	0: the function of WDTRST#/GPIO15 is WDTRST#. 1: the function of WDTRST#/GPIO15 is GPIO15.
4	GPIO14_SEL	R/W	1	Dummy register.
3	GPIO13_SEL	R/W	1	0: the function of GPIO13/SDA/SIN4 is SDA. 1: the function of GPIO13/SDA/SIN4 is GPIO13.

2	GPIO12_SEL	R/W	1	0: the function of GPIO12/SCL/SOUT4 is SCL. 1: the function of GPIO12/SCL/SOUT4 is GPIO12.
1	GPIO11_SEL	R/W	1	0: the function of GPIO11/VCCLED is VCCLED. 1: the function of GPIO11/VCCLED is GPIO11.
0	GPIO10_SEL	R/W	1	0: the function of GPIO10/VSBLED is VSBLED. 1: the function of GPIO10/VSBLED is GPIO10.

8.1.15 GPIO2 Enable Register — Index 2Ch (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO27_SEL	R/W	0	0: the function of RSMRST#/GPIO27 is RSMRST#. 1: the function of RSMRST#/GPIO27 is GPIO27.
6	GPIO26_SEL	R/W	0	0: the function of PWROK/GPIO26 is PWROK. 1: the function of PWROK/GPIO27 is GPIO26.
5	GPIO25_SEL	R/W	0	0: the function of PSON#/GPIO25 is PSON#. 1: the function of PSON#/GPIO25 is GPIO25.
4	GPIO24_SEL	R/W	0	0: the function of S3_IN#/GPIO25 is S3_IN#. 1: the function of S3_IN#/GPIO25 is GPIO25.
3	GPIO23_SEL	R/W	0	0: the function of PWSOUT#/GPIO23 is PWSOUT#. 1: the function of PWSOUT#/GPIO23 is GPIO23.
2	GPIO22_SEL	R/W	0	0: the function of PWSIN#/GPIO22 is PWSIN#. 1: the function of PWSIN#/GPIO22 is GPIO22.
1	GPIO21_SEL	R/W	0	0: the function of ATXPG/GPIO21 is ATXPG. 1: the function of ATXPG/GPIO21 is GPIO21.
0	GPIO20_SEL	R/W	0	0: the function of ALERT#/GPIO20 is ALERT#. 1: the function of ALERT#/GPIO20 is GPIO20.

8.1.16 Wakeup Control Register — Index 2Dh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6-4	Reserved	-	-	Reserved
3	WAKEUP_EN	R/W	1	0: disable KB/Mouse wakeup function. 1: enable KB/Mouse wakeup function.

<table>
<tr><td>2-1</td><td>KEY_SEL</td><td>R/W</td><td>00</td><td>Select the keyboard wakeup key. Accompany with KEY_SEL_ADD, there are several key select as list
<table>
<tr><th>KEY_SEL_ADD</th><th>KEY_SEL</th><th>Wake Key</th></tr>
<tr><td>0</td><td>00</td><td>Ctrl + Esc</td></tr>
<tr><td>0</td><td>01</td><td>Ctrl + F1</td></tr>
<tr><td>0</td><td>10</td><td>Ctrl + Space</td></tr>
<tr><td>0</td><td>11</td><td>Any Key</td></tr>
<tr><td>1</td><td>00</td><td>Windows Wakeup Key</td></tr>
<tr><td>1</td><td>01</td><td>Windows Power Key</td></tr>
<tr><td>1</td><td>10</td><td>Ctrl + Alt + Backspace</td></tr>
<tr><td>1</td><td>11</td><td>Ctrl + Alt + Delete</td></tr>
</table></td></tr>
<tr><td>0</td><td>MO_SEL</td><td>R/W</td><td>0</td><td>Select the mouse wakeup key.
0: Wakeup by mouse clicking.
1: Wakeup by mouse clicking or movement.</td></tr>
</table>

8.2 FDC Registers (CR00)

FDC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	FDC_EN	R/W	1	0: disable FDC. 1: enable FDC.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of FDC base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F0h	The LSB of FDC base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELFDCIRQ	R/W	06h	Select the IRQ channel for FDC.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved.
2-0	SELFDCDMA	R/W	010	Select the DMA channel for FDC.

FDD Mode Register — Index F0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	FDC_SW_WP	R/W	0	FDC Software Write Protect. 0: Write protect is determined by WPT# pin. 1: Enable Write Protect.

3-2	IF_MODE	R/W	11	00: Model 30 mode. 01: PS/2 mode. 10: Reserved. 11: AT mode (default).
1	FDMAMODE	R/W	1	0: enable burst mode. 1: non-busrt mode (default).
0	Reserved	R/W	0	Reserved.(Fintek test mode)

FDD Drive Type Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	FDD_TYPE	R/W	11	FDD drive type.

FDD Selection Register — Index F4h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4-3	FDD_DRT	R/W	00	Data rate table select, refer to table A. 00: select regular drives and 2.88 format. 01: reserved. 10: 2 mega tape. 11: reserved.
2	Reserved	-	-	Reserved.
1-0	FDD_DT	R/W	00	Drive type select, refer to table B.

TABLE A

Data Rate Table Select		Data Rate		Selected Data Rate		DENSEL
FDD_DRT[1]	FDD_DRT[0]	DATARATE1	DATARATE0	MFM	FM	
0	0	0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
0	1	0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
1	0	0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0
		1	1	1Meg	---	1

TABLE B

Drive Type		DRVDEN0	Remark
FDD_DT1	FDD_DT0		
0	0	DENSEL	4/2/1 MB 3.5” 2/1 MB 5.25” 1/1.6/1 MB 3.5” (3-Mode)
0	1	DATARATE1	
1	0	DENSEL#	
1	1	DATARATE0	

8.3 Parallel Port Registers (CR03)

Parallel Port Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PRT_EN	R/W	1	0: disable Parallel Port. 1: enable Parallel Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of Parallel Port base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	78h	The LSB of Parallel Port base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELPRTIRQ	R/W	7h	Select the IRQ channel for Parallel Port.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	ECP_DMA_MODE	R/W	0	0: non-burst mode DMA. 1: enable burst mode DMA.
3	Reserved	-	-	Reserved.
2-0	SELPRTDMA	R/W	011	Select the DMA channel for Parallel Port.

PRT Mode Select Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6-3	ECP_FIFO_THR	R/W	1000	ECP FIFO threshold.

2-0	PRT_MODE	R/W	010	000: Standard and Bi-direction (SPP) mode. 001: EPP 1.9 and SPP mode. 010: ECP mode (default). 011: ECP and EPP 1.9 mode. 100: Printer mode. 101: EPP 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP1.7 mode.

8.4 Hardware Monitor Registers (CR04)

Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

8.5 KBC Registers (CR05)

KBC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	KBC_EN	R/W	1	0: disable KBC. 1: enable KBC.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of KBC command port address. The address of data port is command port address + 4

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELKIRQ	R/W	0h	Select the IRQ channel for keyboard interrupt.

Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELMIRQ	R/W	0h	Select the IRQ channel for PS/2 mouse interrupt.

PS/2 Swap Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	AUTO_DET_EN	R/W	0	PS/2 auto detect enable. 0: disable auto detect. 1: enable auto detect, KB_MO_SWAP will be updated by hardware after LRESET# de-assert.
6-5	Reserved	-	-	Reserved
4	KB_MO_SWAP	R/W	0	Keyboard Mouse Swap. 0: Keyboard/Mouse is not swapped. 1: Keyboard/Mouse is swapped. This bit could be programmed by user. If AUTO_DET_EN is set, this bit is also updated by hardware.
3-0	KBC_TEST_BIT	R/W	1h	Fintek test mode bits.

8.6 GPIO Registers (CR06)

***Index Port = Base Address + 5**

GPIO Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	GPIO_EN	R/W	0	0: disable GPIO I/O port. 1: enable GPIO I/O port.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	GP_BASE_ADDR_HI	R/W	00h	The MSB of GPIO I/O port address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	GP_BASE_ADDR_LO	R/W	60h	The LSB of GPIO I/O port address.

GPIRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELGPIRQ	R/W	0h	Select the IRQ channel for GPIO interrupt.

GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	GPIO07_OE	R/W	0	0: GPIO07 is input. 1: GPIO07 is output.
6	GPIO06_OE	R/W	0	0: GPIO06 is input. 1: GPIO06 is output.
5	GPIO05_OE	R/W	0	0: GPIO05 is input. 1: GPIO05 is output.
4	GPIO04_OE	R/W	0	0: GPIO04 is input. 1: GPIO04 is output.
3	GPIO03_OE	R/W	0	0: GPIO03 is input. 1: GPIO03 is output.
2	GPIO02_OE	R/W	0	0: GPIO02 is input. 1: GPIO02 is output.
1	GPIO01_OE	R/W	0	0: GPIO01 is input. 1: GPIO01 is output.
0	GPIO00_OE	R/W	0	0: GPIO00 is input. 1: GPIO00 is output.

GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Default	Description
7	GPIO07_DATA	R/W	0	GPIO07 output data in output mode.
6	GPIO06_DATA	R/W	0	GPIO06 output data in output mode.
5	GPIO05_DATA	R/W	0	GPIO05 output data in output mode.
4	GPIO04_DATA	R/W	0	GPIO04 output data in output mode.
3	GPIO03_DATA	R/W	0	GPIO03 output data in output mode.
2	GPIO02_DATA	R/W	0	GPIO02 output data in output mode.
1	GPIO01_DATA	R/W	0	GPIO01 output data in output mode.
0	GPIO00_DATA	R/W	0	GPIO00 output data in output mode.

GPIO0 Pin Status Register — Index F2h

Bit	Name	R/W	Default	Description
7	GPIO07_ST	R	1	GPIO07 pin status.
6	GPIO06_ST	R	1	GPIO06 pin status.
5	GPIO05_ST	R	1	GPIO05 pin status.
4	GPIO04_ST	R	1	GPIO04 pin status.
3	GPIO03_ST	R	1	GPIO03 pin status.
2	GPIO02_ST	R	1	GPIO02 pin status.
1	GPIO01_ST	R	1	GPIO01 pin status.
0	GPIO00_ST	R	1	GPIO00 pin status.

GPIO0 Drive Enable Register — Index F3h

Bit	Name	R/W	Default	Description
7	GPIO07_DRV_EN	R/W	0	GPIO07 Drive Enable. 0: GPIO07 is open drain. 1: GPIO07 is push pull.
6	GPIO06_DRV_EN	R/W	0	GPIO06 Drive Enable. 0: GPIO06 is open drain. 1: GPIO06 is push pull.
5	GPIO05_DRV_EN	R/w	0	GPIO05 Drive Enable. 0: GPIO05 is open drain. 1: GPIO05 is push pull.
4	GPIO04_DRV_EN	R/W	0	GPIO04 Drive Enable. 0: GPIO04 is open drain. 1: GPIO04 is push pull.
3	GPIO03_DRV_EN	R/W	0	GPIO03 Drive Enable. 0: GPIO03 is open drain. 1: GPIO03 is push pull.
2	GPIO02_DRV_EN	R/W	0	GPIO02 Drive Enable. 0: GPIO02 is open drain. 1: GPIO02 is push pull.
1	GPIO01_DRV_EN	R/W	0	GPIO01 Drive Enable. 0: GPIO01 is open drain. 1: GPIO01 is push pull.
0	GPIO00_DRV_EN	R/W	0	GPIO00 Drive Enable. 0: GPIO00 is open drain. 1: GPIO00 is push pull.

GPIO0 Output Mode 1 Register — Index F4h

Bit	Name	R/W	Default	Description
7-6	GPIO03_MODE	R/W	00b	GPIO03 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO03_PW_SEL.
5-4	GPIO02_MODE	R/w	00b	GPIO02 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO02_PW_SEL.
3-2	GPIO01_MODE	R/W	00b	GPIO01 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO01_PW_SEL.

1-0	GPIO00_MODE	R/W	00b	GPIO00 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO00_PW_SEL.

GPIO0 Output Mode 2 Register — Index F5h

Bit	Name	R/W	Default	Description
7-6	GPIO07_MODE	R/W	00b	GPIO07 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO07_PW_SEL.
5-4	GPIO06_MODE	R/w	00b	GPIO06 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO06_PW_SEL.
3-2	GPIO05_MODE	R/W	00b	GPIO05 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO05_PW_SEL.
1-0	GPIO04_MODE	R/W	00b	GPIO04 output mode select: 00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode. The pulse width is determined by GPIO04_PW_SEL.

GPIO0 Pulse Width Select 1 Register — Index F6h

Bit	Name	R/W	Default	Description
7-6	GPIO03_PW_SEL	R/W	00b	GPIO03 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
5-4	GPIO02_PW_SEL	R/w	00b	GPIO02 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.

3-2	GPIO01_PW_SEL	R/W	00b	GPIO01 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
1-0	GPIO00_PW_SEL	R/W	00b	GPIO00 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.

GPIO0 Pulse Width Select 2 Register — Index F7h

Bit	Name	R/W	Default	Description
7-6	GPIO07_PW_SEL	R/W	00b	GPIO07 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
5-4	GPIO06_PW_SEL	R/w	00b	GPIO06 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
3-2	GPIO05_PW_SEL	R/W	00b	GPIO05 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
1-0	GPIO04_PW_SEL	R/W	00b	GPIO04 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.

GPIO0 Interrupt Enable Register — Index F8h

Bit	Name	R/W	Default	Description
7	GPIO07_INT_EN	R/W	0b	0: disable GPIO07 interrupt 1: enable GPIO07 interrupt when GPIO07_INT_ST is set.
6	GPIO06_INT_EN	R/W	0b	0: disable GPIO06 interrupt 1: enable GPIO06 interrupt when GPIO06_INT_ST is set.
5	GPIO05_INT_EN	R/W	0b	0: disable GPIO05 interrupt 1: enable GPIO05 interrupt when GPIO05_INT_ST is set.
4	GPIO04_INT_EN	R/W	0b	0: disable GPIO04 interrupt 1: enable GPIO04 interrupt when GPIO04_INT_ST is set.
3	GPIO03_INT_EN	R/W	0b	0: disable GPIO03 interrupt 1: enable GPIO03 interrupt when GPIO03_INT_ST is set.

2	GPIO02_INT_EN	R/W	0b	0: disable GPIO02 interrupt 1: enable GPIO02 interrupt when GPIO02_INT_ST is set.
1	GPIO01_INT_EN	R/W	0b	0: disable GPIO01 interrupt 1: enable GPIO01 interrupt when GPIO01_INT_ST is set.
0	GPIO00_INT_EN	R/W	0b	0: disable GPIO00 interrupt 1: enable GPIO00 interrupt when GPIO00_INT_ST is set.

GPIO0 Interrupt Status Register — Index F9h

Bit	Name	R/W	Default	Description
7	GPIO07_INT_ST	R/W	0b	This bit only works when GPIO07 is in input mode. 0: no change at GPIO07 input. 1: change had occurred at GPIO07 input. Write "1" to this bit to clear.
6	GPIO06_INT_ST	R/W	0b	This bit only works when GPIO06 is in input mode. 0: no change at GPIO06 input. 1: change had occurred at GPIO06 input. Write "1" to this bit to clear.
5	GPIO05_INT_ST	R/W	0b	This bit only works when GPIO05 is in input mode. 0: no change at GPIO05 input. 1: change had occurred at GPIO05 input. Write "1" to this bit to clear.
4	GPIO04_INT_ST	R/W	0b	This bit only works when GPIO04 is in input mode. 0: no change at GPIO04 input. 1: change had occurred at GPIO04 input. Write "1" to this bit to clear.
3	GPIO03_INT_ST	R/W	0b	This bit only works when GPIO03 is in input mode. 0: no change at GPIO03 input. 1: change had occurred at GPIO03 input. Write "1" to this bit to clear.
2	GPIO02_INT_ST	R/W	0b	This bit only works when GPIO02 is in input mode. 0: no change at GPIO02 input. 1: change had occurred at GPIO02 input. Write "1" to this bit to clear.
1	GPIO01_INT_ST	R/W	0b	This bit only works when GPIO01 is in input mode. 0: no change at GPIO01 input. 1: change had occurred at GPIO01 input. Write "1" to this bit to clear.
0	GPIO00_INT_ST	R/W	0b	This bit only works when GPIO00 is in input mode. 0: no change at GPIO00 input. 1: change had occurred at GPIO00 input. Write "1" to this bit to clear.

GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	GPIO17_OE	R/W	0	0: GPIO17 is in input mode. 1: GPIO17 is in output mode.

6	GPIO16_OE	R/W	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Default	Description
7	GPIO17_VAL	R/W	1	0: GPIO17 outputs 0 when in output mode. 1: GPIO17 outputs1 when in output mode.
6	GPIO16_VAL	R/W	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5	GPIO15_VAL	R/W	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_VAL	R/W	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Default	Description
7	GPIO17_IN	R	-	The pin status of GPIO17.
6	GPIO16_IN	R	-	The pin status of GPIO16.
5	GPIO15_IN	R	-	The pin status of GPIO15.
4	GPIO14_IN	R	-	The pin status of GPIO14.
3	GPIO13_IN	R	-	The pin status of GPIO13.
2	GPIO12_IN	R	-	The pin status of GPIO12.
1	GPIO11_IN	R	-	The pin status of GPIO11.
0	GPIO10_IN	R	-	The pin status of GPIO10.

GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Default	Description
7	GPIO17_DRV_EN	R/W	0	0: GPIO17 is open drain in output mode. 1: GPIO17 is push pull in output mode.
6	GPIO16_DRV_EN	R/W	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5	GPIO15_DRV_EN	R/W	0	0: GPIO15 is open drain in output mode. 1: GPIO15 is push pull in output mode.
4	GPIO14_DRV_EN	R/W	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode.
0	GPIO10_DRV_EN	R/W	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode.

LED S3 Mode Register — Index EFh

Bit	Name	R/W	Default	Description
7	LED_S3_MODE_EN	R/W	0	0: VSBLED_S3_MODE & VCCLED_S3_MODE are disabled. 1: VSBLED_S3_MODE & VCCLED_S3_MODE are enabled.
6-4	Reserved	-	-	Reserved.
3-2	VSBLED_S3_MODE	R/W	2'b00	VSBLED mode in S3 state. 00: VSBLED drives low. 01: VSBLED is tri-state. 10: VSBLED drives a 0.5HZ clock. 11: VSBLED drives a 1HZ clock. (Clock output is inversed with VCCLED clock output).
1-0	VCCLED_S3_MODE	R/W	2'b00	VCCLED mode in S3 state. 00: VCCLED drives low. 01: VCCLED is tri-state. 10: VCCLED drives a 0.5HZ clock. 11: VCCLED drives a 1HZ clock. (Clock output is inversed with VSBLED clock output).

GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Default	Description
7	GPIO27_OE	R/W	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	0	0: GPIO26 is in input mode. 1: GPIO26 is in output mode.
5	GPIO25_OE	R/W	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.

4	GPIO24_OE	R/W	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.
2	GPIO22_OE	R/W	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

GPIO2 Output Data Register — Index D1h

Bit	Name	R/W	Default	Description
7	GPIO27_VAL	R/W	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs1 when in output mode.
6	GPIO26_VAL	R/W	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs1 when in output mode.
5	GPIO25_VAL	R/W	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	1	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

GPIO2 Pin Status Register — Index D2h

Bit	Name	R/W	Default	Description
7	GPIO27_IN	R	-	The pin status of RSMRST#/GPIO27.
6	GPIO26_IN	R	-	The pin status of PWOK/GPIO26.
5	GPIO25_IN	R	-	The pin status of PS_ON#/GPIO25.
4	GPIO24_IN	R	-	The pin status of S3#/GPIO24.
3	GPIO23_IN	R	-	The pin status of PWSOUT#/GPIO23.
2	GPIO22_IN	R	-	The pin status of PWSIN#/GPIO22.
1	GPIO21_IN	R	-	The pin status of ATXPG_IN#/GPIO21.
0	GPIO20_IN	R	-	The pin status of ALERT#/GPIO20.

GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Default	Description
7	GPIO27_DRV_EN	R/W	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.

6	GPIO26_DRV_EN	R/W	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4	GPIO24_DRV_EN	R/W	0	0: GPIO24 is open drain in output mode. 1: GPIO24 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	0	0: GPIO23 is open drain in output mode. 1: GPIO23 is push pull in output mode.
2	GPIO22_DRV_EN	R/W	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.
1	GPIO21_DRV_EN	R/W	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Default	Description
7	GPIO37_OE	R/W	0	0: GPIO37 is input. 1: GPIO37 is output.
6	GPIO36_OE	R/W	0	0: GPIO36 is input. 1: GPIO36 is output.
5	GPIO35_OE	R/W	0	0: GPIO35 is input. 1: GPIO35 is output.
4	GPIO34_OE	R/W	0	0: GPIO34 is input. 1: GPIO34 is output.
3	GPIO33_OE	R/W	0	0: GPIO33 is input. 1: GPIO33 is output.
2	GPIO32_OE	R/W	0	0: GPIO32 is input. 1: GPIO32 is output.
1	GPIO31_OE	R/W	0	0: GPIO31 is input. 1: GPIO31 is output.
0	GPIO30_OE	R/W	0	0: GPIO30 is input. 1: GPIO30 is output.

GPIO3 Output Data Register — Index C1h

Bit	Name	R/W	Default	Description
7	GPIO37_DATA	R/W	1	GPIO37 output data in output mode.
6	GPIO36_DATA	R/W	1	GPIO36 output data in output mode.
5	GPIO35_DATA	R/W	1	GPIO35 output data in output mode.
4	GPIO34_DATA	R/W	1	GPIO34 output data in output mode.
3	GPIO33_DATA	R/W	1	GPIO33 output data in output mode.
2	GPIO32_DATA	R/W	1	GPIO32 output data in output mode.
1	GPIO31_DATA	R/W	1	GPIO31 output data in output mode.
0	GPIO30_DATA	R/W	1	GPIO30 output data in output mode.

GPIO3 Pin Status Register — Index C2h

Bit	Name	R/W	Default	Description
7	GPIO37_ST	R	1	GPIO37 pin status.
6	GPIO36_ST	R	1	GPIO36 pin status.
5	GPIO35_ST	R	1	GPIO35 pin status.
4	GPIO34_ST	R	1	GPIO34 pin status.
3	GPIO33_ST	R	1	GPIO33 pin status.
2	GPIO32_ST	R	1	GPIO32 pin status.
1	GPIO31_ST	R	1	GPIO31 pin status.
0	GPIO30_ST	R	1	GPIO30 pin status.

GPIO3 Drive Enable Register — Index C3h

Bit	Name	R/W	Default	Description
7	GPIO37_DRV_EN	R/W	0	GPIO37 Drive Enable. 0: GPIO37 is open drain. 1: GPIO37 is push pull.
6	GPIO36_DRV_EN	R/W	0	GPIO36 Drive Enable. 0: GPIO36 is open drain. 1: GPIO36 is push pull.
5	GPIO35_DRV_EN	R/w	0	GPIO35 Drive Enable. 0: GPIO35 is open drain. 1: GPIO35 is push pull.
4	GPIO34_DRV_EN	R/W	0	GPIO34 Drive Enable. 0: GPIO34 is open drain. 1: GPIO34 is push pull.
3	GPIO33_DRV_EN	R/W	0	GPIO33 Drive Enable. 0: GPIO33 is open drain. 1: GPIO33 is push pull.
2	GPIO32_DRV_EN	R/W	0	GPIO32 Drive Enable. 0: GPIO32 is open drain. 1: GPIO32 is push pull.
1	GPIO31_DRV_EN	R/W	0	GPIO31 Drive Enable. 0: GPIO31 is open drain. 1: GPIO31 is push pull.
0	GPIO30_DRV_EN	R/W	0	GPIO30 Drive Enable. 0: GPIO30 is open drain. 1: GPIO30 is push pull.

GPIO4 Output Enable Register — Index B0h

Bit	Name	R/W	Default	Description
7	GPIO47_OE	R/W	0	0: GPIO47 is input. 1: GPIO47 is output.
6	GPIO46_OE	R/W	0	0: GPIO46 is input. 1: GPIO46 is output.
5	GPIO45_OE	R/W	0	0: GPIO45 is input. 1: GPIO45 is output.

4	GPIO44_OE	R/W	0	0: GPIO44 is input. 1: GPIO44 is output.
3	GPIO43_OE	R/W	0	0: GPIO43 is input. 1: GPIO43 is output.
2	GPIO42_OE	R/W	0	0: GPIO42 is input. 1: GPIO42 is output.
1	GPIO41_OE	R/W	0	0: GPIO41 is input. 1: GPIO41 is output.
0	GPIO40_OE	R/W	0	0: GPIO40 is input. 1: GPIO40 is output.

GPIO4 Output Data Register — Index B1h

Bit	Name	R/W	Default	Description
7	GPIO47_DATA	R/W	1	GPIO47 output data in output mode.
6	GPIO46_DATA	R/W	1	GPIO46 output data in output mode.
5	GPIO45_DATA	R/W	1	GPIO45 output data in output mode.
4	GPIO44_DATA	R/W	1	GPIO44 output data in output mode.
3	GPIO43_DATA	R/W	1	GPIO43 output data in output mode.
2	GPIO42_DATA	R/W	1	GPIO42 output data in output mode.
1	GPIO41_DATA	R/W	1	GPIO41 output data in output mode.
0	GPIO40_DATA	R/W	1	GPIO40 output data in output mode.

GPIO4 Pin Status Register — Index B2h

Bit	Name	R/W	Default	Description
7	GPIO47_ST	R	1	GPIO47 pin status.
6	GPIO46_ST	R	1	GPIO46 pin status.
5	GPIO45_ST	R	1	GPIO45 pin status.
4	GPIO44_ST	R	1	GPIO44 pin status.
3	GPIO43_ST	R	1	GPIO43 pin status.
2	GPIO42_ST	R	1	GPIO42 pin status.
1	GPIO41_ST	R	1	GPIO41 pin status.
0	GPIO40_ST	R	1	GPIO40 pin status.

GPIO4 Drive Enable Register — Index B3h

Bit	Name	R/W	Default	Description
7	GPIO47_DRV_EN	R/W	0	GPIO47 Drive Enable. 0: GPIO47 is open drain. 1: GPIO47 is push pull.
6	GPIO46_DRV_EN	R/W	0	GPIO46 Drive Enable. 0: GPIO46 is open drain. 1: GPIO46 is push pull.
5	GPIO45_DRV_EN	R/w	0	GPIO45 Drive Enable. 0: GPIO45 is open drain. 1: GPIO45 is push pull.

4	GPIO44_DRV_EN	R/W	0	GPIO44 Drive Enable. 0: GPIO44 is open drain. 1: GPIO44 is push pull.
3	GPIO43_DRV_EN	R/W	0	GPIO43 Drive Enable. 0: GPIO43 is open drain. 1: GPIO43 is push pull.
2	GPIO42_DRV_EN	R/W	0	GPIO42 Drive Enable. 0: GPIO42 is open drain. 1: GPIO42 is push pull.
1	GPIO41_DRV_EN	R/W	0	GPIO41 Drive Enable. 0: GPIO41 is open drain. 1: GPIO41 is push pull.
0	GPIO40_DRV_EN	R/W	0	GPIO40 Drive Enable. 0: GPIO40 is open drain. 1: GPIO40 is push pull.

GPIO5 Output Enable Register — Index A0h

Bit	Name	R/W	Default	Description
7	GPIO57_OE	R/W	0	0: GPIO57 is input. 1: GPIO57 is output.
6	GPIO56_OE	R/W	0	0: GPIO56 is input. 1: GPIO56 is output.
5	GPIO55_OE	R/W	0	0: GPIO55 is input. 1: GPIO55 is output.
4	GPIO54_OE	R/W	0	0: GPIO54 is input. 1: GPIO54 is output.
3	GPIO53_OE	R/W	0	0: GPIO53 is input. 1: GPIO53 is output.
2	GPIO52_OE	R/W	0	0: GPIO52 is input. 1: GPIO52 is output.
1	GPIO51_OE	R/W	0	0: GPIO51 is input. 1: GPIO51 is output.
0	GPIO50_OE	R/W	0	0: GPIO50 is input. 1: GPIO50 is output.

GPIO5 Output Data Register — Index A1h

Bit	Name	R/W	Default	Description
7	GPIO57_DATA	R/W	1	GPIO57 output data in output mode.
6	GPIO56_DATA	R/W	1	GPIO56 output data in output mode.
5	GPIO55_DATA	R/W	1	GPIO55 output data in output mode.
4	GPIO54_DATA	R/W	1	GPIO54 output data in output mode.
3	GPIO53_DATA	R/W	1	GPIO53 output data in output mode.
2	GPIO52_DATA	R/W	1	GPIO52 output data in output mode.
1	GPIO51_DATA	R/W	1	GPIO51 output data in output mode.
0	GPIO50_DATA	R/W	1	GPIO50 output data in output mode.

GPIO5 Pin Status Register — Index A2h

Bit	Name	R/W	Default	Description
7	GPIO57_ST	R	1	GPIO57 pin status.
6	GPIO56_ST	R	1	GPIO56 pin status.
5	GPIO55_ST	R	1	GPIO55 pin status.
4	GPIO54_ST	R	1	GPIO54 pin status.
3	GPIO53_ST	R	1	GPIO53 pin status.
2	GPIO52_ST	R	1	GPIO52 pin status.
1	GPIO51_ST	R	1	GPIO51 pin status.
0	GPIO50_ST	R	1	GPIO50 pin status.

GPIO5 Drive Enable Register — Index A3h

Bit	Name	R/W	Default	Description
7	GPIO57_DRV_EN	R/W	0	GPIO57 Drive Enable. 0: GPIO57 is open drain. 1: GPIO57 is push pull.
6	GPIO56_DRV_EN	R/W	0	GPIO56 Drive Enable. 0: GPIO56 is open drain. 1: GPIO56 is push pull.
5	GPIO55_DRV_EN	R/w	0	GPIO55 Drive Enable. 0: GPIO55 is open drain. 1: GPIO55 is push pull.
4	GPIO54_DRV_EN	R/W	0	GPIO54 Drive Enable. 0: GPIO54 is open drain. 1: GPIO54 is push pull.
3	GPIO53_DRV_EN	R/W	0	GPIO53 Drive Enable. 0: GPIO53 is open drain. 1: GPIO53 is push pull.
2	GPIO52_DRV_EN	R/W	0	GPIO52 Drive Enable. 0: GPIO52 is open drain. 1: GPIO52 is push pull.
1	GPIO51_DRV_EN	R/W	0	GPIO51 Drive Enable. 0: GPIO51 is open drain. 1: GPIO51 is push pull.
0	GPIO50_DRV_EN	R/W	0	GPIO50 Drive Enable. 0: GPIO50 is open drain. 1: GPIO50 is push pull.

GPIO6 Output Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO64_OE	R/W	0	0: GPIO64 is input. 1: GPIO64 is output.
3	GPIO63_OE	R/W	0	0: GPIO63 is input. 1: GPIO63 is output.

2	GPIO62_OE	R/W	0	0: GPIO62 is input. 1: GPIO62 is output.
1	GPIO61_OE	R/W	0	0: GPIO61 is input. 1: GPIO61 is output.
0	GPIO60_OE	R/W	0	0: GPIO60 is input. 1: GPIO60 is output.

GPIO6 Output Data Register — Index 91h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO64_DATA	R/W	1	GPIO64 output data in output mode.
3	GPIO63_DATA	R/W	1	GPIO63 output data in output mode.
2	GPIO62_DATA	R/W	1	GPIO62 output data in output mode.
1	GPIO61_DATA	R/W	1	GPIO61 output data in output mode.
0	GPIO60_DATA	R/W	1	GPIO60 output data in output mode.

GPIO6 Pin Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO64_ST	R	1	GPIO64 pin status.
3	GPIO63_ST	R	1	GPIO63 pin status.
2	GPIO62_ST	R	1	GPIO62 pin status.
1	GPIO61_ST	R	1	GPIO61 pin status.
0	GPIO60_ST	R	1	GPIO60 pin status.

GPIO6 Drive Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO64_DRV_EN	R/W	0	GPIO64 Drive Enable. 0: GPIO64 is open drain. 1: GPIO64 is push pull.
3	GPIO63_DRV_EN	R/W	0	GPIO63 Drive Enable. 0: GPIO63 is open drain. 1: GPIO63 is push pull.
2	GPIO62_DRV_EN	R/W	0	GPIO62 Drive Enable. 0: GPIO62 is open drain. 1: GPIO62 is push pull.
1	GPIO61_DRV_EN	R/W	0	GPIO61 Drive Enable. 0: GPIO61 is open drain. 1: GPIO61 is push pull.
0	GPIO60_DRV_EN	R/W	0	GPIO60 Drive Enable. 0: GPIO60 is open drain. 1: GPIO60 is push pull.

8.7 WDT Registers (CR07)

WDT Device Base Address Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	WDT_EN	R/W	0	0: disable WDT base address. 1: enable WDT base address.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of WDT base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of WDT base address.

Watchdog Control Configuration Register 1 — Index F5h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

Watchdog Timer Configuration Register 2 — Index F6h

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	Time of watchdog timer (0~255)

Watchdog PME Enable Configuration Register 2 — Index FAh

Bit	Name	R/W	Default	Description
7	WDT_PME	R	--	The PME Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5-1	Reserved	--	--	Reserved.
0	WDOUT_EN	R/W	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.

8.8 SPI Registers (CR08)

SPI Control Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	SPTIE	R/W	0	SPI interrupt enable. Set to 1, SPIE enabled, set to 0 SPIE disabled.

4	MSTR	R/W	1	Master mode select. Set to 1, SPI function is master mode; set to 0 is disable SPI function
3	CPOL	R/W	0	Clock polarity this bit selects inverted or non-inverted SPI clock. Set to 1, active low clock selected; SCK idles high. Set to 0, active high clock selected; SCK idles low.
2	CPHA	R/W	0	Clock phase. This bit is used to shift the SCK serial clock. Set to 1, the first SCK edge is issued at the beginning of the transfer operation. Set to 0, the first SCK edge is issued one-half cycle into the transfer operation.
1	Reserved	-	0	Reserved
0	LSBFE	R/W	0	This bit control data shift from LSB or MSB. Set to 1, data is transferred from LSB to MSB. Set to 0, data is transferred from MSB to LSB.

Reserved — Index F1h

Bit	Name	R/W	Default	Description
7-0	Reserved	-	-	Reserved

SPI Baud Rate Divisor Register — Index F2h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	1	Reserved
2-0	Baud_val	R/W	1	This register decides to SCK frequency. Baud rate divisor equation is 2^ (Baud_val + 1)

SPI Status Register — Index F3h

Bit	Name	R/W	Default	Description
7	SPIE	R/W	0	SPI interrupt status. When SPI is transferred or received data from device finish, this bit will be set. Write 1 to clear this bit.
6-4	Reserved	R/W	-	Reserved.
3	SPTEF	R	0	SPI operation status. When SPI is transferred or received data from device, this bit will be set 1, Clear by SPI operation finish.
2-0	Reserved	-	-	Reserved

SPI High Byte Data Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	H_DATA	R	0	When SPI is received 16 bits data from device. This register saves high byte data.

SPI command data Register — Index F5h

Bit	Name	R/W	Default	Description
7-0	CMD_DATA	R/W	0	This register provides command value for flash command.

SPI chip select Register — Index F6h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved
1	CS1	R/W	0	Chip select 1. To select device 1
0	CS0	R/W	0	Chip select 0. To select device 0

SPI memory mapping Register — Index F7h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	0	Reserved

2-0	Mem_map	R/W	-	This register decides memory size. 3'b000: 512k bit. 3'b001: 1024k bit. 3'b100: 2048k bit. 3'b011: 4096k bit. 3'b100: 8092k bit.

SPI operate Register — Index F8h

Bit	Name	R/W	Default	Description
7	TYPE	R/W	0	This bit decide flash continuous programming mode. Set to 1, if programming continuous mode is same as the SST flash. Set to 0 if programming continuous mode is same as the ATMEL flash
6	IO_SPI	R/W	0	This bit control SPI function transfer 8 bit command to device. Clear 0 by operation finish.
5	RDSR	R/W	0	This bit control SPI function read status from to device. Clear 0 by operation finish.
4	WRSR	R/W	0	This bit control SPI function write status to device. Clear 0 by operation finish.
3	SECTOR_ERASE	R/W	0	This bit control SPI function sector erase device. Clear 0 by operation finish.
2	READ_ID	R/W	0	This bit control SPI function read id from device. Clear 0 by operation finish.
1	PROG	R/W	0	This bit control SPI function program data to device or set to 1 when memory cycle for LPC interface program flash. Clear 0 by operation finish.
0	READ	R/W	0	This bit control SPI function read data from device or set to 1 when memory cycle for LPC interface read flash. Clear 0 by operation finish.

SPI Low Byte Data Register — Index FAh

Bit	Name	R/W	Default	Description
7-0	L_DATA	R	0	When SPI is received 16 bits or 8 bits data from device. This register saves low byte data.

SPI address high byte Register — Index FBh

Bit	Name	R/W	Default	Description
7-0	Addr_H_byte	R/W	0	This register provides high byte address for sector erase, program, read operation.

SPI address medium byte Register — Index FCh

Bit	Name	R/W	Default	Description
7-0	Addr_M_byte	R/W	0	This register provides medium byte address for sector erase, program, read operation.

SPI address low byte Register — Index FDh

Bit	Name	R/W	Default	Description
7-0	Addr_L_byte	R/W	0	This register provides low byte address for sector erase, program, read operation.

SPI program byte Register — Index FEh

Bit	Name	R/W	Default	Description
7-0	PORG_BYTE	R/W	0	This register provides number to program flash for continuous mode.

SPI write data Register — Index FFh

Bit	Name	R/W	Default	Description
7-0	WR_dat	R/W	0	This register provides data to write flash for program, write status function.

8.9 PME and ACPI Registers (CR0A)

Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PME_EN	R/W	0	0: disable PME. 1: enable PME.

PME Event Enable 1 Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	WDT_PME_EN	R/W	0	Watchdog PME event enable. 0: disable watchdog PME event. 1: enable watchdog PME event.
5	GP_PME_EN	R/W	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.
4	MO_PME_EN	R/W	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
3	KB_PME_EN	R/W	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
2	HM_PME_EN	R/W	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
1	PRT_PME_EN	R/W	0	Parallel port PME event enable. 0: disable parallel port PME event. 1: enable parallel port PME event.
0	FDC_PME_EN	R/W	0	FDC PME event enable. 0: disable FDC PME event. 1: enable FDC PME event.

PME Event Enable 2 Register — Index F1h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5	UR6_PME_EN	R/W	0	UART 6 PME event enable. 0: disable UART 6 PME event. 1: enable UART 6 PME event.
4	UR5_PME_EN	R/W	0	UART 5 PME event enable. 0: disable UART 5 PME event. 1: enable UART 5 PME event.
3	UR4_PME_EN	R/W	0	UART 4 PME event enable. 0: disable UART 4 PME event. 1: enable UART 4 PME event.
2	UR3_PME_EN	R/W	0	UART 3 PME event enable. 0: disable UART 3 PME event. 1: enable UART 3 PME event.

1	UR2_PME_EN	R/W	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.
0	UR1_PME_EN	R/W	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.

PME Event Status 1 Register — Index F2h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	WDT_PME_ST	R/W	-	Watchdog PME event status. 0: Watchdog has no PME event. 1: Watchdog has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	GP_PME_ST	R/W	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	MO_PME_ST	R/W	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	KB_PME_ST	R/W	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	HM_PME_ST	R/W	-	Hardware monitor PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	PRT_PME_ST	R/W	-	Parallel port PME event status. 0: Parallel port has no PME event. 1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	FDC_PME_ST	R/W	-	FDC PME event status. 0: FDC has no PME event. 1: FDC has a PME event to assert. Write 1 to clear to be ready for next PME event.

PME Event Status 1 Register — Index F3h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5	UR6_PME_ST	R/W	-	UART 6 PME event status. 0: UART 6 has no PME event. 1: UART 6 has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	UR5_PME_ST	R/W	-	UART 5 PME event status. 0: UART 5 has no PME event. 1: UART 5 has a PME event to assert. Write 1 to clear to be ready for next PME event.

3	UR4_PME_ST	R/W	-	UART 4 PME event status. 0: UART 4 has no PME event. 1: UART 4 has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	UR3_PME_ST	R/W	-	UART 3 PME event status. 0: UART 3 has no PME event. 1: UART 3 has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	UR2_PME_ST	R/W	-	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	UR1_PME_ST	R/W	-	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.

ACPI Control Register — Index F4h

Bit	Name	R/W	Default	Description
7	TS3	R/W	0	KBC S3 test mode register. (Fintek only) Set one to force KBC into S3 state.
6	SPI_RST_EN	R/W	0	0: disable SPI time out reset via PWROK. 1: enable SPI time out reset via PWROK.
5	KEY_SEL_ADD	R/W	0	See KEY_SEL for detail.
4	EN_KBWAKEUP	R/W	0	Set one to enable keyboard wakeup event asserted via PWSOUT#.
3	EN_MOWAKEUP	R/W	0	Set one to enable mouse wakeup event asserted via PWSOUT#.
2-1	PWRCTRL	R/W	11	The ACPI Control the PSON_N to the following stages 00 : keep last state 01 :Bypass mode (Always on without PSOUT#) 10 : Always on 11: Always off
0	VSB_PWR_LOSS	R/W	0	When VSB 3V comes, it will set to 1 (default). Then write 1 to clear it.

ACPI Control Register — Index F5h

Bit	Name	R/W	Default	Description
7	SOFT_RST_ACPI	R/W	0	Software Reset to ACPI (auto clear after reset)
6-5	PWROK_DELAY	R/W	00	PWROK additional delay. 00: 0ms 01: 100ms. 10: 200ms. 11: 400ms.
4-3	DELAY	R/W	11	The PWROK delay timing from VDD3VOK by followed setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms
2	VINDB_EN	R/W	1	Enable the PCIRSTIN_N and ATXPWGD de-bounce.
1-0	Reserved	-	-	Reserved

ACPI Control Register — Index F6h

Bit	Name	R/W	Default	Description
7	S3_SEL	R/W	0	0: The S3 state for KBC is controlled by VDD3VOK. 1: The S3 state for KBC is force to 1 or inverted of S3# select by TS3.
6-5	Reserved	-	-	Reserved.
4	PSON_DEL_EN	R/W	0	PSON# delay enable. 0: PSON# is the invert of S3#. 1: PSON# will delay 4 seconds to turn on after last turn off.
3-2	Reserved	-	-	Reserved
1	BYPASS_DB_ACPI	R/W	0	Disable all the de-bounce circuit.
0	TEST_PWR_EN	R/W	0	For testing only.

8.10 RTC Registers (CR0B)

Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	RTC_EN	R/W	0	0: disable RTC I/O access. 1: enable RTC I/O access.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of RTC I/O port address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of RTC I/O port address.

KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELRTCIRQ	R/W	0h	Select the IRQ channel for RTC interrupt.

8.11 UART1 Registers (CR10)

UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR1_EN	R/W	1	1: disable UART 1. 1: enable UART 1.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART 1 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 1 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR1IRQ	R/W	4h	Select the IRQ channel for UART 1.

IRQ Share Register — Index F0h

Bit	Name	R/W	Default	Description
7	UR1_9BIT_MODE	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	UR1_AUTO_ADDR	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_UR1 and SADEN_UR1)
5	UR1_RS485_INV	R/W	0	Invert RTS# if UR1_RS485_EN is set.
4	UR1_RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# high when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	Reserved.
1	UR1IRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.
0	UR1IRQ_SHARE	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

Clock Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	UR1_CLK_SEL	R/W	00b	Select the clock source for UART1. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	SADDR_UR1	R/W	00h	This byte accompanying with SADEN_UR1 will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 1. given address: If bit n of SADEN_UR1 is “0”, then the corresponding bit of SADDR_UR1 is don’t care. 2. broadcast address: If bit n of ORed SADDR_UR1 and SADEN_UR1 is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR_UR1	0101_1100b
SADEN_UR1	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7:0	SADEN_UR1	R/W	00h	This byte accompanying with SADDR_UR1 will determine the given address and broadcast address in 9-bit mode. The UART_UR1 will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 3. given address: If bit n of SADEN_UR1 is "0", then the corresponding bit of SADDR_UR1 is don't care. 4. broadcast address: If bit n of ORed SADDR_UR1 and SADEN_UR1 is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR_UR1: 0101_1100b SADEN_UR1: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

8.12 UART2 Registers (CR11)

UART 2 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR2_EN	R/W	1	0: disable UART 2 1: enable UART 2.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of UART 2 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-1	BASE_ADDR_LO	R/W	F8h	The LSB of UART 2 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR12RQ	R/W	3h	Select the IRQ channel for UART 2.

IRQ Share Register — Index F0h

Bit	Name	R/W	Default	Description
7	UR2_9BIT_MODE	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	UR2_AUTO_ADDR	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_UR2 and SADEN_UR2)
5	UR2_RS485_INV	R/W	0	Invert RTS# if UR2_RS485_EN is set.
4	UR2_RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# high when transmitting data, otherwise is kept low.

3-2	Reserved	-	-	Reserved.
1	UR2IRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.
0	UR2IRQ_SHARE	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

Clock Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	UR2_CLK_SEL	R/W	00b	Select the clock source for UART2. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	SADDR_UR2	R/W	00h	This byte accompanying with SADEN_UR2 will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 5. given address: If bit n of SADEN_UR2 is "0", then the corresponding bit of SADDR_UR2 is don't care. 6. broadcast address: If bit n of ORed SADDR_UR2 and SADEN_UR2 is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex.

SADDR_UR2	0101_1100b
SADEN_UR2	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7:0	SADEN_UR2	R/W	00h	This byte accompanying with SADDR_UR2 will determine the given address and broadcast address in 9-bit mode. The UART_UR2 will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 7. given address: If bit n of SADEN_UR2 is "0", then the corresponding bit of SADDR_UR2 is don't care. 8. broadcast address: If bit n of ORed SADDR_UR2 and SADEN_UR2 is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex.

SADDR_UR2	0101_1100b
SADEN_UR2	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

8.13 UART3 Registers (CR12)

UART 3 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR3_EN	R/W	1	0: disable UART 3. 1: enable UART 3.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART 3 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	E8h	The LSB of UART 3 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR3IRQ	R/W	3h	Select the IRQ channel for UART 3.

IRQ Share Register — Index F0h

Bit	Name	R/W	Default	Description
7	UR3_9BIT_MODE	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	UR3_AUTO_ADDR	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_UR3 and SADEN_UR3)
5	UR3_RS485_INV	R/W	0	Invert RTS# if UR3_RS485_EN is set.
4	UR3_RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# high when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	Reserved.
1	UR3IRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.
0	UR3IRQ_SHARE	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

Clock Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	UR3_CLK_SEL	R/W	00b	Select the clock source for UART3. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	SADDR_UR3	R/W	00h	This byte accompanying with SADEN_UR3 will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 9. given address: If bit n of SADEN_UR3 is "0", then the corresponding bit of SADDR_UR3 is don't care. 10. broadcast address: If bit n of ORed SADDR_UR3 and SADEN_UR3 is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR_UR3: 0101_1100b SADEN_UR3: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7:0	SADEN_UR3	R/W	00h	This byte accompanying with SADDR_UR3 will determine the given address and broadcast address in 9-bit mode. The UART_UR3 will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 11. given address: If bit n of SADEN_UR3 is "0", then the corresponding bit of SADDR_UR3 is don't care. 12. broadcast address: If bit n of ORed SADDR_UR3 and SADEN_UR3 is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR_UR3: 0101_1100b SADEN_UR3: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

8.14 UART4 Registers (CR13)

UART 4 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR3_EN	R/W	1	0: disable UART 4. 1: enable UART 4.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART 4 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	E8h	The LSB of UART 4 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR4IRQ	R/W	3h	Select the IRQ channel for UART 4.

IRQ Share Register — Index F0h

Bit	Name	R/W	Default	Description
7	UR4_9BIT_MODE	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	UR4_AUTO_ADDR	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_UR4 and SADEN_UR4)
5	UR4_RS485_INV	R/W	0	Invert RTS# if UR4_RS485_EN is set.
4	UR4_RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# high when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	Reserved.
1	UR4IRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.
0	UR4IRQ_SHARE	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

Clock Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	UR4_CLK_SEL	R/W	00b	Select the clock source for UART4. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	SADDR_UR4	R/W	00h	This byte accompanying with SADEN_UR4 will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 13. given address: If bit n of SADEN_UR4 is “0”, then the corresponding bit of SADDR_UR4 is don’t care. 14. broadcast address: If bit n of ORed SADDR_UR4 and SADEN_UR4 is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR_UR4	0101_1100b
SADEN_UR4	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7:0	SADEN_UR4	R/W	00h	This byte accompanying with SADDR_UR4 will determine the given address and broadcast address in 9-bit mode. The UART_UR4 will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 15. given address: If bit n of SADEN_UR4 is "0", then the corresponding bit of SADDR_UR4 is don't care. 16. broadcast address: If bit n of ORed SADDR_UR4 and SADEN_UR4 is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR_UR4 0101_1100b SADEN_UR4 1111_1001b Given Address 0101_1xx0b Broadcast Address 1111_11x1b

8.15 UART5 Registers (CR14)

UART 5 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR5_EN	R/W	0	0: disable UART 5. 1: enable UART 5.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of UART 5 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of UART 5 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR5IRQ	R/W	3h	Select the IRQ channel for UART 5.

IRQ Share Register — Index F0h

Bit	Name	R/W	Default	Description
7	UR5_9BIT_MODE	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	UR5_AUTO_ADDR	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_UR5 and SADEN_UR5)
5	UR5_RS485_INV	R/W	0	Invert RTS# if UR5_RS485_EN is set.
4	UR5_RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# high when transmitting data, otherwise is kept low.

3-2	Reserved	-	-	Reserved.
1	UR5IRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.
0	UR5IRQ_SHARE	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

Clock Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	UR5_CLK_SEL	R/W	00b	Select the clock source for UART5. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	SADDR_UR5	R/W	00h	This byte accompanying with SADEN_UR5 will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 17. given address: If bit n of SADEN_UR5 is “0”, then the corresponding bit of SADDR_UR5 is don’t care. 18. broadcast address: If bit n of ORed SADDR_UR5 and SADEN_UR5 is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex. SADDR_UR5 0101_1100b SADEN_UR5 1111_1001b Given Address 0101_1xx0b Broadcast Address 1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7:0	SADEN_UR5	R/W	00h	This byte accompanying with SADDR_UR5 will determine the given address and broadcast address in 9-bit mode. The UART_UR5 will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 19. given address: If bit n of SADEN_UR5 is “0”, then the corresponding bit of SADDR_UR5 is don’t care. 20. broadcast address: If bit n of ORed SADDR_UR5 and SADEN_UR5 is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex. SADDR_UR5 0101_1100b SADEN_UR5 1111_1001b Given Address 0101_1xx0b Broadcast Address 1111_11x1b

8.16 UART6 Registers (CR15)

UART 6 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR6_EN	R/W	0	0: disable UART 6. 1: enable UART 6.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of UART 6 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of UART 6 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR6IRQ	R/W	3h	Select the IRQ channel for UART 6.

IRQ Share Register — Index F0h

Bit	Name	R/W	Default	Description
7	UR6_9BIT_MODE	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	UR6_AUTO_ADDR	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_UR6 and SADEN_UR6)
5	UR6_RS485_INV	R/W	0	Invert RTS# if UR6_RS485_EN is set.
4	UR6_RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# high when transmitting data, otherwise is kept low.
3	RXW4C_IR	R/W	0	0 : No reception delay when SIR is changed from TX to RX. 1 : Reception delay 4 character-time when SIR is changed from TX to RX.
2	TXW4C_IR	R/W	0	0 : No transmission delay when SIR is changed from RX to TX. 1 : Transmission delay 4 character-time when SIR is changed from RX to TX.
1	UR6IRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.
0	UR6IRQ_SHARE	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

IR Mode Select Register — Index F1h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved. Return 010b when read.
4-3	IRMODE1 IRMODE0	R/W	00b	0X: Disable IR1 function. 10 : Enable IR1 function, active pulse is 1.6uS. 11 : Enable IR1 function, active pulse is 3/16 bit time.

2	HDUPLX	R/W	0	0 : Full Duplex function for IR self test. 1 : Half Duplex function. Return 1 when read.
1	TXINV_IR	R/W	0	0 : IRTX is not inversed. 1 : Inverse the IRTX.
0	RXINV_IR	R/W	0	0 : IRRX is not inversed. 1 : Inverse the IRRX.

Clock Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	UR6_CLK_SEL	R/W	00b	Select the clock source for UART6. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	SADDR_UR6	R/W	00h	This byte accompanying with SADEN_UR6 will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 21. given address: If bit n of SADEN_UR6 is “0”, then the corresponding bit of SADDR_UR6 is don’t care. 22. broadcast address: If bit n of ORed SADDR_UR6 and SADEN_UR6 is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex. SADDR_UR6 0101_1100b SADEN_UR6 1111_1001b Given Address 0101_1xx0b Broadcast Address 1111_11x1b

9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7:0	SADEN_UR6	R/W	00h	This byte accompanying with SADDR_UR6 will determine the given address and broadcast address in 9-bit mode. The UART_UR6 will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 23. given address: If bit n of SADEN_UR6 is “0”, then the corresponding bit of SADDR_UR6 is don’t care. 24. broadcast address: If bit n of ORed SADDR_UR6 and SADEN_UR6 is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex. SADDR_UR6 0101_1100b SADEN_UR6 1111_1001b Given Address 0101_1xx0b Broadcast Address 1111_11x1b

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Operating Temperature-I	-40 to +85	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

9.2 DC Characteristics

(T_A = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

Parameter	Conditions	MIN	TYP	MAX	Unit
Temperature Error, Remote Diode	60 °C < T_D < 145 °C, VCC = 3.0V to 3.6V 0 °C <T_D < 60°C 100 °C <T_D < 145°C		± 1 ± 1	± 3 ± 3	°C
Supply Voltage range		3.0	3.3	3.6	V
Average operating supply current			10		mA
Standby supply current			5		uA
Resolution			1		°C
Power on reset threshold			2.6	2.8	V
Diode source current	High Level		95		uA
	Low Level		10		uA

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_{st}-TTL level input pin with schmitt trigger.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$IN_{t,5V}$-TTL level input pin, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$IN_{st,5V}$-TTL level input pin with schmitt trigger, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$O_{8,u47,5V}$-Output pin with 8 mA sink/source capability, internal 47K ohms pull-up and 5V tolerance.						
Output High Current	IOL		-8		mA	VOH = 2.4V
Output Low Current	IOL		+8		mA	VOL = 0.4V
O_{12}-Output pin with 12 mA sink/source capability.						
Output High Current	IOL		-12		mA	VOH = 2.4V

Output Low Current	IOL		+12		mA	VOL = 0.4V
O_8 -Output pin with 8 mA sink/source capability.						
Output High Current	IOL		-8		mA	VOH = 2.4V
Output Low Current	IOL		+8		mA	VOL = 0.4V
OD_{14}-Open drain output pin with 14 mA sink capability.						
Output Low Current	IOL		+14		mA	VOL = 0.4V
$OD_{16,u10,5V}$-Open drain output pin with 14 mA sink capability, internal 10K ohms pull-up and 5V tolerance.						
Output Low Current	IOL		+16		mA	VOL = 0.4V
OD_{24}-Open drain output pin with 24 mA sink capability, 5V tolerance.						
Output Low Current	IOL		+24		mA	VOL = 0.4V
$I/O_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-12		mA	VOH = 2.4V
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/O_{8t}-TTL level bi-directional pin with schmitt trigger, Open-drain output with 8mA sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-8		mA	VOH = 2.4V
Output Low Current	IOL		+8		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_{12t}-TTL level bi-directional pin with schmitt trigger, output with 12 mA sink/source capability or open drain with 12mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-12		mA	VOH = 0.4V
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_{14}-TTL level bi-directional pin with schmitt trigger, output with 14 mA sink/source capability or open drain with 14mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-14		mA	VOH = 0.4V
Output Low Current	IOL		+14		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_8-TTL level bi-directional pin with schmitt trigger, output with 8 mA sink/source capability or open drain with 8mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output High Current	IOL		-8		mA	VOH = 0.4V
Output Low Current	IOL		+8		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OD_{16t,5v}$-TTL level bi-directional pin, Open-drain output with16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD

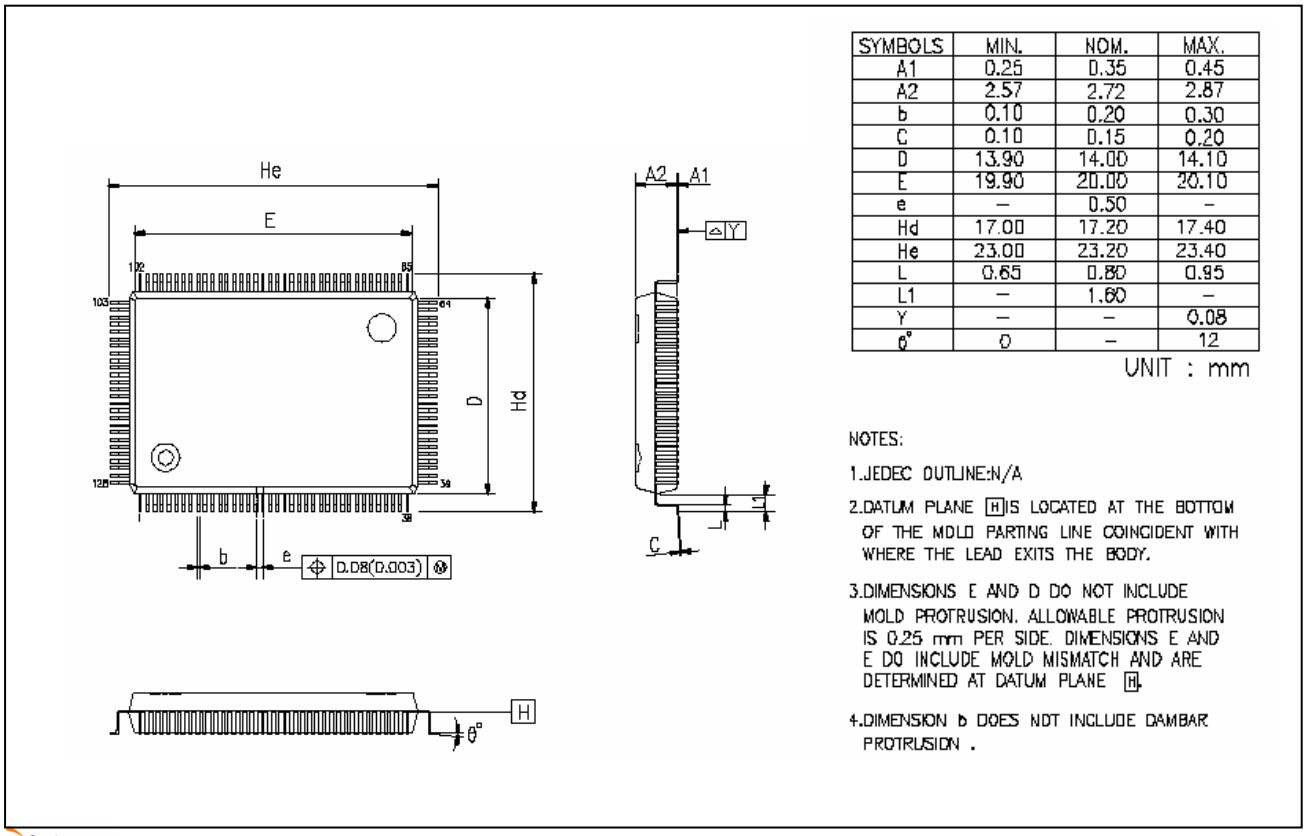
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/O_{24t}-TTL level bi-directional pin, Output pin with 24mA sink/source capability.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-24		mA	VOL = 0.4 V
Output High Current	IOH		+24		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V

10.Ordering Information

Part Number	Package Type	Production Flow
F81865F-I	128-PQFP Green Package	Industrial, -40°C to +85°C
F81865F	128-PQFP Green Package	Commercial, 0°C to +70°C

11.Package Dimensions

128 PQFP



SYMBOLS	MIN.	NOM.	MAX.
A1	0.25	0.35	0.45
A2	2.57	2.72	2.87
b	0.10	0.20	0.30
C	0.10	0.15	0.20
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e	–	0.50	–
Hd	17.00	17.20	17.40
He	23.00	23.20	23.40
L	0.65	0.80	0.95
L1	–	1.60	–
Y	–	–	0.08
θ°	0	–	12

UNIT : mm

NOTES:

1.JEDEC OUTLINE:N/A

2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

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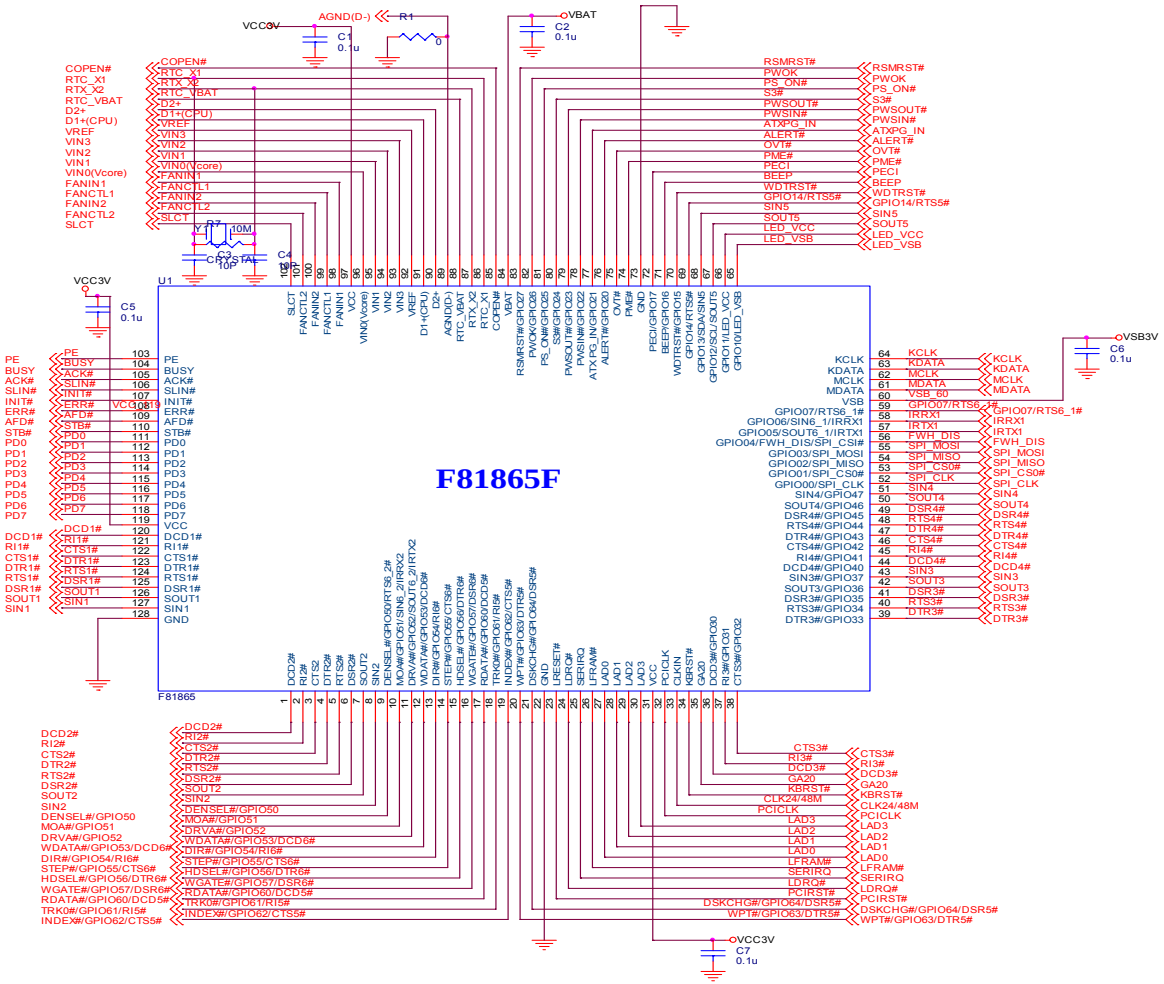
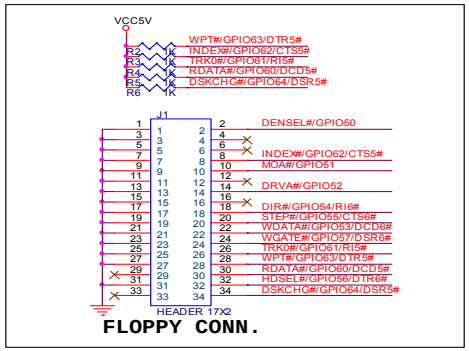
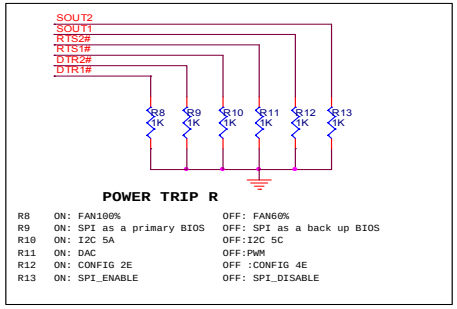
12. Application Circuit







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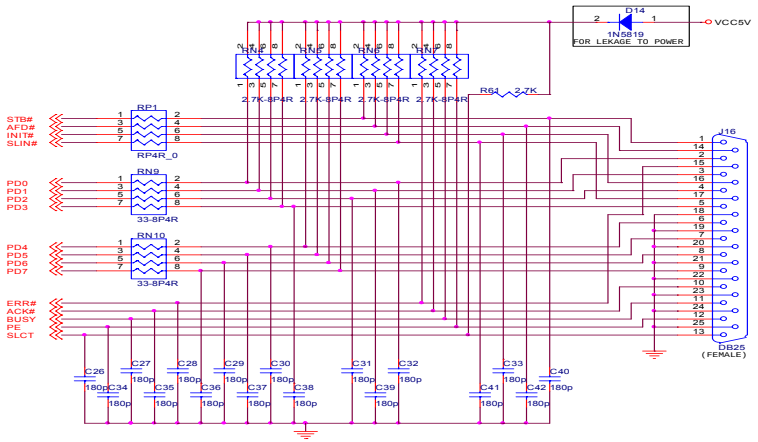
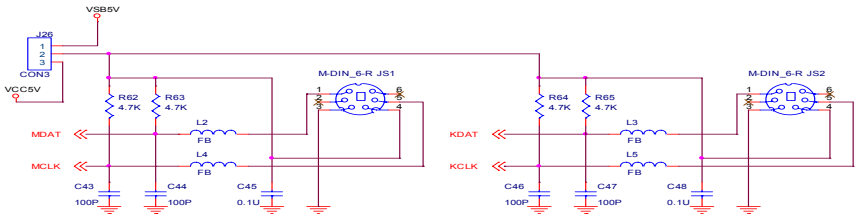
Size B	Document Number <Doc>	Rev 0.1
Date: Thursday, December 18, 2008	Sheet 1 of 1	

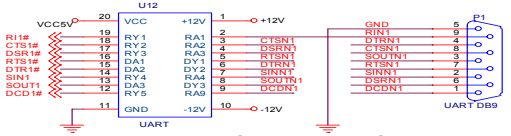


PARALLEL PORT INTERFACE

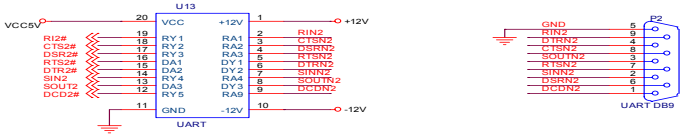


PS2 MOUSE INTERFACE

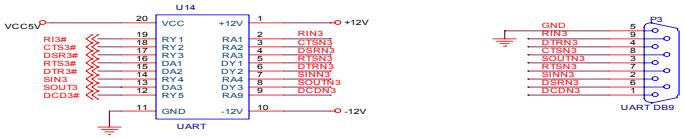
PS2 KEYBOARD INTERFACE



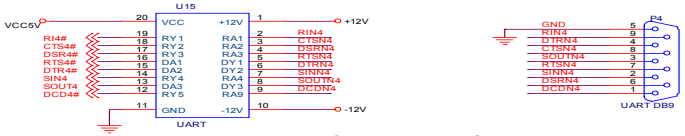
UART 1 PORT INTERFACE



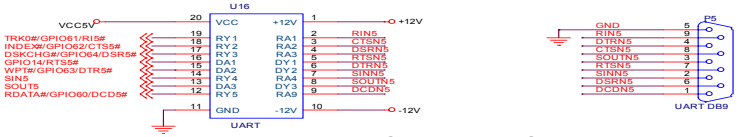
UART 2 PORT INTERFACE



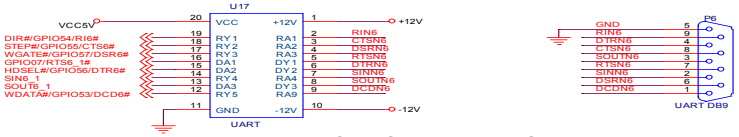
UART 3 PORT INTERFACE



UART 4 PORT INTERFACE



UART 5 PORT INTERFACE



UART 6 PORT INTERFACE

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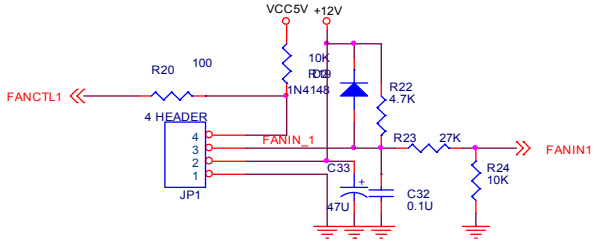
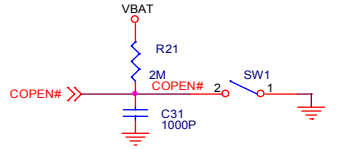
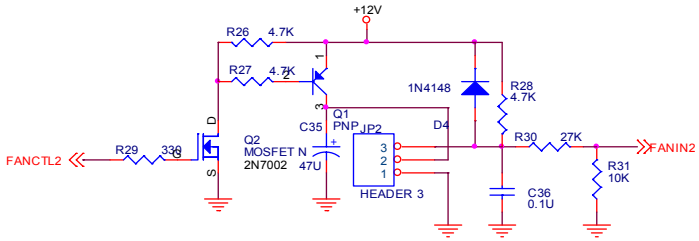


PWM

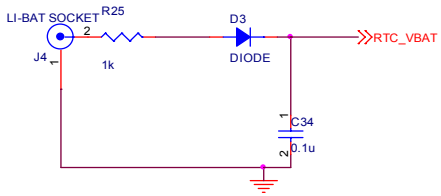


CASE OPEN CIRCUIT

FAN1 CONTROL CIRCUIT



FAN2 PWM CONTROL CIRCUIT



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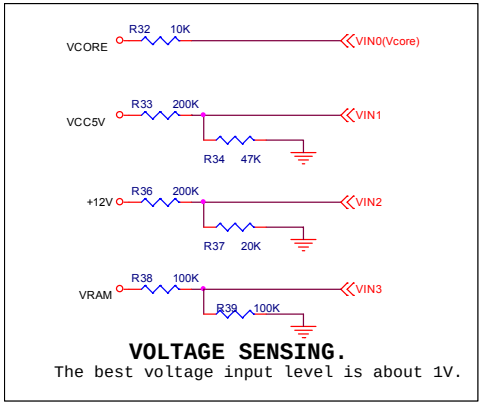
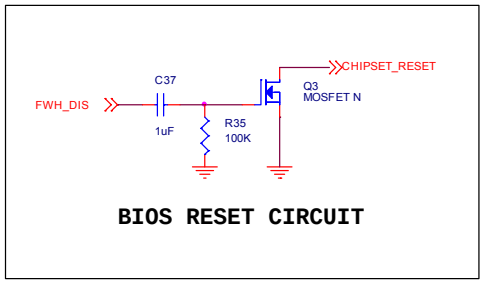
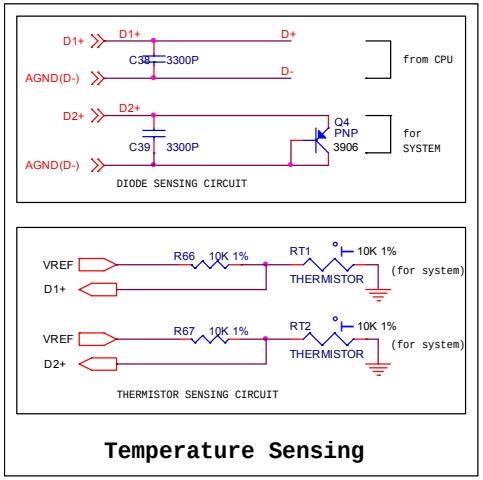


VOLTAGE SENSING.

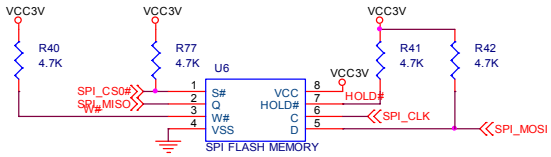
The best voltage input level is about 1V.



BIOS RESET CIRCUIT



Temperature Sensing



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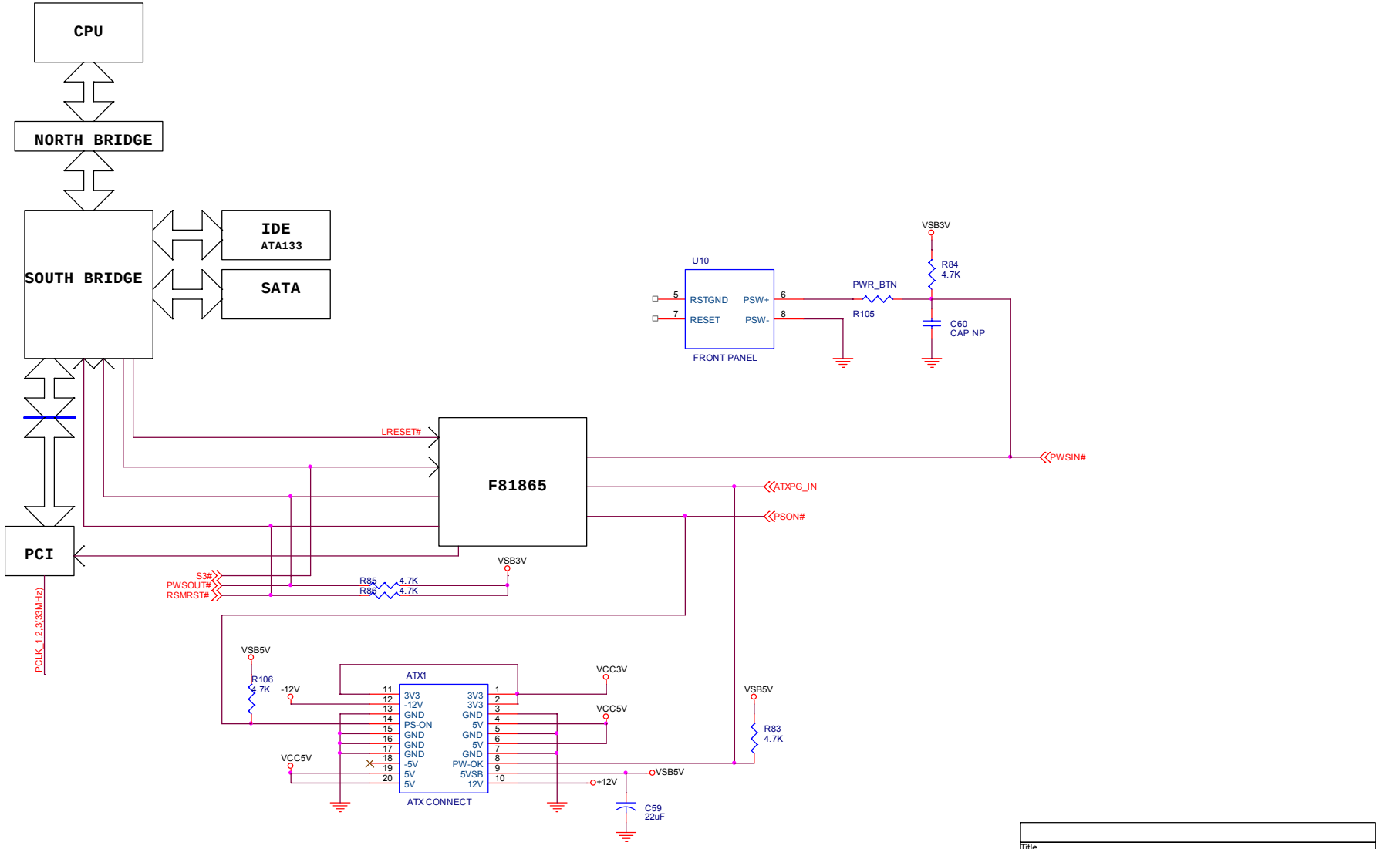

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