F75122R/F75122RG

Dynamic VID Control + 8 GPIO Datasheet

Release Date: July, 2007
Revision: V0.28P

F75122 Datasheet Revision History

Version	Date	Page	Revision History
0.20P	Jan/2004		Preliminary Version
0.21P	Feb/2004	41	Add DC spec description for low level input pin($IN_{lv)}$
0.22P	Feb/2004	5-7	Revise pin10 ~ 12 configuration and description
0.23P	May/2004	40-41	Update DC spec about Input High/Low Leakage Current
0.24P	June/2004	13-17	Delete redundant register description
0.25P	Sep/2004	18	Add VID Offset table on index30h
0.26P	Jan/2005	31	Add Green Package support (F75122RG)
0.27P	Jan/2005		Update application circuit
0.28P	July/2007	-	Add company address

Table of Contents

1. General Description

The F75122 is the dynamic voltage ID controller chip to provide the advanced CPU voltage programming when over clocking. F75122 supports the dynamic VID spec. for new generation Intel Prescott CPU and also compatible to VRM10.0/VRM9.X spec.. Auto sensing CPU replacement and setting watch dog timer for OS idling protection. Besides of VID controlling function, F75122 also supports pure 8 GPIO pins. Level or pulse modes can be programmed by registers. With 2 sets of watchdog timer, F75122 provides more flexible control for PC system, and there are four kinds of pulse width of the time out alert output pin can be selected.

2. Features

- Supporting new generation Intel dynamic Processor VID input /output
- Supporting Intel Prescott CPU low level input (V_{IH} > 0.9V, V_{IL} <0.8V)
- Compatible VRM 9.X and VRM10.0
- Auto detecting the CPU replacement
- Pure 8 GPIO pins
- Two sets of Watch dog timer to protect system from hanging when over-clocking
- SMbus interface
- Package in 28-SSOP (150mil)

3. Key Specifications

- Supply Voltage 3.0V to 3.6V
- Operating Supply Current 1mA typ.

4. Pin Configuration

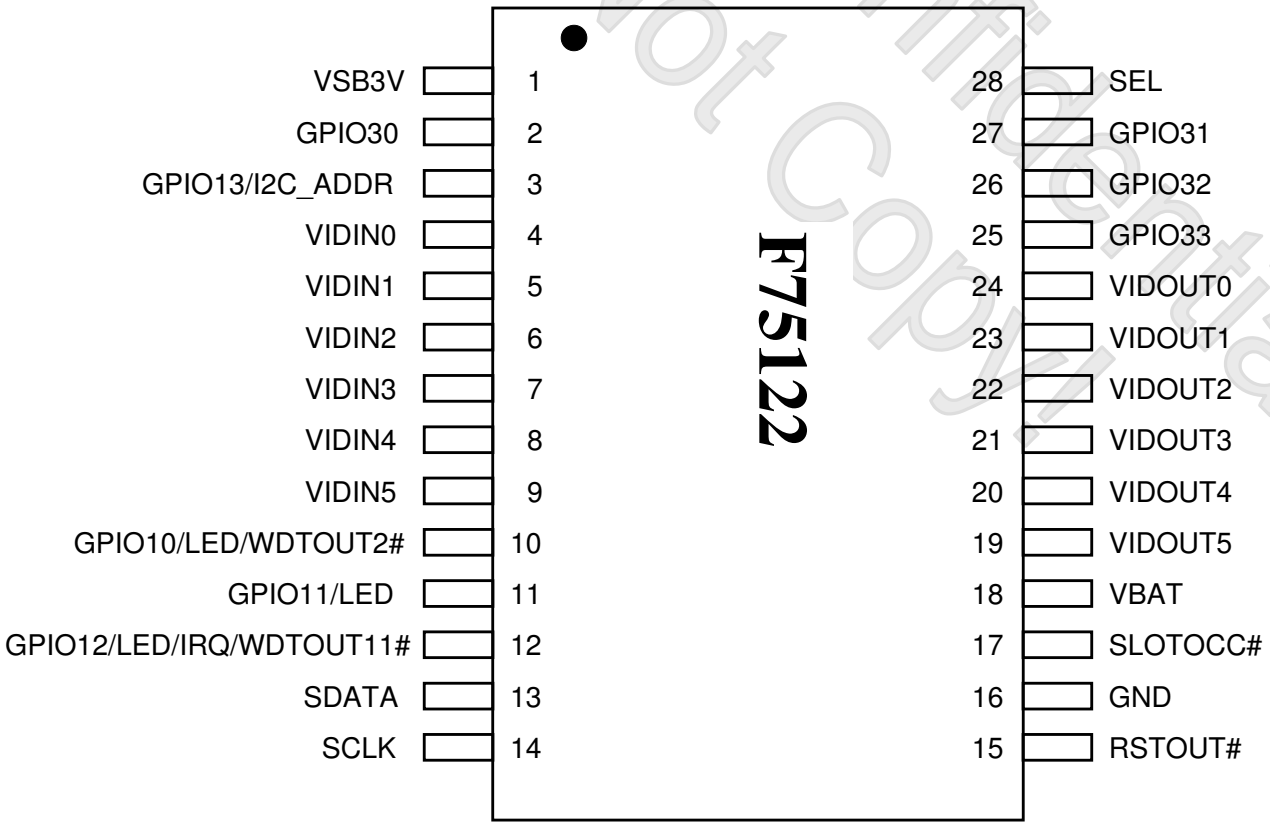


Figure 1.

5. Pin Description

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts} - TTL level and schmitt trigger
I/OOD_{12t} - TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability
I/OD_{12} - TTL level bi-directional pin, Open-drain outpu with 12 mA sink capability
OUT_{12} - Output pin with 12 mA source-sink capability
AOUT - Output pin(Analog)
OD_{12} - Open-drain output pin with 12 mA sink capability
IN_t - TTL level input pin
IN_{ts} - TTL level input pin and schmitt trigger
IN_{lv} -- Low level input pin
AIN - Input pin(Analog)
P - Power

5.1 Power Pin

Pin No.	Pin Name	Type	Description
1	VSB3V	P	Standard Power Supply Voltage Input with 3.3V
18	VBAT	P	3V Battery
16	GND	P	GND

5.2 VID Control and GPIO pins

Pin No.	Pin Name	Type	PWR	Description
10	GPIO10	I/OOD_{16ts}	VSB3V	General purpose I/O pin.
	LED	OD_{16}	VSB3V	LED control output. The multi-function pin is selected by register, so does the freq. programming
	WDTOUT2#	OD_{16}	VSB3V	The 2nd Watch Dog Timer time out output
11	GPIO11	I/OOD_{16ts}	VSB3V	General purpose I/O pin.
	LED	OD_{16}	VSB3V	LED control output. The multi-function pin is selected by register, so does the freq. programming
12	GPIO12	I/OOD_{16ts}	VSB3V	General purpose I/O pin.

	LED	OD_{16}	VSB3V	LED control output. The multi-function pin is selected by register, so does the freq. programming
	IRQ	OD_{16}	VSB3V	IRQ and SMI# function
	WDTOUT11#	OD_{16}	VSB3V	The 1st Watch Dog Timer time out output. System reset signal when the Reset-Out timer is time out. This pin will generate 100mS pulse (default) when the Reset-Out timer is timeout.
4 ~ 9	VIDIN[0:5]	IN_{lv}	VSB3V	CPU Voltage ID input
3	GPIO13	I/O_{16ts}	VSB3V	General purpose I/O pin.
	I2C_ADDR	$IN_{tsd100k}$		The GPIO serial bus hardware power on setting pin. Default address is 0x9C (when I2C_ADDR=0). Another one is 0x6E (when I2C_ADDR=1). This pin internal pull-down 100k to Ground. If this pin is pull-up 10k to VSB3V, this pin will be trapped to 1.
13	SDATA	I/OD_{12ts}	VSB3V	SMbus data.
14	SCLK	IN_{ts}	VSB3V	SMBus clock
15	RSTOUT#	OD_{12}	VSB3V	System reset signal when the Reset-Out timer is time out. This pin will generate 100mS pulse when the Reset-Out timer is timeout.
17	SLOTOCC#	IN_{ts}	VBAT	Powered by VBAT. CPU detect pin.
24 ~ 19	VIDOUT[0:5]	OD_{16}	VSB3V	CPU Voltage ID output.
28	SEL	$IN_{tsd100k}$	VSB3V	Default pull up to 3VSB.
2,27,26,25	GPIO[30:33]	I/OD_{12ts}	VSB3V	General purpose I/O pins.

6. Functional Description

6.1 General Description

The F75122 provides VIDIN, VIDOUT function. It can latch the VIDIN from CPU side, and output VIDOUT to PWM. The VIDOUT value can be programmed by the interface GPIO Serial Bus serial interface.

Dedicate GPIO functions. That includes two set watchdog timer. The watchdog timer timeout unit is set to second and range is 0 to 31 seconds. When the timeout has occurred, that will generate a status bit to indicate it and write one will be clear.

All GPIO can be programmed to logic one or zero or high pulse or low pulse.

Providing CPU on board detection (SLOTOCC#). The detection circuit is powered by battery. That is latch circuit is powered by VBAT. The de-bounce circuit should be added to avoid low power noise. The de-bounce circuit is generated by internal low frequency clock with 32K Hz to filter out the low-to-high or high-to-low glitch.

6.2 Access Interface

The F75122 provides one serial access interface, Serial Bus, to read/write internal registers. The address of Serial Bus is configurable by using power-on trapping of standby power VBS3V. The pin 11 (GPIO11/I2C _ADDR) is multi-function pin. During the VSB 3V power-on, this pin serves as input detection of logic high or logic low. This pin is default pull-down resistor with 100K ohms mapping the Serial Bus address 0x9C (1001_1100). Another Serial Bus address 0x6E (0110_1110) is set when external pull-up resistor with 10K ohms is connected in this pin.

6.3 The SMBus access timing are shown as follow:

(a) SMBus write to internal address register followed by the data byte

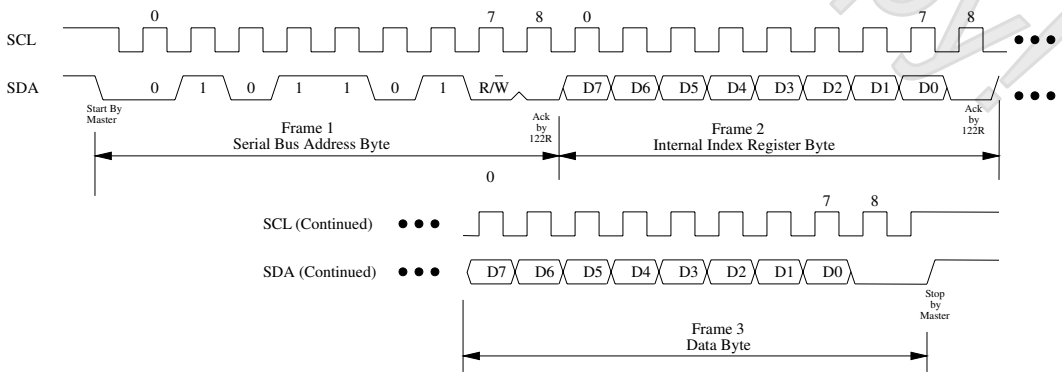


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus write to internal address register only

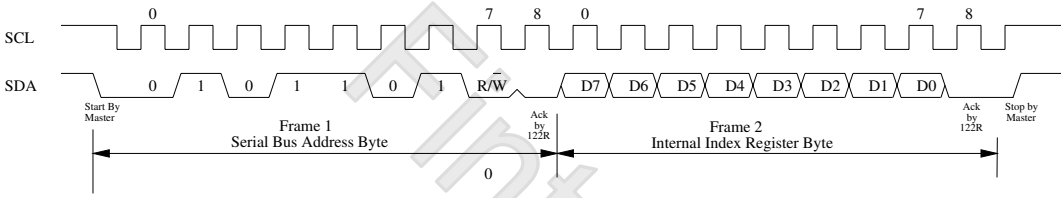


Figure 2. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location

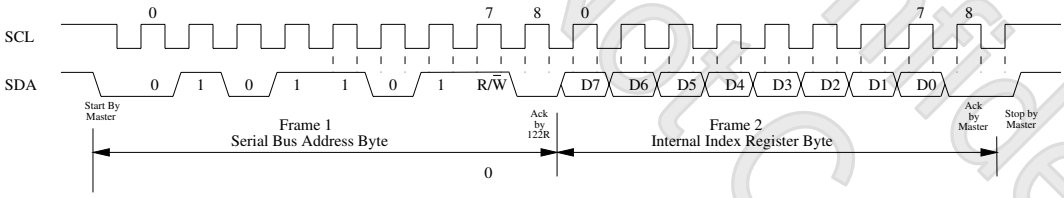


Figure 3. Serial Bus Read from Internal Address Register

6.4 VID Function

Please refer to control registers.

6.5 GPIO Function

The GPIO functions in the F75122 include general GPIO with programming Input and output. The output function also can be programmed high level or low level or high pulse or low pulse.

CPU Voltage ID (VID) function

The F75122 provides a voltage adjustment in the CPU with VID control. In general, the VIDIN is connected to CPU VID<4:0>(VRM9.X) or VID<5:0>(VRM10.0) and VIDOUT is connected to PWM Vcore VID. In the first power-on, the VIDIN is bypassed to VIDOUT.

6.5.1 General GPIO Function

Please refer to control registers.

6.5.3 Reset Out (RSTOUT) Function

Please refer to control registers.

6..4 Watchdog Function

Please refer to control register.

7. Registers Description

7.1 Configuration and Control Register – Index 01h

Power-on default [7:0] =0000_1000b

Bit	Name	R/W	PWR	Description
7	INIT	R/W	VSB3V	Software reset for all registers including Test Mode registers. Users use only.
6	CPU_SEL	R/W	VSB3V	CPU select, if set this bit to 1 will select AMD CPU, else if set to 0 is Intel CPU(default), this bit clear by SLOTOCC#, and protect write command by VID_KEY REG 0x30.
5	EN_RSTOUT	R/W	VSB3V	Enable Reset Out. If set to 1, enable RSTOUT output. Default is disable.
4	EN_OTF	R/W	VSB3V	If set this bit to 1 will enable VID on the fly mode, user can change new VID value by program the REG 0x30 VID_OFFSET, this bit will clear by SLOTOCC#, and protect write command by VID_KEY REG 0x30.
3	VID_EXTEND	R/W	VSB3V	Set this bit to 1 to enable Intel VRM10 mode, then GPIO14 and GPIO15 will be implement to VID_IN[5] and VID_OUT[5], this bit default is enable, , this bit will clear by SLOTOCC#, and protect write command by VID_KEY REG 0x30.
2	Reserved	R/W	VSB3V	
1	AUTO_POWR_MODE	R/W	VSB3V	Set this bit to 1 will enable auto power down mode, when all function are idle then 20ms the chip will auto power down, it will wakeup when GPIO state change or read write register
0	SOFT_POWR_DOWN	R/W	VSB3V	Set this bit to 1 will power down all of the analog block and stop internal clock, write 0 to clear this bit or when GPIO state change will auto clear this bit to 0.

7.2 Status Register – Index 02h

Power-on default [7:0] =0000_000xb

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	
3	POWR_DOWN	RO	VSB3V	If this bit is set to 1, it mean the chip is in power down mode
2	FUNC_SEL	RO	VSB3V	VID and GPIO function select. This is dedicated pin. if input value is 1(external pull-down 10K), the function is selected to VID. Otherwise, the input value is 0, the function is selected to GPIO.
1	I2C_ADDR	RO	VSB3V	GPIO serial bus address Select. Internal pull-down 100K ohms are address 0x9C. If external is pull-up 10K ohms, the address is 0x6E. This pin is trapped during the VSB3VOK.
0	STS_SLOTOCC	R/W	VBAT	Indicate the SLOTOCC# pin value. This pin will be latched till write this bit to 1. Writing 0 is invalid.

Design note:

Bit0: Once the RSTOUT# is asserted (negative edge). This bit should be set to 1. Clear signal can be generated by "write_command & write_data[0]==1".

7.3 Configuration and function select Register – Index 03h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	Reserved	RO	VSB3V	
6	IRQ_LEVEL	R/W	VSB3V	Select IRQ Polarity (Level). Set to 1, IRQ is low active and SMI# is high active. Default, the IRQ is high active and SMI# is low active.
5	IRQ_MODE	R/W	VSB3V	IRQ/SMI# mode select. 0 – Level mode (IRQ mode), 1 – Pulse Mode (SMI# mode). If pulse mode is selected, the active pulse is over 100us.
4-3	PIN12_MODE	R/W	VSB3V	00: GPIO12 01: LED12 IN this mode can use REG 0x06(bit5,4) to select LED frequency. 10: IRQ 11: RSTOUT1#:
2	PIN11_MODE	R/W	VSB3V	0: GPIO11 1: LED11 IN this mode can use REG 0x06(bit3,2) to select LED frequency.

1-0	PIN10_MODE	R/W	VSB3V	00: GPIO10 01: LED10 IN this mode can use REG 0x06(bit1,0) to select LED frequency. 10,11: WD_OUT

7.6 LED Freq Control Register – Index 06h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-6	Reserved	R/W	VSB3V	
5-4	LED12_FREQ	R/W	VSB3V	LED output frequency. Bit: Description 00: Tri-state (default). 01: 0.5Hz (period is 2 seconds, duty cycle is 50%) 10: 1 Hz (period is 1 second) 11: Low.
3-2	LED11_FREQ	R/W	VSB3V	LED output frequency. Bit: Description 00: Tri-state (default). 01: 0.5Hz (period is 2 seconds, duty cycle is 50%) 10: 1 Hz (period is 1 second) 11: Low.
1-0	LED10_FREQ	R/W	VSB3V	LED output frequency. Bit: Description 00: Tri-state (default). 01: 0.5Hz (period is 2 seconds, duty cycle is 50%) 10: 1 Hz (period is 1 second) 11: Low.

7.10 GPIO1x Output Control Register – Index 10h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	GP13_OCTRL	R/W	VSB3V	GPIO 13 output control. Set to 1 for output function. Set to 0 for input function(default).
2	GP12_OCTRL	R/W	VSB3V	GPIO 12 output control. If this pin serves as IRQ/SMI#, this bit has no effect. Set to 1 for output function. Set to 0 for input function(default).
1	GP11_OCTRL	R/W	VSB3V	GPIO 11 output control. Set to 1 for output function. Set to 0 for input function(default).
0	GP10_OCTRL	R/W	VSB3V	GPIO 10 output control. Set to 1 for output function. Set to 0 for input function(default).

7.11 GPIO1x Output Data Register – Index 11h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	GP13_ODATA	R/W	VSB3V	GPIO 13 output data.
2	GP12_ODATA	R/W	VSB3V	GPIO 12 output data. If this pin serves as IRQ/SMI#, this bit has no effect.
1	GP11_ODATA	R/W	VSB3V	GPIO 11 output data.
0	GP10_ODATA	R/W	VSB3V	GPIO 10 output data.

7.12 GPIO1x Input Status Register – Index 12h

Power-on default [7:0] =xxxx_xxxxb

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	GP13_PSTS	RO	VSB3V	Read the GPIO13 data on the pin.
2	GP12_PSTS	RO	VSB3V	Read the GPIO12 data on the pin.
1	GP11_PSTS	RO	VSB3V	Read the GPIO11 data on the pin.
0	GP10_PSTS	RO	VSB3V	Read the GPIO10 data on the pin.

7.13 GPIO1x Level/Pulse Control Register – Index 13h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	GP13_OMODE	R/W	VSB3V	GPIO 13 output mode. 0 – level, 1 – pulse.
2	GP12_OMODE	R/W	VSB3V	GPIO 12 output mode. 0 – level, 1 – pulse. If this serves as IRQ/SMI# mode, it will have same function.
1	GP11_OMODE	R/W	VSB3V	GPIO 11 output mode. 0 – level, 1 – pulse.
0	GP10_OMODE	R/W	VSB3V	GPIO 10 output mode. 0 – level, 1 – pulse.

7.14 GPIO1x Pulse Width Control Register – Index 14h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7:2	Reserved	R/W	VSB3V	Reserved. Read return 0.
1:0	GP1_PSWDTH[1:0]	R/W	VSB3V	GPIO1x pulse width. If set the GPIO1x to pulse mode, the pulse width can be defined as follows. 00b – 500us (Default) 01b – 1ms 10b – 20ms 11b – 100ms

7.15 GPIO1x Pull-up Resistor Control Register – Index 15h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
3-7	Reserved	R/W	VSB3V	
2	GP12_RESON	R/W	VSB3V	Set to 1, turn on the GPIO12 internal pull-up resistor. If this pin serves as IRQ/SMI#, this bit also control IRQ/SMI# pull-up switch.
1	GP11_RESON	R/W	VSB3V	Set to 1, turn on the GPIO11 internal pull-up resistor.
0	GP10_RESON	R/W	VSB3V	Set to 1, turn on the GPIO10 internal pull-up resistor.

7.16 GPIO1x Input De-bounce Register – Index 16h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	GP13_ENDB	R/W	VSB3V	Enable GPIO13 input de-bounce with 7u or 25ms second that selected by 0x1C bit3.
2	GP12_ENDB	R/W	VSB3V	Enable GPIO12 input de-bounce with 7u or 25ms second that selected by 0x1C bit2.
1	GP11_ENDB	R/W	VSB3V	Enable GPIO11 input de-bounce with 7u or 25ms second that selected by 0x1C bit1.
0	GP10_ENDB	R/W	VSB3V	Enable GPIO10 input de-bounce with 7u or 25ms second that selected by 0x1C bit0.

7.17 GPIO1x Pulse Inverse Register – Index 17h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	GP13_PULSINV	R/W	VSB3V	GPIO13 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14.
2	GP12_PULSINV	R/W	VSB3V	GPIO12 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. If this pin services as IRQ/SMI#, this bit has no effect.
1	GP11_PULSINV	R/W	VSB3V	GPIO 11 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14.
0	GP10_PULSINV	R/W	VSB3V	GPIO10 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14.

7.18 Edge Detector Enable Register – Index 0x18

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	EN_GP13EDGE	R/W	VSB3V	Enable GPIO13 Edge Detector. If set to 1, enable GPIO13 edge detection. Default is disable.
2	EN_GP12EDGE	R/W	VSB3V	Enable GPIO12 Edge Detector. If set to 1, enable GPIO12 edge detection. Default is disable. If this bit serves as IRQ/SMI#, this bit has no effect.
1	EN_GP11EDGE	R/W	VSB3V	Enable GPIO11 Edge Detector. If set to 1, enable GPIO11 edge detection. Default is disable.
0	EN_GP10EDGE	R/W	VSB3V	Enable GPIO10 Edge Detector. If set to 1, enable GPIO10 edge detection. Default is disable.

7.19 Edge Detector Status Register – Index 0x19

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	STS_GP13EDGE	RW	VSB3V	Indicate GPIO13 Edge Status. If set to 1, the edge of GPIO13 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid.
2	STS_GP12EDGE	RW	VSB3V	Indicate GPIO12 Edge Status. If set to 1, the edge of GPIO12 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. If this bit serves as IRQ/SMI#, this bit has no effect.
1	STS_GP11EDGE	RW	VSB3V	Indicate GPIO11 Edge Status. If set to 1, the edge of GPIO11 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid.
0	STS_GP10EDGE	RW	VSB3V	Indicate GPIO10 Edge Status. If set to 1, the edge of GPIO10 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid.

7.20 IRQ or SMI# Enable Register – Index 0x1A

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	EN_GP13IRQ	R/W	VSB3V	Enable GPIO13 IRQ or SMI# Generation. If this bit set to 1, enable GPIO13 to generate IRQ or SMI#.
2	EN_GP12IRQ	R/W	VSB3V	Enable GPIO12 IRQ or SMI# Generation. If this bit set to 1, enable GPIO12

				to generate IRQ or SMI#.
1	EN_GP11IRQ	R/W	VSB3V	Enable GPIO11 IRQ or SMI# Generation. If this bit set to 1, enable GPIO11 to generate IRQ or SMI#.
0	EN_GP10IRQ	R/W	VSB3V	Enable GPIO10 IRQ or SMI# Generation. If this bit set to 1, enable GPIO10 to generate IRQ or SMI#.

7.21 Output Driving Enable – Index 0x1B

Power-on default [7:0] =0000_1000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	EN_GP13_OBUF	R/W	VSB3V	Enable GPIO13 drive high buffer. If this bit is set to 0, the pin GPIO13 will be I/OD pin, if set to 1 the pin GPIO13 is I/O pin(default).
2	EN_GP12_OBUF	R/W	VSB3V	Enable GPIO12 drive high buffer. If this bit is set to 0, the pin GPIO12 will be I/OD pin, if set to 1 the pin GPIO12 is I/O pin.
1	EN_GP11_OBUF	R/W	VSB3V	Enable GPIO11 drive high buffer. If this bit is set to 0, the pin GPIO11 will be I/OD pin, if set to 1 the pin GPIO11 is I/O pin.
0	EN_GP10_OBUF	R/W	VSB3V	Enable GPIO10 drive high buffer. If this bit is set to 0, the pin GPIO10 will be I/OD pin, if set to 1 the pin GPIO10 is I/O pin.

7.22 Output Driving Enable – Index 0x1C

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
4-7	Reserved			
3	DB_TIME13_SEL	R/W	VSB3V	Select GPIO13 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default).
2	DB_TIME12_SEL	R/W	VSB3V	Select GPIO12 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default).
1	DB_TIME11_SEL	R/W	VSB3V	Select GPIO11 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default).
0	DB_TIME10_SEL	R/W	VSB3V	Select GPIO10 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default).

7.36 VID on the fly offset Register – Index 30h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-5	Reserved	RO	VSB3V	Reserved. Read return 0
4-0	VID_OFFSET	R/W	VSB3V	VID offset register. The offset value is representative in 2's complement. The real VID value will be added by this offset and then will be put into VID_OUT(when EN_OTF is set). The offset ranges from -16 to +15. 0Fh : +15. 01h : +1. 00h : +0. 1Fh : -1. 1Eh : -2. 10h : -16. If want to extend the offset ranges to +31~-32, please set CRF1 bit4

31	011111	**-1**	111111
30	011110	**-2**	111110
29	011101	**-3**	111101
28	011100	**-4**	111100
27	011011	**-5**	111011
26	011010	**-6**	111010
25	011001	**-7**	111001
24	011000	**-8**	111000
23	010111	**-9**	110111
22	010110	**-10**	110110
21	010101	**-11**	110101
20	010100	**-12**	110100
19	010011	**-13**	110011
18	010010	**-14**	110010
17	010001	**-15**	110001
16	010000	**-16**	110000
15	001111	**-17**	101111
14	001110	**-18**	101110
13	001101	**-19**	101101
12	001100	**-20**	101100
11	001011	**-21**	101011
10	001010	**-22**	101010
9	001001	**-23**	101001
8	001000	**-24**	101000

				7	000111	**-25**	100111	
				6	000110	**-26**	100110	
				5	000101	**-27**	100101	
				4	000100	**-28**	100100	
				3	000011	**-29**	100011	
				2	000010	**-30**	100010	
				1	000001	**-31**	100001	
				0	000000	**-32**	100000	

7.37 VID Output Data Register – Index 31h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	EN_VIDOUT	R/W	VSB3V	Enable VIDOUT. If set to one and VID output key is asserted referred as VIDKEY, the VIDOUT_DATA will output to these pins of VIDOUT. This bit is supplied by VSB3V and reset by the VSB3V power good or RSTOUT is asserted or SLOTOCC# is asserted.
6	VIDKEY_OK	RO	VSB3V	When the sequential key is programmed to register 22H. this bit will set to 1. if program exit sequential key to register 22H, this bit read back will be 0
5:0	VIDOUT_DATA	R/W	VSB3V	VIDOUT Data. These bits is mapping to VIDOUT[4:0] if EN_VIDOUT is enable. These bits power is supplied by VSB3V for keeping data when VDD3V power is lose.

7.38 VIDKEY Protection Register – Index 32h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	VIDKEY	R/W	VSB3V	VID Key for protection the VIDOUT. If would like to program VID Output Data Register, the sequential key should be programmed first. The VID Output Register is disable in the default (VSB3V power on). The sequential keys are defined as 0x32, 0x5d, 0x42, 0xac. And the exit key is 0x35.

7.39 VID Input Latch Register – Index 33h

Power-on default [7:0] =000x_xxxxb

Bit	Name	R/W	PWR	Description
7-6	Reserved	RO	--	Reserved, read return 0.
5-0	LVIDIN	RO	VSB3V	VIDIN data.

7.40 RSTOUT Control Register – Index 34h

Power-on default [7:0] =0000_0000b

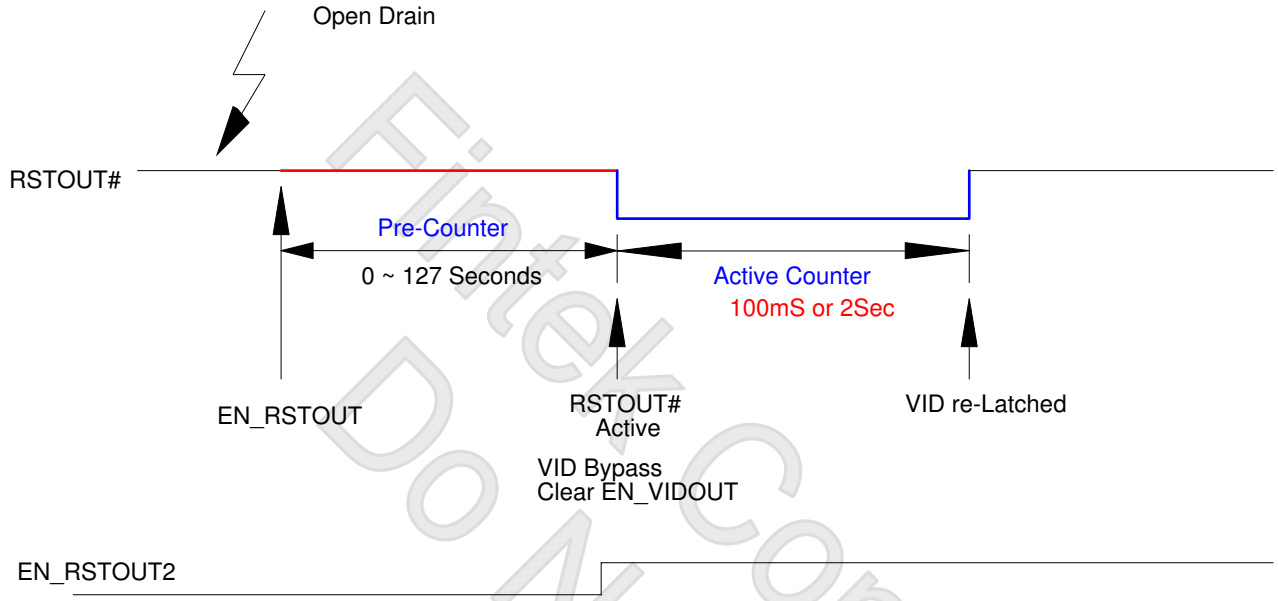
Bit	Name	R/W	PWR	Description
7-3	Reserved	RO		
2	SEL_RST_2S	R/W	VSB3V	When set this bit to 1, the RSTOUT low pulse width is 2 Sec, if set to 0 the low pulse width is 100ms.
1	RSTOUT_OINV	R/W	VSB3V	RSTOUT# output level inverting. When write 1, the output pin will be inverted. Default is low active when time is out.
0	STS_RSTOUT	R/W	VSB3V	Indicate RSTOUT is occurred. Write 1 to clear this bit. Writing 0 is invalid.

7.41 RSTOUT Control Register – Index 35h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	RST_ENABLE	R/W	VSB3V	Enable RESET Output Timer. If set to 1, the RSTOUT timer will be started. When RSTOUT# is asserted, low pulse is occurred, the VID will re-latched and disable EN_VIDOUT. The status of Reset Out is stored in CR02.b1.
6-0	WD1_PTIME	R/W	VSB3V	RSTOUT Pre-counter time in second. 000_0000b – 0 second (Default) 000_0001b – 1 second 000_0010b – 2 seconds : 111_1111b – 127 seconds

Reset Out timing is shown as follows.



Design note:

1. Pre-counter and Active-counter can use same clock source with 10Hz. An 1 second is counted to 10. Two seconds is counted to 20. And so on.
2. Test mode clock is set to CLKIN in external clock. Test clock is set as follows.
   a. Program RSTOUT control register.
   b. Set EN_CLKIN.
   c. Set TESTCLK.
3. Bit 5: Once the RSTOUT# is asserted (negative edge), this bit will be set to 1. Clear signal can be generated by "write_command & write_data[1]==1".

7.42 Watchdog Timer Control Register – Index 36h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	Reserved	RO	VSB3V	Reserved. Read will return 0.
6	STS_WD_TMOUT	R/W	VSB3V	Watchdog is timeout. When the watchdog is timeout, this bit will be set to one. If set to 1, write 1 will clear this bit. Write 0, no effect.
5	WD_ENABLE	R/W	VSB3V	Enable watchdog timer.
4	WD_PULSE	R/W	VSB3V	Watchdog output level or pulse. If set 0 (default), the pin of watchdog is level output. If write 1, the pin will output with a pulse.
3	WD_UNIT	R/W	VSB3V	Watchdog unit select. Default 0 is select second. Write 1 to select minute.
2	WD_HACTIVE	R/W	VSB3V	Program WD output level. If set to 1 and watchdog asserted, the pin will be

				high. If set to 0 and watchdog asserted, this pin will drive low(default).
1-0	WD_PSWIDTH	R/W	VSB3V	Watchdog pulse width selection. If the pin output is selected to pulse mode. The pulse width can be choice. 00b – 1m second. 01b – 20m second. 10b – 100m second 11b – 4 second

The is flexible reset out with watchdog

7.43 Watchdog Timer Range Register – Index 37h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	WD_TIME	R/W	VSB3V	Watchdog timing range from 0 ~ 255. The unit is either second or minute programmed by the watchdog timer control register bit3.

7.44 GPIO3x Output Control Register – Index 40h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	GP33_OCTRL	R/W	VSB3V	GPIO 33 output control
2	GP32_OCTRL	R/W	VSB3V	GPIO 32 output control
1	GP31_OCTRL	R/W	VSB3V	GPIO 31 output control
0	GP30_OCTRL	R/W	VSB3V	GPIO 30 output control

7.45 GPIO3x Output Data Register – Index 41h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero

3	GP33_ODATA	R/W	VSB3V	GPIO 33 output data.
2	GP32_ODATA	R/W	VSB3V	GPIO 32 output data.
1	GP31_ODATA	R/W	VSB3V	GPIO 31 output data.
0	GP30_ODATA	R/W	VSB3V	GPIO 30 output data.

7.46 GPIO3x Input Status Register – Index 42h

Power-on default [7:0] =xxxx_xxxxb

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	GP33_PSTS	RO	VSB3V	Read the GPIO33 data on the pin.
2	GP32_PSTS	RO	VSB3V	Read the GPIO32 data on the pin.
1	GP31_PSTS	RO	VSB3V	Read the GPIO31 data on the pin.
0	GP30_PSTS	RO	VSB3V	Read the GPIO30 data on the pin.

7.47 GPIO3x Level/Pulse Control Register – Index 43h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	GP33_OMODE	R/W	VSB3V	GPIO 33 output mode. 0 – level, 1 – pulse.
2	GP32_OMODE	R/W	VSB3V	GPIO 32 output mode. 0 – level, 1 – pulse.
1	GP31_OMODE	R/W	VSB3V	GPIO 31 output mode. 0 – level, 1 – pulse.
0	GP37_OMODE	R/W	VSB3V	GPIO 30 output mode. 0 – level, 1 – pulse.

7.48 GPIO3x Pulse Width Control Register – Index 44h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7:2	Reserved	R/W	VSB3V	Reserved. Read return 0.
1:0	GP3_PLSWD[1:0]	R/W	VSB3V	GPIO3x pulse width. If set the GPIO3x to pulse mode, the pulse width can be defined as follows.

				00b – 500us (Default) 01b – 1ms 10b – 20ms 11b – 100ms

7.49 GPIO3x Input De-bounce Register – Index 46h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	GP33_ENDB	R/W	VSB3V	Enable GPIO33 input de-bounce with 7u or 25ms second that selected by 0x4C bit3.
2	GP32_ENDB	R/W	VSB3V	Enable GPIO32 input de-bounce with 7u or 25ms second that selected by 0x4C bit2.
1	GP31_ENDB	R/W	VSB3V	Enable GPIO31 input de-bounce with 7u or 25ms second that selected by 0x4C bit1.
0	GP30_ENDB	R/W	VSB3V	Enable GPIO30 input de-bounce with 7u or 25ms second that selected by 0x4C bit0.

7.50 GPIO3x Pulse Inverse Register – Index 47h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	GP33_PULSINV	R/W	VSB3V	GPIO33 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR44.
2	GP32_PULSINV	R/W	VSB3V	GPIO32 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR44.
1	GP31_PULSINV	R/W	VSB3V	GPIO 31 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR44.
0	GP30_PULSINV	R/W	VSB3V	GPIO30 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR44.

7.51 GP3x Edge Detector Enable Register – Index 0x48

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	EN_GP33EDGE	R/W	VSB3V	Enable GPIO33 Edge Detector. If set to 1, enable GPIO33 edge detection. Default is disable.
2	EN_GP32EDGE	R/W	VSB3V	Enable GPIO32 Edge Detector. If set to 1, enable GPIO32 edge detection. Default is disable.
1	EN_GP31EDGE	R/W	VSB3V	Enable GPIO31 Edge Detector. If set to 1, enable GPIO31 edge detection. Default is disable.
0	EN_GP30EDGE	R/W	VSB3V	Enable GPIO30 Edge Detector. If set to 1, enable GPIO30 edge detection. Default is disable.

7.52 Edge Detector Status Register – Index 0x49

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	STS_GP33EDGE	R/W	VSB3V	Indicate GPIO33 Edge Status. If set to 1, the edge of GPIO33 has occurred. Write 1 to clear this bit. Writing 0 is invalid.
2	STS_GP32EDGE	R/W	VSB3V	Indicate GPIO32 Edge Status. If set to 1, the edge of GPIO32 has occurred. Write 1 to clear this bit. Writing 0 is invalid.
1	STS_GP31EDGE	R/W	VSB3V	Indicate GPIO31 Edge Status. If set to 1, the edge of GPIO31 has occurred. Write 1 to clear this bit. Writing 0 is invalid.
0	STS_GP30EDGE	R/W	VSB3V	Indicate GPIO10 Edge Status. If set to 1, the edge of GPIO30 has occurred. Write 1 to clear this bit. Writing 0 is invalid.

7.53 IRQ or SMI# Enable Register – Index 0x4A

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	EN_GP33IRQ	R/W	VSB3V	Enable GPIO33 IRQ or SMI# Generation. If this bit set to 1, enable GPIO33 to generate IRQ or SMI#.
2	EN_GP32IRQ	R/W	VSB3V	Enable GPIO32 IRQ or SMI# Generation. If this bit set to 1, enable GPIO32 to generate IRQ or SMI#.
1	EN_GP31IRQ	R/W	VSB3V	Enable GPIO31 IRQ or SMI# Generation. If this bit set to 1, enable GPIO31 to generate IRQ or SMI#.
0	EN_GP30IRQ	R/W	VSB3V	Enable GPIO30 IRQ or SMI# Generation. If this bit set to 1, enable GPIO30 to generate IRQ or SMI#.

7.54 Output Driving Enable – Index 0x4C

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-4	Reserved	RO	VSB3V	Read back will be zero
3	DB_TIME33_SEL	R/W	VSB3V	Select GPIO33 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default).
2	DB_TIME32_SEL	R/W	VSB3V	Select GPIO32 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default).
1	DB_TIME31_SEL	R/W	VSB3V	Select GPIO31 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default).
0	DB_TIME30_SEL	R/W	VSB3V	Select GPIO30 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default).

7.55 CHIPID(1) Register – Index 5Ah

Power-on default [7:0] =0000_0011b

Bit	Name	R/W	PWR	Description
7-0	CHIPID	RO	VSB3V	Chip ID, High byte (8'h03).

7.56 CHIPID(2) Register – Index 5Bh

Power-on default [7:0] =0000_0001b

Bit	Name	R/W	PWR	Description
7-0	CHIPID	RO	VSB3V	Chip ID, Low byte (8'h01).

7.57 VENDOR ID(1) Register – Index 5Dh

Power-on default [7:0] =0001_1001b

Bit	Name	R/W	PWR	Description
7-0	VENDOR1	RO	VSB3V	Vendor ID, 8'h19

7.58 VENDOR ID(2) Register – Index 5Eh

Power-on default [7:0] =0011_0100b

Bit	Name	R/W	PWR	Description
7-0	VENDOR2	RO	VSB3V	Vendor ID, 8h34

7.59 Register – Index F1h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	EN_RST_GPIO	R/W	VSB3V	Set this bit to 1 will enable reset out timer to clear GPIO data and in-out control register.
6	EN_WD_GPIO	R/W	VSB3V	Set this bit to 1 will enable watchdog timer to clear GPIO data and in-out control register.
5	Reserved	R/W	VSB3V	Fintek test mode use only

4	VID_EXTEND	R/W	VSB3V	VID offset extend bit.
3-0	Reserved	R/W	VSB3V	Fintek test mode use only

8. Electron Characteristic

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 4.0	V
Input Voltage	-0.5 to 5.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

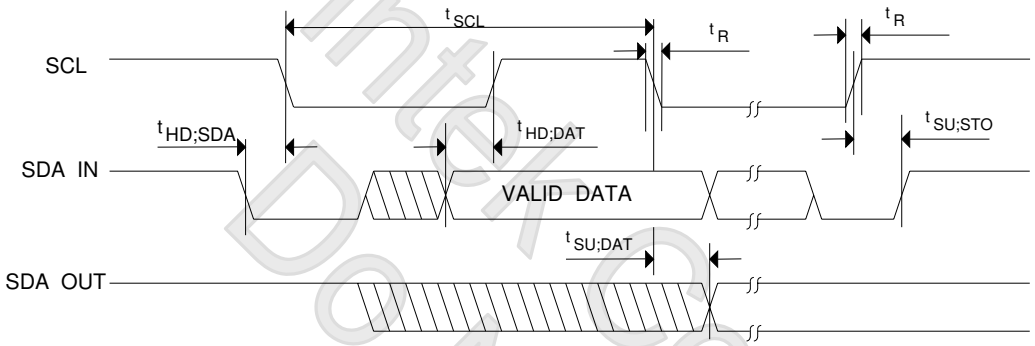
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = - 12 mA
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3 V
Hysteresis	VTH	0.5	1.2		V	VDD = 3.3 V

Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = - 12 mA
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0V

8.2 DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
OD_{16} - Open-drain output pin with sink capability of 16 mA						
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
IN_t - TTL level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
IN_{lv} - Low level input pin						
Input Low Voltage	VIL	0.6	0.8		V	
Input High Voltage	VIH		0.9	1.0	V	
Input High Leakage	ILIH			+1	μA	VIN = 1.2V
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3V
Hysteresis	VTH	0.5	1.2		V	VDD = 3.3 V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V

8.3 AC Characteristics



Serial Bus Timing Diagram

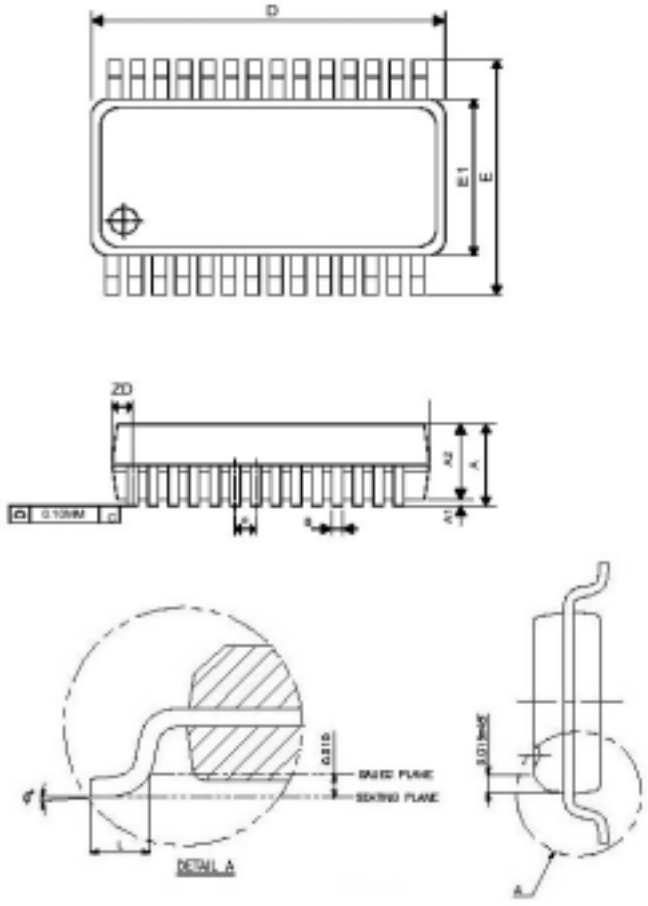
Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

9. Ordering Information

Part Number	Package Type	Production Flow
F75122RG	28 PIN SSOP (Green Package)	Commercial, 0°C to +70°C
F75122R	28 PIN SSOP	Commercial, 0°C to +70°C

10. Package Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			0.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025BASIC		
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
H	0.25		0.50	0.010		0.020
ZD	0.838 REF			0.033 REF		
θ	0^0		8^0	0^0		8^0

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Application circuit