

F75113

Low Power GPIO with LED Function

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Version: V0.13P

F75113 Datasheet Revision History

| Version | Date | Page | Revision History |
|---------|---------|--|--|
| V0.10P | 2010/12 | | Preliminary version |
| V0.11P | 2011/01 | 4, 8 63-65 91-92 | 1. Add SERIRQ on F75113U pin5 2. Add Register 50 ~ 54h 3. Update Reference Circuits |
| V0.12P | 2011/07 | 17, 21 30, 31 39, 40 48, 49 59, 60 74, 75 68 68 84 87 | 1. Update Global Control Register for LPC Interface 2. Update GPIO0X Input De-bounce Register — Index 16h 3. Update GPIO1X Input De-bounce Register — Index 26h 4. Update GPIO2X Input De-bounce Register — Index 36h 5. Update GPIO3X Input De-bounce Register — Index 46h 6. Update GPIO4X Input De-bounce Register — Index 76h 7. Add Chip ID1 & ID 2 Register — Index 5Ah, 5Bh 8. Add Vendor ID1 & ID2 Register — Index 5Dh, 5Eh 9. Delete 32 QFN Package 10. Update Reference Circuits (for SPI) |
| V0.13P | 2011/12 | | 1. Made Clarification and Correction 2. Modify Pin 9~16 Type |
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LIFE SUPPORT APPLICATIONS

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1. General Description

F75113 is a low power general purpose IO chip providing 40 GPIO. Level or pulse mode can be programmed by registers so all GPIO can be programmed to logic one, zero, high pulse or low pulse. GPIO0X~GPIO2X can be programmed to be power LED. F75113 includes two sets of watchdog timer for system reset. Besides, two power-down modes (Manual or Smart) can be selected to save power and control the total consumption under 10uA, so F75113 can fit the requirement of mobile device such as PDA or cell phone.

2. Features

- Support up to 40 GPIO pins
- Each GPIO pin can be programmed to be high/low level or pulse mode
- Each GPIO pin has de-bounce function
- Support 8 GPIO pins for low level($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) input mode
- 24 pins can be programmed to be LED
- 8 pins has SMI function
- Two sets of watchdog timer
- Two power down mode selection --- Manual or Smart Power Management mode
- Support LPC/SMBus/SPI interface
- Package in 48-TQFP

3. Key Specifications

- Supply Voltage 3.0V to 3.6V
- Operating Supply Current

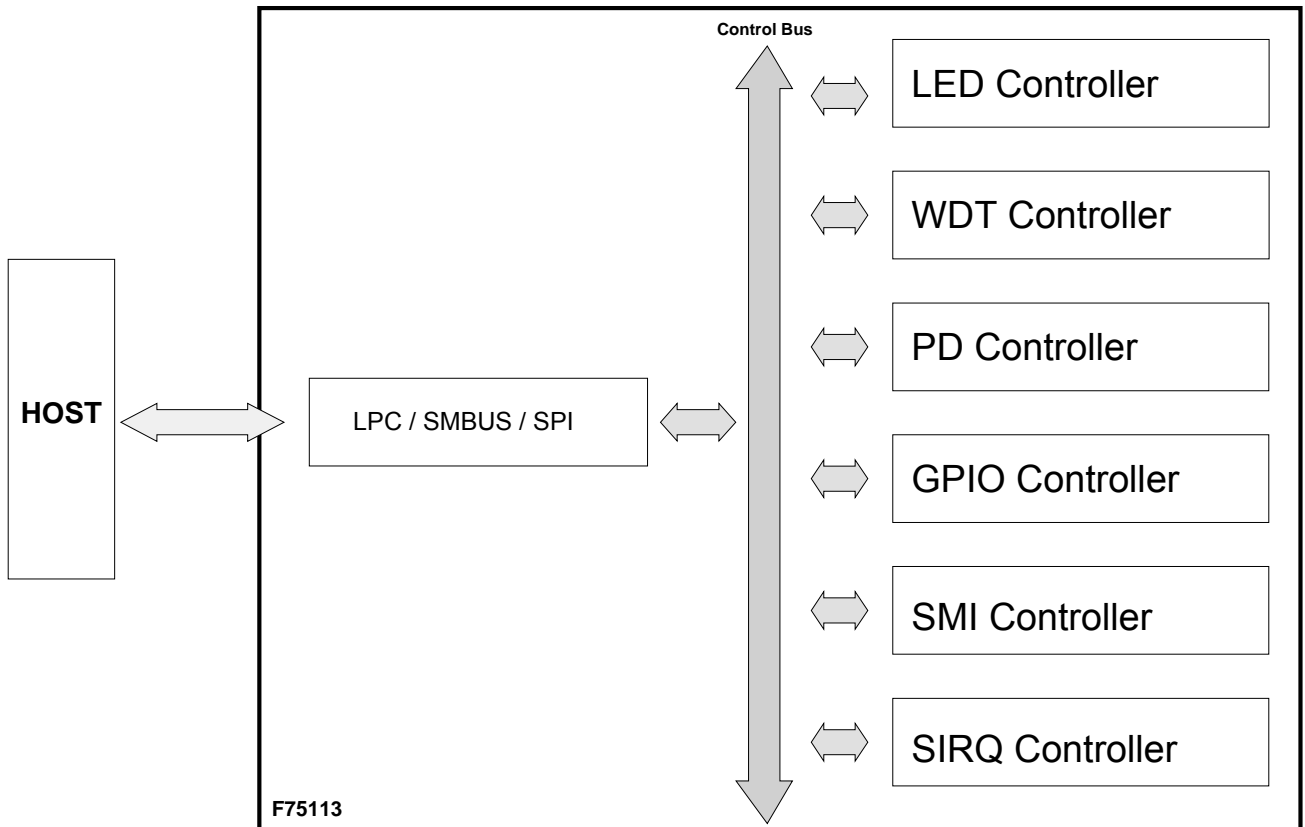
Testing Condition: 1. Enable Smart Power-Down

2. Access 1 Register per 100 ms for Each Interface

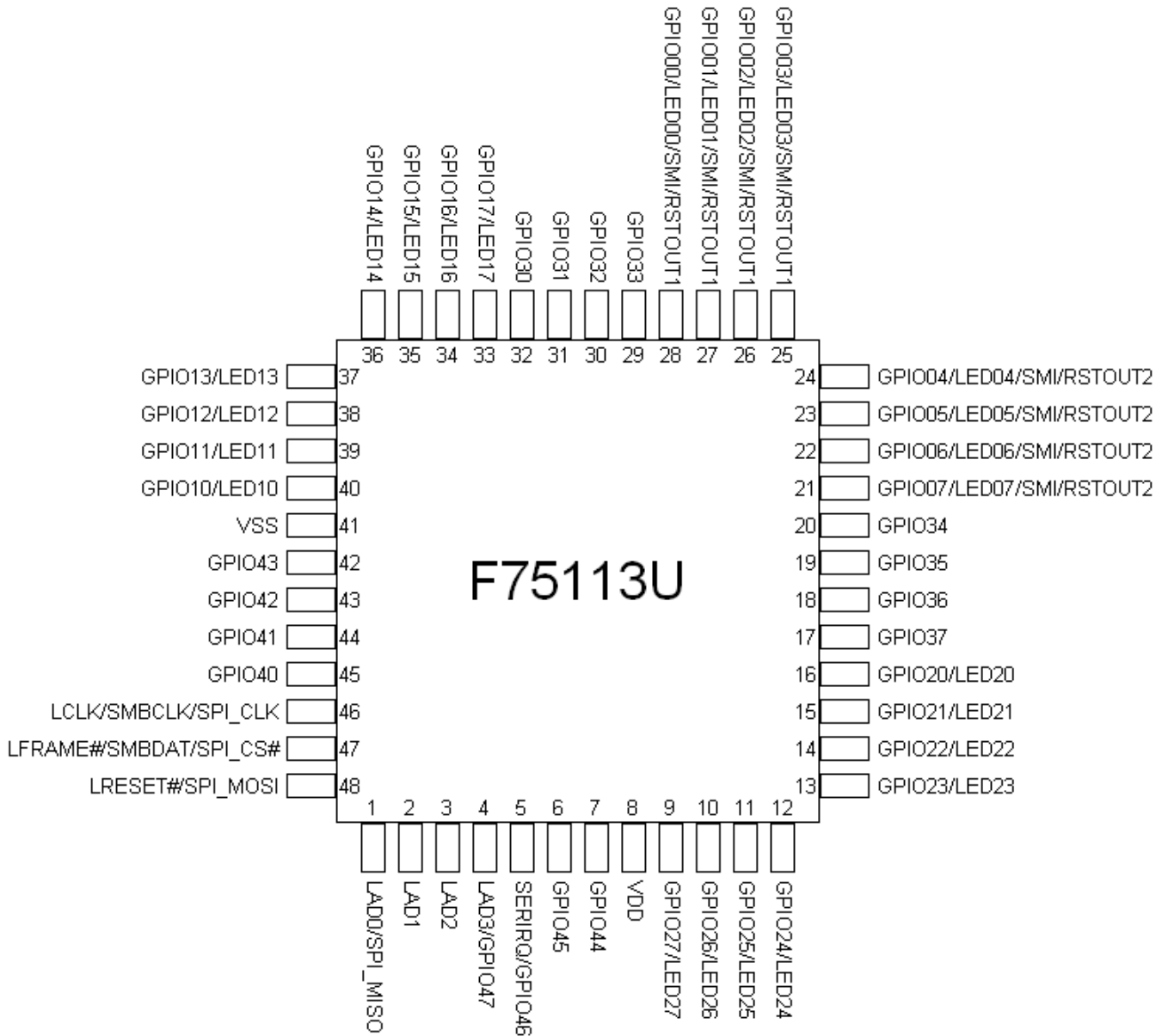
| Interface | Operation current (Max.) |
|-----------|--------------------------|
| LPC | 2mA |
| SPI | 100uA |
| SMBus | 100uA |

- Power Down Current 10uA typ.

4. Block Diagram



5. Pin Configuration



6. Pin Description

| | |
|-------------------------|--|
| I/O _{16st5v} | TTL level bi-directional pin with schmitt trigger, 16 mA source-sink capability and 5V tolerance |
| I/OOD _{16st5v} | TTL level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 16 mA source-sink capability and 5v tolerance |
| I/OD _{16st5v} | TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5v tolerance |
| O _{16-5v} | Output pin with 16 mA source-sink capability, 5V tolerance. |
| OOD _{16-5v} | OD or OUT selected by register with 16 mA sink capability, 5V tolerance. |
| IN _{st.5v} | TTL level input pin with schmitt trigger, 5V tolerance. |
| IN _v | Low Level input pin |
| AIN | Input pin (Analog) |
| P | Power |

6.1 Power Pin

| Pin No. | Pin Name | Type | Description |
|---------|----------|------|---|
| 08 | VDD | P | Standard Power Supply Voltage Input with 3.3V |
| 41 | VSS | P | GND |

6.2 GPIO Function

| Pin No. | Pin Name | Type | PWR | Description |
|-------------------------------------|--|-------------------------|-----|---|
| 21,22, 23,24 | GPIO07, GPIO06, GPIO05, GPIO04 | I/OOD _{16st5v} | VDD | General purpose I/O pins. |
| | LED07, LED06, LED05, LED04 | OOD _{16-5v} | VDD | Power LED. Blink frequency selection and LED function selected by register setting. |
| | RSTOUT2 | OOD _{16-5v} | VDD | WDT2 Resetout signal output. |
| 25,26, 27,28 | GPIO03, GPIO02, GPIO01, GPIO00 | I/OOD _{16st5v} | VDD | General purpose I/O pins. |
| | LED03, LED02, LED01, LED00 | OOD _{16-5v} | VDD | Power LED. Blink frequency selection and LED function selected by register setting. |
| | RSTOUT1 | OOD _{16-5v} | VDD | WDT1 Resetout signal output. |
| 33,34, 35,36, 37,38, 39,40 | GPIO17, GPIO16, GPIO15, GPIO14, | I/OOD _{16st5v} | VDD | General purpose I/O pins. |

| | | | | |
|-------------------------------------|---|--|-----|---|
| | GPIO13, GPIO12, GPIO11, GPIO10 | | | |
| | LED17, LED16, LED15, LED14, LED13, LED12, LED11, LED10 | OOD _{16-5v} | VDD | Power LED. Blink frequency selection and LED function selected by register setting. |
| 09 | GPIO27, | I/OOD _{16st,5v} IN _{lv} | VDD | General purpose I/O pins. The GPIO2X port support low level input signal by register 0x3Fh setting. |
| | LED27 | OOD _{16-5v} | VDD | Power LED. Blink frequency selection and LED function selected by register setting. |
| 10, 11, 12, 13, 14, 15, 16 | GPIO26, GPIO25, GPIO24, GPIO23, GPIO22, GPIO21, GPIO20 | I/OOD _{16st,5v} IN _{lv} | VDD | General purpose I/O pins. The GPIO2X port support low level input signal by register 0x3Fh setting. |
| | LED26, LED25, LED24, LED23, LED22, LED21, LED20 | OOD _{16-5v} | VDD | Power LED. Blink frequency selection and LED function selected by register setting. |
| 29,30, 31,32 | GPIO33, GPIO32, GPIO31, GPIO30 | I/OOD _{16st5v} | VDD | General purpose I/O pins. |
| 17, 18, 19,20 | GPIO37, GPIO36, GPIO35, GPIO34 | I/OOD _{16st5v} | VDD | General purpose I/O pins. |
| 42,43, 44, 45 | GPIO43, GPIO42, GPIO41, GPIO40 | I/OOD _{16st5v} | VDD | General purpose I/O pins. |
| 06, 07 | GPIO45, GPIO44 | I/OOD _{16st5v} | VDD | General purpose I/O pins. |

6.3 Access Interface

| Pin No. (F75113U) | Pin Name | Type | PWR | Description |
|----------------------|---------------|-------------------------|-----|--|
| 46 | LCLK | IN _{st5v} | VDD | LPC clock input. |
| | SMBCLK | IN _{st5v} | VDD | SMBus clock. |
| | SPI_CLK | IN _{st5v} | VDD | SPI clock. |
| 47 | LFRAME# | IN _{st5v} | VDD | LPC LFRAME# signal. |
| | SMBDAT | I/OD _{16st5v} | VDD | SMBus data |
| | SPI_CS# | IN _{st5v} | VDD | SPI chip select |
| 48 | LRESET# | IN _{st5v} | VDD | LPC reset signal |
| | SPI_MOSI | IN _{st5v} | VDD | SPI master output, slave input |
| 01 | LAD0 | I/O _{16st5v} | VDD | LPC LAD signal. |
| | SPI_MISO | O _{16-5v} | VDD | SPI master input, slave output |
| 02,03 | LAD1, LAD2 | I/O _{16st5v} | VDD | LPC LAD signal. |
| 04 | LAD3 | I/O _{16st5v} | VDD | LPC LAD signal. |
| | GPIO47 | I/OOD _{16st5v} | VDD | General purpose I/O pin. |
| 05 | SERIRQ | I/O _{16st5v} | VDD | Serial IRQ input/Output. (for LPC interface) |
| | GPIO46 | I/OOD _{16st5v} | VDD | General purpose I/O pin. |

7. Functional Description

Access Interface

The F75113 provides three auto-detected access interfaces, LPC, SMBus or SPI, to read/write internal registers. In LPC interface, the default address of Configuration Register I/O port is 2Eh. When user writes data 10h to LPC configuration register 27h, the address of Configuration Register I/O port will be 4Eh. In SMBus interface, Serial Bus address default value is 6Eh (0110_1110). Another SPI interface only care the least eight bits (LSB) of 24 bits address. SPI interface write register by 02h instruction (Page Program) and read register by 03h instruction (Read Data). Also SPI interface supported byte write/read function.

Besides, the pin 46, 47, 48, 1, 2, 3, 4 are multi-function pins. If user want to access internal register by LPC interface, the F75113 will only supported 39 GPIO function and the pin 4 won't be used for GPIO function. If user wants to access internal register by SMBus interface, the pin 48, 1, 2, 3 must be set internal pull-high with 10KΩ. When user don't use the pin 4 (GPIO function), the pin will must be set internal pull-high. In SPI interface, the pin 2, 3 must be set internal pull-high with 10KΩ. Also, the pin 4 will be selectively set internal pull-high with 10KΩ by user.

GPIO Function

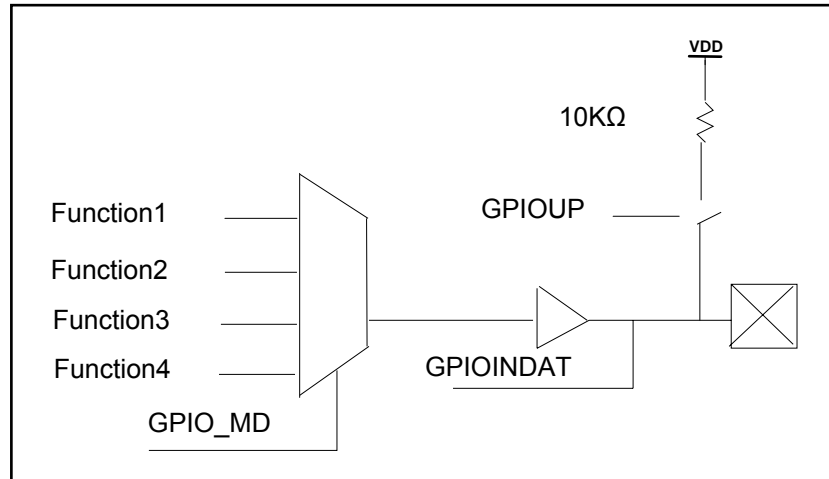
The F75113 with GPIO0X~GPIO4X General Purpose I/O port is composed of independent I/O pins controlled and controls multi-pin function by Index 02~06h register. Each of GPIO group has input capability, output (push-pull and open-drain) capability, internal pull-up resister with 10KΩ. Also F75113 has GPIO2x groups with the Low Level Input, LED, SMI and RSTOUT function. Please check below table how to select the GPIO multi-function pin that user wants.

F75113

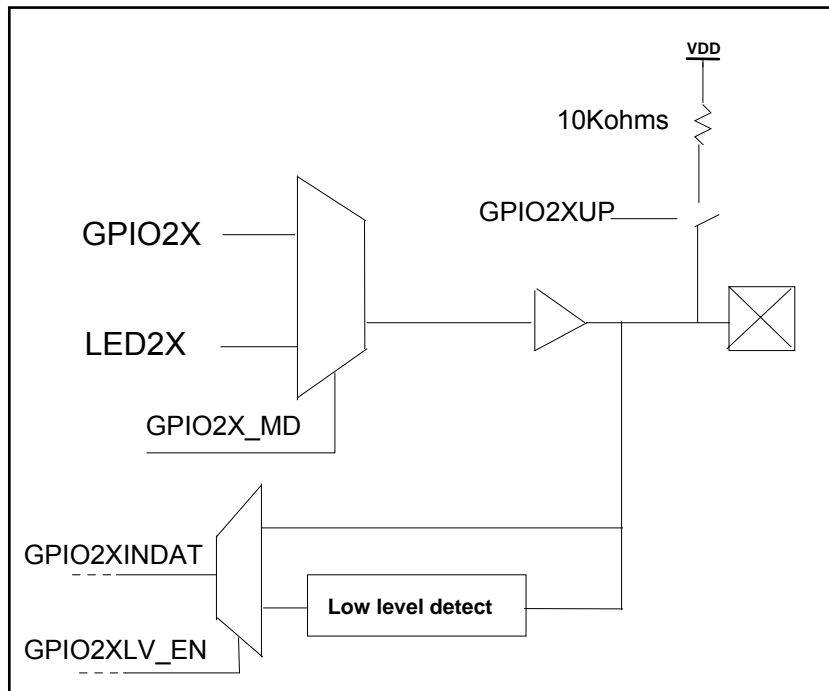
| Group | Pin | Function1 | Condition | Function2 | Condition | Function3 | Condition | Function4 | Condition | Pull Cap | |
|-------|-----|-----------|--|--|-----------|-------------|-----------|-------------|-----------|-------------|----|
| GPIO0 | 0 | 28 | GPIO00 | GPIO00_MD=0 | LED00 | GPIO00_MD=1 | SMI | GPIO00_MD=2 | RSTOUT1 | GPIO00_MD=3 | UP |
| | 1 | 27 | GPIO01 | GPIO01_MD=0 | LED01 | GPIO01_MD=1 | SMI | GPIO01_MD=2 | RSTOUT1 | GPIO01_MD=3 | UP |
| | 2 | 26 | GPIO02 | GPIO02_MD=0 | LED02 | GPIO02_MD=1 | SMI | GPIO02_MD=2 | RSTOUT1 | GPIO02_MD=3 | UP |
| | 3 | 25 | GPIO03 | GPIO03_MD=0 | LED03 | GPIO03_MD=1 | SMI | GPIO03_MD=2 | RSTOUT1 | GPIO03_MD=3 | UP |
| | 4 | 24 | GPIO04 | GPIO04_MD=0 | LED04 | GPIO04_MD=1 | SMI | GPIO04_MD=2 | RSTOUT2 | GPIO04_MD=3 | UP |
| | 5 | 23 | GPIO05 | GPIO05_MD=0 | LED05 | GPIO05_MD=1 | SMI | GPIO05_MD=2 | RSTOUT2 | GPIO05_MD=3 | UP |
| | 6 | 22 | GPIO06 | GPIO06_MD=0 | LED06 | GPIO06_MD=1 | SMI | GPIO06_MD=2 | RSTOUT2 | GPIO06_MD=3 | UP |
| | 7 | 21 | GPIO07 | GPIO07_MD=0 | LED07 | GPIO07_MD=1 | SMI | GPIO07_MD=2 | RSTOUT2 | GPIO07_MD=3 | UP |
| GPIO1 | 0 | 40 | GPIO10 | GPIO10_MD=0 | LED10 | GPIO10_MD=1 | | | | | UP |
| | 1 | 39 | GPIO11 | GPIO11_MD=0 | LED11 | GPIO11_MD=1 | | | | | UP |
| | 2 | 38 | GPIO12 | GPIO12_MD=0 | LED12 | GPIO12_MD=1 | | | | | UP |
| | 3 | 37 | GPIO13 | GPIO13_MD=0 | LED13 | GPIO13_MD=1 | | | | | UP |
| | 4 | 36 | GPIO14 | GPIO14_MD=0 | LED14 | GPIO14_MD=1 | | | | | UP |
| | 5 | 35 | GPIO15 | GPIO15_MD=0 | LED15 | GPIO15_MD=1 | | | | | UP |
| | 6 | 34 | GPIO16 | GPIO16_MD=0 | LED16 | GPIO16_MD=1 | | | | | UP |
| | 7 | 33 | GPIO17 | GPIO17_MD=0 | LED17 | GPIO17_MD=1 | | | | | UP |
| GPIO2 | 0 | 16 | GPIO20/LV_IN | GPIO20_MD=0 | LED20 | GPIO20_MD=1 | | | | | UP |
| | 1 | 15 | GPIO21/LV_IN | GPIO21_MD=0 | LED21 | GPIO21_MD=1 | | | | | UP |
| | 2 | 14 | GPIO22/LV_IN | GPIO22_MD=0 | LED22 | GPIO22_MD=1 | | | | | UP |
| | 3 | 13 | GPIO23/LV_IN | GPIO23_MD=0 | LED23 | GPIO23_MD=1 | | | | | UP |
| | 4 | 12 | GPIO24/LV_IN | GPIO24_MD=0 | LED24 | GPIO24_MD=1 | | | | | UP |
| | 5 | 11 | GPIO25/LV_IN | GPIO25_MD=0 | LED25 | GPIO25_MD=1 | | | | | UP |
| | 6 | 10 | GPIO26/LV_IN | GPIO26_MD=0 | LED26 | GPIO26_MD=1 | | | | | UP |
| | 7 | 09 | GPIO27/LV_IN | GPIO27_MD=0 | LED27 | GPIO27_MD=1 | | | | | UP |
| GPIO3 | 0 | 32 | GPIO30 | | | | | | | | UP |
| | 1 | 31 | GPIO31 | | | | | | | | UP |
| | 2 | 30 | GPIO32 | | | | | | | | UP |
| | 3 | 29 | GPIO33 | | | | | | | | UP |
| | 4 | 20 | GPIO34 | | | | | | | | UP |
| | 5 | 19 | GPIO35 | | | | | | | | UP |
| | 6 | 18 | GPIO36 | | | | | | | | UP |
| | 7 | 17 | GPIO37 | | | | | | | | UP |
| GPIO4 | 0 | 45 | GPIO40 | | | | | | | | UP |
| | 1 | 44 | GPIO41 | | | | | | | | UP |
| | 2 | 43 | GPIO42 | | | | | | | | UP |
| | 3 | 42 | GPIO43 | | | | | | | | UP |
| | 4 | 07 | GPIO44 | | | | | | | | UP |
| | 5 | 06 | GPIO45 | | | | | | | | UP |
| | 6 | 05 | SIRQ/GPIO46 | Can't use GPIO46 under LPC interface | | | | | | | |
| 7 | 04 | GPIO47 | Can't use GPIO47 under LPC interface | | | | | | | | UP |

F75113

F75113 provides multi-function to system control by GPIO0X_MD, GPIO1X_MD or GPIO2X_MD setting. There is a figure describe how multi-function pin will be applied to F75113.

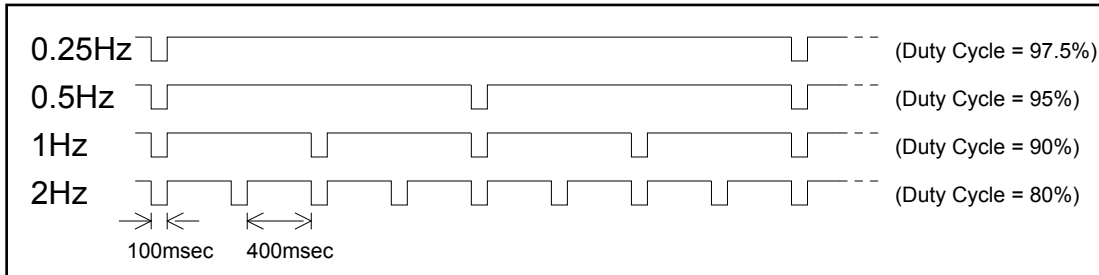


F75113 provides eight low level input pins at GPIO2X port. There is a figure describe how low level input will be designed.



LED Function

F75113 provides 24 pin LED (GPIO0X~GPIO2X) display for system control. The LED blinked by 0.25Hz, 0.5Hz, 1Hz and 2Hz with open drain capability (Default). There is a figure describe how the LEDs will perform.



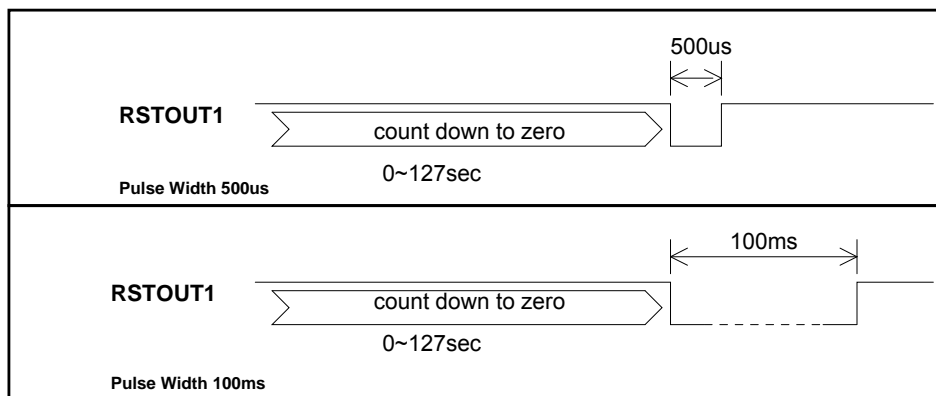
SMI Function

F75113 provides 7 SMI output pins for system control. Also, SMI can be programming to level mode or pulse mode. In pulse mode, users can select 200us or 150ms pulse width for SMI output. Then, the SMI can be triggered by any of the GPIO0X ~ GPIO4X pins.

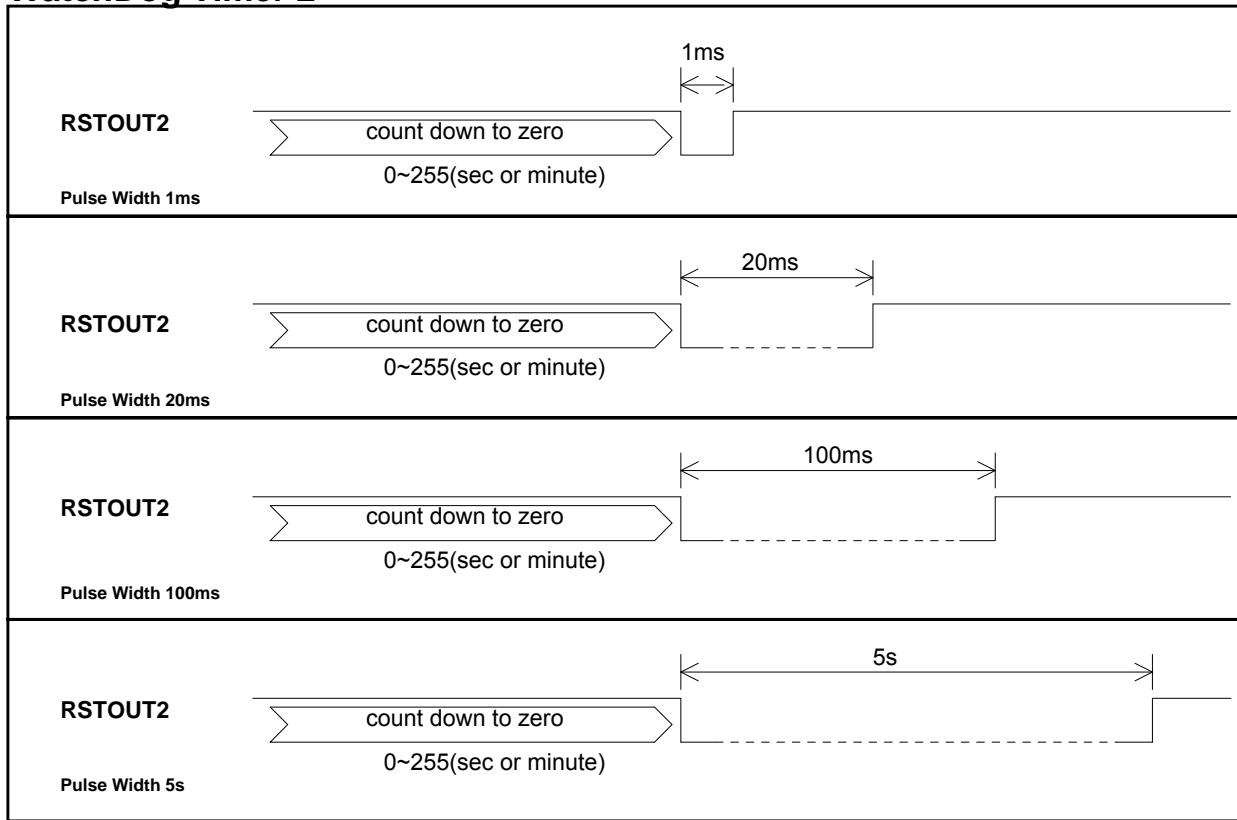
WatchDog Timer Function

F75113 provides two sets of WatchDog Timers for system reset. The watchdog timer1 timeout unit is set to second and range is 0 to 127 seconds. When the timeout has occurred, that will generate a active pulse signal or level signal. There is a figure describe how WatchDog Timer output RSTOUT signal.

WatchDog Timer 1

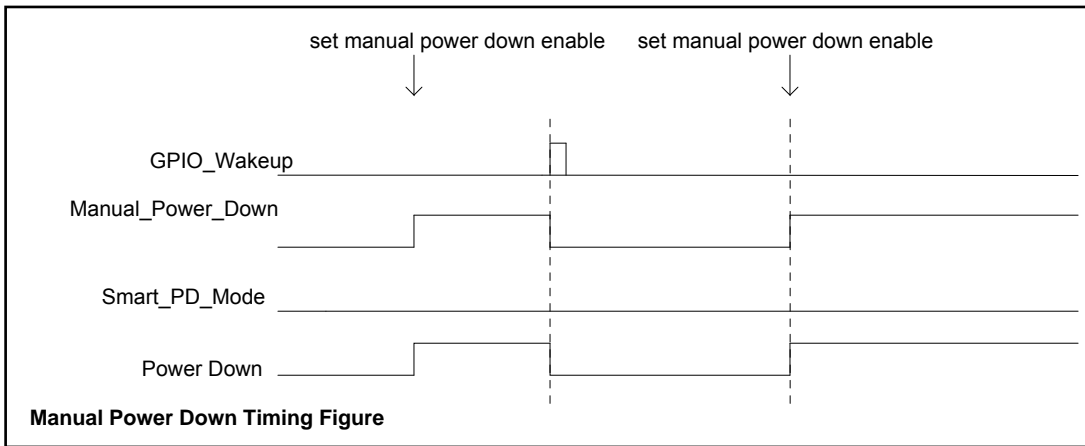
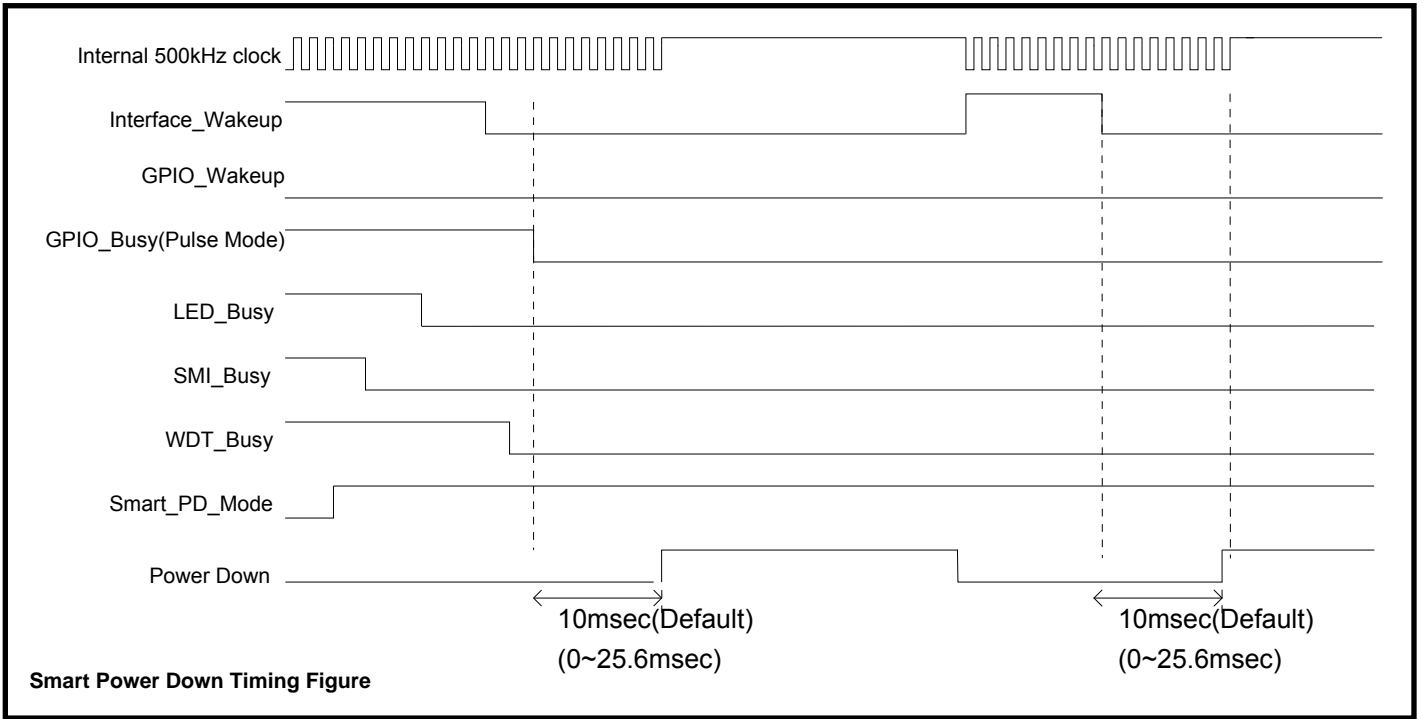


The watchdog timer2 timeout unit is set to second or minutes and range is 0 to 255. When the timeout has occurred, that will generate a active pulse signal or level signal.

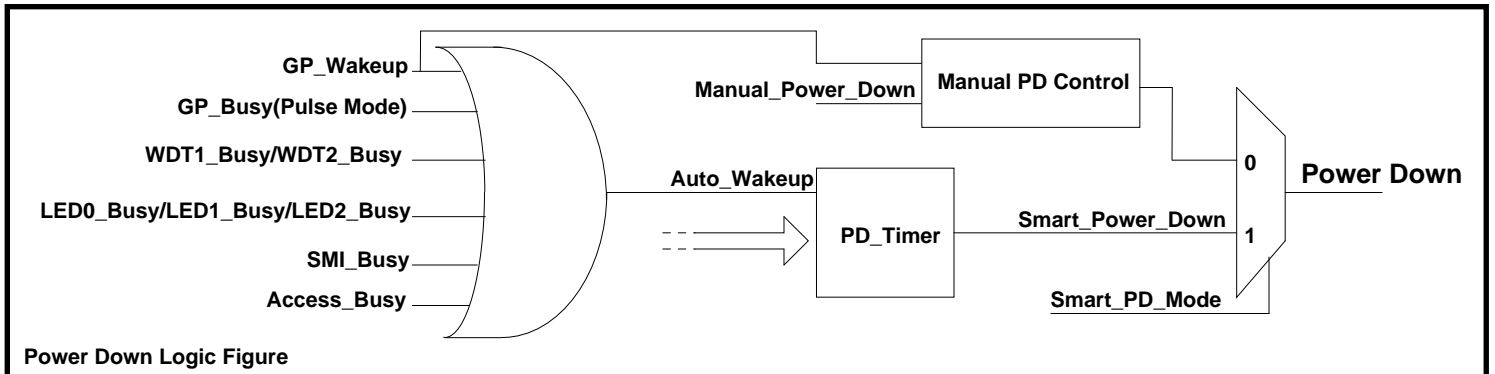
WatchDog Timer 2

Power-Down Control Function

F75113 provides smart power down and manual power down. In the smart power down mode, if all functions idle more than 10ms (Default 63h), the chip would auto power down. Also, it would wakeup when GPIO state change or read/write the registers. There is a figure describe how F75113 Auto-Power-Down the system.

In manual power down, if users set bit 0 to one at index 01h of Configuration Registers, the F75113 will be power down instantly. There is a figure describe how F75113 Power-Down the system in manual power down mode.



Below figure describes F75113 Power-Down design function.



8. Register Description

When users access internal registers by LPC interface, the configuration register will be used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 2Eh and 2Fh respectively. Write data 10h in index 27h of global control register to change the default value to 4Eh/4Fh. To enable configuration, the entry key 50h must be written to the index port. To disable configuration, write exit key AAh to the index port. Following is an example to enable configuration and disable configuration by using debug.

```
-o 2e 50
-o 2e 50          (enable configuration)
-o 2e aa          (disable configuration)
```

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

Global Control Registers_(for LPC interface)

“-“ Reserved or Tri-State

| Global Control Registers | | | | | | | | | |
|--------------------------|------------------------------------|---------------|---|---|---|---|---|---|-----|
| Register 0x[HEX] | Register Name | Default Value | | | | | | | |
| | | MSB | | | | | | | LSB |
| 07 | Logic Device Number Register (LDN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20 | Chip ID Register | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 21 | Chip ID Register | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 23 | Vendor ID Register | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 24 | Vendor ID Register | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 27 | Configuration Port Select Register | - | - | - | 0 | - | - | - | - |
| 30 | Base Address Enable | - | - | - | - | - | - | - | 0 |

8.1.1 Global – Logic Device Number Register - Index 07h

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|---|
| 7-0 | LDN | R/W | 00h | 00h: Global control registers. 01h: Select GPIO control registers. |

8.1.2 Global – Chip ID Register - Index 20h

| Bit | Name | R/W | Default | Description |
|-----|----------|-----|---------|----------------------|
| 7-0 | CHIP_ID1 | R | 10h | Chip ID 1 of F75113. |

8.1.3 Global – Chip ID Register - Index 21h

| Bit | Name | R/W | Default | Description |
|-----|----------|-----|---------|----------------------|
| 7-0 | CHIP_ID2 | R | 11h | Chip ID 1 of F75113. |

8.1.4 Global – Vendor ID Register - Index 23h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|--------------------------------|
| 7-0 | VENDOR_ID1 | R | 19h | Vendor ID 1 of Fintek devices. |

8.1.5 Global – Vendor ID Register - Index 24h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|--------------------------------|
| 7-0 | VENDOR_ID2 | R | 34h | Vendor ID 2 of Fintek devices. |

8.1.5 Global – Configuration Port Select Register - Index 27h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|-------------------------------------|
| 7-5 | Reserved | - | - | Reserved |
| 4 | CFG_PORT_SEL | R/W | 0 | Configuration Port Select Register. |
| 3-0 | Reserved | - | - | Reserved |

8.1.5 Global – Base Address Enable Register - Index 30h

| Bit | Name | R/W | Default | Description |
|-----|----------|-----|---------|----------------------|
| 7-1 | Reserved | - | - | Reserved |
| 0 | BADDR_EN | R/W | 0 | Base Address Enable. |

GPIO Control Registers

If users want to access GPIO configuration register, the index 07h of LPC global control registers must be write data 01h. When the Base address enable register was write data 01h, the entry key will be unnecessary and users can get GPIO port status or let GPIO port output data immediately.

“-” Reserved or Tri-State

| GPIO Device Configuration Registers (LDN 01h) | | | | | | | | | |
|---|---|---------------|---|---|---|-----|---|---|---|
| Register 0x[HEX] | Register Name | Default Value | | | | | | | |
| | | MSB | | | | LSB | | | |
| 00 | Reserved | - | - | - | - | - | - | - | - |
| 01 | Chip control Register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 02 | GPIO0X mode control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03 | GPIO0X mode control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04 | GPIO1X mode control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05 | GPIO1X mode control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06 | GPIO2X mode control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08 | WDT1 control Register | - | - | - | - | - | 0 | - | 0 |
| 09 | WDT1 count Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0A | WDT2 control Register | - | - | 0 | 0 | 0 | 0 | 0 | 0 |
| 0B | WDT2 count Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0C | PD count Register | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0E | Reserved | - | - | - | - | - | - | - | - |
| 0F | Reserved | - | - | - | - | - | - | - | - |
| 10 | Chip control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | GPIO0X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | GPIO0X pin status Register | - | - | - | - | - | - | - | - |
| 13 | GPIO0X Level / Pulse Control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14 | GPIO0X pulse width control Register | - | - | - | - | - | - | 0 | 0 |
| 15 | GPIO0X internal pull-high enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | GPIO0X debounce enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17 | GPIO0X pin inverse enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18 | GPIO0X edge detect enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19 | GPIO0X edge detect status Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1A | SMI event of GPIO0X port enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1B | GPIO0X output buffer enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1C | GPIO0X debounce timing select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1D | LED0X frequency select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1E | LED0X frequency select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20 | GPIO1X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21 | GPIO1X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 22 | GPIO1X pin status Register | - | - | - | - | - | - | - | - |

| | | | | | | | | | |
|----|---|---|---|---|---|---|---|---|---|
| 23 | GPIO1X Level / Pulse Control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24 | GPIO1X pulse width control Register | - | - | - | - | - | - | 0 | 0 |
| 25 | GPIO1X internal pull-high enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 26 | GPIO1X debounce enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 27 | GPIO1X pin inverse enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28 | GPIO1X edge detect enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 29 | GPIO1X edge detect status Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2A | SMI event of GPIO1x port enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2B | GPIO1X output buffer enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2C | GPIO1X debounce timing select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2D | LED1X frequency select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2E | LED1X frequency select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 30 | GPIO2X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 31 | GPIO2X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 32 | GPIO2X pin status Register | - | - | - | - | - | - | - | - |
| 33 | GPIO2X Level / Pulse Control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 34 | GPIO2X pulse width control Register | - | - | - | - | - | - | 0 | 0 |
| 35 | GPIO2X internal pull-high enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 36 | GPIO2X debounce enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 37 | GPIO2X pin inverse enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 38 | GPIO2X edge detect enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 39 | GPIO2X edge detect status Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3A | SMI event of GPIO2X port enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3B | GPIO2X output buffer enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3C | GPIO2X debounce timing select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3D | LED2X frequency select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3E | LED2X frequency select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3F | GPIO2X low level input enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 40 | GPIO3X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 41 | GPIO3X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 42 | GPIO3X pin status Register | - | - | - | - | - | - | - | - |
| 43 | GPIO3X Level / Pulse Control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 44 | GPIO3X pulse width control Register | - | - | - | - | - | - | 0 | 0 |
| 45 | GPIO3X internal pull-high enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 46 | GPIO3X debounce enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 47 | GPIO3X pin inverse enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | | | | | | | |
|-------|--|---|---|---|---|---|---|---|---|
| 48 | GPIO3X edge detect enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 49 | GPIO3X edge detect status Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4A | SMI event of GPIO3X port enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4B | GPIO3X output buffer enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4C | GPIO3X debounce timing select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 50 | GPIO Port Edge Status Register | - | - | - | 0 | 0 | 0 | 0 | 0 |
| 51 | SIRQ Enable Register | - | - | - | 0 | 0 | 0 | 0 | 0 |
| 52 | SIRQ Channel Select0 Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 53 | SIRQ Channel Select1 Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 54 | SIRQ Channel Select2 Register | 0 | - | - | - | 0 | 0 | 0 | 0 |
| 56 | Access Function Internal Pull-up Enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 57 | WDT1 Reset GPIO Function Enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 58 | WDT2 Reset GPIO Function Enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 59 | LRESET Reset GPIO Function Enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5A | Chip ID1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 5B | Chip ID2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 5D | Vender ID1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 5E | Vender ID2 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 60 | Base Address high-byte Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 61 | Base Address low-byte Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 70 | GPIO4X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 71 | GPIO4X output control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 72 | GPIO4X pin status Register | - | - | - | - | - | - | - | - |
| 73 | GPIO4X Level / Pulse Control Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 74 | GPIO4X pulse width control Register | - | - | - | - | - | - | 0 | 0 |
| 75 | GPIO4X internal pull-high enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 76 | GPIO4X debounce enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 77 | GPIO4X pin inverse enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 78 | GPIO4X edge detect enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 79 | GPIO4x edge detect status Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7A | SMI event of GPIO4X port enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7B | GPIO4X output buffer enable Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7C | GPIO4X debounce timing select Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 80-8E | Reserved | - | - | - | - | - | - | - | - |

8.2.1 Chip Control Register — Index 01h

| Bit | Name | R/W | Default | Description |
|-----|---------------|-----|---------|---|
| 7 | PD_STUS | R | 0 | Power down status |
| 6 | WDT2OUT_EN | R/W | 0 | If the bit is set to 1, WDT2 resetout signal will output from GPIO04~GPIO07 pin. |
| 5 | WDT1OUT_EN | R/W | 0 | If the bit is set to 1, WDT1 resetout signal will output from GPIO00~GPIO03 pin. |
| 4 | SMIOUT_EN | R/W | 0 | If the bit is set to 1, SMI signal will output from GPIO0X port. |
| 3 | SEL_SMI_WIDTH | R/W | 0 | 0: SMI pulse width is 200usec. 1: SMI pulse width is 150msec. |
| 2 | SMI_MD | R/W | 0 | SMI output mode is level or pulse mode. 0: Level mode 1: Pulse mode |
| 1 | SMART_PD_MD | R/W | 1 | Set this bit to 1 will enable auto power down mode, when all function are idle then 10ms, the chip will auto power down. it will wakeup when GPIO state change or read write register |
| 0 | MANUAL_PD | R/W | 0 | Set this bit to 1 will power down all of the analog block and stop internal clock, write 0 to clear this bit or when GPIO state change will auto clear this bit to 0. |

8.2.2 GPIO0X Mode Control Register — Index 02h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7-6 | GPIO07_MD | R/W | 0 | 00b: GPIO07 pin is GPIO function. 01b: GPIO07 pin is LED function. 10b: GPIO07 pin is SMI function. 11b: GPIO07 pin is RSTOUT2. |
| 5-4 | GPIO06_MD | R/W | 0 | 00b: GPIO06 pin is GPIO function. 01b: GPIO06 pin is LED function. 10b: GPIO06 pin is SMI function. 11b: GPIO06 pin is RSTOUT2. |

| | | | | |
|-----|-----------|-----|---|--|
| 3-2 | GPIO05_MD | R/W | 0 | 00b: GPIO05 pin is GPIO function. 01b: GPIO05 pin is LED function. 10b: GPIO05 pin is SMI function. 11b: GPIO05 pin is RSTOUT2. |
| 1-0 | GPIO04_MD | R/W | 0 | 00b: GPIO04 pin is GPIO function. 01b: GPIO04 pin is LED function. 10b: GPIO04 pin is SMI function. 11b: GPIO04 pin is RSTOUT2. |

8.2.3 GPIO1X Mode Control Register — Index 03h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7-6 | GPIO03_MD | R/W | 0 | 00b: GPIO03 pin is GPIO function. 01b: GPIO03 pin is LED function. 10b: GPIO03 pin is SMI function. 11b: GPIO03 pin is RSTOUT1. |
| 5-4 | GPIO02_MD | R/W | 0 | 00b: GPIO02 pin is GPIO function. 01b: GPIO02 pin is LED function. 10b: GPIO02 pin is SMI function. 11b: GPIO02 pin is RSTOUT1. |
| 3-2 | GPIO01_MD | R/W | 0 | 00b: GPIO01 pin is GPIO function. 01b: GPIO01 pin is LED function. 10b: GPIO01 pin is SMI function. 11b: GPIO01 pin is RSTOUT1. |
| 1-0 | GPIO00_MD | R/W | 0 | 00b: GPIO00 pin is GPIO function. 01b: GPIO00 pin is LED function. 10b: GPIO00 pin is SMI function. 11b: GPIO00 pin is RSTOUT1. |

8.2.4 GPIO1X Mode Control Register — Index 04h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7-6 | GPIO17_MD | R/W | 0 | 00b: GPIO17 pin is GPIO function. 01b: GPIO17 pin is LED function. 10b: Reserved 11b: Reserved |
| 5-4 | GPIO16_MD | R/W | 0 | 00b: GPIO16 pin is GPIO function. 01b: GPIO16 pin is LED function. 10b: Reserved 11b: Reserved |
| 3-2 | GPIO15_MD | R/W | 0 | 00b: GPIO15 pin is GPIO function. 01b: GPIO15 pin is LED function. 10b: Reserved 11b: Reserved |
| 1-0 | GPIO14_MD | R/W | 0 | 00b: GPIO14 pin is GPIO function. 01b: GPIO14 pin is LED function. 10b: Reserved 11b: Reserved |

8.2.5 GPIO1X Mode Control Register — Index 05h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7-6 | GPIO13_MD | R/W | 0 | 00b: GPIO13 pin is GPIO function. 01b: GPIO13 pin is LED function. 10b: Reserved 11b: Reserved |
| 5-4 | GPIO12_MD | R/W | 0 | 00b: GPIO12 pin is GPIO function. 01b: GPIO12 pin is LED function. 10b: Reserved 11b: Reserved |

| | | | | |
|-----|-----------|-----|---|---|
| 3-2 | GPIO11_MD | R/W | 0 | 00b: GPIO11 pin is GPIO function. 01b: GPIO11 pin is LED function. 10b: Reserved 11b: Reserved |
| 1-0 | GPIO10_MD | R/W | 0 | 00b: GPIO10 pin is GPIO function. 01b: GPIO10 pin is LED function. 10b: Reserved 11b: Reserved |

8.2.6 GPIO2X Mode Control Register — Index 06h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7 | GPIO27_MD | R/W | 0 | 0b: GPIO27 pin is GPIO function. 1b: GPIO27 pin is LED function. |
| 6 | GPIO26_MD | R/W | 0 | 0b: GPIO26 pin is GPIO function. 1b: GPIO26 pin is LED function. |
| 5 | GPIO25_MD | R/W | 0 | 0b: GPIO25 pin is GPIO function. 1b: GPIO25 pin is LED function. |
| 4 | GPIO24_MD | R/W | 0 | 0b: GPIO24 pin is GPIO function. 1b: GPIO24 pin is LED function. |
| 3 | GPIO23_MD | R/W | 0 | 0b: GPIO23 pin is GPIO function. 1b: GPIO23 pin is LED function. |
| 2 | GPIO22_MD | R/W | 0 | 0b: GPIO22 pin is GPIO function. 1b: GPIO22 pin is LED function. |
| 1 | GPIO21_MD | R/W | 0 | 0b: GPIO21 pin is GPIO function. 1b: GPIO21 pin is LED function. |
| 0 | GPIO20_MD | R/W | 0 | 0b: GPIO20 pin is GPIO function. 1b: GPIO20 pin is LED function. |

8.2.7 WDT1 Control Register — Index 08h

| Bit | Name | R/W | Default | Description |
|-----|---------------|-----|---------|--|
| 7-3 | Reserved | - | - | Reserved |
| 2 | SEL_RSTOUT_PW | R/W | 0 | 0b: RSTOUT pulse width for WDT1 is 500usec 1b: RSTOUT pulse width for WDT1 is 100msec |
| 1 | Reserved | - | - | Reserved |
| 0 | WDT1_RST_ST | R | 0 | WDT1 RSTOUT status. Write 1 to clear the bit. |

8.2.8 WDT1 Count Register — Index 09h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7 | WDT1_EN | R/W | 0 | 0b: Disable WDT1 count. 1b: Enable WDT1 count. |
| 6-0 | WDT1_TIME | R/W | 0 | Watchdog1 timing range from 0 ~ 127sec. 0000000b: 0sec 0000001b: 1sec ... 1111111b: 127sec |

8.2.9 WDT2 Control Register — Index 0Ah

| Bit | Name | R/W | Default | Description |
|-----|-------------|-----|---------|---|
| 7-6 | Reserved | - | - | Reserved |
| 5 | WDT2_RST_ST | R | 0 | WDT2 RSTOUT status. Write 1 to clear the bit. |
| 4 | WDT2_EN | R/W | 0 | 0b: Disable WDT2 count. 1b: Enable WDT2 count. |
| 3 | WDT2_PS_EN | R/W | 0 | 0b: Level mode 1b: WDT2 pulse mode output enable. |
| 2 | WDT2_UNIT | R/W | 0 | WDT2 unit select. Default 0 is select second. Write 1 to select minute. |

| | | | | |
|-----|---------|-----|---|--|
| 1-0 | WDT2_PW | R/W | 0 | Active width of pulse mode. 00b: Pulse width is 1msec. 01b: Pulse width is 20msec. 10b: Pulse width is 100msec 11b: Pulse width is 5sec. |
|-----|---------|-----|---|--|

8.2.10 WDT2 Count Register — Index 0Bh

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7-0 | WDT2_TIMIE | R/W | 00h | WDT1 timing range from 0 ~ 255. 00000000b: 0 (second/minute) 00000001b: 1 (second/minute) ... 11111111b: 255(second/minute) The unit is either second or minute programmed by the watchdog timer control register bit2 in index 0Ah. |

8.2.11 Power Down Count Register — Index 0Ch

| Bit | Name | R/W | Default | Description |
|-----|---------|-----|---------|---|
| 7-0 | PD_TIME | R/W | 63h | Power down timing range from 0 ~ 25.6msec. EX: 01100011b: 10msec(default) 11000111b: 20msec 11111111b: 25.6msec |

8.2.12 GPIO0X Output Control Register — Index 10h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP07_OCTRL | R/W | 0 | GPIO07 output control. 1 : Output. 0 : Input (default). |

| | | | | |
|---|------------|-----|---|---|
| 6 | GP06_OCTRL | R/W | 0 | GPIO06 output control. 1 : Output. 0 : Input (default). |
| 5 | GP05_OCTRL | R/W | 0 | GPIO05 output control. 1 : Output. 0 : Input (default). |
| 4 | GP04_OCTRL | R/W | 0 | GPIO04 output control. 1 : Output. 0 : Input (default). |
| 3 | GP03_OCTRL | R/W | 0 | GPIO03 output control. 1 : Output. 0 : Input (default). |
| 2 | GP02_OCTRL | R/W | 0 | GPIO02 output control. 1 : Output. 0 : Input (default). |
| 1 | GP01_OCTRL | R/W | 0 | GPIO01 output control. 1 : Output. 0 : Input (default). |
| 0 | GP00_OCTRL | R/W | 0 | GPIO00 output control. 1 : Output. 0 : Input (default). |

8.2.13 GPIO0X Output Data Register — Index 11h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---------------------|
| 7 | GP07_ODATA | R/W | 0 | GPIO07 output data. |
| 6 | GP06_ODATA | R/W | 0 | GPIO06 output data. |
| 5 | GP05_ODATA | R/W | 0 | GPIO05 output data. |
| 4 | GP04_ODATA | R/W | 0 | GPIO04 output data. |
| 3 | GP03_ODATA | R/W | 0 | GPIO03 output data. |
| 2 | GP02_ODATA | R/W | 0 | GPIO02 output data. |
| 1 | GP01_ODATA | R/W | 0 | GPIO01 output data. |
| 0 | GP00_ODATA | R/W | 0 | GPIO00 output data. |

8.2.14 GPIO0X Input Status Register — Index 12h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|----------------------------------|
| 7 | GP07_PSTS | R | - | Read the GPIO07 data on the pin. |
| 6 | GP06_PSTS | R | - | Read the GPIO06 data on the pin. |
| 5 | GP05_PSTS | R | - | Read the GPIO05 data on the pin. |
| 4 | GP04_PSTS | R | - | Read the GPIO04 data on the pin. |
| 3 | GP03_PSTS | R | - | Read the GPIO03 data on the pin. |
| 2 | GP02_PSTS | R | - | Read the GPIO02 data on the pin. |
| 1 | GP01_PSTS | R | - | Read the GPIO01 data on the pin. |
| 0 | GP00_PSTS | R | - | Read the GPIO00 data on the pin. |

8.2.15 GPIO0X Level/Pulse Control Register — Index 13h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP07_OMODE | R/W | 0 | GPIO07 output mode. 0 – level, 1 – pulse. |
| 6 | GP06_OMODE | R/W | 0 | GPIO06 output mode. 0 – level, 1 – pulse. |
| 5 | GP05_OMODE | R/W | 0 | GPIO05 output mode. 0 – level, 1 – pulse. |
| 4 | GP04_OMODE | R/W | 0 | GPIO04 output mode. 0 – level, 1 – pulse. |
| 3 | GP03_OMODE | R/W | 0 | GPIO03 output mode. 0 – level, 1 – pulse. |
| 2 | GP02_OMODE | R/W | 0 | GPIO02 output mode. 0 – level, 1 – pulse. |
| 1 | GP01_OMODE | R/W | 0 | GPIO01 output mode. 0 – level, 1 – pulse. |
| 0 | GP00_OMODE | R/W | 0 | GPIO00 output mode. 0 – level, 1 – pulse. |

8.2.16 GPIO0X Pulse Width Control Register — Index 14h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7-2 | Reserved | - | - | Reserved |
| 1-0 | GP0_PLSWD | R/W | 0 | GPIO0X pulse width. If set the GPIO0X to pulse mode, the pulse width can be defined as follows. 00b – 500us (Default) 01b – 1ms 10b – 20ms 11b – 100ms |

8.2.17 GPIO0X Pull-up Resistor Control Register — Index 15h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP07_RESON | R/W | 0 | Turn on the GPIO07 pin internal pull-up resistor with 10KΩ. |
| 6 | GP06_RESON | R/W | 0 | Turn on the GPIO06 pin internal pull-up resistor with 10KΩ. |
| 5 | GP05_RESON | R/W | 0 | Turn on the GPIO05 pin internal pull-up resistor with 10KΩ. |
| 4 | GP04_RESON | R/W | 0 | Turn on the GPIO04 pin internal pull-up resistor with 10KΩ. |
| 3 | GP03_RESON | R/W | 0 | Turn on the GPIO03 pin internal pull-up resistor with 10KΩ. |
| 2 | GP02_RESON | R/W | 0 | Turn on the GPIO02 pin internal pull-up resistor with 10KΩ. |
| 1 | GP01_RESON | R/W | 0 | Turn on the GPIO01 pin internal pull-up resistor with 10KΩ. |
| 0 | GP00_RESON | R/W | 0 | Turn on the GPIO00 pin internal pull-up resistor with 10KΩ. |

8.2.18 GPIO0X Input De-bounce Register — Index 16h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7 | GP07_ENDB | R/W | 0 | Enable GPIO07 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 1Ch bit7 . |
| 6 | GP06_ENDB | R/W | 0 | Enable GPIO06 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 1Ch bit6 . |
| 5 | GP05_ENDB | R/W | 0 | Enable GPIO05 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 1Ch bit5 . |
| 4 | GP04_ENDB | R/W | 0 | Enable GPIO04 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 1Ch bit4 . |
| 3 | GP03_ENDB | R/W | 0 | Enable GPIO03 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 1Ch bit3 . |

| | | | | |
|---|-----------|-----|---|--|
| 2 | GP02_ENDB | R/W | 0 | Enable GPIO02 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 1Ch bit2. |
| 1 | GP01_ENDB | R/W | 0 | Enable GPIO01 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 1Ch bit1. |
| 0 | GP00_ENDB | R/W | 0 | Enable GPIO00 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 1Ch bit0. |

8.2.19 GPIO0X Pin Inverse Enable Register — Index 17h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7 | GP07_PINV | R/W | 0 | If the GPIO07 pin inverse was selected, the output signal would be inverted. |
| 6 | GP06_PINV | R/W | 0 | If the GPIO06 pin inverse was selected, the output signal would be inverted. |
| 5 | GP05_PINV | R/W | 0 | If the GPIO05 pin inverse was selected, the output signal would be inverted. |
| 4 | GP04_PINV | R/W | 0 | If the GPIO04 pin inverse was selected, the output signal would be inverted. |
| 3 | GP03_PINV | R/W | 0 | If the GPIO03 pin inverse was selected, the output signal would be inverted. |
| 2 | GP02_PINV | R/W | 0 | If the GPIO02 pin inverse was selected, the output signal would be inverted. |
| 1 | GP01_PINV | R/W | 0 | If the GPIO01 pin inverse was selected, the output signal would be inverted. |
| 0 | GP00_PINV | R/W | 0 | If the GPIO00 pin inverse was selected, the output signal would be inverted. |

8.2.20 GPIO0X Edge Detector Enable Register — Index 18h

| Bit | Name | R/W | Default | Description |
|-----|-------------|-----|---------|--|
| 7 | EN_GP07EDGE | R/W | 0 | Enable GPIO07 Edge Detector. If this bit set to 1 and GPIO07 set to input mode (10h) will enable GPIO07 edge detection. Default is disabled. |
| 6 | EN_GP06EDGE | R/W | 0 | Enable GPIO06 Edge Detector. If this bit set to 1 and GPIO06 set to input mode (10h) will enable GPIO06 edge detection. Default is disabled. |
| 5 | EN_GP05EDGE | R/W | 0 | Enable GPIO05 Edge Detector. If this bit set to 1 and GPIO05 set to input mode (10h) will enable GPIO05 edge detection. Default is disabled. |
| 4 | EN_GP04EDGE | R/W | 0 | Enable GPIO04 Edge Detector. If this bit set to 1 and GPIO04 set to input mode (10h) will enable GPIO04 edge detection. Default is disabled. |
| 3 | EN_GP03EDGE | R/W | 0 | Enable GPIO03 Edge Detector. If this bit set to 1 and GPIO03 set to input mode (10h) will enable GPIO03 edge detection. Default is disabled. |
| 2 | EN_GP02EDGE | R/W | 0 | Enable GPIO02 Edge Detector. If this bit set to 1 and GPIO02 set to input mode (10h) will enable GPIO02 edge detection. Default is disabled. |
| 1 | EN_GP01EDGE | R/W | 0 | Enable GPIO01 Edge Detector. If this bit set to 1 and GPIO01 set to input mode (10h) will enable GPIO01 edge detection. Default is disabled. |
| 0 | EN_GP00EDGE | R/W | 0 | Enable GPIO00 Edge Detector. If this bit set to 1 and GPIO00 set to input mode (10h) will enable GPIO00 edge detection. Default is disabled. |

8.2.21 GPIO0X Edge Detector Status Register — Index 19h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | STS_GP07EDGE | R | - | Indicate GPIO07 Edge Status. If set to 1, the edge of GPIO07 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 6 | STS_GP06EDGE | R | - | Indicate GPIO06 Edge Status. If set to 1, the edge of GPIO06 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

| | | | | |
|---|--------------|---|---|---|
| 5 | STS_GP05EDGE | R | - | Indicate GPIO05 Edge Status. If set to 1, the edge of GPIO05 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 4 | STS_GP04EDGE | R | - | Indicate GPIO04 Edge Status. If set to 1, the edge of GPIO04 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 3 | STS_GP03EDGE | R | - | Indicate GPIO03 Edge Status. If set to 1, the edge of GPIO03 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 2 | STS_GP02EDGE | R | - | Indicate GPIO02 Edge Status. If set to 1, the edge of GPIO02 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 1 | STS_GP01EDGE | R | - | Indicate GPIO01 Edge Status. If set to 1, the edge of GPIO01 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 0 | STS_GP00EDGE | R | - | Indicate GPIO00 Edge Status. If set to 1, the edge of GPIO00 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

8.2.22 GPIO0X SMI Enable Register — Index 1Ah

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|--|
| 7 | EN_GP07SMI | R/W | 0 | Enable GPIO07 SMI Generation. If this bit set to 1, enable GPIO07 to generate SMI. |
| 6 | EN_GP06SMI | R/W | 0 | Enable GPIO06 SMI Generation. If this bit set to 1, enable GPIO06 to generate SMI. |
| 5 | EN_GP05SMI | R/W | 0 | Enable GPIO05 SMI Generation. If this bit set to 1, enable GPIO05 to generate SMI. |
| 4 | EN_GP04SMI | R/W | 0 | Enable GPIO04 SMI Generation. If this bit set to 1, enable GPIO04 to generate SMI. |
| 3 | EN_GP03SMI | R/W | 0 | Enable GPIO03 SMI Generation. If this bit set to 1, enable GPIO03 to generate SMI. |
| 2 | EN_GP02SMI | R/W | 0 | Enable GPIO02 SMI Generation. If this bit set to 1, enable GPIO02 to generate SMI. |
| 1 | EN_GP01SMI | R/W | 0 | Enable GPIO01 SMI Generation. If this bit set to 1, enable GPIO01 to generate SMI. |
| 0 | EN_GP00SMI | R/W | 0 | Enable GPIO00 SMI Generation. If this bit set to 1, enable GPIO00 to generate SMI. |

8.2.23 GPIO0X Output Driving Enable Register — Index 1Bh

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | EN_GP07_OBUF | R/W | 0 | Enable GPIO07 drive high buffer. If this bit is set to 0, the pin GPIO07 will be I/OD pin, if set to 1 the pin GPIO07 is I/O pin. |
| 6 | EN_GP06_OBUF | R/W | 0 | Enable GPIO06 drive high buffer. If this bit is set to 0, the pin GPIO06 will be I/OD pin, if set to 1 the pin GPIO06 is I/O pin. |
| 5 | EN_GP05_OBUF | R/W | 0 | Enable GPIO05 drive high buffer. If this bit is set to 0, the pin GPIO05 will be I/OD pin, if set to 1 the pin GPIO05 is I/O pin. |
| 4 | EN_GP04_OBUF | R/W | 0 | Enable GPIO04 drive high buffer. If this bit is set to 0, the pin GPIO04 will be I/OD pin, if set to 1 the pin GPIO04 is I/O pin. |
| 3 | EN_GP03_OBUF | R/W | 0 | Enable GPIO03 drive high buffer. If this bit is set to 0, the pin GPIO03 will be I/OD pin, if set to 1 the pin GPIO03 is I/O pin. |
| 2 | EN_GP02_OBUF | R/W | 0 | Enable GPIO02 drive high buffer. If this bit is set to 0, the pin GPIO02 will be I/OD pin, if set to 1 the pin GPIO02 is I/O pin. |
| 1 | EN_GP01_OBUF | R/W | 0 | Enable GPIO01 drive high buffer. If this bit is set to 0, the pin GPIO01 will be I/OD pin, if set to 1 the pin GPIO01 is I/O pin. |
| 0 | EN_GP00_OBUF | R/W | 0 | Enable GPIO00 drive high buffer. If this bit is set to 0, the pin GPIO00 will be I/OD pin, if set to 1 the pin GPIO00 is I/O pin. |

8.2.24 GPIO0X De-bounce Time Select Register — Index 1Ch

| Bit | Name | R/W | Default | Description |
|-----|---------------|-----|---------|---|
| 7 | DB_TIME07_SEL | R/W | 0 | Select GPIO07 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 6 | DB_TIME06_SEL | R/W | 0 | Select GPIO06 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 5 | DB_TIME05_SEL | R/W | 0 | Select GPIO05 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 4 | DB_TIME04_SEL | R/W | 0 | Select GPIO04 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 3 | DB_TIME03_SEL | R/W | 0 | Select GPIO03 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |

| | | | | |
|---|---------------|-----|---|---|
| 2 | DB_TIME02_SEL | R/W | 0 | Select GPIO02 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 1 | DB_TIME01_SEL | R/W | 0 | Select GPIO01 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 0 | DB_TIME00_SEL | R/W | 0 | Select GPIO00 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |

8.2.25 LED0X Frequency Select Register — Index 1Dh

| Bit | Name | R/W | Default | Description | |
|-----|------------|-----|---------|-------------------------|---------------------------------------|
| 7-6 | LED07_FREQ | R/W | 0 | LED07 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 5-4 | LED06_FREQ | R/W | 0 | LED06 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 3-2 | LED05_FREQ | R/W | 0 | LED05 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 1-0 | LED04_FREQ | R/W | 0 | LED04 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| | | | | 2Hz (duty cycle is 80%) | |

8.2.26 LED0X Frequency Select Register — Index 1Eh

| Bit | Name | R/W | Default | Description | |
|-----|-------------------------|-----|---------|-------------------------|---------------------------------------|
| 7-6 | LED03_FREQ | R/W | 0 | LED03 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 5-4 | LED02_FREQ | R/W | 0 | LED02 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 3-2 | LED01_FREQ | R/W | 0 | LED01 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 1-0 | LED00_FREQ | R/W | 0 | LED00 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |

8.2.27 GPIO1X Output Control Register — Index 20h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP17_OCTRL | R/W | 0 | GPIO17 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 6 | GP16_OCTRL | R/W | 0 | GPIO16 output control. Set to 1 for output function. Set to 0 for input function (default). |

| | | | | |
|---|------------|-----|---|---|
| 5 | GP15_OCTRL | R/W | 0 | GPIO15 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 4 | GP14_OCTRL | R/W | 0 | GPIO14 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 3 | GP13_OCTRL | R/W | 0 | GPIO13 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 2 | GP12_OCTRL | R/W | 0 | GPIO12 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 1 | GP11_OCTRL | R/W | 0 | GPIO11 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 0 | GP10_OCTRL | R/W | 0 | GPIO10 output control. Set to 1 for output function. Set to 0 for input function (default). |

8.2.28 GPIO1X Output Data Register — Index 21h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---------------------|
| 7 | GP17_ODATA | R/W | 0 | GPIO17 output data. |
| 6 | GP16_ODATA | R/W | 0 | GPIO16 output data. |
| 5 | GP15_ODATA | R/W | 0 | GPIO15 output data. |
| 4 | GP14_ODATA | R/W | 0 | GPIO14 output data. |
| 3 | GP13_ODATA | R/W | 0 | GPIO13 output data. |
| 2 | GP12_ODATA | R/W | 0 | GPIO12 output data. |
| 1 | GP11_ODATA | R/W | 0 | GPIO11 output data. |
| 0 | GP10_ODATA | R/W | 0 | GPIO10 output data. |

8.2.29 GPIO1X Input Status Register — Index 22h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|----------------------------------|
| 7 | GP17_PSTS | R | - | Read the GPIO17 data on the pin. |
| 6 | GP16_PSTS | R | - | Read the GPIO16 data on the pin. |
| 5 | GP15_PSTS | R | - | Read the GPIO15 data on the pin. |
| 4 | GP14_PSTS | R | - | Read the GPIO14 data on the pin. |
| 3 | GP13_PSTS | R | - | Read the GPIO13 data on the pin. |

| | | | | |
|---|-----------|---|---|----------------------------------|
| 2 | GP12_PSTS | R | - | Read the GPIO12 data on the pin. |
| 1 | GP11_PSTS | R | - | Read the GPIO11 data on the pin. |
| 0 | GP10_PSTS | R | - | Read the GPIO10 data on the pin. |

8.2.30 GPIO1X Level/Pulse Control Register — Index 23h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP17_OMODE | R/W | 0 | GPIO17 output mode. 0 – level, 1 – pulse. |
| 6 | GP16_OMODE | R/W | 0 | GPIO16 output mode. 0 – level, 1 – pulse. |
| 5 | GP15_OMODE | R/W | 0 | GPIO15 output mode. 0 – level, 1 – pulse. |
| 4 | GP14_OMODE | R/W | 0 | GPIO14 output mode. 0 – level, 1 – pulse. |
| 3 | GP13_OMODE | R/W | 0 | GPIO13 output mode. 0 – level, 1 – pulse. |
| 2 | GP12_OMODE | R/W | 0 | GPIO12 output mode. 0 – level, 1 – pulse. |
| 1 | GP11_OMODE | R/W | 0 | GPIO11 output mode. 0 – level, 1 – pulse. |
| 0 | GP10_OMODE | R/W | 0 | GPIO10 output mode. 0 – level, 1 – pulse. |

8.2.31 GPIO1X Pulse Width Control Register — Index 24h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7-2 | Reserved | - | - | Reserved |
| 1-0 | GP1_PLSWD | R/W | 00b | GPIO1X pulse width. If set the GPIO1X to pulse mode, the pulse width can be defined as follows. 00b – 500us (Default) 01b – 1ms 10b – 20ms 11b – 100ms |

8.2.32 GPIO1X Pull-up Resistor Control Register — Index 25h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP17_RESON | R/W | 0 | Turn on the GPIO17 pin internal pull-up resistor with 10KΩ. |
| 6 | GP16_RESON | R/W | 0 | Turn on the GPIO16 pin internal pull-up resistor with 10KΩ. |
| 5 | GP15_RESON | R/W | 0 | Turn on the GPIO15 pin internal pull-up resistor with 10KΩ. |
| 4 | GP14_RESON | R/W | 0 | Turn on the GPIO14 pin internal pull-up resistor with 10KΩ. |
| 3 | GP13_RESON | R/W | 0 | Turn on the GPIO13 pin internal pull-up resistor with 10KΩ. |

| | | | | |
|---|------------|-----|---|---|
| 2 | GP12_RESON | R/W | 0 | Turn on the GPIO12 pin internal pull-up resistor with 10KΩ. |
| 1 | GP11_RESON | R/W | 0 | Turn on the GPIO11 pin internal pull-up resistor with 10KΩ. |
| 0 | GP10_RESON | R/W | 0 | Turn on the GPIO10 pin internal pull-up resistor with 10KΩ. |

8.2.33 GPIO1X Input De-bounce Register — Index 26h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7 | GP17_ENDB | R/W | 0 | Enable GPIO17 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 2Ch bit7 . |
| 6 | GP16_ENDB | R/W | 0 | Enable GPIO16 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 2Ch bit6 . |
| 5 | GP15_ENDB | R/W | 0 | Enable GPIO15 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 2Ch bit5 . |
| 4 | GP14_ENDB | R/W | 0 | Enable GPIO14 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 2Ch bit4 . |
| 3 | GP13_ENDB | R/W | 0 | Enable GPIO13 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 2Ch bit3 . |
| 2 | GP12_ENDB | R/W | 0 | Enable GPIO12 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 2Ch bit2 . |
| 1 | GP11_ENDB | R/W | 0 | Enable GPIO11 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 2Ch bit1 . |

| | | | | |
|---|-----------|-----|---|--|
| 0 | GP10_ENDB | R/W | 0 | Enable GPIO10 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 2Ch bit0. |
|---|-----------|-----|---|--|

8.2.34 GPIO1X Pin Inverse Enable Register — Index 27h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7 | GP17_PINV | R/W | 0 | If the GPIO17 pin inverse was selected, the output signal would be inverted. |
| 6 | GP16_PINV | R/W | 0 | If the GPIO16 pin inverse was selected, the output signal would be inverted. |
| 5 | GP15_PINV | R/W | 0 | If the GPIO15 pin inverse was selected, the output signal would be inverted. |
| 4 | GP14_PINV | R/W | 0 | If the GPIO14 pin inverse was selected, the output signal would be inverted. |
| 3 | GP13_PINV | R/W | 0 | If the GPIO13 pin inverse was selected, the output signal would be inverted. |
| 2 | GP12_PINV | R/W | 0 | If the GPIO12 pin inverse was selected, the output signal would be inverted. |
| 1 | GP11_PINV | R/W | 0 | If the GPIO11 pin inverse was selected, the output signal would be inverted. |
| 0 | GP10_PINV | R/W | 0 | If the GPIO10 pin inverse was selected, the output signal would be inverted. |

8.2.35 GPIO1X Edge Detector Enable Register — Index 28h

| Bit | Name | R/W | Default | Description |
|-----|-------------|-----|---------|--|
| 7 | EN_GP17EDGE | R/W | 0 | Enable GPIO17 Edge Detector. If this bit set to 1 and GPIO17 set to input mode (20h) will enable GPIO17 edge detection. Default is disabled. |
| 6 | EN_GP16EDGE | R/W | 0 | Enable GPIO16 Edge Detector. If this bit set to 1 and GPIO16 set to input mode (20h) will enable GPIO16 edge detection. Default is disabled. |

| | | | | |
|---|-------------|-----|---|--|
| 5 | EN_GP15EDGE | R/W | 0 | Enable GPIO15 Edge Detector. If this bit set to 1 and GPIO15 set to input mode (20h) will enable GPIO15 edge detection. Default is disabled. |
| 4 | EN_GP14EDGE | R/W | 0 | Enable GPIO14 Edge Detector. If this bit set to 1 and GPIO14 set to input mode (20h) will enable GPIO14 edge detection. Default is disabled. |
| 3 | EN_GP13EDGE | R/W | 0 | Enable GPIO13 Edge Detector. If this bit set to 1 and GPIO13 set to input mode (20h) will enable GPIO13 edge detection. Default is disabled. |
| 2 | EN_GP12EDGE | R/W | 0 | Enable GPIO12 Edge Detector. If this bit set to 1 and GPIO12 set to input mode (20h) will enable GPIO12 edge detection. Default is disabled. |
| 1 | EN_GP11EDGE | R/W | 0 | Enable GPIO11 Edge Detector. If this bit set to 1 and GPIO11 set to input mode (20h) will enable GPIO11 edge detection. Default is disabled. |
| 0 | EN_GP10EDGE | R/W | 0 | Enable GPIO10 Edge Detector. If this bit set to 1 and GPIO10 set to input mode (20h) will enable GPIO10 edge detection. Default is disabled. |

8.2.36 GPIO1X Edge Detector Status Register — Index 29h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | STS_GP17EDGE | R | - | Indicate GPIO17 Edge Status. If set to 1, the edge of GPIO17 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 6 | STS_GP16EDGE | R | - | Indicate GPIO16 Edge Status. If set to 1, the edge of GPIO16 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 5 | STS_GP15EDGE | R | - | Indicate GPIO15 Edge Status. If set to 1, the edge of GPIO15 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 4 | STS_GP14EDGE | R | - | Indicate GPIO14 Edge Status. If set to 1, the edge of GPIO14 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 3 | STS_GP13EDGE | R | - | Indicate GPIO13 Edge Status. If set to 1, the edge of GPIO13 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 2 | STS_GP12EDGE | R | - | Indicate GPIO12 Edge Status. If set to 1, the edge of GPIO12 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

| | | | | |
|---|--------------|---|---|---|
| 1 | STS_GP11EDGE | R | - | Indicate GPIO11 Edge Status. If set to 1, the edge of GPIO11 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 0 | STS_GP10EDGE | R | - | Indicate GPIO10 Edge Status. If set to 1, the edge of GPIO10 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

8.2.37 GPIO1X SMI Enable Register — Index 2Ah

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|--|
| 7 | EN_GP17SMI | R/W | 0 | Enable GPIO17 SMI Generation. If this bit set to 1, enable GPIO17 to generate SMI. |
| 6 | EN_GP16SMI | R/W | 0 | Enable GPIO16 SMI Generation. If this bit set to 1, enable GPIO16 to generate SMI. |
| 5 | EN_GP15SMI | R/W | 0 | Enable GPIO15 SMI Generation. If this bit set to 1, enable GPIO15 to generate SMI. |
| 4 | EN_GP14SMI | R/W | 0 | Enable GPIO14 SMI Generation. If this bit set to 1, enable GPIO14 to generate SMI. |
| 3 | EN_GP13SMI | R/W | 0 | Enable GPIO13 SMI Generation. If this bit set to 1, enable GPIO13 to generate SMI. |
| 2 | EN_GP12SMI | R/W | 0 | Enable GPIO12 SMI Generation. If this bit set to 1, enable GPIO12 to generate SMI. |
| 1 | EN_GP11SMI | R/W | 0 | Enable GPIO11 SMI Generation. If this bit set to 1, enable GPIO11 to generate SMI. |
| 0 | EN_GP10SMI | R/W | 0 | Enable GPIO10 SMI Generation. If this bit set to 1, enable GPIO10 to generate SMI. |

8.2.38 GPIO1X Output Driving Enable Register — Index 2Bh

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | EN_GP17_OBUF | R/W | 0 | Enable GPIO17 drive high buffer. If this bit is set to 0, the pin GPIO17 will be I/OD pin, if set to 1 the pin GPIO17 is I/O pin. |
| 6 | EN_GP16_OBUF | R/W | 0 | Enable GPIO16 drive high buffer. If this bit is set to 0, the pin GPIO16 will be I/OD pin, if set to 1 the pin GPIO16 is I/O pin. |
| 5 | EN_GP15_OBUF | R/W | 0 | Enable GPIO15 drive high buffer. If this bit is set to 0, the pin GPIO15 will be I/OD pin, if set to 1 the pin GPIO15 is I/O pin. |

| | | | | |
|---|--------------|-----|---|---|
| 4 | EN_GP14_OBUF | R/W | 0 | Enable GPIO14 drive high buffer. If this bit is set to 0, the pin GPIO14 will be I/OD pin, if set to 1 the pin GPIO14 is I/O pin. |
| 3 | EN_GP13_OBUF | R/W | 0 | Enable GPIO13 drive high buffer. If this bit is set to 0, the pin GPIO13 will be I/OD pin, if set to 1 the pin GPIO13 is I/O pin. |
| 2 | EN_GP12_OBUF | R/W | 0 | Enable GPIO12 drive high buffer. If this bit is set to 0, the pin GPIO12 will be I/OD pin, if set to 1 the pin GPIO12 is I/O pin. |
| 1 | EN_GP11_OBUF | R/W | 0 | Enable GPIO11 drive high buffer. If this bit is set to 0, the pin GPIO11 will be I/OD pin, if set to 1 the pin GPIO11 is I/O pin. |
| 0 | EN_GP10_OBUF | R/W | 0 | Enable GPIO10 drive high buffer. If this bit is set to 0, the pin GPIO10 will be I/OD pin, if set to 1 the pin GPIO10 is I/O pin. |

8.2.39 GPIO1X De-bounce Time Select Register — Index 2Ch

| Bit | Name | R/W | Default | Description |
|-----|---------------|-----|---------|---|
| 7 | DB_TIME17_SEL | R/W | 0 | Select GPIO17 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 6 | DB_TIME16_SEL | R/W | 0 | Select GPIO16 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 5 | DB_TIME15_SEL | R/W | 0 | Select GPIO15 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 4 | DB_TIME14_SEL | R/W | 0 | Select GPIO14 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 3 | DB_TIME13_SEL | R/W | 0 | Select GPIO13 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 2 | DB_TIME12_SEL | R/W | 0 | Select GPIO12 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 1 | DB_TIME11_SEL | R/W | 0 | Select GPIO11 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 0 | DB_TIME10_SEL | R/W | 0 | Select GPIO10 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |

8.2.40 LED1X Frequency Select Register — Index 2Dh

| Bit | Name | R/W | Default | Description | |
|-----|-------------------------|-----|---------|-------------------------|---------------------------------------|
| 7-6 | LED17_FREQ | R/W | 0 | LED17 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 5-4 | LED16_FREQ | R/W | 0 | LED16 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 3-2 | LED15_FREQ | R/W | 0 | LED15 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 1-0 | LED14_FREQ | R/W | 0 | LED14 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |

8.2.41 LED1X Frequency Select Register — Index 2Eh

| Bit | Name | R/W | Default | Description | |
|-----|-------------------------|-----|---------|-------------------------|---------------------------------------|
| 7-6 | LED13_FREQ | R/W | 0 | LED13 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 5-4 | LED12_FREQ | R/W | 0 | LED12 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 3-2 | LED11_FREQ | R/W | 0 | LED11 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 1-0 | LED10_FREQ | R/W | 0 | LED10 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |

8.2.42 GPIO2X Output Control Register — Index 30h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP27_OCTRL | R/W | 0 | GPIO27 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 6 | GP26_OCTRL | R/W | 0 | GPIO26 output control. Set to 1 for output function. Set to 0 for input function (default). |

| | | | | |
|---|------------|-----|---|---|
| 5 | GP25_OCTRL | R/W | 0 | GPIO25 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 4 | GP24_OCTRL | R/W | 0 | GPIO24 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 3 | GP23_OCTRL | R/W | 0 | GPIO23 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 2 | GP22_OCTRL | R/W | 0 | GPIO22 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 1 | GP21_OCTRL | R/W | 0 | GPIO21 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 0 | GP20_OCTRL | R/W | 0 | GPIO20 output control. Set to 1 for output function. Set to 0 for input function (default). |

8.2.43 GPIO2X Output Data Register — Index 31h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---------------------|
| 7 | GP27_ODATA | R/W | 0 | GPIO27 output data. |
| 6 | GP26_ODATA | R/W | 0 | GPIO26 output data. |
| 5 | GP25_ODATA | R/W | 0 | GPIO25 output data. |
| 4 | GP24_ODATA | R/W | 0 | GPIO24 output data. |
| 3 | GP23_ODATA | R/W | 0 | GPIO23 output data. |
| 2 | GP22_ODATA | R/W | 0 | GPIO22 output data. |
| 1 | GP21_ODATA | R/W | 0 | GPIO21 output data. |
| 0 | GP20_ODATA | R/W | 0 | GPIO20 output data. |

8.2.44 GPIO2X Input Status Register — Index 32h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|----------------------------------|
| 7 | GP27_PSTS | R | - | Read the GPIO27 data on the pin. |
| 6 | GP26_PSTS | R | - | Read the GPIO26 data on the pin. |
| 5 | GP25_PSTS | R | - | Read the GPIO25 data on the pin. |
| 4 | GP24_PSTS | R | - | Read the GPIO24 data on the pin. |
| 3 | GP23_PSTS | R | - | Read the GPIO23 data on the pin. |

| | | | | |
|---|-----------|---|---|----------------------------------|
| 2 | GP22_PSTS | R | - | Read the GPIO22 data on the pin. |
| 1 | GP21_PSTS | R | - | Read the GPIO21 data on the pin. |
| 0 | GP20_PSTS | R | - | Read the GPIO20 data on the pin. |

8.2.45 GPIO2X Level/Pulse Control Register — Index 33h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP27_OMODE | R/W | 0 | GPIO27 output mode. 0 – level, 1 – pulse. |
| 6 | GP26_OMODE | R/W | 0 | GPIO26 output mode. 0 – level, 1 – pulse. |
| 5 | GP25_OMODE | R/W | 0 | GPIO25 output mode. 0 – level, 1 – pulse. |
| 4 | GP24_OMODE | R/W | 0 | GPIO24 output mode. 0 – level, 1 – pulse. |
| 3 | GP23_OMODE | R/W | 0 | GPIO23 output mode. 0 – level, 1 – pulse. |
| 2 | GP22_OMODE | R/W | 0 | GPIO22 output mode. 0 – level, 1 – pulse. |
| 1 | GP21_OMODE | R/W | 0 | GPIO21 output mode. 0 – level, 1 – pulse. |
| 0 | GP20_OMODE | R/W | 0 | GPIO20 output mode. 0 – level, 1 – pulse. |

8.2.46 GPIO2X Pulse Width Control Register — Index 34h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7-2 | Reserved | - | - | Reserved |
| 1-0 | GP2_PLSWD | R/W | 00b | GPIO2x pulse width. If set the GPIO2x to pulse mode, the pulse width can be defined as follows. 00b – 500us (Default) 01b – 1ms 10b – 20ms 11b – 100ms |

8.2.47 GPIO2X Pull-up Resistor Control Register — Index 35h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP27_RESON | R/W | 0 | Turn on the GPIO27 pin internal pull-up resistor with 10KΩ. |
| 6 | GP26_RESON | R/W | 0 | Turn on the GPIO26 pin internal pull-up resistor with 10KΩ. |
| 5 | GP25_RESON | R/W | 0 | Turn on the GPIO25 pin internal pull-up resistor with 10KΩ. |
| 4 | GP24_RESON | R/W | 0 | Turn on the GPIO24 pin internal pull-up resistor with 10KΩ. |
| 3 | GP23_RESON | R/W | 0 | Turn on the GPIO23 pin internal pull-up resistor with 10KΩ. |

| | | | | |
|---|------------|-----|---|---|
| 2 | GP22_RESON | R/W | 0 | Turn on the GPIO22 pin internal pull-up resistor with 10KΩ. |
| 1 | GP21_RESON | R/W | 0 | Turn on the GPIO21 pin internal pull-up resistor with 10KΩ. |
| 0 | GP20_RESON | R/W | 0 | Turn on the GPIO20 pin internal pull-up resistor with 10KΩ. |

8.2.48 GPIO2X Input De-bounce Register — Index 36h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7 | GP27_ENDB | R/W | 0 | Enable GPIO27 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 3Ch bit7 . |
| 6 | GP26_ENDB | R/W | 0 | Enable GPIO26 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 3Ch bit6 . |
| 5 | GP25_ENDB | R/W | 0 | Enable GPIO25 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 3Ch bit5 . |
| 4 | GP24_ENDB | R/W | 0 | Enable GPIO24 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 3Ch bit4 . |
| 3 | GP23_ENDB | R/W | 0 | Enable GPIO23 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 3Ch bit3 . |
| 2 | GP22_ENDB | R/W | 0 | Enable GPIO22 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 3Ch bit2 . |
| 1 | GP21_ENDB | R/W | 0 | Enable GPIO21 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 3Ch bit1 . |

| | | | | |
|---|-----------|-----|---|--|
| 0 | GP20_ENDB | R/W | 0 | Enable GPIO20 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 3Ch bit0. |
|---|-----------|-----|---|--|

8.2.49 GPIO2X Pin Inverse Enable Register — Index37h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7 | GP27_PINV | R/W | 0 | If the GPIO27 pin inverse was selected, the output signal would be inverted. |
| 6 | GP26_PINV | R/W | 0 | If the GPIO26 pin inverse was selected, the output signal would be inverted. |
| 5 | GP25_PINV | R/W | 0 | If the GPIO25 pin inverse was selected, the output signal would be inverted. |
| 4 | GP24_PINV | R/W | 0 | If the GPIO24 pin inverse was selected, the output signal would be inverted. |
| 3 | GP23_PINV | R/W | 0 | If the GPIO23 pin inverse was selected, the output signal would be inverted. |
| 2 | GP22_PINV | R/W | 0 | If the GPIO22 pin inverse was selected, the output signal would be inverted. |
| 1 | GP21_PINV | R/W | 0 | If the GPIO21 pin inverse was selected, the output signal would be inverted. |
| 0 | GP20_PINV | R/W | 0 | If the GPIO20 pin inverse was selected, the output signal would be inverted. |

8.2.50 GPIO2X Edge Detector Enable Register — Index 38h

| Bit | Name | R/W | Default | Description |
|-----|-------------|-----|---------|--|
| 7 | EN_GP27EDGE | R/W | 0 | Enable GPIO27 Edge Detector. If this bit set to 1 and GPIO27 set to input mode (30h) will enable GPIO27 edge detection. Default is disabled. |
| 6 | EN_GP26EDGE | R/W | 0 | Enable GPIO26 Edge Detector. If this bit set to 1 and GPIO26 set to input mode (30h) will enable GPIO26 edge detection. Default is disabled. |

| | | | | |
|---|-------------|-----|---|--|
| 5 | EN_GP25EDGE | R/W | 0 | Enable GPIO25 Edge Detector. If this bit set to 1 and GPIO25 set to input mode (30h) will enable GPIO25 edge detection. Default is disabled. |
| 4 | EN_GP24EDGE | R/W | 0 | Enable GPIO24 Edge Detector. If this bit set to 1 and GPIO24 set to input mode (30h) will enable GPIO24 edge detection. Default is disabled. |
| 3 | EN_GP23EDGE | R/W | 0 | Enable GPIO23 Edge Detector. If this bit set to 1 and GPIO23 set to input mode (30h) will enable GPIO23 edge detection. Default is disabled. |
| 2 | EN_GP22EDGE | R/W | 0 | Enable GPIO22 Edge Detector. If this bit set to 1 and GPIO22 set to input mode (30h) will enable GPIO22 edge detection. Default is disabled. |
| 1 | EN_GP21EDGE | R/W | 0 | Enable GPIO21 Edge Detector. If this bit set to 1 and GPIO21 set to input mode (30h) will enable GPIO21 edge detection. Default is disabled. |
| 0 | EN_GP20EDGE | R/W | 0 | Enable GPIO20 Edge Detector. If this bit set to 1 and GPIO20 set to input mode (30h) will enable GPIO20 edge detection. Default is disabled. |

8.2.51 GPIO2X Edge Detector Status Register — Index 39h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | STS_GP27EDGE | R | - | Indicate GPIO27 Edge Status. If set to 1, the edge of GPIO27 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 6 | STS_GP26EDGE | R | - | Indicate GPIO26 Edge Status. If set to 1, the edge of GPIO26 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 5 | STS_GP25EDGE | R | - | Indicate GPIO25 Edge Status. If set to 1, the edge of GPIO25 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 4 | STS_GP24EDGE | R | - | Indicate GPIO24 Edge Status. If set to 1, the edge of GPIO24 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 3 | STS_GP23EDGE | R | - | Indicate GPIO23 Edge Status. If set to 1, the edge of GPIO23 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 2 | STS_GP22EDGE | R | - | Indicate GPIO22 Edge Status. If set to 1, the edge of GPIO22 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

| | | | | |
|---|--------------|---|---|---|
| 1 | STS_GP21EDGE | R | - | Indicate GPIO21 Edge Status. If set to 1, the edge of GPIO21 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 0 | STS_GP20EDGE | R | - | Indicate GPIO20 Edge Status. If set to 1, the edge of GPIO20 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

8.2.52 GPIO2X SMI Enable Register — Index 3Ah

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|--|
| 7 | EN_GP27SMI | R/W | 0 | Enable GPIO27 SMI Generation. If this bit set to 1, enable GPIO27 to generate SMI. |
| 6 | EN_GP26SMI | R/W | 0 | Enable GPIO26 SMI Generation. If this bit set to 1, enable GPIO26 to generate SMI. |
| 5 | EN_GP25SMI | R/W | 0 | Enable GPIO25 SMI Generation. If this bit set to 1, enable GPIO25 to generate SMI. |
| 4 | EN_GP24SMI | R/W | 0 | Enable GPIO24 SMI Generation. If this bit set to 1, enable GPIO24 to generate SMI. |
| 3 | EN_GP23SMI | R/W | 0 | Enable GPIO23 SMI Generation. If this bit set to 1, enable GPIO23 to generate SMI. |
| 2 | EN_GP22SMI | R/W | 0 | Enable GPIO22 SMI Generation. If this bit set to 1, enable GPIO22 to generate SMI. |
| 1 | EN_GP21SMI | R/W | 0 | Enable GPIO21 SMI Generation. If this bit set to 1, enable GPIO21 to generate SMI. |
| 0 | EN_GP20SMI | R/W | 0 | Enable GPIO20 SMI Generation. If this bit set to 1, enable GPIO20 to generate SMI. |

8.2.53 GPIO2X Output Driving Enable Register — Index 3Bh

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | EN_GP27_OBUF | R/W | 0 | Enable GPIO27 drive high buffer. If this bit is set to 0, the pin GPIO27 will be I/OD pin, if set to 1 the pin GPIO27 is I/O pin. |
| 6 | EN_GP26_OBUF | R/W | 0 | Enable GPIO26 drive high buffer. If this bit is set to 0, the pin GPIO26 will be I/OD pin, if set to 1 the pin GPIO26 is I/O pin. |
| 5 | EN_GP25_OBUF | R/W | 0 | Enable GPIO25 drive high buffer. If this bit is set to 0, the pin GPIO25 will be I/OD pin, if set to 1 the pin GPIO25 is I/O pin. |

| | | | | |
|---|--------------|-----|---|---|
| 4 | EN_GP24_OBUF | R/W | 0 | Enable GPIO24 drive high buffer. If this bit is set to 0, the pin GPIO24 will be I/OD pin, if set to 1 the pin GPIO24 is I/O pin. |
| 3 | EN_GP23_OBUF | R/W | 0 | Enable GPIO23 drive high buffer. If this bit is set to 0, the pin GPIO23 will be I/OD pin, if set to 1 the pin GPIO23 is I/O pin. |
| 2 | EN_GP22_OBUF | R/W | 0 | Enable GPIO22 drive high buffer. If this bit is set to 0, the pin GPIO22 will be I/OD pin, if set to 1 the pin GPIO22 is I/O pin. |
| 1 | EN_GP21_OBUF | R/W | 0 | Enable GPIO21 drive high buffer. If this bit is set to 0, the pin GPIO21 will be I/OD pin, if set to 1 the pin GPIO21 is I/O pin. |
| 0 | EN_GP20_OBUF | R/W | 0 | Enable GPIO20 drive high buffer. If this bit is set to 0, the pin GPIO20 will be I/OD pin, if set to 1 the pin GPIO20 is I/O pin. |

8.2.54 GPIO2X De-bounce Time Select Register — Index 3Ch

| Bit | Name | R/W | Default | Description |
|-----|---------------|-----|---------|---|
| 7 | DB_TIME27_SEL | R/W | 0 | Select GPIO27 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 6 | DB_TIME26_SEL | R/W | 0 | Select GPIO26 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 5 | DB_TIME25_SEL | R/W | 0 | Select GPIO25 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 4 | DB_TIME24_SEL | R/W | 0 | Select GPIO24 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 3 | DB_TIME23_SEL | R/W | 0 | Select GPIO23 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 2 | DB_TIME22_SEL | R/W | 0 | Select GPIO22 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 1 | DB_TIME21_SEL | R/W | 0 | Select GPIO21 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 0 | DB_TIME20_SEL | R/W | 0 | Select GPIO20 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |

8.2.55 LED2X Frequency Select Register — Index 3Dh

| Bit | Name | R/W | Default | Description | |
|-----|-------------------------|-----|---------|-------------------------|---------------------------------------|
| 7-6 | LED27_FREQ | R/W | 0 | LED27 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 5-4 | LED26_FREQ | R/W | 0 | LED26 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 3-2 | LED25_FREQ | R/W | 0 | LED25 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 1-0 | LED24_FREQ | R/W | 0 | LED24 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |

8.2.56 LED2X Frequency Select Register — Index 3Eh

| Bit | Name | R/W | Default | Description | |
|-----|-------------------------|-----|---------|-------------------------|---------------------------------------|
| 7-6 | LED23_FREQ | R/W | 0 | LED23 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 5-4 | LED22_FREQ | R/W | 0 | LED22 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 3-2 | LED21_FREQ | R/W | 0 | LED21 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |
| 1-0 | LED20_FREQ | R/W | 0 | LED20 output frequency. | |
| | | | | Bit | Description |
| | | | | 00b | 0.25Hz (default, duty cycle is 97.5%) |
| | | | | 01b | 0.5Hz (duty cycle is 95%) |
| | | | | 10b | 1 Hz (duty cycle is 90%) |
| 11b | 2Hz (duty cycle is 80%) | | | | |

8.2.2 GPIO2X Low Level Input Enable Register — Index 3Fh

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|--|
| 7 | GP27_LVIN_EN | R/W | 0 | Enable GPIO27 low level input detection. ($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) |
| 6 | GP26_LVIN_EN | R/W | 0 | Enable GPIO26 low level input detection. ($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) |
| 5 | GP25_LVIN_EN | R/W | 0 | Enable GPIO25 low level input detection. ($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) |
| 4 | GP24_LVIN_EN | R/W | 0 | Enable GPIO24 low level input detection. ($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) |

| | | | | |
|---|--------------|-----|---|--|
| 3 | GP23_LVIN_EN | R/W | 0 | Enable GPIO23 low level input detection. ($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) |
| 2 | GP22_LVIN_EN | R/W | 0 | Enable GPIO22 low level input detection. ($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) |
| 1 | GP21_LVIN_EN | R/W | 0 | Enable GPIO21 low level input detection. ($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) |
| 0 | GP20_LVIN_EN | R/W | 0 | Enable GPIO20 low level input detection. ($V_{IH} > 0.9V$, $V_{IL} < 0.3V$) |

8.2.3 GPIO3X Output Control Register — Index 40h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP37_OCTRL | R/W | 0 | GPIO37 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 6 | GP36_OCTRL | R/W | 0 | GPIO36 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 5 | GP35_OCTRL | R/W | 0 | GPIO35 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 4 | GP34_OCTRL | R/W | 0 | GPIO34 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 3 | GP33_OCTRL | R/W | 0 | GPIO33 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 2 | GP32_OCTRL | R/W | 0 | GPIO32 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 1 | GP31_OCTRL | R/W | 0 | GPIO31 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 0 | GP30_OCTRL | R/W | 0 | GPIO30 output control. Set to 1 for output function. Set to 0 for input function (default). |

8.2.4 GPIO3X Output Data Register — Index 41h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---------------------|
| 7 | GP37_ODATA | R/W | 0 | GPIO37 output data. |
| 6 | GP36_ODATA | R/W | 0 | GPIO36 output data. |
| 5 | GP35_ODATA | R/W | 0 | GPIO35 output data. |
| 4 | GP34_ODATA | R/W | 0 | GPIO34 output data. |
| 3 | GP33_ODATA | R/W | 0 | GPIO33 output data. |

| | | | | |
|---|------------|-----|---|---------------------|
| 2 | GP32_ODATA | R/W | 0 | GPIO32 output data. |
| 1 | GP31_ODATA | R/W | 0 | GPIO31 output data. |
| 0 | GP30_ODATA | R/W | 0 | GPIO30 output data. |

8.2.5 GPIO3X Input Status Register — Index 42h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|----------------------------------|
| 7 | GP37_PSTS | R | - | Read the GPIO37 data on the pin. |
| 6 | GP36_PSTS | R | - | Read the GPIO36 data on the pin. |
| 5 | GP35_PSTS | R | - | Read the GPIO35 data on the pin. |
| 4 | GP34_PSTS | R | - | Read the GPIO34 data on the pin. |
| 3 | GP33_PSTS | R | - | Read the GPIO33 data on the pin. |
| 2 | GP32_PSTS | R | - | Read the GPIO32 data on the pin. |
| 1 | GP31_PSTS | R | - | Read the GPIO31 data on the pin. |
| 0 | GP30_PSTS | R | - | Read the GPIO30 data on the pin. |

8.2.6 GPIO3X Level/Pulse Control Register — Index 43h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP37_OMODE | R/W | 0 | GPIO37 output mode. 0 – level, 1 – pulse. |
| 6 | GP36_OMODE | R/W | 0 | GPIO36 output mode. 0 – level, 1 – pulse. |
| 5 | GP35_OMODE | R/W | 0 | GPIO35 output mode. 0 – level, 1 – pulse. |
| 4 | GP34_OMODE | R/W | 0 | GPIO34 output mode. 0 – level, 1 – pulse. |
| 3 | GP33_OMODE | R/W | 0 | GPIO33 output mode. 0 – level, 1 – pulse. |
| 2 | GP32_OMODE | R/W | 0 | GPIO32 output mode. 0 – level, 1 – pulse. |
| 1 | GP31_OMODE | R/W | 0 | GPIO31 output mode. 0 – level, 1 – pulse. |
| 0 | GP30_OMODE | R/W | 0 | GPIO30 output mode. 0 – level, 1 – pulse. |

8.2.7 GPIO3X Pulse Width Control Register — Index 44h

| Bit | Name | R/W | Default | Description |
|-----|----------|-----|---------|-------------|
| 7-2 | Reserved | - | - | Reserved |

| | | | | |
|-----|-----------|-----|-----|--|
| 1-0 | GP3_PLSWD | R/W | 00b | GPIO3x pulse width. If set the GPIO3x to pulse mode, the pulse width can be defined as follows. 00b – 500us (Default) 01b – 1ms 10b – 20ms 11b – 100ms |
|-----|-----------|-----|-----|--|

8.2.8 GPIO3X Pull-up Resistor Control Register — Index 45h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP37_RESON | R/W | 0 | Turn on the GPIO37 pin internal pull-up resistor with 10KΩ. |
| 6 | GP36_RESON | R/W | 0 | Turn on the GPIO36 pin internal pull-up resistor with 10KΩ. |
| 5 | GP35_RESON | R/W | 0 | Turn on the GPIO35 pin internal pull-up resistor with 10KΩ. |
| 4 | GP34_RESON | R/W | 0 | Turn on the GPIO34 pin internal pull-up resistor with 10KΩ. |
| 3 | GP33_RESON | R/W | 0 | Turn on the GPIO33 pin internal pull-up resistor with 10KΩ. |
| 2 | GP32_RESON | R/W | 0 | Turn on the GPIO32 pin internal pull-up resistor with 10KΩ. |
| 1 | GP31_RESON | R/W | 0 | Turn on the GPIO31 pin internal pull-up resistor with 10KΩ. |
| 0 | GP30_RESON | R/W | 0 | Turn on the GPIO30 pin internal pull-up resistor with 10KΩ. |

8.2.9 GPIO3X Input De-bounce Register — Index 46h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7 | GP37_ENDB | R/W | 0 | Enable GPIO37 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 4Ch bit7 . |
| 6 | GP36_ENDB | R/W | 0 | Enable GPIO36 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 4Ch bit6 . |
| 5 | GP35_ENDB | R/W | 0 | Enable GPIO35 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 4Ch bit5 . |

| | | | | |
|---|-----------|-----|---|---|
| 4 | GP34_ENDB | R/W | 0 | Enable GPIO34 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 4Ch bit4 . |
| 3 | GP33_ENDB | R/W | 0 | Enable GPIO33 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 4Ch bit3 . |
| 2 | GP32_ENDB | R/W | 0 | Enable GPIO32 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 4Ch bit2 . |
| 1 | GP31_ENDB | R/W | 0 | Enable GPIO31 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 4Ch bit1 . |
| 0 | GP30_ENDB | R/W | 0 | Enable GPIO30 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 4Ch bit0 . |

8.2.10 GPIO3X Pin Inverse Enable Register — Index47h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7 | GP37_PINV | R/W | 0 | If the GPIO37 pin inverse was selected, the output signal would be inverted. |
| 6 | GP36_PINV | R/W | 0 | If the GPIO36 pin inverse was selected, the output signal would be inverted. |
| 5 | GP35_PINV | R/W | 0 | If the GPIO35 pin inverse was selected, the output signal would be inverted. |
| 4 | GP34_PINV | R/W | 0 | If the GPIO34 pin inverse was selected, the output signal would be inverted. |
| 3 | GP33_PINV | R/W | 0 | If the GPIO33 pin inverse was selected, the output signal would be inverted. |

| | | | | |
|---|-----------|-----|---|--|
| 2 | GP32_PINV | R/W | 0 | If the GPIO32 pin inverse was selected, the output signal would be inverted. |
| 1 | GP31_PINV | R/W | 0 | If the GPIO31 pin inverse was selected, the output signal would be inverted. |
| 0 | GP30_PINV | R/W | 0 | If the GPIO30 pin inverse was selected, the output signal would be inverted. |

8.2.11 GPIO3X Edge Detector Enable Register — Index 48h

| Bit | Name | R/W | Default | Description |
|-----|-------------|-----|---------|--|
| 7 | EN_GP37EDGE | R/W | 0 | Enable GPIO37 Edge Detector. If this bit set to 1 and GPIO37 set to input mode (40h) will enable GPIO37 edge detection. Default is disabled. |
| 6 | EN_GP36EDGE | R/W | 0 | Enable GPIO36 Edge Detector. If this bit set to 1 and GPIO36 set to input mode (40h) will enable GPIO36 edge detection. Default is disabled. |
| 5 | EN_GP35EDGE | R/W | 0 | Enable GPIO35 Edge Detector. If this bit set to 1 and GPIO35 set to input mode (40h) will enable GPIO35 edge detection. Default is disabled. |
| 4 | EN_GP34EDGE | R/W | 0 | Enable GPIO34 Edge Detector. If this bit set to 1 and GPIO34 set to input mode (40h) will enable GPIO34 edge detection. Default is disabled. |
| 3 | EN_GP33EDGE | R/W | 0 | Enable GPIO33 Edge Detector. If this bit set to 1 and GPIO33 set to input mode (40h) will enable GPIO33 edge detection. Default is disabled. |
| 2 | EN_GP32EDGE | R/W | 0 | Enable GPIO32 Edge Detector. If this bit set to 1 and GPIO32 set to input mode (40h) will enable GPIO32 edge detection. Default is disabled. |
| 1 | EN_GP31EDGE | R/W | 0 | Enable GPIO31 Edge Detector. If this bit set to 1 and GPIO31 set to input mode (40h) will enable GPIO31 edge detection. Default is disabled. |
| 0 | EN_GP30EDGE | R/W | 0 | Enable GPIO30 Edge Detector. If this bit set to 1 and GPIO30 set to input mode (40h) will enable GPIO30 edge detection. Default is disabled. |

8.2.12 GPIO3X Edge Detector Status Register — Index 49h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | STS_GP37EDGE | R | - | Indicate GPIO37 Edge Status. If set to 1, the edge of GPIO37 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 6 | STS_GP36EDGE | R | - | Indicate GPIO36 Edge Status. If set to 1, the edge of GPIO36 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 5 | STS_GP35EDGE | R | - | Indicate GPIO35 Edge Status. If set to 1, the edge of GPIO35 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 4 | STS_GP34EDGE | R | - | Indicate GPIO34 Edge Status. If set to 1, the edge of GPIO34 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 3 | STS_GP33EDGE | R | - | Indicate GPIO33 Edge Status. If set to 1, the edge of GPIO33 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 2 | STS_GP32EDGE | R | - | Indicate GPIO32 Edge Status. If set to 1, the edge of GPIO32 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 1 | STS_GP31EDGE | R | - | Indicate GPIO31 Edge Status. If set to 1, the edge of GPIO31 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 0 | STS_GP30EDGE | R | - | Indicate GPIO30 Edge Status. If set to 1, the edge of GPIO30 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

8.2.13 GPIO3X SMI Enable Register — Index 4Ah

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|--|
| 7 | EN_GP37SMI | R/W | 0 | Enable GPIO37 SMI Generation. If this bit set to 1, enable GPIO37 to generate SMI. |
| 6 | EN_GP36SMI | R/W | 0 | Enable GPIO36 SMI Generation. If this bit set to 1, enable GPIO36 to generate SMI. |
| 5 | EN_GP35SMI | R/W | 0 | Enable GPIO35 SMI Generation. If this bit set to 1, enable GPIO35 to generate SMI. |
| 4 | EN_GP34SMI | R/W | 0 | Enable GPIO34 SMI Generation. If this bit set to 1, enable GPIO34 to generate SMI. |
| 3 | EN_GP33SMI | R/W | 0 | Enable GPIO33 SMI Generation. If this bit set to 1, enable GPIO33 to generate SMI. |

| | | | | |
|---|------------|-----|---|--|
| 2 | EN_GP32SMI | R/W | 0 | Enable GPIO32 SMI Generation. If this bit set to 1, enable GPIO32 to generate SMI. |
| 1 | EN_GP31SMI | R/W | 0 | Enable GPIO31 SMI Generation. If this bit set to 1, enable GPIO31 to generate SMI. |
| 0 | EN_GP30SMI | R/W | 0 | Enable GPIO30 SMI Generation. If this bit set to 1, enable GPIO30 to generate SMI. |

8.2.14 GPIO3X Output Driving Enable Register — Index 4Bh

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | EN_GP37_OBUF | R/W | 0 | Enable GPIO37 drive high buffer. If this bit is set to 0, the pin GPIO37 will be I/OD pin, if set to 1 the pin GPIO37 is I/O pin. |
| 6 | EN_GP36_OBUF | R/W | 0 | Enable GPIO36 drive high buffer. If this bit is set to 0, the pin GPIO36 will be I/OD pin, if set to 1 the pin GPIO36 is I/O pin. |
| 5 | EN_GP35_OBUF | R/W | 0 | Enable GPIO35 drive high buffer. If this bit is set to 0, the pin GPIO35 will be I/OD pin, if set to 1 the pin GPIO35 is I/O pin. |
| 4 | EN_GP34_OBUF | R/W | 0 | Enable GPIO34 drive high buffer. If this bit is set to 0, the pin GPIO34 will be I/OD pin, if set to 1 the pin GPIO34 is I/O pin. |
| 3 | EN_GP33_OBUF | R/W | 0 | Enable GPIO33 drive high buffer. If this bit is set to 0, the pin GPIO33 will be I/OD pin, if set to 1 the pin GPIO33 is I/O pin. |
| 2 | EN_GP32_OBUF | R/W | 0 | Enable GPIO32 drive high buffer. If this bit is set to 0, the pin GPIO32 will be I/OD pin, if set to 1 the pin GPIO32 is I/O pin. |
| 1 | EN_GP31_OBUF | R/W | 0 | Enable GPIO31 drive high buffer. If this bit is set to 0, the pin GPIO31 will be I/OD pin, if set to 1 the pin GPIO31 is I/O pin. |
| 0 | EN_GP30_OBUF | R/W | 0 | Enable GPIO30 drive high buffer. If this bit is set to 0, the pin GPIO30 will be I/OD pin, if set to 1 the pin GPIO30 is I/O pin. |

8.2.15 GPIO3X De-bounce Time Select Register — Index 4Ch

| Bit | Name | R/W | Default | Description |
|-----|---------------|-----|---------|---|
| 7 | DB_TIME37_SEL | R/W | 0 | Select GPIO37 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 6 | DB_TIME36_SEL | R/W | 0 | Select GPIO36 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |

| | | | | |
|---|---------------|-----|---|---|
| 5 | DB_TIME35_SEL | R/W | 0 | Select GPIO35 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 4 | DB_TIME34_SEL | R/W | 0 | Select GPIO34 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 3 | DB_TIME33_SEL | R/W | 0 | Select GPIO33 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 2 | DB_TIME32_SEL | R/W | 0 | Select GPIO32 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 1 | DB_TIME31_SEL | R/W | 0 | Select GPIO31 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 0 | DB_TIME30_SEL | R/W | 0 | Select GPIO30 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |

8.2.16 GPIO Port Edge Status Register — Index 50h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7-5 | Reserved | - | - | Reserved |
| 4 | STS_GP4EG | R | 0 | Indicate GPIO4X Edge Status. If set to 1, the one edge of GPIO4X port has occurred (reference index 79h). |
| 3 | STS_GP3EG | R | 0 | Indicate GPIO3X Edge Status. If set to 1, the one edge of GPIO3X port has occurred (reference index 49h). |
| 2 | STS_GP2EG | R | 0 | Indicate GPIO2X Edge Status. If set to 1, the one edge of GPIO2X port has occurred (reference index 39h). |
| 1 | STS_GP1EG | R | 0 | Indicate GPIO1X Edge Status. If set to 1, the one edge of GPIO1X port has occurred (reference index 29h). |
| 0 | STS_GP0EG | R | 0 | Indicate GPIO0X Edge Status. If set to 1, the one edge of GPIO0X port has occurred (reference index 19h). |

8.2.17 SIRQ Enable Register — Index 51h

| Bit | Name | R/W | Default | Description |
|-----|----------|-----|---------|-------------|
| 7-5 | Reserved | - | - | Reserved |

| | | | | |
|---|------------|-----|---|---|
| 4 | SERIRQ4_EN | R/W | 0 | 1b: Enable SIRQ function of GPIO4X port. 0b: Disable SIRQ function of GPIO4X port. |
| 3 | SERIRQ3_EN | R/W | 0 | 1b: Enable SIRQ function of GPIO3X port. 0b: Disable SIRQ function of GPIO3X port. |
| 2 | SERIRQ2_EN | R/W | 0 | 1b: Enable SIRQ function of GPIO2X port. 0b: Disable SIRQ function of GPIO2X port. |
| 1 | SERIRQ1_EN | R/W | 0 | 1b: Enable SIRQ function of GPIO1X port. 0b: Disable SIRQ function of GPIO1X port. |
| 0 | SERIRQ0_EN | R/W | 0 | 1b: Enable SIRQ function of GPIO0X port. 0b: Disable SIRQ function of GPIO0X port. |

8.2.18 SIRQ Channel Select0 Register — Index 52h

| Bit | Name | R/W | Default | Description |
|-----|-------------|-----|---------|--|
| 7-4 | SIRQCH_SEL1 | R/W | 0 | The register would select SIRQ channel of GPIO1X port. |
| 3-0 | SIRQCH_SEL0 | R/W | 0 | The register would select SIRQ channel of GPIO0X port. |

8.2.19 SIRQ Channel Select1 Register — Index 53h

| Bit | Name | R/W | Default | Description |
|-----|-------------|-----|---------|--|
| 7-4 | SIRQCH_SEL3 | R/W | 0 | The register would select SIRQ channel of GPIO3X port. |
| 3-0 | SIRQCH_SEL2 | R/W | 0 | The register would select SIRQ channel of GPIO2X port. |

8.2.20 SIRQ Channel Select2 Register — Index 54h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | SIRQ_ACTL_EN | R/W | 0 | 0b: SIRQ function is active high. 1b: SIRQ function is active low. |
| 6-4 | Reserved | - | - | Reserved |
| 3-0 | SIRQCH_SEL4 | R/W | 0 | The register would select SIRQ channel of GPIO4X port. |

8.2.21 Access Function Internal Pull-up Enable Register — Index 56h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | Reserved | - | - | Reserved |
| 6 | ACS6_UP_EN | R/W | 0 | Enable Internal pull-up in the LAD3/GPIO47 pin. |
| 5 | ACS5_UP_EN | R/W | 0 | Enable Internal pull-up in the LAD2 pin. |
| 4 | ACS4_UP_EN | R/W | 0 | Enable Internal pull-up in the LAD1 pin. |
| 3 | ACS3_UP_EN | R/W | 0 | Enable Internal pull-up in the LAD0/SPI_MISO pin. |
| 2 | ACS2_UP_EN | R/W | 0 | Enable Internal pull-up in the LRESET#/SPI_MOSI pin. |
| 1 | ACS1_UP_EN | R/W | 0 | Enable Internal pull-up in the LFRAME#/SMBDAT/SPI_CS pin. |
| 0 | ACS0_UP_EN | R/W | 0 | Enable Internal pull-up in the LCLK/SMBCLK/SPI_CLK pin. |

8.2.22 WDT1 Reset GPIO Function Enable Register — Index 57h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|--|
| 7 | Reserved | - | - | Reserved |
| 6 | Reserved | - | - | Reserved |
| 5 | Reserved | - | - | Reserved |
| 4 | WDT1_CGP4_EN | R/W | 0 | Set 1 to enable clear function of GPIO4X register by WDT1 resetout. When WatchDog timer1 count down to zero, the WDT1 resetout will clear GP_OCTRL(70h), GP_ODATA(71h), GP_OMODE(73h), GP_PLSWD(74h), GP_RESON(75h), GP_ENDB(76h), GP_PLSINV(77h), EN_GPEDGE(78h), STS_GPEDGE(79h), EN_GPSMI(7Ah), EN_GP_OBUF(7Bh), DB_TIME_SEL(7Ch) register. |
| 3 | WDT1_CGP3_EN | R/W | 0 | Set 1 to enable clear function of GPIO3X register by WDT1 resetout. When WatchDog timer1 count down to zero, the WDT1 resetout will clear GP_OCTRL(40h), GP_ODATA(41h), GP_OMODE(43h), GP_PLSWD(44h), GP_RESON(45h), GP_ENDB(46h), GP_PLSINV(47h), EN_GPEDGE(48h), STS_GPEDGE(49h), EN_GPSMI(4Ah), EN_GP_OBUF(4Bh), DB_TIME_SEL(4Ch) register. |

| | | | | |
|---|--------------|-----|---|--|
| 2 | WDT1_CGP2_EN | R/W | 0 | Set 1 to enable clear function of GPIO2X register by WDT1 resetout. When WatchDog timer1 count down to zero, the WDT1 resetout will clear GP_OCTRL(30h), GP_ODATA(31h), GP_OMODE(33h), GP_PLSWD(34h), GP_RESON(35h), GP_ENDB(36h), GP_PLSINV(37h), EN_GPEDGE(38h), STS_GPEDGE(39h), EN_GPSMI(3Ah), EN_GP_OBUF(3Bh), DB_TIME_SEL(3Ch) register. |
| 1 | WDT1_CGP1_EN | R/W | 0 | Set 1 to enable clear function of GPIO1X register by WDT1 resetout. When WatchDog timer1 count down to zero, the WDT1 resetout will clear GP_OCTRL(20h), GP_ODATA(21h), GP_OMODE(23h), GP_PLSWD(24h), GP_RESON(25h), GP_ENDB(26h), GP_PLSINV(27h), EN_GPEDGE(28h), STS_GPEDGE(29h), EN_GPSMI(2Ah), EN_GP_OBUF(2Bh), DB_TIME_SEL(2Ch) register. |
| 0 | WDT1_CGP0_EN | R/W | 0 | Set 1 to enable clear function of GPIO0X register by WDT1 resetout. When WatchDog timer1 count down to zero, the WDT1 resetout will clear GP_OCTRL(10h), GP_ODATA(11h), GP_OMODE(13h), GP_PLSWD(14h), GP_RESON(15h), GP_ENDB(16h), GP_PLSINV(17h), EN_GPEDGE(18h), STS_GPEDGE(19h), EN_GPSMI(1Ah), EN_GP_OBUF(1Bh), DB_TIME_SEL(1Ch) register. |

8.2.23 WDT2 Reset GPIO Function Enable Register — Index 58h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|--|
| 7 | Reserved | - | - | Reserved |
| 6 | Reserved | - | - | Reserved |
| 5 | Reserved | - | - | Reserved |
| 4 | WDT2_CGP4_EN | R/W | 0 | Set 1 to enable clear function of GPIO4X register by WDT2 resetout. When WatchDog timer2 count down to zero, the WDT2 resetout will clear GP_OCTRL(70h), GP_ODATA(71h), GP_OMODE(73h), GP_PLSWD(74h), GP_RESON(75h), GP_ENDB(76h), GP_PLSINV(77h), EN_GPEDGE(78h), STS_GPEDGE(79h), EN_GPSMI(7Ah), EN_GP_OBUF(7Bh), DB_TIME_SEL(7Ch) register. |

| | | | | |
|---|--------------|-----|---|--|
| 3 | WDT2_CGP3_EN | R/W | 0 | Set 1 to enable clear function of GPIO3X register by WDT2 resetout. When WatchDog timer2 count down to zero, the WDT2 resetout will clear GP_OCTRL(40h), GP_ODATA(41h), GP_OMODE(43h), GP_PLSWD(44h), GP_RESON(45h), GP_ENDB(46h), GP_PLSINV(47h), EN_GPEDGE(48h), STS_GPEDGE(49h), EN_GPSMI(4Ah), EN_GP_OBUF(4Bh), DB_TIME_SEL(4Ch) register. |
| 2 | WDT2_CGP2_EN | R/W | 0 | Set 1 to enable clear function of GPIO2X register by WDT2 resetout. When WatchDog timer2 count down to zero, the WDT2 resetout will clear GP_OCTRL(30h), GP_ODATA(31h), GP_OMODE(33h), GP_PLSWD(34h), GP_RESON(35h), GP_ENDB(36h), GP_PLSINV(37h), EN_GPEDGE(38h), STS_GPEDGE(39h), EN_GPSMI(3Ah), EN_GP_OBUF(3Bh), DB_TIME_SEL(3Ch) register. |
| 1 | WDT2_CGP1_EN | R/W | 0 | Set 1 to enable clear function of GPIO1X register by WDT2 resetout. When WatchDog timer2 count down to zero, the WDT2 resetout will clear GP_OCTRL(20h), GP_ODATA(21h), GP_OMODE(23h), GP_PLSWD(24h), GP_RESON(25h), GP_ENDB(26h), GP_PLSINV(27h), EN_GPEDGE(28h), STS_GPEDGE(29h), EN_GPSMI(2Ah), EN_GP_OBUF(2Bh), DB_TIME_SEL(2Ch) register. |
| 0 | WDT2_CGP0_EN | R/W | 0 | Set 1 to enable clear function of GPIO0X register by WDT2 resetout. When WatchDog timer2 count down to zero, the WDT2 resetout will clear GP_OCTRL(10h), GP_ODATA(11h), GP_OMODE(13h), GP_PLSWD(14h), GP_RESON(15h), GP_ENDB(16h), GP_PLSINV(17h), EN_GPEDGE(18h), STS_GPEDGE(19h), EN_GPSMI(1Ah), EN_GP_OBUF(1Bh), DB_TIME_SEL(1Ch) register. |

8.2.24 LRESET Reset GPIO Function Enable Register — Index 59h

| Bit | Name | R/W | Default | Description |
|-----|----------|-----|---------|-------------|
| 7 | Reserved | - | - | Reserved |
| 6 | Reserved | - | - | Reserved |
| 5 | Reserved | - | - | Reserved |

| | | | | |
|---|--------------|-----|---|---|
| 4 | LRST_CGP4_EN | R/W | 0 | Set 1 to enable clear function of GPIO4X register by lreset. Then LRESET will clear GP_OCTRL(70h), GP_ODATA(71h), GP_OMODE(73h), GP_PLSWD(74h), GP_RESON(75h), GP_ENDB(76h), GP_PLSINV(77h), EN_GPEDGE(78h), STS_GPEDGE(79h), EN_GPSMI(7ah), EN_GP_OBUF(7bh), DB_TIME_SEL(7ch) register. |
| 3 | LRST_CGP3_EN | R/W | 0 | Set 1 to enable GPIO3X register clear function by lreset. Then LRESET will clear GP_OCTRL(40h), GP_ODATA(41h), GP_OMODE(43h), GP_PLSWD(44h), GP_RESON(45h), GP_ENDB(46h), GP_PLSINV(47h), EN_GPEDGE(48h), STS_GPEDGE(49h), EN_GPSMI(4Ah), EN_GP_OBUF(4Bh), DB_TIME_SEL(4Ch) register. |
| 2 | LRST_CGP2_EN | R/W | 0 | Set 1 to enable GPIO2X register clear function by lreset. Then LRESET will clear GP_OCTRL(30h), GP_ODATA(31h), GP_OMODE(33h), GP_PLSWD(34h), GP_RESON(35h), GP_ENDB(36h), GP_PLSINV(37h), EN_GPEDGE(38h), STS_GPEDGE(39h), EN_GPSMI(3Ah), EN_GP_OBUF(3Bh), DB_TIME_SEL(3Ch) register. |
| 1 | LRST_CGP1_EN | R/W | 0 | Set 1 to enable GPIO1X register clear function by lreset. Then LRESET will clear GP_OCTRL(20h), GP_ODATA(21h), GP_OMODE(23h), GP_PLSWD(24h), GP_RESON(25h), GP_ENDB(26h), GP_PLSINV(27h), EN_GPEDGE(28h), STS_GPEDGE(29h), EN_GPSMI(2Ah), EN_GP_OBUF(2Bh), DB_TIME_SEL(2Ch) register. |
| 0 | LRST_CGP0_EN | R/W | 0 | Set 1 to enable GPIO0X register clear function by lreset. Then LRESET will clear GP_OCTRL(10h), GP_ODATA(11h), GP_OMODE(13h), GP_PLSWD(14h), GP_RESON(15h), GP_ENDB(16h), GP_PLSINV(17h), EN_GPEDGE(18h), STS_GPEDGE(19h), EN_GPSMI(1Ah), EN_GP_OBUF(1Bh), DB_TIME_SEL(1Ch) register. |

8.2.25 Chip ID1 Register – Index 5Ah

| Bit | Name | R/W | Default | Description |
|-----|----------|-----|---------|-------------|
| 7-0 | CHIP_ID1 | R | 10h | CHIP ID1 |

8.2.26 Chip ID2 Register – Index 5Bh

| Bit | Name | R/W | Default | Description |
|-----|----------|-----|---------|-------------|
| 7-0 | CHIP_ID2 | R | 11h | CHIP ID2 |

8.2.27 Vender ID1 Register – Index 5Dh

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|-------------|
| 7-0 | VENDER_ID1 | R | 19h | VENDER ID1 |

8.2.28 Vender ID2 Register – Index 5Eh

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|-------------|
| 7-0 | VENDER_ID2 | R | 34h | VENDER ID2 |

8.2.29 Base Address High Byte Register — Index 60h

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|-------------------------------|
| 7-0 | BA_H | R/W | 00h | The high-byte of Base Address |

8.2.30 Base Address Low Byte Register — Index 61h

| Bit | Name | R/W | Default | Description |
|-----|------|-----|---------|------------------------------|
| 7-0 | BA_L | R/W | 00h | The low-byte of Base Address |

If Base-Address was set to 0200h and users wrote data at index 0200h(0201h, 0202h, 0203h and 0204h), the GPIO0X(GPIO1X, GPIO2X, GPIO3X and GPIO4X) would output the data that users wrote. Then, users read index 0200h(0201h, 0202h, 0203h or 0204h) and would get the status of GPIO0X(GPIO1X, GPIO2X, GPIO3X and GPIO4X) pins. Also, 0205h, 0206h and 0207h was reserved, so F75113 would only compare bit 23 ~ bit 3 of Base-Address.

8.2.31 GPIO4X Output Control Register — Index 70h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP47_OCTRL | R/W | 0 | GPIO47 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 6 | GP46_OCTRL | R/W | 0 | GPIO46 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 5 | GP45_OCTRL | R/W | 0 | GPIO45 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 4 | GP44_OCTRL | R/W | 0 | GPIO44 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 3 | GP43_OCTRL | R/W | 0 | GPIO43 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 2 | GP42_OCTRL | R/W | 0 | GPIO42 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 1 | GP41_OCTRL | R/W | 0 | GPIO41 output control. Set to 1 for output function. Set to 0 for input function (default). |
| 0 | GP40_OCTRL | R/W | 0 | GPIO40 output control. Set to 1 for output function. Set to 0 for input function (default). |

8.2.32 GPIO4X Output Data Register — Index 71h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---------------------|
| 7 | GP47_ODATA | R/W | 0 | GPIO47 output data. |
| 6 | GP46_ODATA | R/W | 0 | GPIO46 output data. |
| 5 | GP45_ODATA | R/W | 0 | GPIO45 output data. |
| 4 | GP44_ODATA | R/W | 0 | GPIO44 output data. |
| 3 | GP43_ODATA | R/W | 0 | GPIO43 output data. |
| 2 | GP42_ODATA | R/W | 0 | GPIO42 output data. |
| 1 | GP41_ODATA | R/W | 0 | GPIO41 output data. |
| 0 | GP40_ODATA | R/W | 0 | GPIO40 output data. |

8.2.33 GPIO4X Input Status Register — Index 72h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|----------------------------------|
| 7 | GP47_PSTS | R | - | Read the GPIO47 data on the pin. |
| 6 | GP46_PSTS | R | - | Read the GPIO46 data on the pin. |
| 5 | GP45_PSTS | R | - | Read the GPIO45 data on the pin. |
| 4 | GP44_PSTS | R | - | Read the GPIO44 data on the pin. |
| 3 | GP43_PSTS | R | - | Read the GPIO43 data on the pin. |
| 2 | GP42_PSTS | R | - | Read the GPIO42 data on the pin. |
| 1 | GP41_PSTS | R | - | Read the GPIO41 data on the pin. |
| 0 | GP40_PSTS | R | - | Read the GPIO40 data on the pin. |

8.2.34 GPIO4X Level/Pulse Control Register — Index 73h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP47_OMODE | R/W | 0 | GPIO47 output mode. 0 – level, 1 – pulse. |
| 6 | GP46_OMODE | R/W | 0 | GPIO46 output mode. 0 – level, 1 – pulse. |
| 5 | GP45_OMODE | R/W | 0 | GPIO45 output mode. 0 – level, 1 – pulse. |
| 4 | GP44_OMODE | R/W | 0 | GPIO44 output mode. 0 – level, 1 – pulse. |
| 3 | GP43_OMODE | R/W | 0 | GPIO43 output mode. 0 – level, 1 – pulse. |
| 2 | GP42_OMODE | R/W | 0 | GPIO42 output mode. 0 – level, 1 – pulse. |
| 1 | GP41_OMODE | R/W | 0 | GPIO41 output mode. 0 – level, 1 – pulse. |
| 0 | GP40_OMODE | R/W | 0 | GPIO40 output mode. 0 – level, 1 – pulse. |

8.2.35 GPIO4X Pulse Width Control Register — Index 74h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7-2 | Reserved | - | - | Reserved |
| 1-0 | GP4_PLSWD | R/W | 0 | GPIO4x pulse width. If set the GPIO4x to pulse mode, the pulse width can be defined as follows. 00b – 500us (Default) 01b – 1ms 10b – 20ms 11b – 100ms |

8.2.36 GPIO4X Pull-up Resistor Control Register — Index 75h

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|---|
| 7 | GP47_RESON | R/W | 0 | Turn on the GPIO47 pin internal pull-up resistor with 10KΩ. |
| 6 | GP46_RESON | R/W | 0 | Turn on the GPIO46 pin internal pull-up resistor with 10KΩ. |
| 5 | GP45_RESON | R/W | 0 | Turn on the GPIO45 pin internal pull-up resistor with 10KΩ. |
| 4 | GP44_RESON | R/W | 0 | Turn on the GPIO44 pin internal pull-up resistor with 10KΩ. |
| 3 | GP43_RESON | R/W | 0 | Turn on the GPIO43 pin internal pull-up resistor with 10KΩ. |
| 2 | GP42_RESON | R/W | 0 | Turn on the GPIO42 pin internal pull-up resistor with 10KΩ. |
| 1 | GP41_RESON | R/W | 0 | Turn on the GPIO41 pin internal pull-up resistor with 10KΩ. |
| 0 | GP40_RESON | R/W | 0 | Turn on the GPIO40 pin internal pull-up resistor with 10KΩ. |

8.2.37 GPIO4X Input De-bounce Register — Index 76h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|---|
| 7 | GP47_ENDB | R/W | 0 | Enable GPIO47 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 7Ch bit7 . |
| 6 | GP46_ENDB | R/W | 0 | Enable GPIO46 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 7Ch bit6 . |
| 5 | GP45_ENDB | R/W | 0 | Enable GPIO45 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 7Ch bit5 . |
| 4 | GP44_ENDB | R/W | 0 | Enable GPIO44 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 7Ch bit4 . |
| 3 | GP43_ENDB | R/W | 0 | Enable GPIO43 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 7Ch bit3 . |

| | | | | |
|---|-----------|-----|---|--|
| 2 | GP42_ENDB | R/W | 0 | Enable GPIO42 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 7Ch bit2. |
| 1 | GP41_ENDB | R/W | 0 | Enable GPIO41 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 7Ch bit1. |
| 0 | GP40_ENDB | R/W | 0 | Enable GPIO40 input de-bounce with 10u (Maximum, when input signal and detected clock is synchronicity) or 25ms (Maximum, when input signal and detected clock is synchronicity) second that selected by 7Ch bit0. |

8.2.38 GPIO4X Pin Inverse Enable Register — Index77h

| Bit | Name | R/W | Default | Description |
|-----|-----------|-----|---------|--|
| 7 | GP47_PINV | R/W | 0 | If the GPIO47 pin inverse was selected, the output signal would be inverted. |
| 6 | GP46_PINV | R/W | 0 | If the GPIO46 pin inverse was selected, the output signal would be inverted. |
| 5 | GP45_PINV | R/W | 0 | If the GPIO45 pin inverse was selected, the output signal would be inverted. |
| 4 | GP44_PINV | R/W | 0 | If the GPIO44 pin inverse was selected, the output signal would be inverted. |
| 3 | GP43_PINV | R/W | 0 | If the GPIO43 pin inverse was selected, the output signal would be inverted. |
| 2 | GP42_PINV | R/W | 0 | If the GPIO42 pin inverse was selected, the output signal would be inverted. |
| 1 | GP41_PINV | R/W | 0 | If the GPIO41 pin inverse was selected, the output signal would be inverted. |
| 0 | GP40_PINV | R/W | 0 | If the GPIO40 pin inverse was selected, the output signal would be inverted. |

8.2.39 GPIO4X Edge Detector Enable Register — Index 78h

| Bit | Name | R/W | Default | Description |
|-----|-------------|-----|---------|--|
| 7 | EN_GP47EDGE | R/W | 0 | Enable GPIO47 Edge Detector. If this bit set to 1 and GPIO47 set to input mode (70h) will enable GPIO47 edge detection. Default is disabled. |
| 6 | EN_GP46EDGE | R/W | 0 | Enable GPIO46 Edge Detector. If this bit set to 1 and GPIO46 set to input mode (70h) will enable GPIO36 edge detection. Default is disabled. |
| 5 | EN_GP45EDGE | R/W | 0 | Enable GPIO45 Edge Detector. If this bit set to 1 and GPIO45 set to input mode (70h) will enable GPIO35 edge detection. Default is disabled. |
| 4 | EN_GP44EDGE | R/W | 0 | Enable GPIO44 Edge Detector. If this bit set to 1 and GPIO44 set to input mode (70h) will enable GPIO34 edge detection. Default is disabled. |
| 3 | EN_GP43EDGE | R/W | 0 | Enable GPIO43 Edge Detector. If this bit set to 1 and GPIO43 set to input mode (70h) will enable GPIO33 edge detection. Default is disabled. |
| 2 | EN_GP42EDGE | R/W | 0 | Enable GPIO42 Edge Detector. If this bit set to 1 and GPIO42 set to input mode (70h) will enable GPIO32 edge detection. Default is disabled. |
| 1 | EN_GP41EDGE | R/W | 0 | Enable GPIO41 Edge Detector. If this bit set to 1 and GPIO41 set to input mode (70h) will enable GPIO31 edge detection. Default is disabled. |
| 0 | EN_GP40EDGE | R/W | 0 | Enable GPIO40 Edge Detector. If this bit set to 1 and GPIO40 set to input mode (70h) will enable GPIO30 edge detection. Default is disabled. |

8.2.40 GPIO4X Edge Detector Status Register — Index 79h

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | STS_GP47EDGE | R | - | Indicate GPIO47 Edge Status. If set to 1, the edge of GPIO47 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 6 | STS_GP46EDGE | R | - | Indicate GPIO46 Edge Status. If set to 1, the edge of GPIO46 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

| | | | | |
|---|--------------|---|---|---|
| 5 | STS_GP45EDGE | R | - | Indicate GPIO45 Edge Status. If set to 1, the edge of GPIO45 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 4 | STS_GP44EDGE | R | - | Indicate GPIO44 Edge Status. If set to 1, the edge of GPIO44 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 3 | STS_GP43EDGE | R | - | Indicate GPIO43 Edge Status. If set to 1, the edge of GPIO43 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 2 | STS_GP42EDGE | R | - | Indicate GPIO42 Edge Status. If set to 1, the edge of GPIO42 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 1 | STS_GP41EDGE | R | - | Indicate GPIO41 Edge Status. If set to 1, the edge of GPIO41 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 0 | STS_GP40EDGE | R | - | Indicate GPIO40 Edge Status. If set to 1, the edge of GPIO40 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

8.2.41 GPIO4X SMI Enable Register — Index 7Ah

| Bit | Name | R/W | Default | Description |
|-----|------------|-----|---------|--|
| 7 | EN_GP47SMI | R/W | 0 | Enable GPIO47 SMI Generation. If this bit set to 1, enable GPIO47 to generate SMI. |
| 6 | EN_GP46SMI | R/W | 0 | Enable GPIO46 SMI Generation. If this bit set to 1, enable GPIO46 to generate SMI. |
| 5 | EN_GP45SMI | R/W | 0 | Enable GPIO45 SMI Generation. If this bit set to 1, enable GPIO45 to generate SMI. |
| 4 | EN_GP44SMI | R/W | 0 | Enable GPIO44 SMI Generation. If this bit set to 1, enable GPIO44 to generate SMI. |
| 3 | EN_GP43SMI | R/W | 0 | Enable GPIO43 SMI Generation. If this bit set to 1, enable GPIO43 to generate SMI. |
| 2 | EN_GP42SMI | R/W | 0 | Enable GPIO42 SMI Generation. If this bit set to 1, enable GPIO42 to generate SMI. |
| 1 | EN_GP41SMI | R/W | 0 | Enable GPIO41 SMI Generation. If this bit set to 1, enable GPIO41 to generate SMI. |
| 0 | EN_GP40SMI | R/W | 0 | Enable GPIO40 SMI Generation. If this bit set to 1, enable GPIO40 to generate SMI. |

8.2.42 GPIO4X Output Driving Enable Register — Index 7Bh

| Bit | Name | R/W | Default | Description |
|-----|--------------|-----|---------|---|
| 7 | EN_GP47_OBUF | R/W | 0 | Enable GPIO47 drive high buffer. If this bit is set to 0, the pin GPIO47 will be I/OD pin, if set to 1 the pin GPIO47 is I/O pin. |
| 6 | EN_GP46_OBUF | R/W | 0 | Enable GPIO46 drive high buffer. If this bit is set to 0, the pin GPIO46 will be I/OD pin, if set to 1 the pin GPIO46 is I/O pin. |
| 5 | EN_GP45_OBUF | R/W | 0 | Enable GPIO45 drive high buffer. If this bit is set to 0, the pin GPIO45 will be I/OD pin, if set to 1 the pin GPIO45 is I/O pin. |
| 4 | EN_GP44_OBUF | R/W | 0 | Enable GPIO44 drive high buffer. If this bit is set to 0, the pin GPIO44 will be I/OD pin, if set to 1 the pin GPIO44 is I/O pin. |
| 3 | EN_GP43_OBUF | R/W | 0 | Enable GPIO43 drive high buffer. If this bit is set to 0, the pin GPIO43 will be I/OD pin, if set to 1 the pin GPIO43 is I/O pin. |
| 2 | EN_GP42_OBUF | R/W | 0 | Enable GPIO42 drive high buffer. If this bit is set to 0, the pin GPIO42 will be I/OD pin, if set to 1 the pin GPIO42 is I/O pin. |
| 1 | EN_GP41_OBUF | R/W | 0 | Enable GPIO41 drive high buffer. If this bit is set to 0, the pin GPIO41 will be I/OD pin, if set to 1 the pin GPIO41 is I/O pin. |
| 0 | EN_GP40_OBUF | R/W | 0 | Enable GPIO40 drive high buffer. If this bit is set to 0, the pin GPIO40 will be I/OD pin, if set to 1 the pin GPIO40 is I/O pin. |

8.2.43 GPIO4X De-bounce Time Select Register — Index 7Ch

| Bit | Name | R/W | Default | Description |
|-----|---------------|-----|---------|---|
| 7 | DB_TIME47_SEL | R/W | 0 | Select GPIO47 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 6 | DB_TIME46_SEL | R/W | 0 | Select GPIO46 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 5 | DB_TIME45_SEL | R/W | 0 | Select GPIO45 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 4 | DB_TIME44_SEL | R/W | 0 | Select GPIO44 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 3 | DB_TIME43_SEL | R/W | 0 | Select GPIO43 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |

| | | | | |
|---|---------------|-----|---|---|
| 2 | DB_TIME42_SEL | R/W | 0 | Select GPIO42 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 1 | DB_TIME41_SEL | R/W | 0 | Select GPIO41 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |
| 0 | DB_TIME40_SEL | R/W | 0 | Select GPIO40 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 10us (default). |

9. Electrical Characteristic

Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|-----------------------|-------------|------|
| Power Supply Voltage | -0.5 to 4.0 | V |
| Input Voltage | -0.5 to 5.5 | V |
| Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -55 to +150 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

($T_a = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.3\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$) (Note)

| PARAMETER | CONDITONS | MIN | TYP | MAX | Unit |
|----------------------------------|--|-----|--------------------|--------------------|------|
| Temperature Error, Remote Diode | $60^\circ\text{C} < T_D < 145^\circ\text{C}$, $V_{CC} = 3.0\text{V}$ to 3.6V $0^\circ\text{C} < T_D < 60^\circ\text{C}$ $100^\circ\text{C} < T_D < 145^\circ\text{C}$ | | ± 1 ± 1 | ± 3 ± 3 | °C |
| Supply Voltage range | | 3.0 | 3.3 | 3.6 | V |
| Average operating supply current | | | 8 | | mA |
| Standby supply current | | | 5 | | uA |
| Resolution | | | 1 | | °C |
| Power on reset threshold | | | 2.2 | 2.4 | V |
| Diode source current | High Level | | 95 | | uA |
| | Low Level | | 10 | | uA |

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|------|------|------|------|------|---------------|
| I/O_{16st5v} - TTL level bi-directional pin with source-sink capability of 16 mA, schmitt trigger and 5V tolerance | | | | | | |
| Input Low Threshold Voltage | VIL | | | 0.8 | V | |
| Input High Threshold Voltage | VIH | 2.0 | | | V | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 16 mA |
| Output High Voltage | VOH | 2.4 | | | V | IOH = - 16 mA |
| Input High Leakage | ILIH | | | +1 | μA | VIN = VDD |
| Input Low Leakage | ILIL | -1 | | | μA | VIN = 0V |

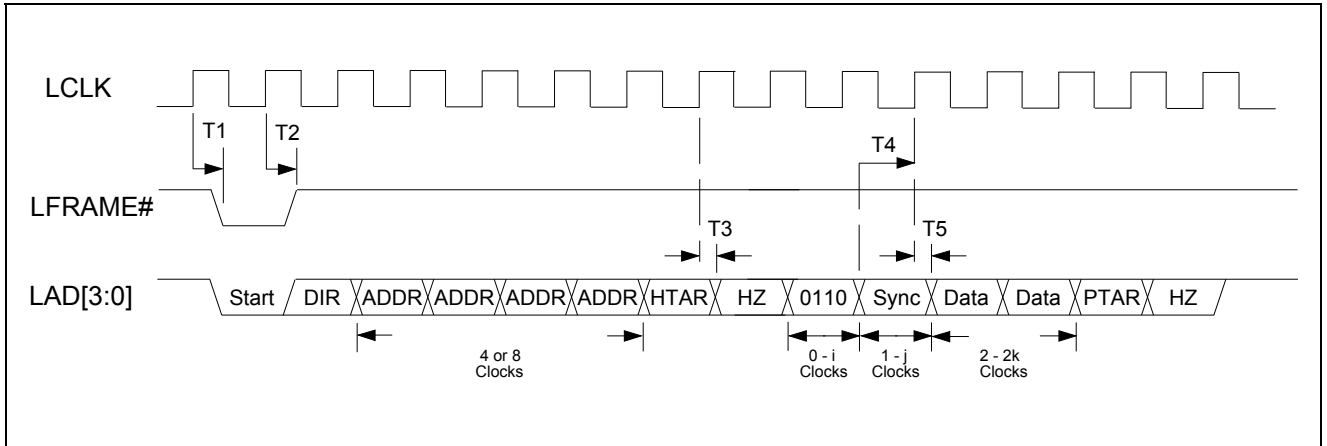
| I/OOD_{16st5v} - TTL level bi-directional pin, Output pin with 16mA source-sink capability, schmitt trigger, 5V tolerance and can programming to open-drain function. | | | | | | |
|--|------|-----|-----|-----|----|-------------|
| Input Low Threshold Voltage | Vt- | | | 0.8 | V | VDD = 3.3 V |
| Input High Threshold Voltage | Vt+ | 2.0 | | | V | VDD = 3.3 V |
| Output Low Current | IOL | | -16 | -9 | mA | VOL = 0.4 V |
| Output High Current | IOH | +9 | +16 | | mA | VOH = 2.4V |
| Input High Leakage | ILIH | | | +1 | μA | VIN = VDD |
| Input Low Leakage | ILIL | -1 | | | μA | VIN = 0V |
| IN_{st5v} - TTL level input pin with schmitt trigger, 5V tolerance. | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |
| Input High Leakage | ILIH | | | +1 | μA | VIN = VDD |
| Input Low Leakage | ILIL | -1 | | | μA | VIN = 0 V |
| IN_v - Low level input | | | | | | |
| Input Low Voltage | VIL | | 0.3 | | V | |
| Input High Voltage | VIH | | 0.9 | | V | |
| Input High Leakage | ILIH | | | +1 | μA | VIN = 1.2V |
| Input Low Leakage | ILIL | | | -1 | μA | VIN = 0 V |
| OD_{16st5v} - Open-drain output with 16 mA sink capability, schmitt trigger, 5V tolerance. | | | | | | |
| Output Low Current | IOL | | -16 | | mA | VOL = 0.4V |

AC Characteristics

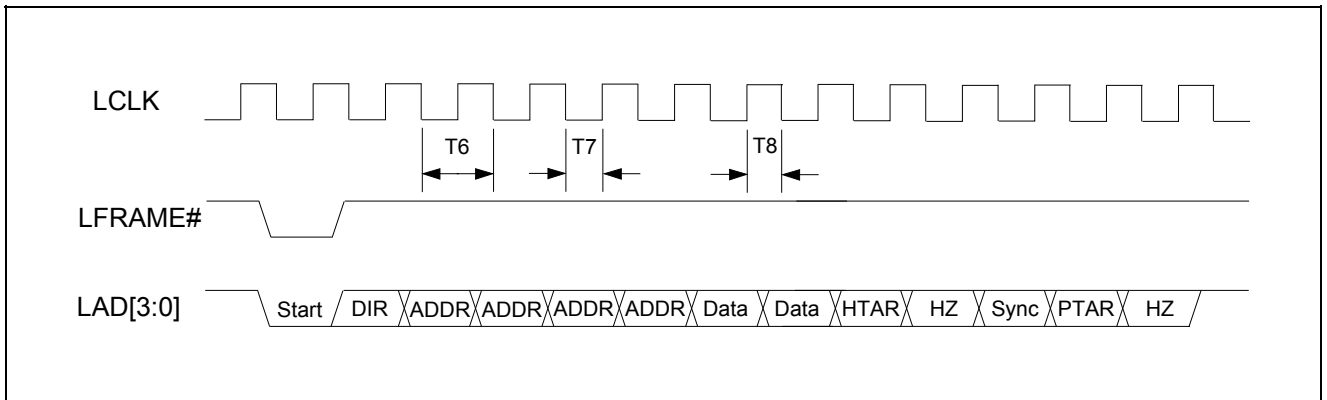
9.3.1 LPC Interface

| NO. | DESCRIPTION | MIN. | MAX. | UNIT |
|-----|--|------|------|------|
| T1 | LFRAME# drive low after rising edge of LCLK | 2 | 12 | nS |
| T2 | LFRAME# drive high after rising edge of LCLK | 2 | 12 | nS |
| T3 | LDA[3:0] floating after rising edge of LCLK | | 28 | nS |
| T4 | LDA[3:0] setup time to rising edge of LCLK | 7 | | nS |
| T5 | LDA[3:0] hold time from rising edge of LCLK | 0 | | nS |
| T6 | Period of LCLK | 27 | 33 | nS |
| T7 | Duration of LCLK low | 12 | | nS |
| T8 | Duration of LCLK high | 12 | | nS |

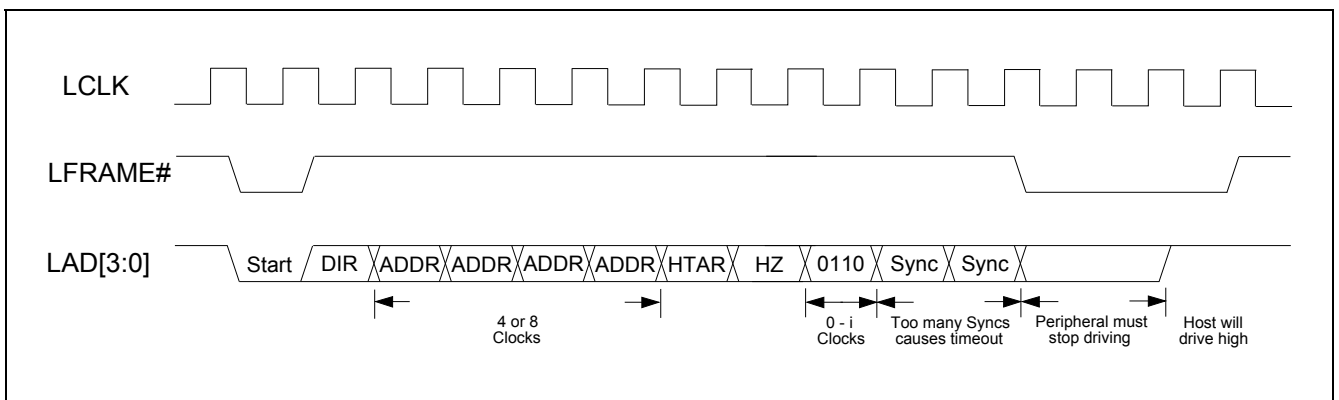
LPC interface timing table

Typical Timing for Host Read


Host read timing diagram

Typical Timing for Host Write


Host write timing diagram

Timing for Abort Mechanism


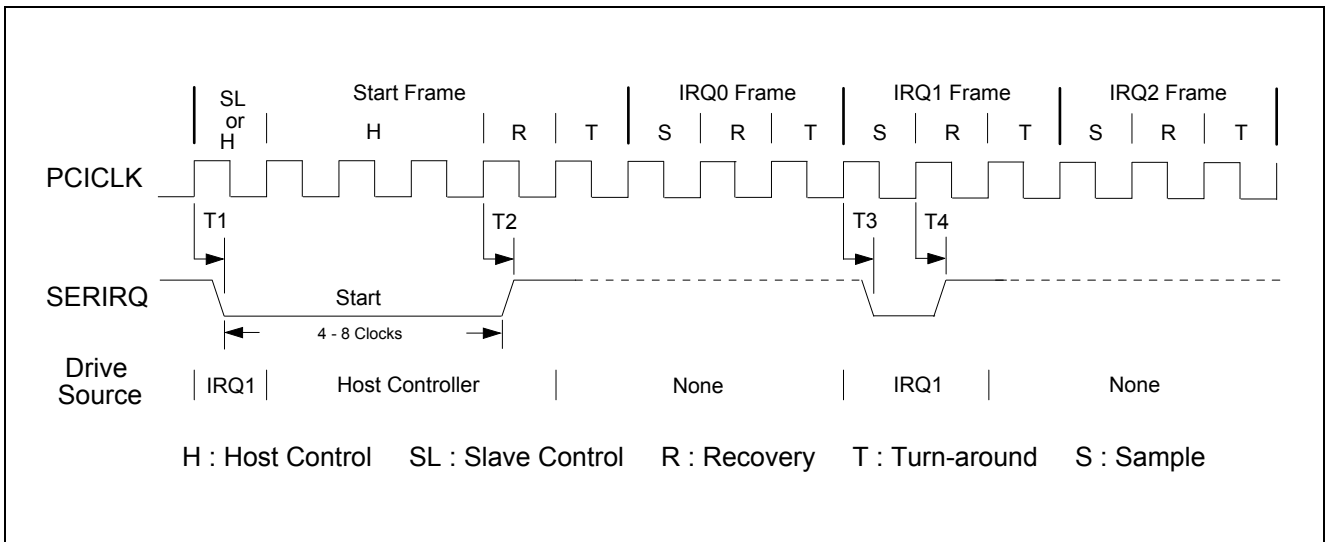
Host abort timing diagram

9.3.2 Serialized IRQ Interface

| NO. | DESCRIPTION | MIN. | MAX. | UNIT |
|-----|---|------|------|------|
| T1 | Host drive SERIRQ low after rising edge of PCICLK | 2 | 12 | nS |
| T2 | Host drive SERIRQ high after rising edge of PCICLK | 2 | 12 | nS |
| T3 | Slave drive SERIRQ low after rising edge of PCICLK | 2 | 12 | nS |
| T4 | Slave drive SERIRQ high after rising edge of PCICLK | 2 | 12 | nS |
| T5 | Period of PCICLK | 27 | 33 | nS |
| T6 | Duration of PCICLK low | 12 | | nS |
| T7 | Duration of PCICLK high | 12 | | nS |

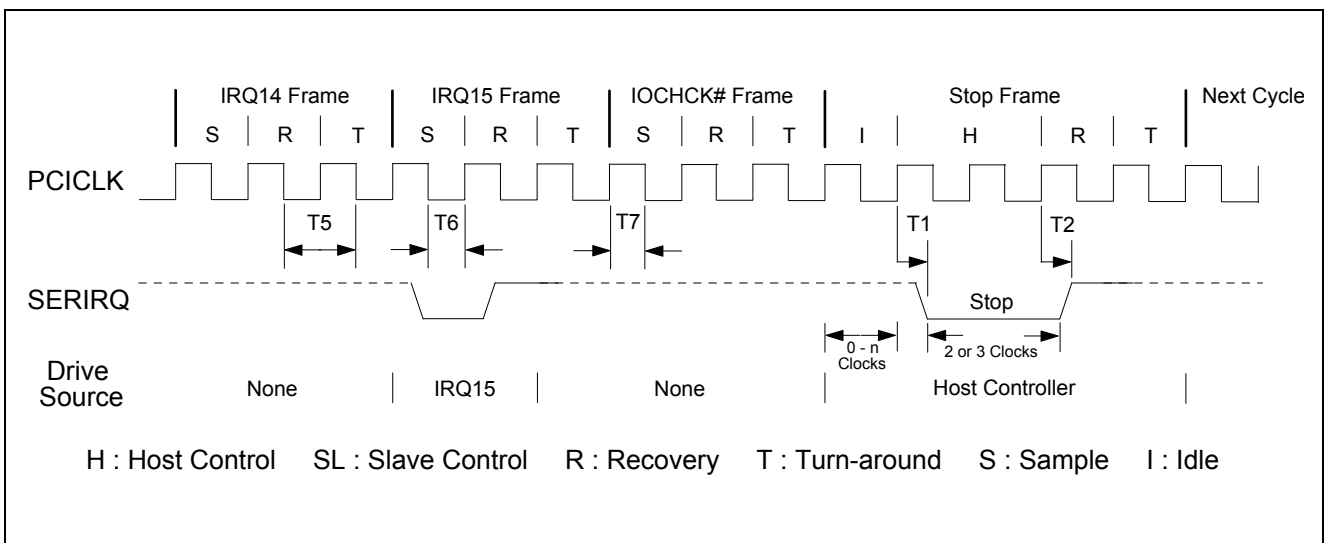
SIRQ interface timing table

Start Frame Timing



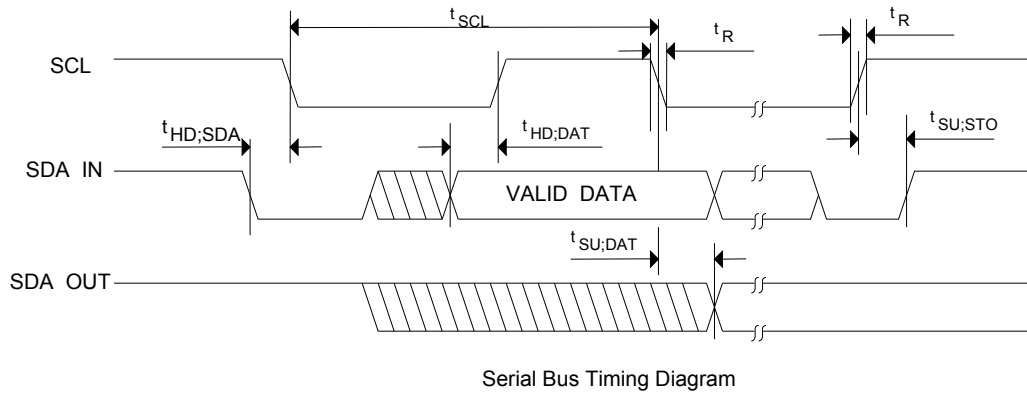
SIRQ start frame timing diagram

Stop Frame Timing



SIRQ stop frame timing diagram

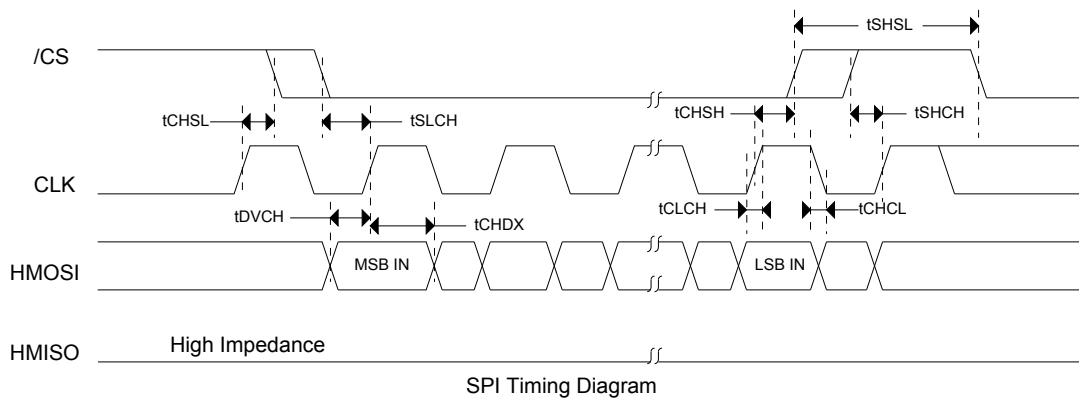
9.3.3 SMBus Interface



Serial Bus Timing

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|------------------------------|--------------|------|------|------|
| SCL clock period | t_{SCL} | 10 | | uS |
| Start condition hold time | $t_{HD;SDA}$ | 4.7 | | uS |
| Stop condition setup-up time | $t_{SU;STO}$ | 4.7 | | uS |
| DATA to SCL setup time | $t_{SU;DAT}$ | 120 | | nS |
| DATA to SCL hold time | $t_{HD;DAT}$ | 5 | | nS |
| SCL and SDA rise time | t_R | | 1.0 | uS |
| SCL and SDA fall time | t_F | | 300 | nS |

9.3.4 SPI Interface



SPI Timing

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|------------|------|------|------|
| /CS not active hold time relative to CLK | t_{CHSL} | 5 | | nS |
| Data in setup time | t_{DVCH} | 2 | | nS |
| /CS active setup time relative to CLK | t_{SLCH} | 5 | | nS |
| Data in hold time | t_{CHDX} | 5 | | nS |
| Clock rise time peak to peak | t_{CLCH} | 0.1 | | V/nS |
| /CS active hold time relative to CLK | t_{CHSH} | 10 | | nS |
| /CS deselect time | t_{SHSL} | 100 | | nS |
| /CS not active setup time relative to CLK | t_{SHCH} | 0 | | nS |
| Clock fall time peak to peak | t_{CHCL} | 0.1 | | V/nS |

9.3.5 Internal Clock

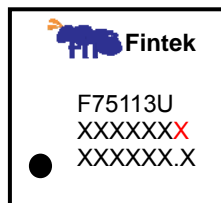
| DESCRIPTION | MIN. | MAX. | UNIT |
|----------------|------|------|------|
| Internal Clock | 400 | 600 | KHz |

10. Ordering Information

| Part Number | Package Type | Production Flow |
|-------------|--------------|--------------------------|
| F75113U | 48 PIN TQFP | Commercial, 0°C to +70°C |

11. Top Marking Specification

The version identification is shown as the bold red three characters. Please refer to below table for detail:



Fintek Logo

● : Pin 1 Identifier

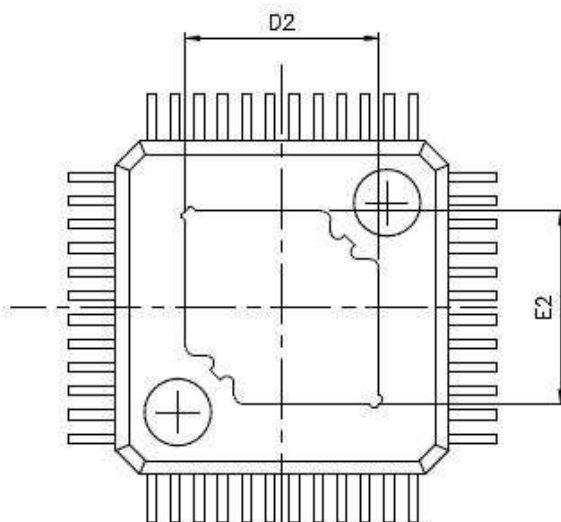
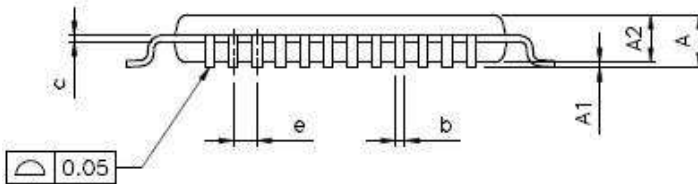
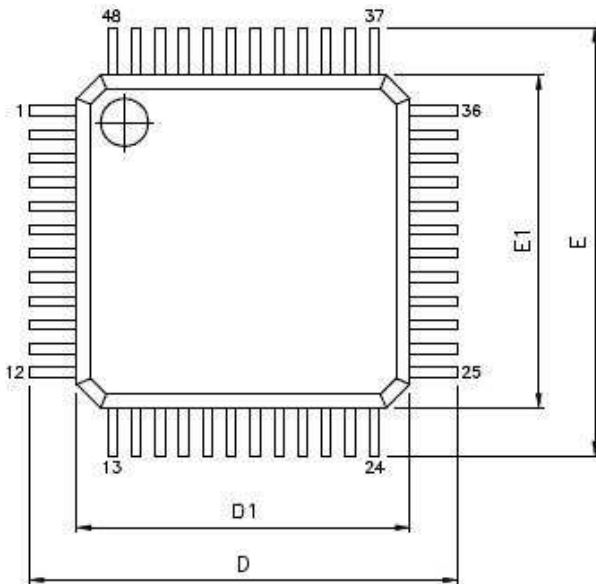
1st Line: Device Name → **F75113U**, where U means the package code

2nd Line: Assembly Plant Code (x) + Assembled Year Code (x) + Week Code (xx) + Fintek Internal Code (xx) + **IC Version (x)** where A means version A, B means version B, ...

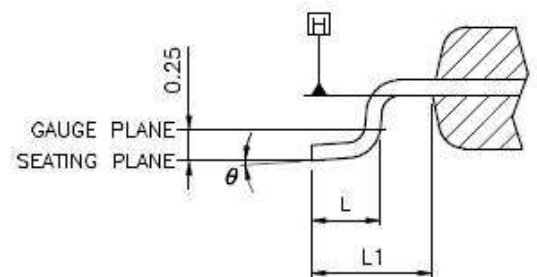
3rd Line: Wafer Fab Code (FXXX...XX)

12. Package Dimensions

48TQFP (7mm x 7mm)



(THERMALLY ENHANCED VARIATIONS ONLY)



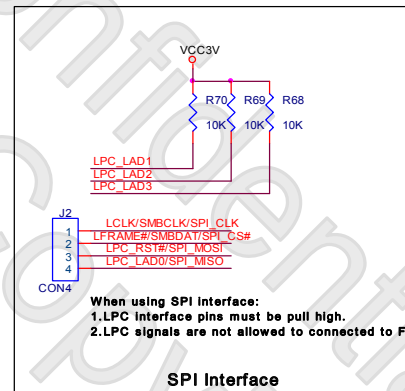
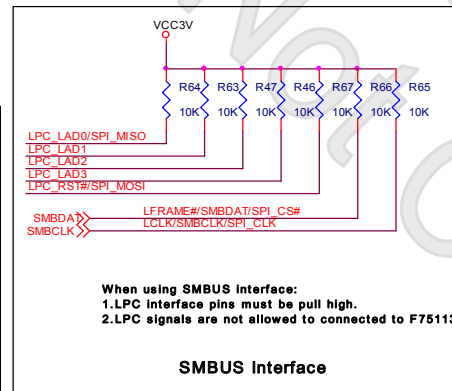
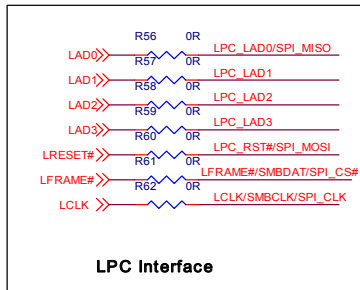
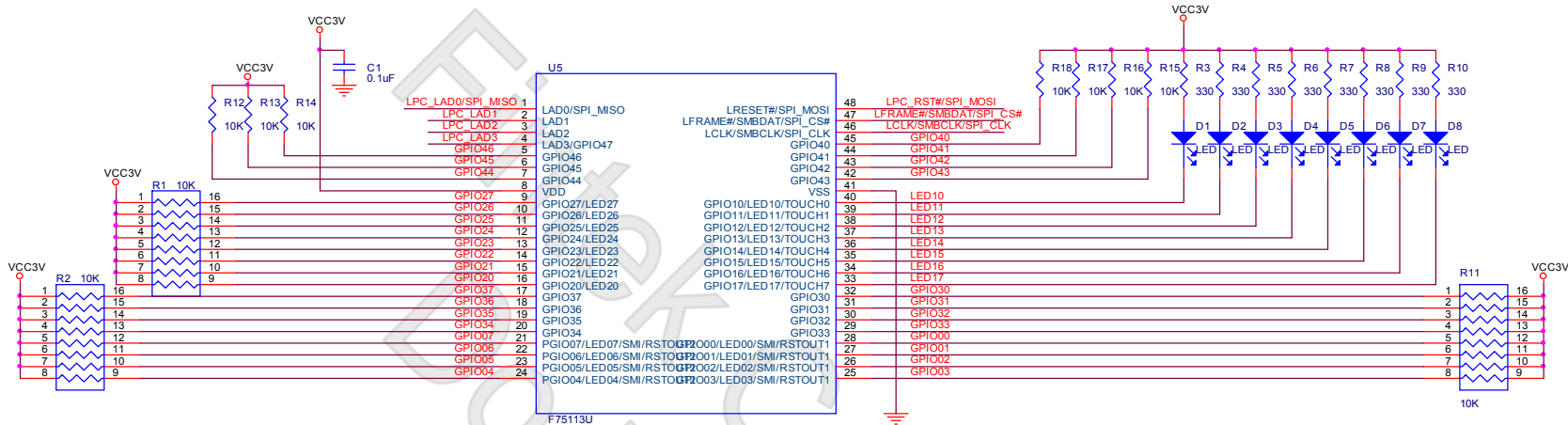
| SYMBOLS | MIN. | NOM. | MAX. |
|----------|----------|------|------|
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | - | 0.16 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| θ | 0° | 3.5° | 7° |

UNIT: mm

| PAD SIZE | E2 | | D2 | |
|--------------------------|------|------|------|------|
| | MIN. | MAX. | MIN. | MAX. |
| 160x160 MIL ² | 3.05 | 4.06 | 3.05 | 4.06 |

UNIT: mm

13. Application Circuits



| | | |
|-----------------------------------|------------------------|----------|
| Title: F75113 application circuit | | |
| Size: B | Document Number: <Doc> | Rev: 1.1 |
| Date: Friday, July 08, 2011 | Sheet: 1 | of 1 |