

**F72830**

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**Four-Phase Linear Controller with I2C  
Interface**

**Release Date: July, 2007  
Version: 0.14P**



## ***F72830 Datasheet Revision History***

| <b>Version</b> | <b>Date</b> | <b>Page</b> | <b>Revision History</b>                           |
|----------------|-------------|-------------|---------------------------------------------------|
| 0.10P          | Sep, 2006   |             | Preliminary version                               |
| 0.11P          | Sep, 2006   | 18          | Register-Chip ID                                  |
| 0.12P          | Dec, 2006   | 4           | Pin configuration                                 |
|                |             | 5           | Pin 9, GND → VSS                                  |
|                |             |             | EN pin description                                |
|                |             | 7           | Electrical characteristic, VCC → VDPA             |
|                |             | 8           | Input high voltage: 2V → 1.5V                     |
|                |             | 21          | Application circuit                               |
| 0.13P          | Feb, 2007   | 7           | V <sub>REF</sub> Range: 0.79~0.83V, typical: 0.8V |
| 0.14P          | Jul, 2007   | 20          | Update company address                            |

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# 1 General Description

The F72830 is a quadro MOSFET drivers specifically designed to drive quadro power N-Channel MOSFETs as a four-phase linear regulators. The device contains under voltage protection for every linear controller, an external ceramic capacitor to adjust slew rate of soft-start, and integrated I2C interface. The built-in I2C interface provides the function to fine tune the output of every linear controller from 0.74V to 1.04V, 0.02V per step, and the default output is set to 0.8V.

The F72830 also offers 3 independent enable pins to control the corresponding linear controller. Linear controller 1 is active as power on, and other remained linear controller 2~4 are controlled by enable pin, EN2~4. Except being a regular linear controller, the F72830 can be paired with the chip, which contains AMD K8 power on/off timing sequence to be used a platform power supplier, for example, F71863, or any specific purpose. The chip is a 16pin SOP package and powered by 5/12V.

# 2 Feature

- ◆ 4 Channels of Linear Controller Supported Controlled by 3 Enable Pins:
  - Linear Controller 1 Will Be Active as Power on
  - Linear Controller 2~4 Can Be Active in any Sequence or at the Same Time(in 3CLK Debounce)
- ◆ Under Voltage Protection of All Linear Controllers
- ◆ External Capacitor for Adjusting Soft-start Slew Rate
- ◆ Integrated I2C Interface to Fine Tune Output of Linear Controller from 0.74V to 1.04V, 0.02V per Step, Typical Output Is 0.8V
- ◆ Independent Enable Pin Controls Single Linear Controller On/Off Individually
- ◆ Powered by  $V_{VDDA}$ : 5~12V
- ◆ 16-SOP Green Package

### 3 Pin Configuration

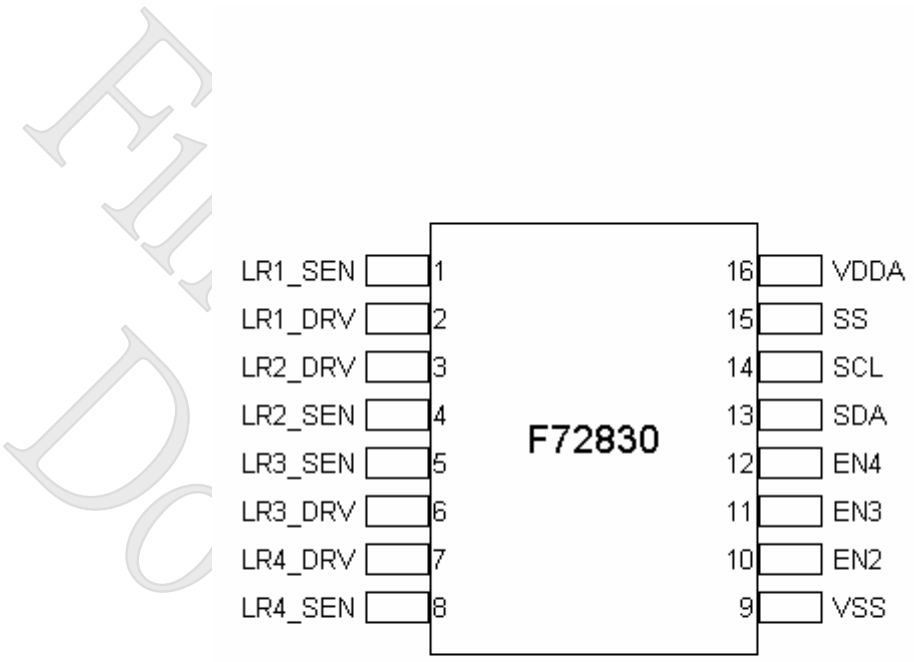


Figure1. F72830 pin configuration

### 4 Pin Description

- I/OD<sub>12st</sub> - TTL level bi-directional pin with schmitt trigger., Open-drain output with 12 mA sink capability.
- IN<sub>st</sub> - TTL level input pin with schmitt trigger.
- AIN- Input pin(Analog).
- AOUT - Output pin(Analog).
- P - Power.

**◆ Power Pins**

| PIN NO | PIN NAME | TYPE | DESCRIPTION |
|--------|----------|------|-------------|
| 9      | VSS      | P    | Power pins  |
| 16     | VDDA     |      |             |

**◆ Control signal**

| PIN NO | PIN NAME | TYPE             | PWR | DESCRIPTION                                                      |
|--------|----------|------------------|-----|------------------------------------------------------------------|
| 10     | EN2      | IN <sub>ts</sub> | VDD | Linear driver2 control signal input, input voltage > 1.5V, L → H |
| 11     | EN3      | IN <sub>ts</sub> | VDD | Linear driver3 control signal input, input voltage > 1.5V, L → H |
| 12     | EN4      | IN <sub>ts</sub> | VDD | Linear driver4 control signal input, input voltage > 1.5V, L → H |

**◆ Switching Signal & Linear/PWM Controller**

| PIN NO | PIN NAME | TYPE | PWR  | DESCRIPTION                                                                                                                                                                                                                                       |
|--------|----------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1      | LR1_SEN  | AIN  | VDD  | Sense the voltage of linear regulator. LR1_SEN and LR1_DRV act as a linear regulator. The linear controller 1 will act while powering on the chip and finishing soft-start.                                                                       |
| 2      | LR1_DRV  | AOUT | VDDA | Connect this pin to the gate of a suitable N-channel MOSFET. LR1_SEN and LR1_DRV act as a linear regulator. The linear controller 1 will act while powering on the chip and finishing soft-start.                                                 |
| 3      | LR2_DRV  | AOUT | VDDA | Connect this pin to the gate of a suitable N-channel MOSFET. LR2_SEN and LR2_DRV act as a linear regulator. The linear controller 2 will act when the input of EN2 acts high. The linear controller 2 will be off when the input of EN2 acts low. |
| 4      | LR2_SEN  | AIN  | VDD  | Sense the voltage of linear regulator. LR2_SEN and LR2_DRV act as a linear regulator. The linear controller 2 will act when the input of EN2 acts high. The linear controller 2 will be off when the input of EN2 acts low.                       |
| 5      | LR3_SEN  | AIN  | VDDA | Sense the voltage of linear regulator. LR3_SEN and LR3_DRV act as a linear regulator. The linear controller 3 will act when the input of EN3 acts high. The linear controller 3 will be off when the input of EN3 acts low.                       |

|   |         |      |      |                                                                                                                                                                                                                                                                 |
|---|---------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6 | LR3_DRV | AOUT | VDDA | <p>Connect this pin to the gate of a suitable N-channel MOSFET.</p> <p>LR3_SEN and LR3_DRV act as a linear regulator. The linear controller 3 will act when the input of EN3 acts high. The linear controller 3 will be off when the input of EN3 acts low.</p> |
| 7 | LR4_DRV | AOUT | VDDA | <p>Sense the voltage of linear regulator. LR4_SEN and LR4_DRV act as a linear regulator. The linear controller 4 will act when the input of EN4 acts high. The linear controller 4 will be off when the input of EN4 acts low.</p>                              |
| 8 | LR4_SEN | AIN  | VDD  | <p>Connect this pin to the gate of a suitable N-channel MOSFET.</p> <p>LR4_SEN and LR4_DRV act as a linear regulator. The linear controller 4 will act when the input of EN4 acts high. The linear controller 4 will be off when the input of EN4 acts low.</p> |

◆ Others

| PIN NO | PIN NAME | TYPE                 | PWR | DESCRIPTION                                                                                                                                            |
|--------|----------|----------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14     | SCLK     | IN <sub>ts</sub>     | VDD | I2C serial bus clock                                                                                                                                   |
| 13     | SDATA    | I/OD <sub>12ts</sub> | VDD | I2C serial bus data                                                                                                                                    |
| 15     | SS       | AIN                  | VDD | Soft-Start. Connect this pin to a small ceramic capacitor to determine the soft-start rate. The value of capacitor is bigger, the slew rate is slower. |

\* The VDD is the internal voltage which is a step-down voltage generated from input voltage, VDDA.

## 5 Electrical Characteristic

### 5.1 Absolute Maximum Ratings

| PARAMETER          | SYMBOL | RATINGS | UNIT |
|--------------------|--------|---------|------|
| IC supply voltage  | VDDA   | 17      | V    |
| ESD classification | HBM    | 2       | kV   |

|                                                  |           |           |    |
|--------------------------------------------------|-----------|-----------|----|
| ※ Maximum junction temperature (plastic package) | $T_j$     | 150       | °C |
| ※ Maximum storage temperature                    | $T_{STO}$ | -65 ~ 150 | °C |
| ※ Maximum lead temperature (soldering 10s)       |           | 260       | °C |

Note: If ICs are stressed beyond the limits listed in the “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

**Package thermal information**

| PARAMETER                           | SYMBOL       | SOIC | UNIT |
|-------------------------------------|--------------|------|------|
| Thermal resistance junction-ambient | $R_{th\_ja}$ | 57   | °C/W |

**Recommended Operating Conditions**

|                                 |              |
|---------------------------------|--------------|
| Supply Voltage, $V_{DDA}$ ----- | 5V~12V . 10% |
| Ambient Temperature Range-----  | 0 C to 70 C  |
| Junction Temperature Range----- | 0 C to 125 C |

**5.2 DC and AC electrical characteristics ( $V_{DDA} = 5V$ ,  $T_A = 25^\circ C$ )**

| PARAMETER                                    | SYMBOL     | TEST CONDITIONS          | MIN. | TYP. | MAX. | UNIT |
|----------------------------------------------|------------|--------------------------|------|------|------|------|
| <b>VDDA SUPPLY CURRENT/Regulated Voltage</b> |            |                          |      |      |      |      |
| Nominal supply current                       | $I_{VDDA}$ |                          |      | 5    | 10   | mA   |
| <b>POWER-ON RESET</b>                        |            |                          |      |      |      |      |
| Rising $V_{DDA}$ threshold                   |            |                          | 3.0  | 3.3  | 3.6  | V    |
| Falling $V_{DDA}$ threshold                  |            |                          | 2.7  | 3.0  | 3.3  | V    |
| <b>OSCILLATOR AND Protection</b>             |            |                          |      |      |      |      |
| Free running frequency                       | $F_{OSC}$  |                          | 200  | 250  | 300  | kHz  |
| Soft-start interval                          | $T_{SS}$   |                          |      | 12   |      | uA   |
| <b>REFERENCE VOLTAGE</b>                     |            |                          |      |      |      |      |
| Reference voltage                            | $V_{REF}$  | $V_{DDA}=12V$ , $T = 25$ | 0.79 | 0.8  | 0.83 | V    |
| <b>LINEAR REGULATOR</b>                      |            |                          |      |      |      |      |

| PARAMETER              | SYMBOL   | TEST CONDITIONS       | MIN. | TYP. | MAX. | UNIT |
|------------------------|----------|-----------------------|------|------|------|------|
| DC gain                | A0       |                       | -    | 70   | -    | dB   |
| Gain-bandwidth product | GBWP     | $C_L = 1000\text{pF}$ | -    | 1.86 | -    | MHz  |
| Under voltage level    | $V_{UV}$ | Percent of nominal    | 0.3  | 0.4  | 0.5  | V    |

※: Design Guarantee

**I/O PAD DC Characteristics**

(Ta = 0° C to 70° C, VDDA = 5~12V ± 10%, VSS = 0V)

| PARAMETER                                                                                                                   | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS   |
|-----------------------------------------------------------------------------------------------------------------------------|------|------|------|------|------|--------------|
| <b>I/OD<sub>12st</sub>-TTL level bi-directional pin with schmitt trigger, Open-drain output with 12 mA sink capability.</b> |      |      |      |      |      |              |
| Input Low Voltage                                                                                                           | VIL  |      |      | 0.8  | V    | VDDA = 5~12V |
| Input High Voltage                                                                                                          | VIH  | 1.5  |      |      | V    | VDDA = 5~12V |
| Output Low Current                                                                                                          | IOL  |      | +12  |      | mA   | VOL = 0.4V   |
| Input High Leakage                                                                                                          | ILIH |      |      | +1   | μA   | VIN = 3.3V   |
| Input Low Leakage                                                                                                           | ILIL | -1   |      |      | μA   | VIN = 0V     |
| <b>I/O<sub>12st</sub>- TTL level bi-directional pin with schmitt trigger and with 12mA source-sink capability.</b>          |      |      |      |      |      |              |
| Input Low Voltage                                                                                                           | VIL  |      |      | 0.8  | V    | VDDA = 5~12V |
| Input High Voltage                                                                                                          | VIH  | 1.5  |      |      | V    | VDDA = 5~12V |
| Output Low Current                                                                                                          | IOL  |      | -12  |      | mA   | VOL = 0.4 V  |
| Input High Leakage                                                                                                          | ILIH |      |      | +1   | μA   | VIN = 3.3V   |
| Input Low Leakage                                                                                                           | ILIL | -1   |      |      | μA   | VIN = 0V     |
| <b>IN<sub>st</sub> - TTL level input pin with schmitt trigger</b>                                                           |      |      |      |      |      |              |
| Input Low Voltage                                                                                                           | VIL  |      |      | 0.8  | V    |              |
| Input High Voltage                                                                                                          | VIH  | 1.5  |      |      | V    |              |
| Input High Leakage                                                                                                          | ILIH |      |      | +1   | μA   | VIN = 3.3V   |
| Input Low Leakage                                                                                                           | ILIL | -1   |      |      | μA   | VIN = 0 V    |
| <b>OD<sub>12</sub>-Open-drain output with 12 mA sink capability.</b>                                                        |      |      |      |      |      |              |
| Output Low Current                                                                                                          | IOL  |      | -12  |      | mA   | VOL = 0.4V   |

**5.3 Specification of Reliability**

| Test Item       | Description                               | Y/N | Test Item    | Description             | Y/N |
|-----------------|-------------------------------------------|-----|--------------|-------------------------|-----|
| <b>ESD</b>      | VHBM > 2KV, VMM > 200V                    |     | <b>TH(B)</b> | 1000Hrs, 85% RH, 85°C   |     |
| <b>Latch-UP</b> | $I_{tr} \Rightarrow 50 \sim 100\text{mA}$ |     | <b>PCT</b>   | 168 Hrs, 100% RH, 121°C |     |



## 6 Block Diagram

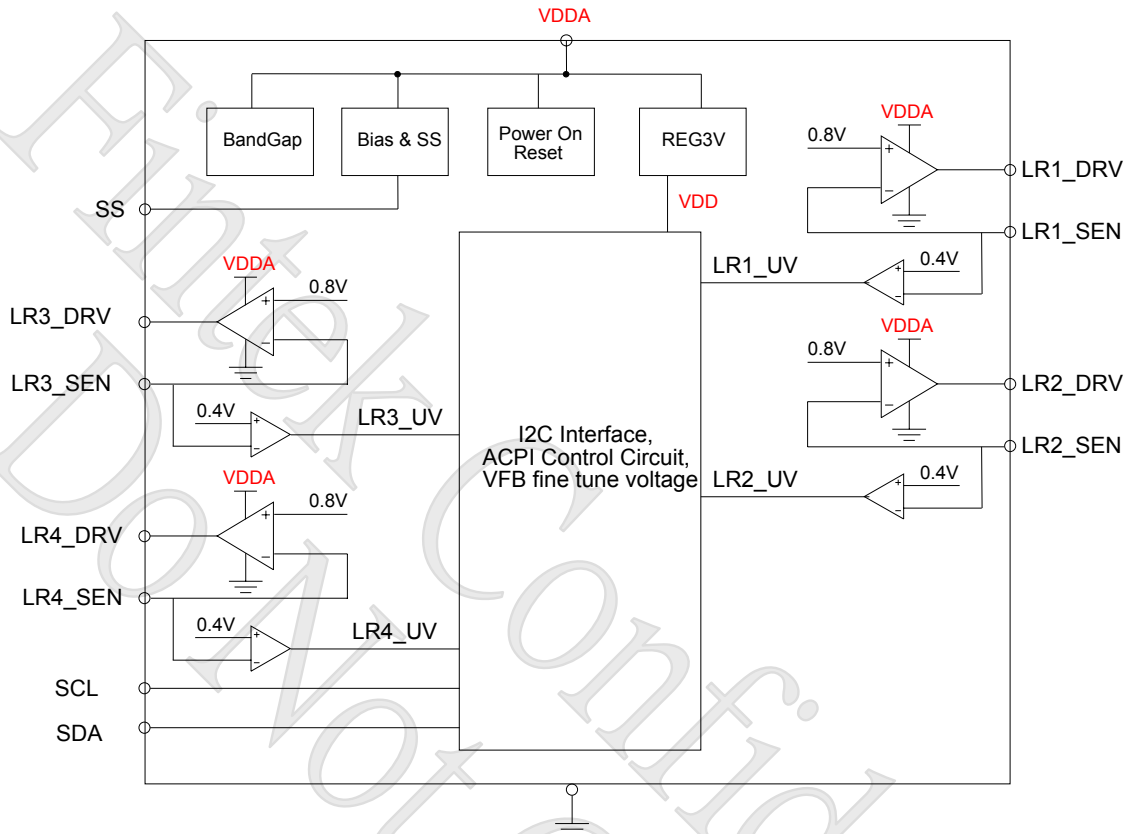


Figure2. F72830 block diagram

## 7 Simplified External Application Diagram

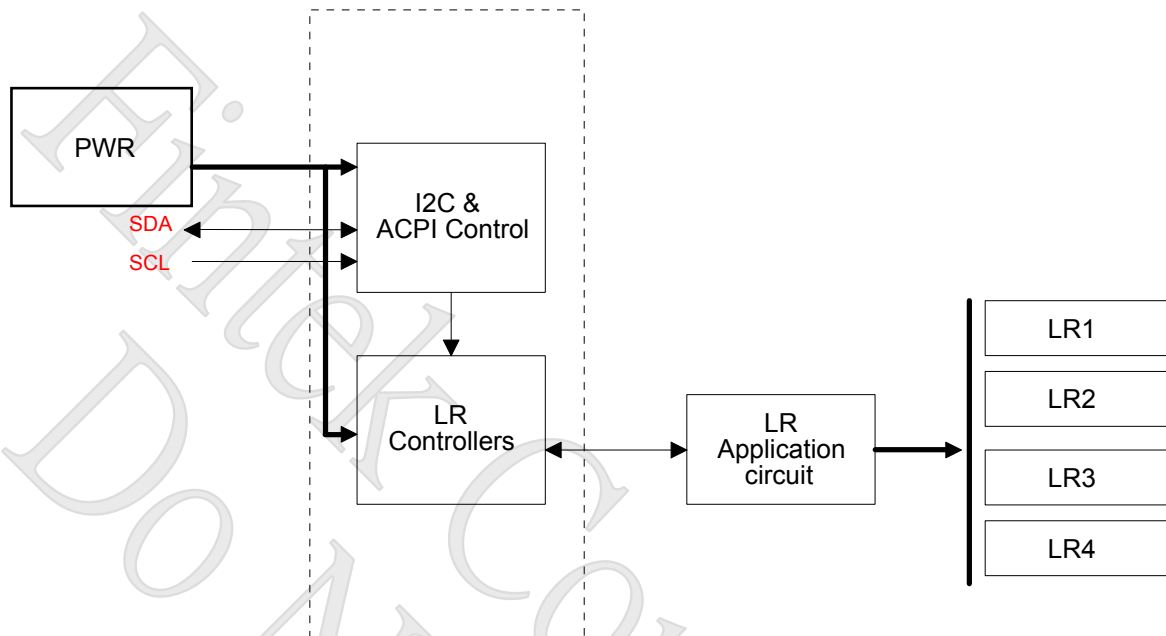


Figure3. F72830 external application diagram

## 8 Functional Description

### 8.1 Linear Controller Description

The F72830 contains 4 sets of linear controllers. When the chip is powered on, soft-start will be active. Then, the first linear controller will generate the output voltage. The other 3 sets of linear controllers, LR\_2, LR\_3, and LR\_4 are controlled by the corresponding enable pin, EN2, EN3, and EN4. There is no priorities in linear controllers 2~4. The output voltage sequence of linear controllers 2~4 issued depends on enable signal of EN2~4 sequence only. If any enable pin acts high before or at the same time as VDDA PWROK, the corresponding linear controller will generate output as linear controller 1 simultaneously. When the enable pin receives enable signal, soft-start and enable status checking will be active. To receive first coming high signal from any enable pin then soft-start will start. Before the duration of soft-start reaching 0.1V, any successive acting high enable signal is considered in the same soft-start sequence. All of the linear regulators corresponding to high acting enable pins will generate output following soft-start procedure. If the successive enable signal is received out of the bound of the duration, the enable sequence will be arranged after this period of soft-start finishes. The detail can be referred in Figure4.

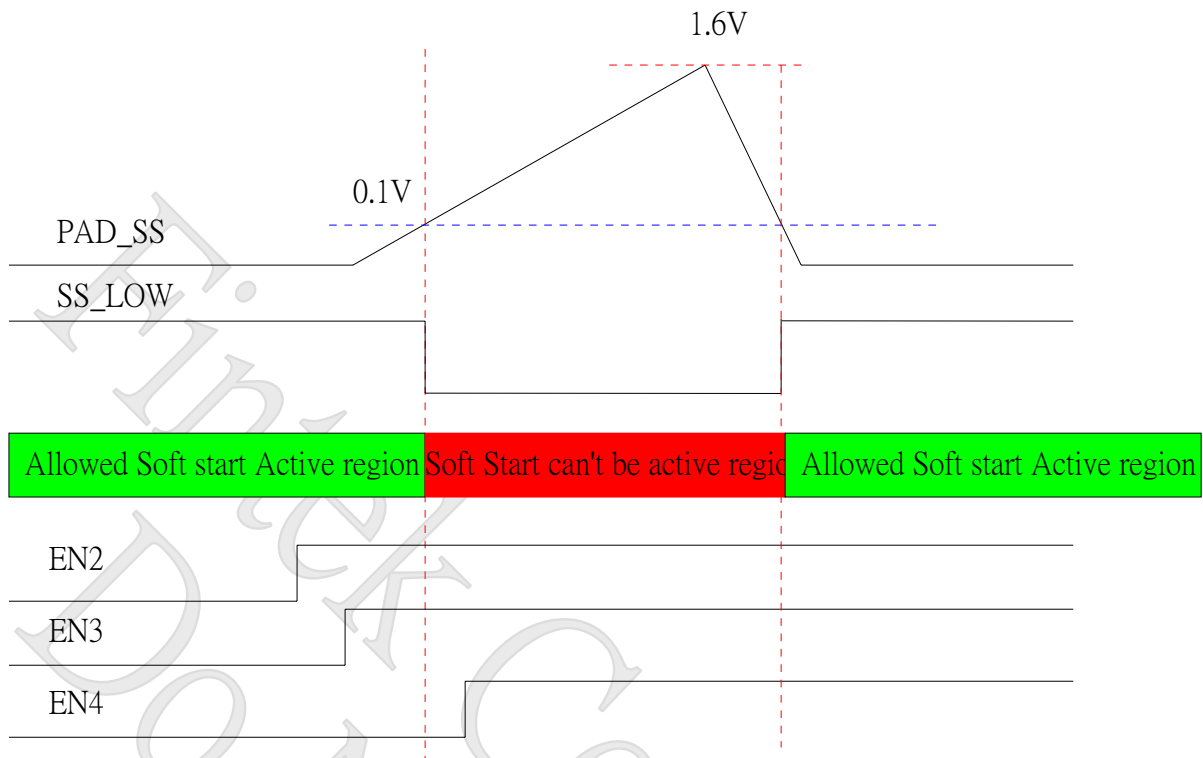
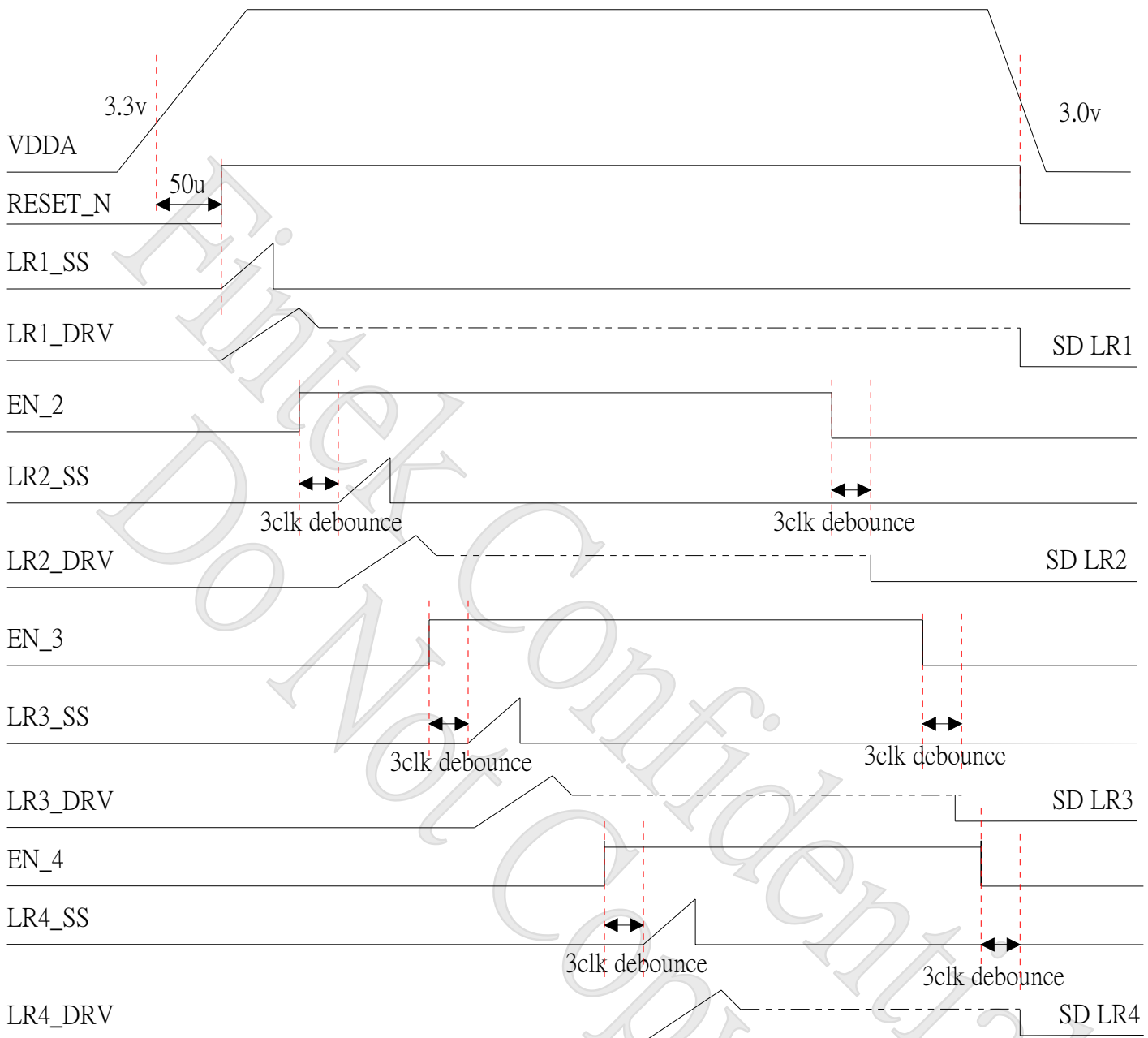


Figure4. F72830 enable and Soft Start Timing Chart

## 8.2 Soft-start

Pin15 of the F72830 acts as soft-start function. As shown in schematic, a ceramic capacitor is attached between this pin and ground. When power is first applied to the chip, a constant current is applied from the pin into an external capacitor, linearly ramping up the voltage. This ramp in turn controls the internal reference of F72830 providing a soft-start for linear regulator. As for switches, they must be either on or off in the system therefore soft-start has no effect on them. It is important to know soft-start is not an enable signal; pulling it low will not be sure to turn off all outputs. But if there are appropriate signals asserted, the switches will be turn on at once. The actual state of F72830 on power up will be determined by the controlled input signal. And the soft-start is effective only during power on. The detail timing chart could be shown as Figure 5.


**F72830**


Note that: LR1, LR2, LR3, and LR4 can be active at the same time or not. (if you want to let the LR2, LR3, and LR4 soft start at the same time, EN\_2, EN\_3, and EN\_4 should be high before SS under 0.1V. It is recommended to set high at the same time, if you want to let the linear regulators soft start at the same time. If you set high after SS is higher than 0.1v, it will wait the soft start finished, and begin the next soft start). If LR2~LR4 are desired to act as LR1 while power on, EN2~ EN4 must be pulled high before VDDA reaches PWROK.

Figure5. Soft-start timing and indication

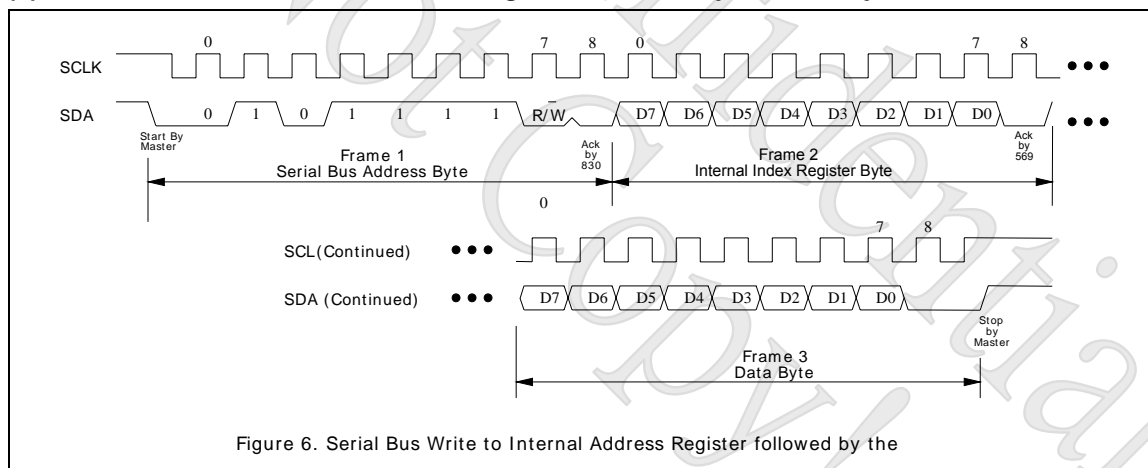
### 8.3 Under voltage protection

If the LR\_SEN voltage drops below 0.4V, a fault signal is generated. When under voltage condition occurs, the related Linear Regulator will shut down.

### 8.4 Access interface

The F72830 can be connected to a compatible 2-wire serial system Management Bus (SMBus) as a slave device under the control of the master device, using two device terminals SCL and SDA. The controller can provide a clock signal to the device SCL pin and read/write data from/to the device through the device SDA pin. The address default is 0x5E(0101\_1110) and the operation of device to the bus is described with details in the following sections.

#### (a) SMBus write to internal address register followed by the data byte



#### (b) Serial bus write to internal address register only

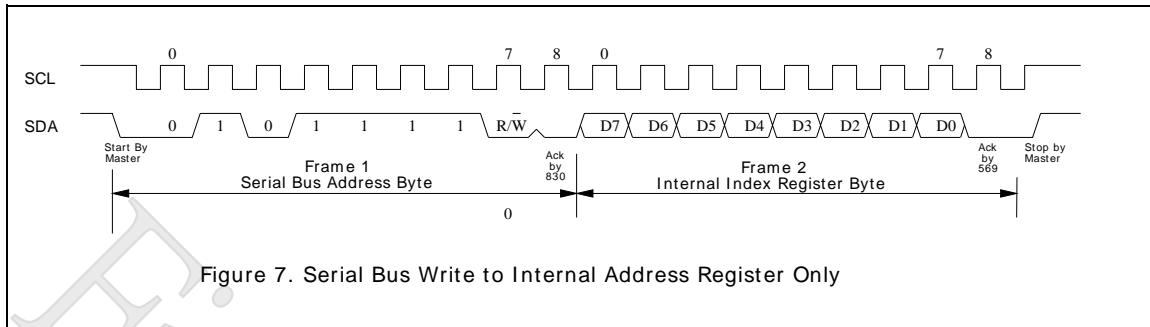

**F72830**


Figure 7. Serial Bus Write to Internal Address Register Only

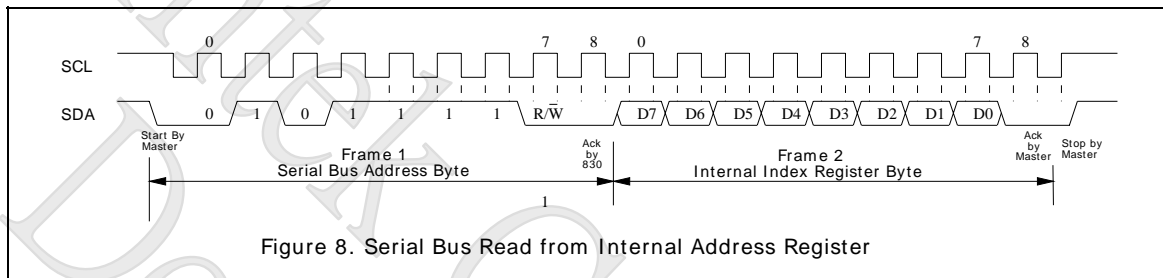
**(c) Serial bus read from a register with the internal address register prefer to desired location**


Figure 8. Serial Bus Read from Internal Address Register



## 9 Register Description

### 9.1 LR\_1, LR\_2 Fine Tune Voltage Register — Index 1

| Bit | Name | R/W | Default | Description                                                                                                                                                                                                                                                                                                                                                            |
|-----|------|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | LR_1 | R/W | 3       | Fine tune LR_1 reference voltage, LR1 Voltage table is set by Register<br>01h bit 7:4.<br>0000 : 0.74V      1000 : 0.90V<br>0001 : 0.76V      1001 : 0.92V<br>0010 : 0.78V      1010 : 0.94V<br>0011 : 0.80V      1011 : 0.96V<br>0100 : 0.82V      1100 : 0.98V<br>0101 : 0.84V      1101 : 1.00V<br>0110 : 0.86V      1110 : 1.02V<br>0111 : 0.88V      1111 : 1.04V |
| 3:0 | LR_2 | R/W | 3       | Fine tune LR_2 reference voltage, LR2 Voltage table is set by Register<br>01h bit 3:0.<br>0000 : 0.74V      1000 : 0.90V<br>0001 : 0.76V      1001 : 0.92V<br>0010 : 0.78V      1010 : 0.94V<br>0011 : 0.80V      1011 : 0.96V<br>0100 : 0.82V      1100 : 0.98V<br>0101 : 0.84V      1101 : 1.00V<br>0110 : 0.86V      1110 : 1.02V<br>0111 : 0.88V      1111 : 1.04V |


**9.2 LR\_3, LR\_4 Fine Tune Voltage Register — Index 2**

| Bit | Name | R/W | Default | Description                                                                                                                                                                                                                                                                                                                                                            |
|-----|------|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | LR_3 | R/W | 3       | Fine tune LR_3 reference voltage, LR3 Voltage table is set by Register<br>02h bit 7:4.<br>0000 : 0.74V      1000 : 0.90V<br>0001 : 0.76V      1001 : 0.92V<br>0010 : 0.78V      1010 : 0.94V<br>0011 : 0.80V      1011 : 0.96V<br>0100 : 0.82V      1100 : 0.98V<br>0101 : 0.84V      1101 : 1.00V<br>0110 : 0.86V      1110 : 1.02V<br>0111 : 0.88V      1111 : 1.04V |
| 3:0 | LR_4 | R/W | 3       | Fine tune LR_4 reference voltage, LR4 Voltage table is set by Register<br>02h bit 3:0.<br>0000 : 0.74V      1000 : 0.90V<br>0001 : 0.76V      1001 : 0.92V<br>0010 : 0.78V      1010 : 0.94V<br>0011 : 0.80V      1011 : 0.96V<br>0100 : 0.82V      1100 : 0.98V<br>0101 : 0.84V      1101 : 1.00V<br>0110 : 0.86V      1110 : 1.02V<br>0111 : 0.88V      1111 : 1.04V |


**9.3 Under Voltage, Over Current Enable Protection Register — Index 03h**

| Bit | Name     | R/W | Default | Description                                                  |
|-----|----------|-----|---------|--------------------------------------------------------------|
| 7   | Reserved | R/W | 1       | Reserved Register                                            |
| 6   | Reserved | R/W | 0       | Reserved Register                                            |
| 5   | Reserved | R/W | 0       | Reserved Register                                            |
| 4   | SAME_UV  | R/W | 0       | If set to 1, one of 4 LR occurs UV, it will shut down all LR |
| 3   | LR1_UVEN | R/W | 1       | LR1 Under voltage enable                                     |
| 2   | LR2_UVEN | R/W | 1       | LR2 Under voltage enable                                     |
| 1   | LR3_UVEN | R/W | 1       | LR3 Under voltage enable                                     |
| 0   | LR4_UVEN | R/W | 1       | LR4 Under voltage enable                                     |

**9.4 Reserved Function, Read back SSOK Status, If LR finished Soft Start, it Will Read back 1 Register — Index**
**04h**

| Bit | Name          | R/W | Default | Description                                                                                                    |
|-----|---------------|-----|---------|----------------------------------------------------------------------------------------------------------------|
| 7   | SOFT_SD_LR1   | R/W | 0       | If set to 1, LR1 will SD, and if set to 0, and the Power is higher than internal PWROK, it will re-soft start. |
| 6   | SOFT_SD_LR2   | R/W | 0       | If set to 1, LR2 will SD, and if set to 0, it will detect EN2 high to do soft start                            |
| 5   | SOFT_SD_LR3   | R/W | 0       | If set to 1, LR3 will SD, and if set to 0, it will detect EN3 high to do soft start                            |
| 4   | SOFT_SD_LR4   | R/W | 0       | If set to 1, LR4 will SD, and if set to 0, it will detect EN4 high to do soft start                            |
| 3   | LATCH_S1_SSOK | R   | 0       | If LR1 finished soft start, it will read back 1                                                                |
| 2   | LATCH_S2_SSOK | R   | 0       | If LR2 finished soft start, it will read back 1                                                                |
| 1   | LATCH_S3_SSOK | R   | 0       | If LR3 finished soft start, it will read back 1                                                                |
| 0   | LATCH_S4_SSOK | R   | 0       | If LR4 finished soft start, it will read back 1                                                                |


**9.5 CHIP ID 1 — Index 5Ah**

| Bit | Name      | R/W | Default | Description       |
|-----|-----------|-----|---------|-------------------|
| 7   | CHIP ID 1 | R   | 0       | CHIP_ID1 = 8'h06; |
| 6   |           |     | 0       |                   |
| 5   |           |     | 0       |                   |
| 4   |           |     | 0       |                   |
| 3   |           |     | 0       |                   |
| 2   |           |     | 1       |                   |
| 1   |           |     | 1       |                   |
| 0   |           |     | 0       |                   |

**9.6 CHIP ID 2 — Index 5Bh**

| Bit | Name      | R/W | Default | Description       |
|-----|-----------|-----|---------|-------------------|
| 7   | CHIP ID 2 | R   | 0       | CHIP_ID1 = 8'h03; |
| 6   |           |     | 0       |                   |
| 5   |           |     | 0       |                   |
| 4   |           |     | 0       |                   |
| 3   |           |     | 0       |                   |
| 2   |           |     | 0       |                   |
| 1   |           |     | 1       |                   |
| 0   |           |     | 1       |                   |

**F72830**

## 10 Ordering Information

| Part Number | Package Type           | Production Flow          |
|-------------|------------------------|--------------------------|
| F72830SG    | 16-SOP (Green Package) | Commercial, 0°C to +70°C |

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# 11 Package Dimensions (16-SOP)

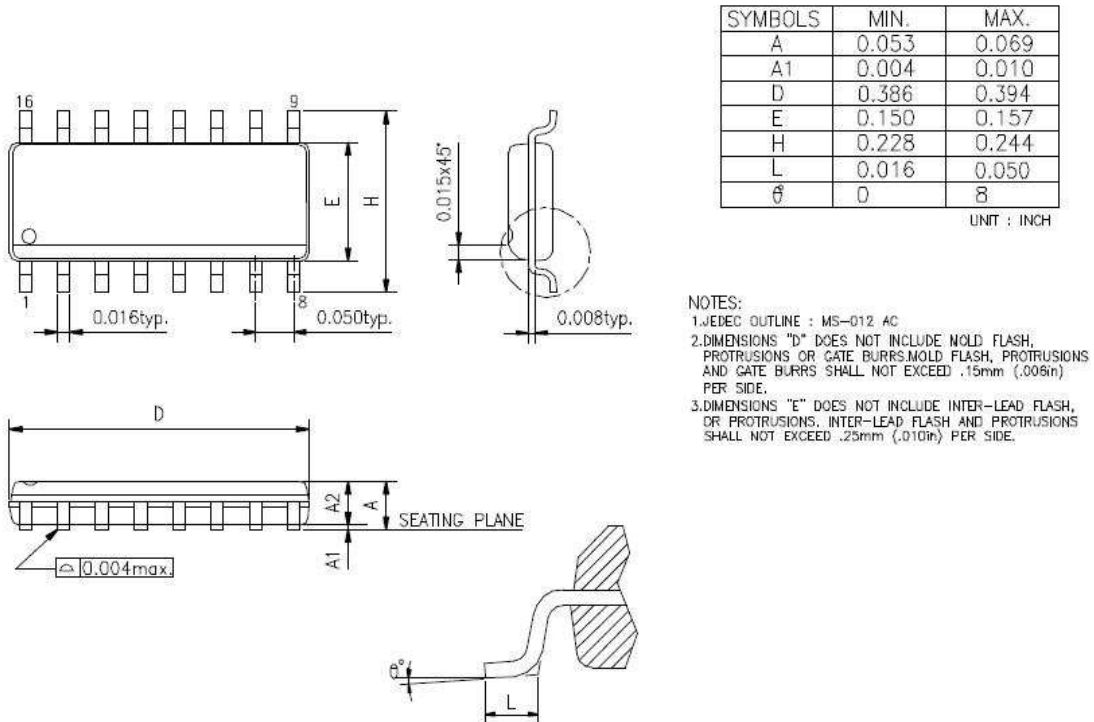


Figure9. 16 Pin SOP Package Diagram

# 12 Application Circuit

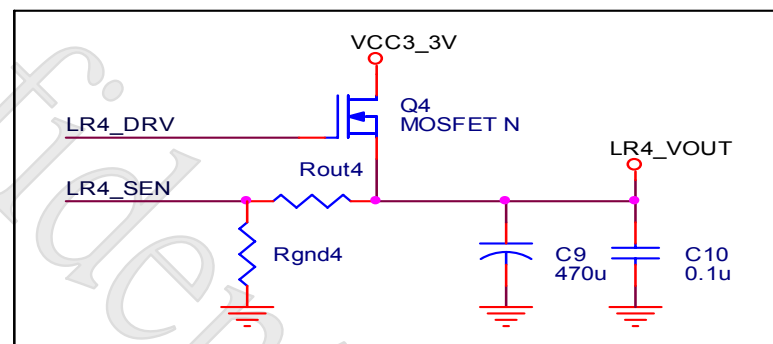
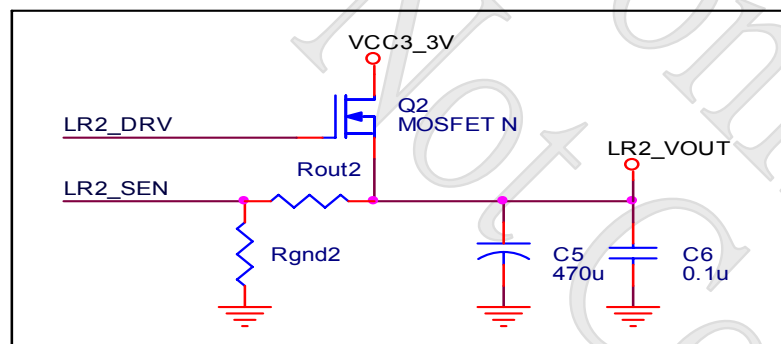
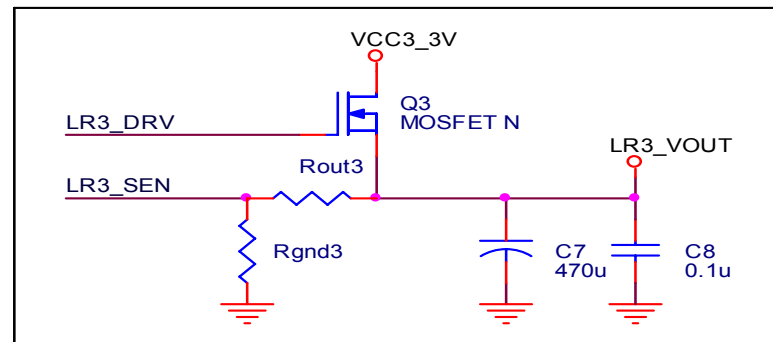
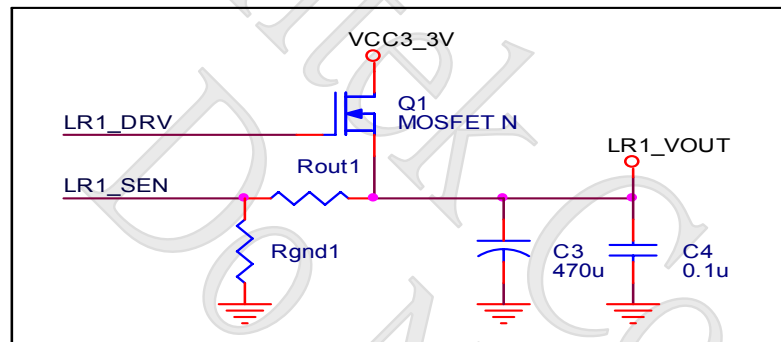
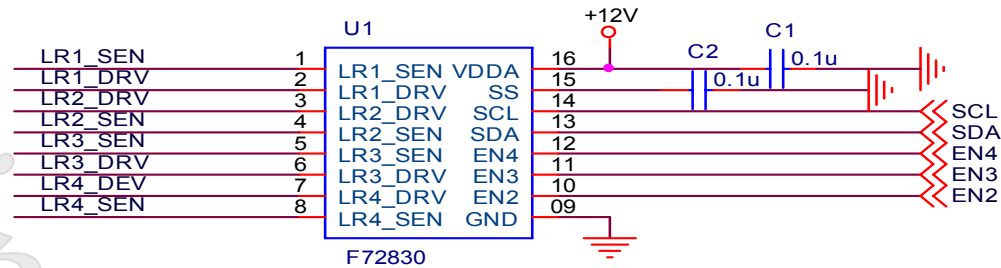


Figure10. F72830SG Application Circuit

# F72830

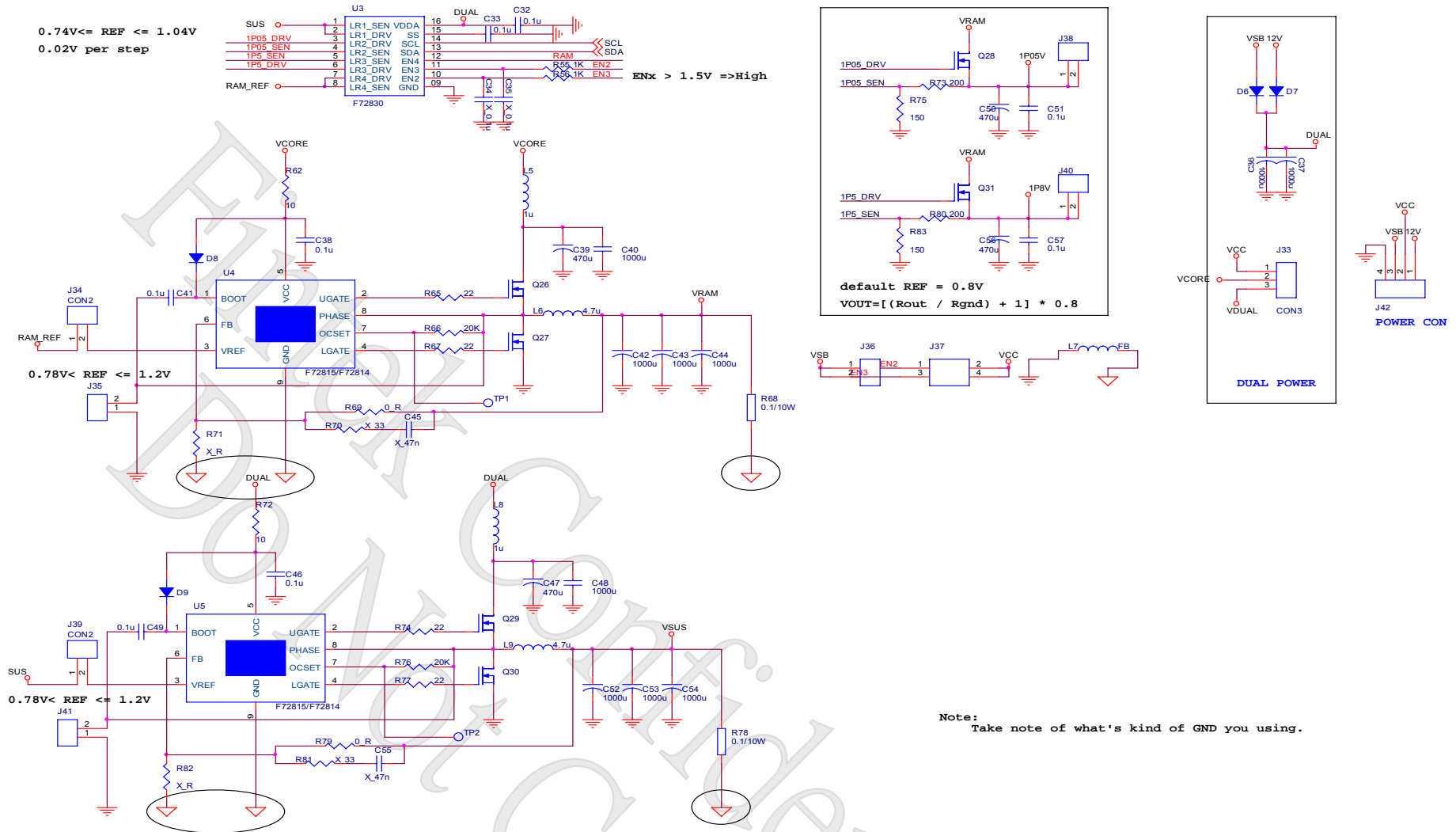


Figure11. F72830 and F72815 Practice Application Circuit