F72569

ACPI Controller IC for AMD K8/AM2 Platform

Release Date: Oct, 2006
Version: 0.26P

F72569 Datasheet Revision History

Version	Date	Page	Revision History
0.20P	Dec, 2005		Preliminary version
0.21P	Apr, 2006		Model name modification
0.22P	May, 2006		Re-compose
		1	Delete the description about Vref for overclock
		14	Description of linear controller correction
		23	Application circuit correction
0.23P	June, 2006	1	Delete the description about Vref in general description
0.24P	Aug, 2006	11	Add over current protection description
0.25P	Sep,2006	3	Pin description
		20	Application circuit correction
0.26P	Oct, 2006	20	Application circuit correction

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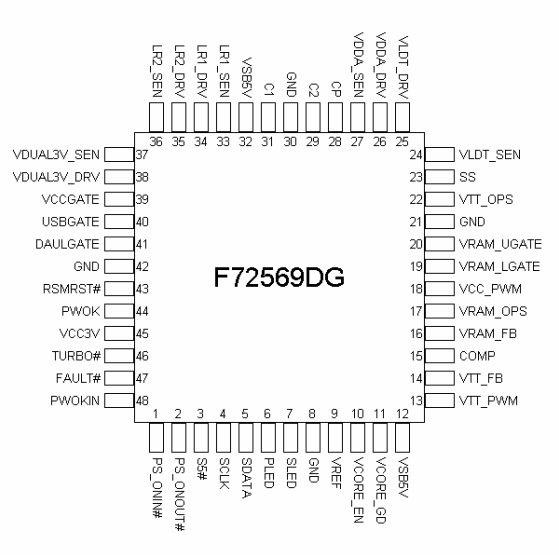
1 General Description

The F72569 is a fully compliant ACPI controller IC specific for AMD K8 CPU platform. The chip is used with an ATX power supply, and it integrates synchronous PWM controllers, regulators, several linear controllers, switching signals, monitoring and control function into a 48 pin LQFP package. Its operation mode (sleep or active) is selectable through some control signals. The F72569 provides 3 switch signals which can provide $5V_{DUAL}$, $5V_{USB}$ & $3.3V_{DUAL}$ etc. The F72569 can also provide 5 linear regulators for system requirements. This chip integrates a charge pump engine to provide higher driving voltage for appropriate gate during standby. Besides, this chip offers current limiting that protects each PWM outputs, and provides soft-start for a linear regulator to avoid rush current. The power LED is programmable and compliant with PC2001. Moreover, this high-performance chip integrates I^2C interface and provides adjustable linear controllers mechanism for dynamic over/under-voltage use. This chip is in a 48pin LQFP package and powered by 5VSB.

2 Feature

- Compliant with AMD K8 timing sequence
- Provide 3 switching controlled signals for $5V_{DUAL}$, $5V_{USB}$ and $3.3V_{DUAL}$
- Programmable $5V_{DUAL}/5V_{STR}/5V_{CC}$ for USB device wake up
- Provide 5 linear controller and typically use for –
  - -- 1 channel for DUAL3V power
  - -- 1 channel for VDDA power
  - -- 1 channel for VLDT power
  - -- 2 channels for 0.8~5V voltage requirement
- Provide one PWM controller for DDR V_{DDQ}
- Provide one PWM regulator for chipset power requirement
- 1 PWROK input signal(typically from ATXPWOKIN) and 1 PWROK output signal
- Provide resume reset signal(RSMRST#)
- Programmable power LED control
- Provide V_{REF} and VSB9V voltage for generating different voltage use
- Power up soft-start and under-voltage monitoring for the linear regulators
- Over current protection(OCP) on PWM controller and under-voltage monitoring of all linear regulators
- Integrate I^2C interface
- 48 pin LQFP package and 5VSB operation

3 Pin Configuration



4 Pin Description

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12ts} - TTL level and schmitt trigger

I/OD_{16} - TTL level bi-directional pin. Open-drain output with 16 mA sink capability

OUT_{12} - Output pin with 12 mA source-sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{16} - Open-drain output pin with 16 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

O_{24V4} - Output pin with 24mA driving capability, output 4V

IN_t - TTL level input pin

IN_{ts} - TTL level input pin and schmitt trigger

AIN - Input pin(Analog)

AOUT - Output pin(Analog)

P - Power

◆ ***Power Pins***

PIN NO	PIN NAME	TYPE	DESCRIPTION
8	GND	P	Power pins
12	VSB5V		
21	GND		
30	GND		
32	VSB5V		
42	GND		
45	VCC3V		
18	VCC_PWM		VRAM_UGATE and VRAM_LGATE signal power, recommend to connect to Vcc12V

◆ ***Reset & Power Good & Control signal***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
1	PS_ONIN#	IN_{ts}	VSB5V	Normal power control signal input.
2	PS_ONOUT#	OD_{12}	VSB5V	Power control signal output. Connected to ATX power ON/OFF pin, normally.
3	S5#	IN_{ts}	VSB5V	A low active ACPI control signal governs the S5 state. Typically, connected to chipset S5# signal.
10	VCORE_EN	OD_{12}	VSB5V	This pin is the open drain output to control CPU Vcore power enabled signal.
11	VCORE_GD	IN_{ts}	VSB5V	This pin is the CPU Vcore power ready signal input.
43	RSMRST#	OD_{12}	VSB5V	As VSB arrives at 3.3V, this pin will generate RSMRST# signal output after 66ms.
44	PWOK	OD_{16}	VSB5V	Power Good output signal.
46	TURBO#	IN_{ts}	VSB5V	Enable adjustable power signal.
47	FAULT#	IN_{ts}	VSB5V	Error input signal for power off.
48	PWOKIN	IN_{ts}	VSB5V	Power Good Schmitt Trigger input signal. Typically, connected to ATX power Good.

◆ ***Switching Signal & Linear/PWM Controller***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
13	VTT_PWM	OUT_5	VSB5V	External buffer PWM control output signal
14	VTT_FB	AIN	VSB5V	External buffer PWM feedback signal
15	COMP	AOUT	VSB5V	Output of the error amplifier used to compensate the feedback loop of the PWM controller.

16	VRAM_FB	AIN	VSB5V	VRAM PWM feedback signal
17	VRAM_OPS	AOUT/AIN	VSB5V	VRAM PWM current protection signal
19	VRAM_LGATE	O	VCC_PWM	VRAM PWM low gate control signal
20	VRAM_UGATE	O	VCC_PWM	VRAM PWM up gate control signal
22	VTT_OPS	AOUT/AIN	VSB9V	External buffer PWM current protection signal
24	VLDT_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. VLDT_SEN and VLDT_DRV act as a linear regulator and generate voltage for S0 state power.
25	VLDT_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. VLDT_SEN and VLDT_DRV act as a linear regulator and generate voltage for S0 state power.
26	VDDA_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. VDDA_SEN and VDDA_DRV act as a linear regulator and generate voltage and generate voltage for S0 sate power.
27	VDDA_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. VDDA_SEN and VDDA_DRV act as a linear regulator and generate voltage and generate voltage for S0 sate power.
33	LR1_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. LR1_SEN and LR1_DRV act as a linear regulator and generate voltage for standby or STR power. The default is for standby power. If VIN is main power, it can generate voltage for S0 sate power.
34	LR1_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. LR1_SEN and LR1_DRV act as a linear regulator and generate voltage for standby or STR power. The default is for standby power. If VIN is main power, it can generate voltage for S0 sate power.
35	LR2_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. LR2_SEN and LR2_DRV act as a linear regulator and generate voltage for standby or STR power. The default is for standby power. If VIN is main power, it can generate voltage for S0 sate power.
36	LR2_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. LR2_SEN and LR2_DRV act as a linear regulator and generate voltage for standby or STR power. The default is for standby power. If VIN is main power, it can generate voltage for S0 sate power.
37	DAUL3V_SEN	AIN	VSB5V	Sense the voltage of the linear regulator. VDUAL3V_SEN and VDUAL3V_DRV act as an adjustable linear regulator and this regulator is typically incorporated with VCCGATE to generate dual voltage.
38	DUAL3V_DRV	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. VDUAL3V_SEN and VDUAL3V_DRV act as an adjustable linear regulator and this regulator is typically incorporated with VCCGATE to

				generate dual voltage.
39	VCCGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. Generate dual 3.3V voltage with VDUAL3V_DRV and VDUAL3V_SEN. Generate USB voltage with USBGATE. Generate dual 5V voltage with DUALGATE.
40	USBGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. Generate USB voltage with VCCGATE.
41	DUALGATE	AOUT	VSB9V	Connect this pin to the gate of a suitable N-channel MOSFET. Generate dual 5V voltage with VCCGATE.

◆ ***Charge Pump***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
28	CP	P	VSB9V	Charge pump output (9V nominal). Decouple this pin with 1uF ceramic capacitor. VSB9V power output.
29	C2	AOUT	VSB9V	Positive end of charge pump capacitor
31	C1	AOUT	VSB5V	Negative end of charge pump capacitor. Connect a 1uF ceramic capacitor between C1 and C2

◆ ***Power LED***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
6	PLED	OD_{24}	VSB5V	Power LED. Can be programmed by setting register
7	SLED	OD_{24}	VSB5V	Suspend LED. Can be programmed by setting register

◆ ***Others***

PIN NO	PIN NAME	TYPE	PWR	DESCRIPTION
4	SCLK	IN_{ts}	VSB5V	I2C serial bus clock
5	SDATA	I/OD_{12ts}	VSB5V	I2C serial bus data
9	VREF	AOUT	VSB5V	Provide 1.25V reference voltage
23	SS	AIN	VSB5V	Soft-Start. Connect this pin to a small ceramic capacitor to determine the soft-start rate. The value of capacitor is bigger, and the slew rate is slower.