F75334DG

Performance Controller

Release Date: July, 2007
Version: V0.25P

F75334DG Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2005/09/01	-	Preliminary Version
V0.20P	2005/09/02	-	Added Register Description and Application Circuit
V0.21P	2005/10/13	-	Updated I2C Address Strapping Description of Function Description
V0.22P	2005/12/19	-	Updated Schematic
V0.23P	2006/07/04	-	Added function on pin7/pin13/pin29
		-	Added Hardware Monitor Register description (CR 0Ah ~ CR0Eh)
		-	Modified Hardware Monitor Register description (CR02h/93h/9Fh/AFh/BFh/CFh)
		-	Added Global Register CR1Ch
		-	Updated application circuit
V0.24P	2006/12/28	-	Added Electrical Characteristic Chapter
		2	Added Patent Note
V0.25P	2007/7/6	-	Company readdress

Table of Content

1. General Description

The F75334DG is an integrated performance control IC. The F75334DG integrated Hardware Monitor, PWM Loading Gauge, VID controller and GPIO functions inside. Part of the Hardware Monitor is for system protection including 6 channels voltage monitor, 4 sets dual current sources temperature sensor, 3 sets fan speed sensor and controller. Besides, provides Intel new generational temperature interfaces PECI/SST for temperature reading and also supports AMDSI interface for AMD series CPU temperature reading. PWM Loading Gauge is sensing the PWM signal change of duty cycle to react related functions for over/under-clocking application. VID controller is the dynamic voltage ID controller chip to provide the advanced CPU voltage programming when over/under clocking. The dynamic VID spec. is for new generation Intel/AMD CPU and also compatible to VRM9.0/VRM10.0/VRM10.X /VRM11.0 spec.. Additionally, the F75334DG provides easy voltage sensor input/output (VSI/VSO) function to sense Vcore voltage, then output the offset voltage for over/under voltage change use. Otherwise, F75334DG provides 21 GPIO pins for flexible application.

The F75334DG supports three main features for system protection, system over/under-clocking and dynamic voltage ID control. The F75334DG can easy save total cost and improve system performance. Especially the Loading Gauge feature will achieve multi-steps dynamic over/under-clocking being easy function. The F75334DG support 2 wire I2C interface, packaged in 48-pin LQFP green package and powered by 3.3V.

2. Feature List

- **General Functions**
  - Support 6 channels voltage monitor
  - Provide 4 temperature sensors
  - Support 3 sets fan control
  - Loading gauge for device loading sensing
  - Provide VID controller with OTF
  - 21 GPIO pins for flexible application
  - Easy voltage sensor I/O (VSI/VSO) for easy over/under voltage change use.
  - Support Intel PECI/SST interfaces for temperature reading.
  - Support AMDSI interface for temperature reading.
  - 2 wire I2C interface
  - 3VCC operation and packaged in 48-LQFP green package

- **Hardware Monitor**
  - Voltage Monitor

1. Provide 2.048V VREF
2. Support 6 channels voltage monitor(VCC3 V + VSB3V + 4 Externals)
3. Voltage monitor resolution is 8mv per LSB
4. Support 8bits high limit and low limit for each voltage channel

- Temperature Monitor
  1. Support 4 temperature sensor (1 local + 3 remote)
  2. Remote sensors support 2 types sensor (thermistor and transistor/thermal diode(Default))
  3. ±1°C accuracy on remote channel (60°C ~ 100°C)
  4. ±3°C accuracy on local channel (60°C ~ 100°C)
  5. Support temperature range from -25°C ~ 145°C
  6. Support high limit for each temperature sensor
  7. Support OVT(over temperature) limit for each temperature sensor
  8. Each temperature with hysteresis for high limit and OVT limit (0°C~15°C)
- Fan Controller and Monitor
  1. Support 3 sets fan speed sensor and fan control
  2. 50K fan speed sampling rate
  3. Support Intel 4-Fan control mode

  (1. Auto RPM Mode 2. Auto Duty Mode(Default) or manual duty 3. Manual RPM)

- **Loading Gauge**
  - Provide 1 PWMIN detection pins
  - Duty cycle reading resolution is 16bits
  - Support 4 duty limit (5 segments), and the resolution is 12 bits
  - Support 4 hysteresis registers for each limit (± offset)
  - Support 3 TURBO# output signals to control CLK Gen.
  - Support 1 STOP# output signal to chipset (Timing flexible)

- **VID controller**
  - Support VRM9.0, VRM10.0, VRM10 extend and VRM11.0
  - Support 5 offset registers to mapping 5 different loading range
  - Support Intel and AMD CPU
  - Easy voltage sensor I/O (VSI/VSO) for easy over/under voltage change use.

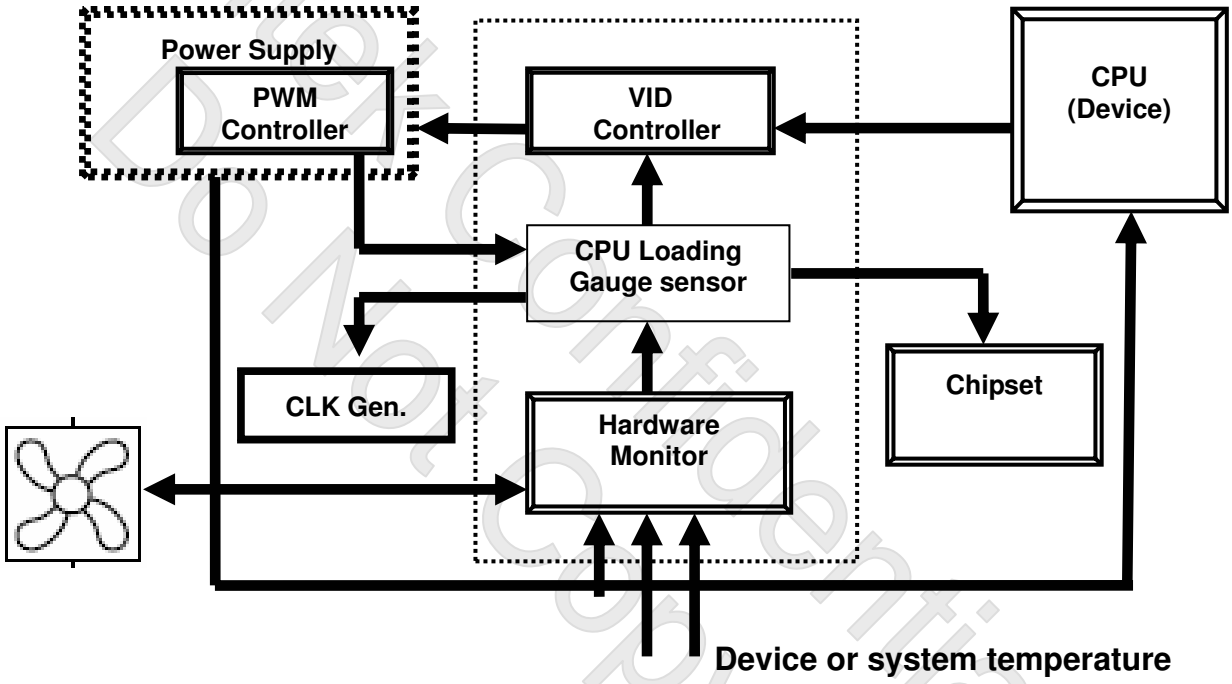
- **GPIO**
  - Support 21 GPIO pins
  - Only support level mode GP output control
  - GPIO pin status can be read by registers

Noted: Patented TWI235553 TWI263778

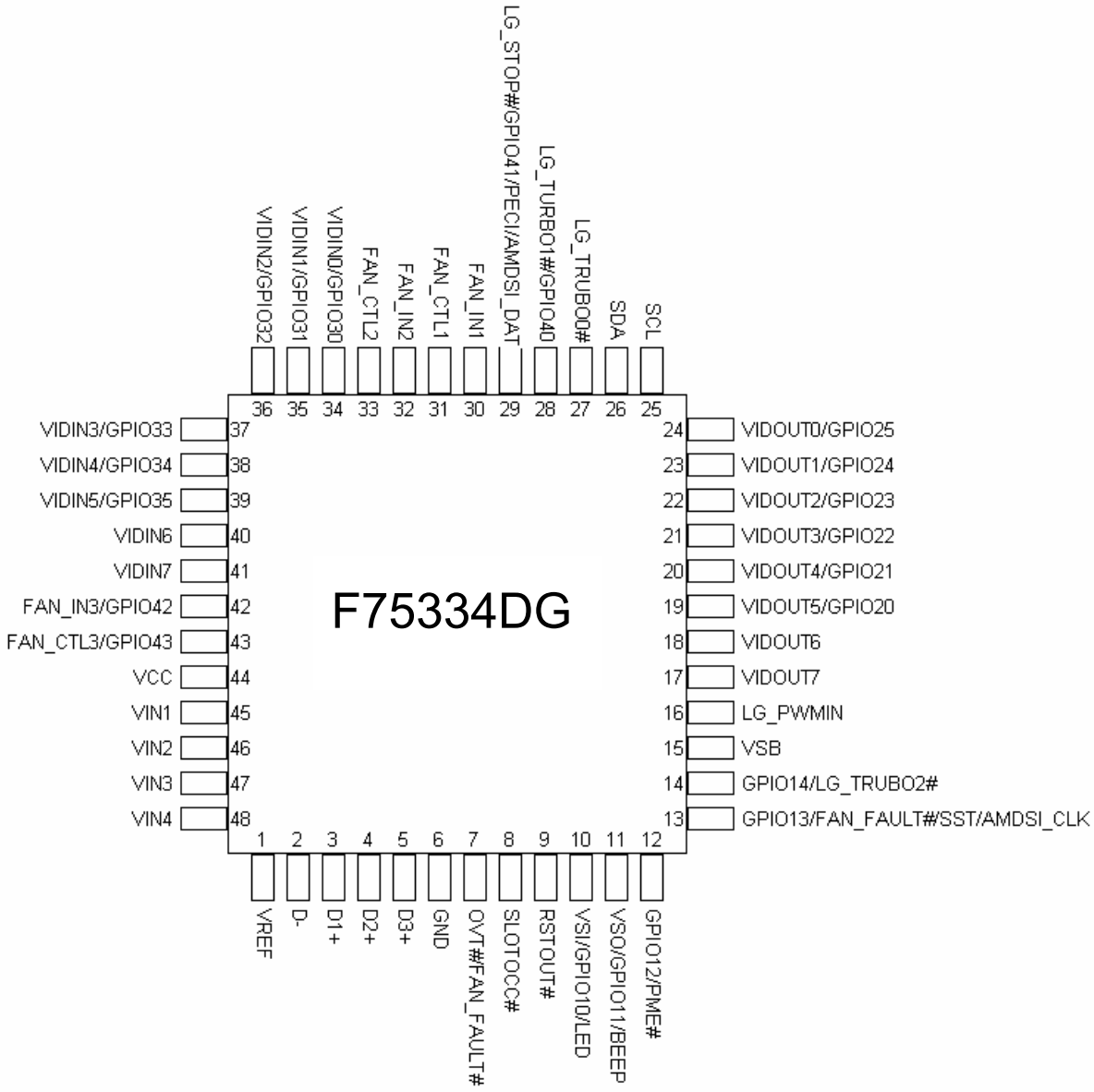
3. Key Specification

- Supply Voltage 3.0V to 3.6V
- Operating Supply Current 2.5 mA typ.

4. Block Diagram



5. Pin Configuration



6. Pin Description

I/OD_{12st} - TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability.
I/O_{12st} - TTL level bi-directional pin with schmitt trigger and with 12mA source-sink capability.
I/OOD_{12st} - TTL level bi-directional pin with schmitt trigger, Output pin with 12mA source-sink capability, and can programming to open-drain function.
I/OOD_{12lv} - Low level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.
I_{Lv}/O_{D8-S1} - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability.
I_{Lv}/OD_{12} - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 12mA sink capability.
OD_{12} - Open-Drain output pin with 12mA sink capability.
OOD_{12} - Output pin with 12mA source-sink capability, and can programming to open-drain function.
IN_{st} - TTL level input pin with schmitt trigger.
IN_{lv} - Low level input pin
AIN - Input pin(Analog).
AOUT - Output pin(Analog).
P - Power.

6.1 Power Pin

Pin No.	Pin Name	Type	Description
15	VSB	P	3.3V Standby Power
44	VCC	P	3.3V VCC Power
6	GND	P	Ground

6.2 Hardware Monitor Pin

Pin No.	Pin Name	Type	PWR	Description
1	VREF	AOUT	VCC3V	Reference voltage output 2.304V.
2	D-	AIN	VCC3V	Temperature sensor ground pin.
3, 4, 5	D0+ ~ D2+	AIN	VCC3V	CPU thermal diode/transistor temperature sensor input.
7	OVT#	I/OD_{12st}	VSB3V	Over temperature signal output. Default open drain active-low output. This pin will be a logic LOW when the temperature exceeds its limit. Default output enable when the temperature exceeds 100°C on initial.
	FAN_FAULT#	OD_{12}		Fan fault signal output pin.
12	GPIO12	I/OOD_{12st}	VSB3V	GPIO pin.
	PME#	OD_{12}		PME# signal output pin. System management interrupt (Pure open drain). This pin will be active low when there is something wrong with voltage,