
ePS5002

**RISC II Series
Microcontroller**

**Product
Specification**

Doc. VERSION 1.0

ELAN MICROELECTRONICS CORP.
November 2010



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ELAN MICROELECTRONICS CORPORATION

Headquarters:

No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
<http://www.emc.com.tw>

Hong Kong:

Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre 95
How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:

Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Korea:**Elan Korea Electronics Company, Ltd.**

301 Dong-A Building
632 Kojan-Dong, Namdong-ku
Incheon City, KOREA
Tel: +82 32 814-7730
Fax: +82 32 813-7730

Shenzhen:**Elan Microelectronics Shenzhen, Ltd.**

3F, SSMEC Bldg., Gaoxin S. Ave. I
Shenzhen Hi-tech Industrial Park
(South Area), Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:**Elan Microelectronics Shanghai, Ltd.**

3F, Building #13
No. 116, Lane 572, Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA 201203
Tel: +86 21 5080-3866
Fax: +86 21 5080-4600
elan-sh@elanic.com.cn

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Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2007/08/29
0.2	1. Added a Note in Section 6 <i>Code Option</i> . 2. Modified the max. supply voltage in Section 9. 3. Modified the supply current in Section 9	2008/10/21
0.3	1. Added the High-frequency 150kHz in Section 2 and Section 9.	2009/04/28
1.0	1. Modified the pin description of the OSCI pin in Section 5.1. 2. Deleted the VDD=3.0V Electrical Characteristics entries. 3. Modified the Operating voltage to 1.5V only.	2010/11/03

1 General Description

The **ePS5002** is an 8-bit RISC MCU embedded with a 5×40 LCD driver along with two 8-bit timers, one 16-bit general timer, and a Watchdog Timer. It also has on-chip 512 bytes RAM and 4K words program ROM. It is highly ideal for advance scientific calculator application, particularly those requiring high performance and low cost solution.

The MCU core is one of ELAN's second generation RISC based IC's, known as RISC II (RII) series. The core is specifically designed for low power and portable device applications. The ePS5002 also supports Fast, Slow and Idle modes, as well as Sleep mode to enhance its low power consumption features.

IMPORTANT NOTES

- Do not use Register BSR (05h) Bit 7 ~ Bit 2.
- Do not use Register BSR1 (07h) Bit 7 ~ Bit 2.
- Check the range of BSR and BSR1, which should be from 0x00~0x03.
- Do not use LCD RAM 28h ~ FFh.
- Do not use Register JDNZ at FSR1 (04h) special register.

2 Features

MCU

- 8 bit RISC MCU
- Operating voltage: 1.2V~1.8V
- Clock Source: Dual system clock
 - Low-frequency: 32kHz Internal RC oscillator / Crystal oscillator
 - High-frequency: 150kHz / 200kHz / 300kHz / 500kHz External RC oscillator
- One Instruction cycle time = 2 × System clock time
- Program ROM addressing: Maximum 4K words
- 128 bytes un-banked RAM including special registers and common registers
- 4×128 bytes banked RAM
- Max. of 32-level RAM stack
- Lookup Table function is fast and highly efficient when combined with Repeat instruction

- Register-to-Register move instruction
- Compare and Branch in one instruction (2 cycles)
- Single Repeat function (256 repeat times max.)
- Decimal ADD and SUB instruction
- Full range Call and Jump ability (2 cycles)

Peripheral

- 4 input pins (Port A.0~3) and 12 general I/O pins (Port A.4~7, Port B.0~7)
- 5/4/3 COM × 40 SEG LCD driver (embedded)
- One 16-bit timer (Timer 0) with event counter function
- One 8-bit timer (Timer 1) with wake-up function
- One 8-bit timer (Timer 2)
- One 8-bit Watchdog Timer
- Key I/O function with a maximum of 48 keys (Key matrix: Port A.0~2 and SEG0~15 with automatic key scan)

Internal Specification

- Watchdog Timer with its own on-chip RC oscillator
- MCU operating modes: Sleep Mode, Idle Mode, Slow Mode, and Fast Mode
- Supports RC and Crystal oscillation for system clock
- MCU wake-up function consists of input wake up and Timer 1 wake up
- MCU interrupt function consist of Input port interrupt and Timer interrupt (Timers 0 ~ 2)
- MCU reset function includes power-on reset, RSTB pin reset, and Watchdog timer reset

3 Block Diagram

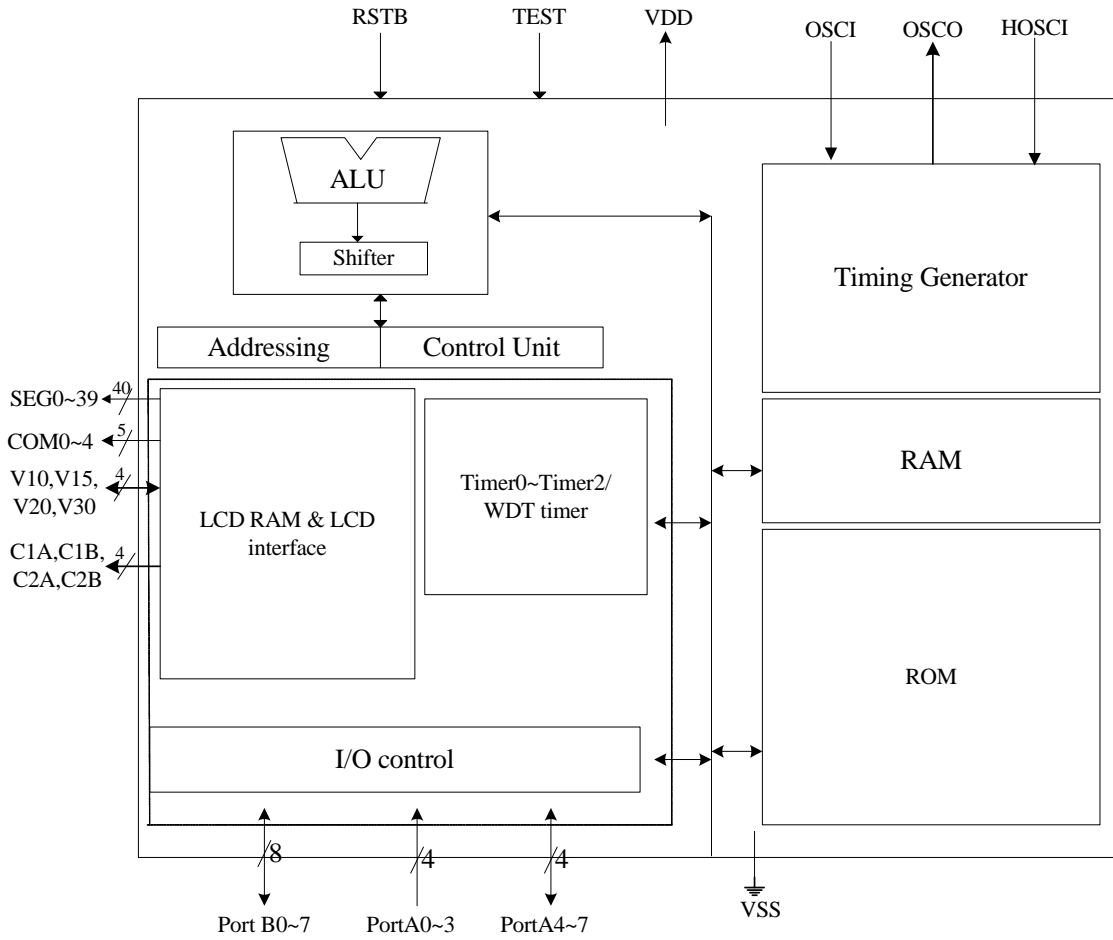


Figure 3-1 ePS5002 Block Diagram

4 Pin Assignment

■ 68-pin Chip form

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	NC	26	NC	51	NC	76	NC
2	NC	27	NC	52	NC	77	NC
3	NC	28	NC	53	NC	78	NC
4	NC	29	NC	54	NC	79	NC
5	NC	30	NC	55	NC	80	NC
6	NC	31	NC	56	NC	81	NC
7	COM4	32	NC	57	SEG29	82	C1A
8	COM3	33	SEG12/Strobe12	58	SEG30	83	C1B
9	COM2	34	SEG13/Strobe13	59	SEG31	84	C2A
10	COM1	35	SEG14/Strobe14	60	PortA.7	85	C2B
11	COM0	36	SEG15/Strobe15	61	PortA.6	86	V20
12	SEG0/Strobe0	37	SEG16	62	PortA.5	87	V15
13	SEG1/Strobe1	38	SEG17	63	PortA.4	88	V10
14	SEG2/Strobe2	39	SEG18	64	VSS	89	PortA.0
15	SEG3/Strobe3	40	SEG19	65	SEG32/PortB.0	90	PortA.1
16	SEG4/Strobe4	41	SEG20	66	SEG33/PortB.1	91	PortA.2
17	SEG5/Strobe5	42	SEG21	67	SEG34/PortB.2	92	PortA.3
18	SEG6/Strobe6	43	SEG22	68	SEG35/PortB.3	93	TEST
19	SEG7/Strobe7	44	SEG23	69	SEG36/PortB.4	94	RESETB
20	SEG8/Strobe8	45	SEG24	70	SEG37/PortB.5	95	OSCO
21	SEG9/Strobe9	46	SEG25	71	SEG38/PortB.6	96	OSCI
22	SEG10/Strobe10	47	SEG26	72	SEG39/PortB.7 (EVIN)	97	HOSCI
23	SEG11/Strobe11	48	SEG27	73	V30	98	VDD
24	NC	49	SEG28	74	NC	99	NC
25	NC	50	NC	75	NC	100	NC

5 Pin Description

5.1 MCU System Pins (7 Pins)

Name	I/O/P Type	Description	Note
VDD	P	Digital and Analog positive power supply, ranging from 1.2V~1.8V. Connect to VSS through the capacitors (0.1 μ F).	–
VSS	P	Digital and Analog negative power supply.	–
RSTB	I	System reset pin. Low active. Connect 0.1 μ F to VSS.	Int. pull-up
TEST	I	Test mode select pin (High active). For chip internal test only. Normally connect to VSS.	Int. Pull Down
OSCI	I	Crystal oscillator connecting pin	–
OSCO	O	Crystal oscillator connecting pin	–
HOSCI	I	Hi-Speed RC oscillator connecting pin	Ext. R to VDD

5.2 Embedded LCD Pins (53 Pins)

Name	I/O/P Type	Description	Note
COM0~COM4	O	LCD common signal output pin	–
SEG0~SEG15	O	LCD segment signal output pin shared with Key Strobe 0~15	–
SEG16~ SEG31	O	LCD segment signal output pin	–
SEG32~SEG39 / Port B.0~7	I/O	LCD segment signal output pin or I/O pin; defined by code option	–
C1A, C1B	–	LCD voltage charge-pump pin. Connect 0.1 μ F between C1A and C1B.	–
C2A, C2B	–	LCD voltage charge-pump pin. Connect 0.1 μ F between C2A and C2B.	–
V30, V20, V15, V10	O	LCD bias Pin. Connect 0.1 μ F to Vss	–

5.3 I/O Port (8 Pins)

Port	Bit	Function	I/O Type	Power Source	Description	Note
Port A	Bits 2~0 (for key scan)	General Input	I	VDD	Key input	Int. Pull-up (R1: small resistor, R2: Large controllable resistor)
		Interrupt and wake up	I	VDD	Input port interrupt and wake-up pin	
	Bit 3	General Input	I	VDD	–	
		Interrupt and wake up	I	VDD	Input port interrupt and wake-up pin	
	Bits 7~4	General Input	I	VDD	–	
		Interrupt and wake up	I	VDD	Input port interrupt and wake-up pin	
General Output		O	VDD	–		

6 Code Option

Located at Address 0x000C~0x000F of Program ROM

- Initial mode after reset:
 - Select “Slow” mode or “Fast” mode

NOTE

For Initial mode after reset, it is recommended that user set it to “Slow mode”.

- The Operating voltage option:
 - Only has “1.5V”
- Low Frequency Oscillator:
 - Select “Crystal” oscillator or “Internal RC” oscillator
- Reset pin’s condition:
 - Select “Level hold” or “One short” for reset pin
- Maximum duty ratio and LCD bias option:
 - Select “1/5 duty and 1/3 bias” or “1/4 duty and 1/3 bias” or “1/3 duty and 1/2 bias”
- Port B low nibble control bit (SEG32~SEG35):
 - Select “LCD segment signal output” or “general I/O functions”
- Port B high nibble control bit (SEG36~SEG39):
 - Select “LCD segment signal output” or “general I/O functions”
- Key matrix combination:
 - Select “Port A and SEG” or “Port A and Port B”

7 MCU System

7.1 Power-up and Reset Timing

- Power-on Reset Timing

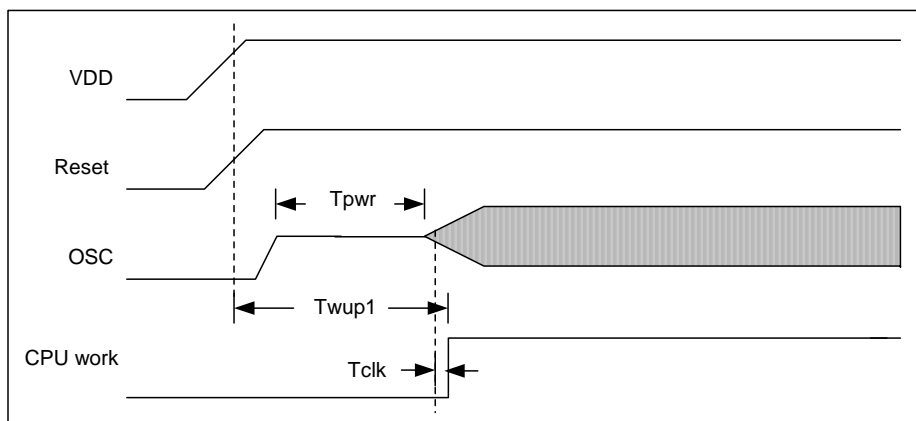


Figure 7-1 Power on Reset Timing Diagram

■ Sleep Mode Wake-up Timing

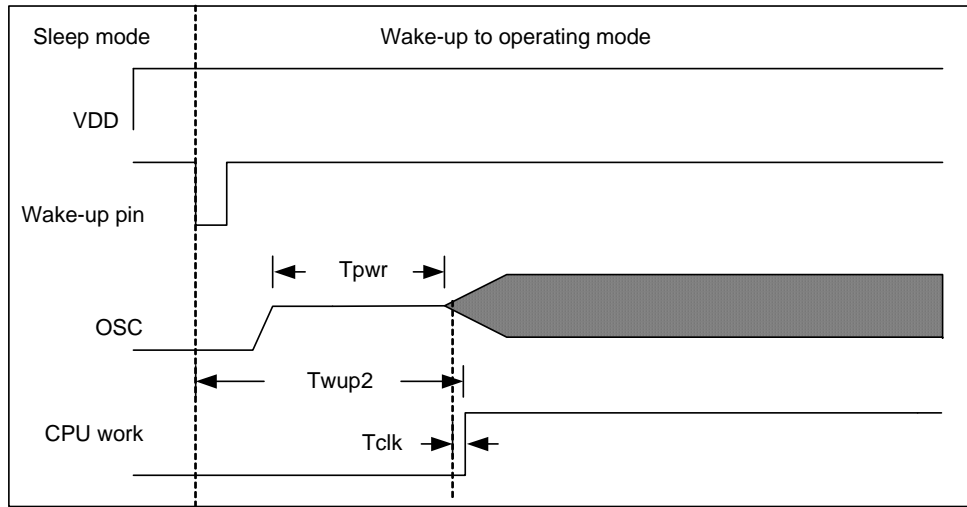


Figure 7-2 Sleep Mode Wake-up Timing Diagram

Condition: Vdd = 1.5V, Cosc = 20pF and Ta = 25°C

Symbol	Characteristics	Min.	Typ.	Max.	Unit
Tpwr	Oscillator start up time	-	480	780	ms
Twup1	CPU warm up time (Power-on reset)	-	500	800	ms
Twup2	CPU warm up time (Sleep mode wake-up)	-	485	785	ms
Tclk	Detect slow clock time	-	1.0	1.1	ms

7.2 MCU Operation Timing

■ Slow Mode to Fast Mode Timing:

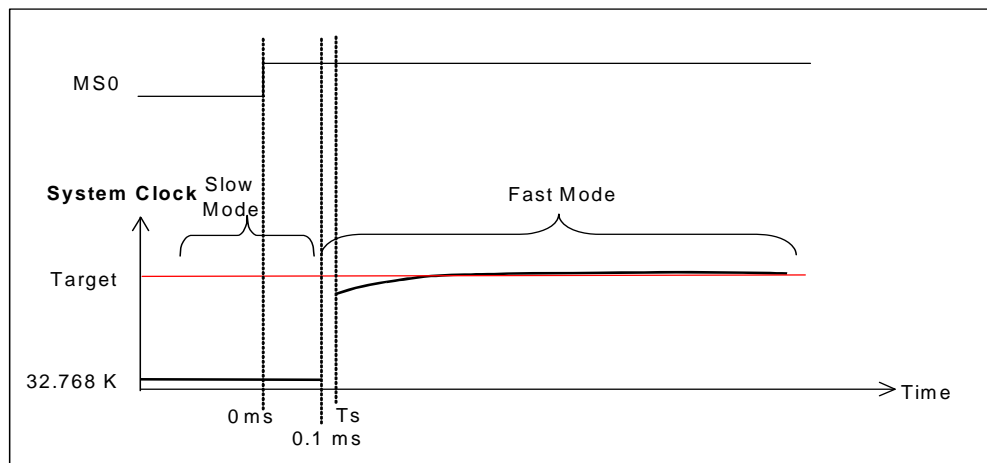


Figure 7-3 Slow Mode to Fast Mode Timing Diagram

- Note:**
1. Slow Mode switches to Fast Mode at Time = 0 ms.
 2. System clock will switch to Fast Mode after a delay of 0.1ms by oscillator and enters into Fast Mode (i.e., system clock will be at 200, 300, or 500kHz).
 3. High frequency RC will be stabilized at Time=Ts (15 μs~30 μs).

8 ROM and RAM

8.1 Program ROM Map

ROM Size = 4K Words	
Address	Description
0000h 000Bh	Interrupt Vector (12 words)
000Ch 000Fh	Code Option (4 words)
0010h 001Fh	Test Program (16 words)
0020h 0FFFh	Program or Fixed data region

8.2 RAM Map

RAM Size: 86 Bytes + 4 Banks × 128 Bytes = 598 Bytes

8.2.1 Un-banked RAM

Address	Unbanked
00h 12h	Special Registers
13h 1Fh	General purpose RAM
20h 36h	Control Registers
37h 7Fh	General purpose RAM

8.2.2 Banked General RAM

Address	Bank 0	Bank 1	Bank 2	Bank 3
80h FFh	General Purpose RAM	General Purpose RAM	General Purpose RAM	General Purpose RAM

8.3 LCD RAM Map

■ 1/5 Duty

RAM Address		COM0	COM1	COM2	COM3	COM4	-	-	-
LCDARL		Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
SEG0	00H								
:	:								
SEG39	27H								

■ 1/4 Duty

RAM Address		COM0	COM1	COM2	COM3	-	-	-	-
LCDARL		Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
SEG0	00H								
:	:								
SEG39	27H								

■ 1/3 Duty

RAM Address		COM0	COM1	COM2	-	-	-	-	-
LCDARL		Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
SEG0	00H								
:	:								
SEG39	27H								

9 Electrical Characteristics

9.1 VDD = 1.5V Electrical Characteristics

■ Absolute Maximum Ratings

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD	–	–0.3 to +2.0	V
Supply voltage for ICE	VCC	–	–0.3 to +3.6	V
Input voltage (general input port)	VIN	–	–0.5 to VDD +0.5	V
Input voltage for ICE	VIN1	–	–0.5 to VCC +0.5	V
Operating temperature range	TOPR	–	–10 to +70	°C
Storage temperature range	TSTR	–	–55 to +125	°C

■ Recommended Operating Conditions

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD	–	1.2 to 1.8	V
Supply voltage for ICE	VCC	–	2.2 to 3.6	
Input voltage	VIH	–	VDD x 0.9 to VDD	V
	VIL	–	0 to VDD x 0.1	V
Input voltage for ICE	VIH	–	VDD x 0.9 to VDD	V
	VIL	–	0 to VDD x 0.1	V
Operating temperature	TOPR	–	–10 to +70	°C

■ DC Electrical Characteristics (Condition: Ta = 25°C, VDD = 1.5V)

Parameter	Sym.	Condition		Min.	Typ.	Max.	Unit
Clock	F _{HOSC}	Main-clock frequency	RC OSC. R=2 MΩ	105	150	195	kHz
			RC OSC. R=1.5 MΩ	140	200	260	
			RC OSC. R=1 MΩ	210	300	390	
			RC OSC. R=560 KΩ	350	500	650	
	F _{osc}	Sub-clock frequency	Internal RC OSC.	24.6	32.8	41	kHz
			Crystal OSC.	–	32.768	–	
Supply Current	I _{dd1}	Sleep mode	VDD=1.5V, no load	–	–	1	μA
	I _{dd2}	Idle mode	VDD=1.5V RC OSC / Crystal, LCD enabled, no load	–	2	3	
	I _{dd3}	Slow mode	VDD=1.5V, RC OSC, LCD disabled, no load	–	3	4	
			VDD=1.5V, Crystal OSC, LCD enabled, no load	–	3	5	
	I _{dd5}	Fast mode	VDD=1.5V, F _{HOSC} =200kHz, LCD enabled, no load	–	15	20	
			VDD=1.5V, F _{HOSC} =300kHz, LCD enabled, no load	–	20	30	
			VDD=1.5V, F _{HOSC} =500kHz, LCD enabled, no load	–	30	50	
Input Voltage	VIH1	PA[0:7] , PB[0:7] (as general input port)		VDD×0.7	–	VDD	V
	VIL1			0	–	VDD×0.3	



Parameter	Sym.	Condition		Min.	Typ.	Max.	Unit	
Input Threshold Voltage (Schmitt)	VT+	RSTB		0.5×VDD	–	0.75×VDD	V	
	VT–			0.2×VDD	–	0.4×VDD		
Input Leakage Current	IIL	All Input port (without pull up/down resistor) Vin= VDD or GND		–	–	±1	μA	
Large Pull-up Resistance	RPU5	RSTB	Vin=GND	300	450	800	KΩ	
Small Pull-up Resistance	RPU6	RSTB	Vin=1V	10	30	60	KΩ	
Large Pull-down Resistance	RPD1	TEST	Vin=VDD	250	500	800	KΩ	
Small Pull-down Resistance	RPD2	TEST	Vin=0.5V	3	6	12	KΩ	
Data Retention Voltage	Vret	–		1.2	–	–	V	
Output Current	IOH1	PA[4:7], PB[0:7] (as general output port)		VDD=1.5V, VOH=1.2V, LCD enabled	-0.1	-0.4	-0.8	mA
	IOL1			VDD=1.5V, VOL=0.2V, LCD enabled	0.6	0.9	1.5	
Large Pull-up Resistance	RPU1	PA[0:7]	Key high resistance, pulled up by R2, LCD enabled, Vin2=0.5V	110	280	800	KΩ	
	RPU3	PB[0:7]	Vin=0.5V, LCD enabled	100	320	800		
Small Pull-up Resistance	RPU2	PA[0:3]	Key high resistance, pulled up by R2//R1, LCD enabled, Vin2=0 V	6	18	60	KΩ	
	RPU4	PA[4:7]	Vin=1V, LCD enabled	15	30	75		
LCD Driver								
LCD Display Output ON-resistance	ROC	Com[0:4]	VOH=V30 ± 0.2V	0.35	0.4	0.5	KΩ	
			VOM=V20 ± 0.2V	0.55	0.65	0.75		
			VOM=V10 ± 0.2V	0.35	0.40	0.45		
			VOL=0.2V	0.25	0.3	0.35		
	ROS	Seg[0:39]	VOH=V30 ± 0.2V	0.35	0.4	0.5	KΩ	
			VOM=V15 ± 0.2V	0.45	0.6	0.85		
VOL=0.1V			0.25	0.3	0.35			
Strobe Output ON-resistance	ROP	Seg[0:15] (as key strobe)	V=VDD-0.2V	80	200	500	KΩ	
	RON		V=0.2V	0.85	1.1	1.3		

10 Application Circuits

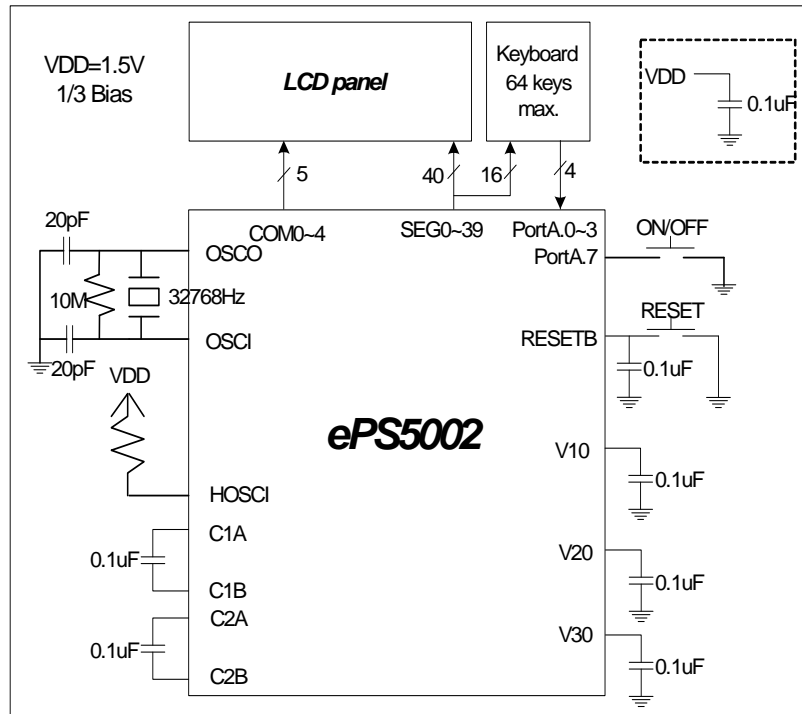


Figure 10-1 VDD=1.5V Application Circuits Diagram