eMG2000A

16-Bit TV Game Processor

Product Specification

DOC. VERSION 1.1

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
1.1	Initial version	2008/04/30

1 General Description

The **EMG2000A** is a single chip designed for TV-Game and simple multi-media related applications. The applications include not only traditional video games, but also many educational tools, kids' favorite interactive toys and leisure products.

The **EMG2000A** contains multi-processors which includes a 16-bit CPU (a RISC DSP developed by EMC), PPU (Picture Processing Unit with true color output ability), and APU (Audio Processing Unit with Midi and PCM output capability). The EMG2000A is able to generate 512 color graphics and well-known gaming style sound for different TV system (NTSC or PAL) through True color TV Encoder or directly to TFT LCD or CSTN.

The operating voltage is from 2.6V to 3.6V with CPU speed at 27MHz. User can also select 6 MHz crystal and PLL to run on 27 MHz speed. It provides 38 programmable multi-function general purpose I/O, RTC with 4 outputs, 4 multi-function 8 bits timer/counter, which offers capture, compare, and PWM functions. In addition, the eMG2000A offers built-in voltage regulator, low voltage reset, UART, master and slave SPI interface, 8 channels 10-bit A/D, and light gun, etc. it also supports external 32K RTC clock source as wake-up source for real time clock application.

2 Features

- **MPU**
  - 16-bit RISC CPU architecture
  - Operating voltage: 2.6V~3.6V
  - Maximum system clock: 27 MHz
  - Real time clock function (RTC) with wake-up function
  - 4 timers for general purpose counter with multi-function PWM generator or capture function
  - Built-in Watchdog Timer (WDT)
  - 4 external interrupt pins
  - Supports external ROM/SRAM , addressing capability: ROM/12M×16 bits and SRAM/4M×16 bits; ROM only/16M×16bits
  - Internal WRAM: 2K words for CPU
  - 22K words internal video RAM for PPU, which can also be used for CPU
  - Built-in 4KW program RAM for timing critical application
  - 38 General Input/Output Ports: 16 bits Port A, 8 bits Port B, and 14 bits Port C

- 10 bits SAR ADC converter with 8 channels general analog inputs
- Specified touch panel ADC
- UART, SPI, PWM, IrDA, Joystick, Light Gun
- Two operating modes: Normal mode, Power-down mode
- CPU wake-up function, including: GPIO wake up, SPI wake up, External Interrupt wake up and External event wake up
- 25 kinds of interrupt sources, including CPU peripheral interrupts, PPU_VBI and PPU_HBI interrupts, Timer interrupts, ADC interrupts, etc.
- CPU reset function includes power-on reset, nRST pin reset
- Four powerful and flexible DMA channels, which can support increase, decrease, periodicity, steps, and even more trigger source selection

■ **PPU**

- Supports 512 colors for two backgrounds
- Supports true color (24 bits) image mode
- Picture size: 320×240
- Background pattern size: 8×8, 16×16
- Background color: 256 colors with 2 palette tables
- 24-bits true color palette pool
- Supports graphic background mode
- Two layers backgrounds
- Supports background rotation with 15 degrees for each angle
- Supports background horizontal and vertical zoom from 0.5× to 2×
- Supports 8 separate horizontal area scrolling
- Max. of 31 sprites per line (8×8 Pixels)/22 sprites per line (16×16 pixels) on 2 BGs
- Sprite color: 256/16/4
- Max. of 256 or 128×2 sprites per screen
- 16 types sprite pattern size: 8×8 to 64×64
- Sprite effect: mirror/rotation/shift/zoom 0.5×~2× (16 levels)
- Priority: 8 layers (6 sprites and 2 background)
- 4 different color effects, including fade in fade out effect
- Palette processor with changeable YCbCr code
- Composite TV signal generator

- 10-bit DAC for TV signal (Composite Video Output)
- Video signal generation in YCbCr domain
- Support smart 4 channels HDMA
- Support CCIR601 8 bits digital data output interface for TFT LCD panel
- Support 256 colors or 65K colors CSTN controller interface with window mode
- Support all world wide standard NTSC, and almost world wide standard PAL with interlace / non-interlace output

- **APU**
  - 8 CH adjustable 6kHz, 8kHz, 12kHz, 16kHz, 20kHz multi-sampling rate PCM
  - 8 CH adjustable 6 bits, 8 bits, 10bits multi-data rate PCM
  - 8 CH separate PCM volume control
  - 16 CH ADSR envelop control
  - 16 CH ADSR Separate Volume Control
  - Two 10-bit DACs for left and right audio channel output
- **System**
  - Operating Voltage: 2.6V~3.6V
  - Operating Temperature: -10°C ~ 70 °C

3 Application

- **TV-Game**
  - Home used game machines
  - Game consoles
- **Handheld Device**
  - Handheld game machines
  - Handheld LCD game console application

4 Functional Block Diagram

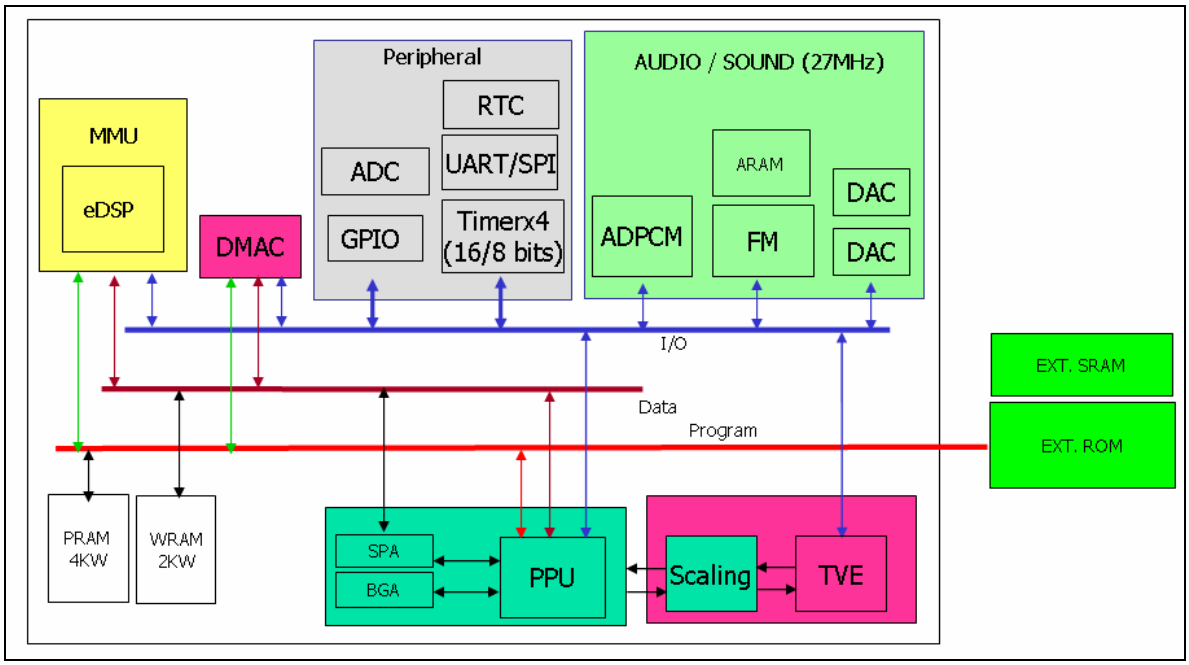


Figure 4 EMG2000A Functional Block Diagram

5 Pin Description

- **System Pin**

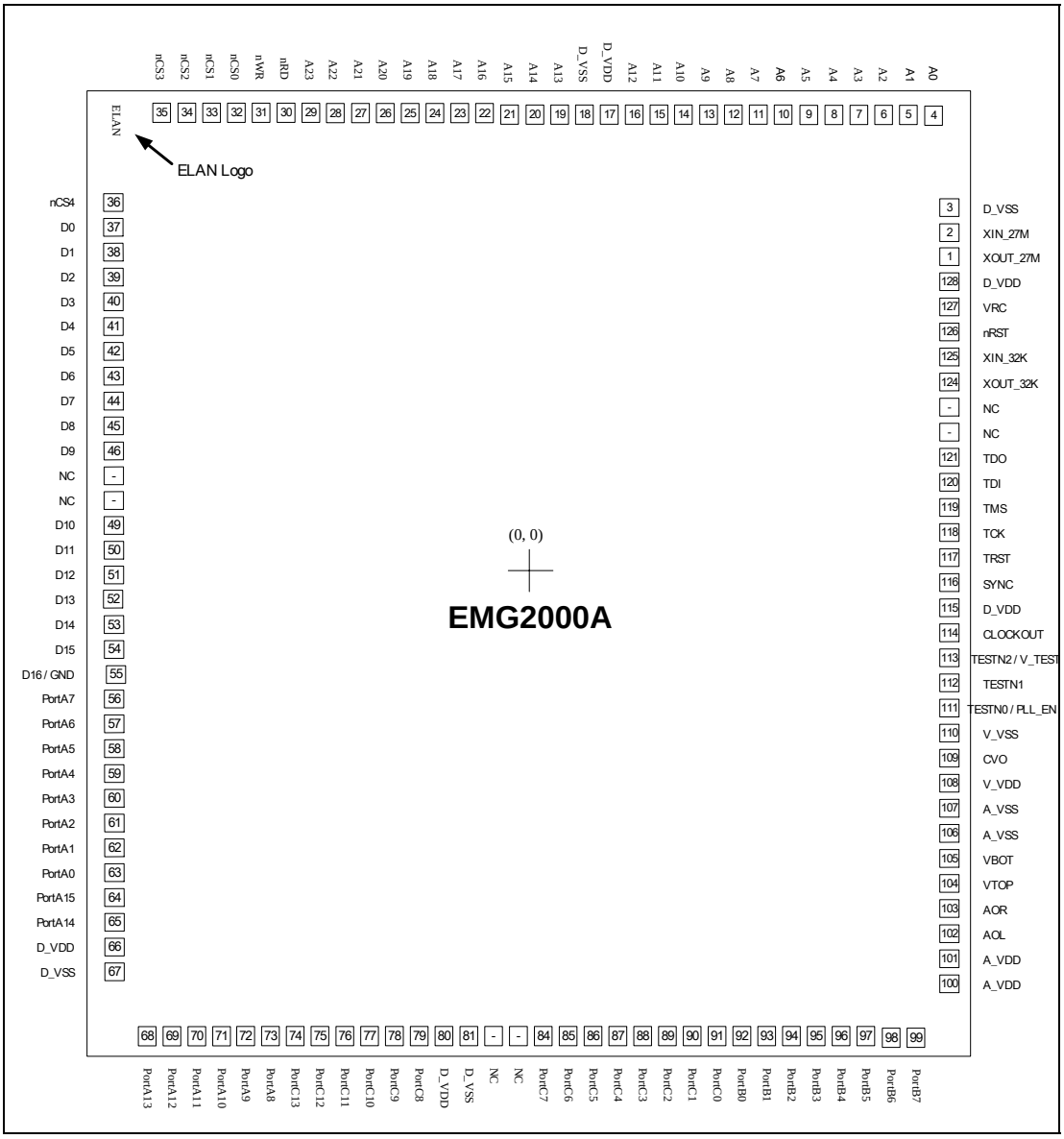
Name	I/O Type	Description	Note
D_VDD	I	Digital Power supply	–
D_VSS	I	Digital Ground	–
V_VDD	I	Video Power supply	–
V_VSS	I	Video Ground	–
A_VDD	I	Audio Power supply	–
A_VSS	I	Audio Ground	–
nRST(Schmitt)	I	System reset pin (Low Active); with Schmitt Trigger	Int. pull-up
XIN_27M	I	27MHz or 6MHz Crystal connecting pin	–
XOUT_27M	O	27MHz or 6MHz Crystal connecting pin	–
XIN_32K	I	External 32K RTC Crystal connecting pin	–
XOUT_32K	O	External 32K RTC Crystal connecting pin	–
A[23:0]	O	System address	–
D[16:0]	TRI	Data Bus	–
nRD	O	Read Strobe (Low Active)	–
nWR	O	Write Strobe (Low Active)	–
nCS[4:0]	O	Memory Chip Select(Low Active) nCS0 : External 4MW ROM(0x000000~0x3FFFFF) nCS1 : External 4MW ROM (0x400000~0x7FFFFF) nCS2 : External 4MW ROM(0x800000~0xBFFFFF) nCS3 : External 4MW SRAM/ROM(0xC00000~0xFFFFFF) nCS4 : External 8MW ROM(0x000000~0x7FFFFF)	–
GPIO_A[15:0]	I/O	General Purpose Input/Output A with Programmable Pull up/down resistor. It can also be select as Ext. IRQ, UART, PWM, SPI, External timer, Lightgun	Int. pull-up/pull-down (Programmable)
GPIO_B[7:0]	I/O	General Purpose Input/Output B with Programmable Pull up/down resistor. It can also be select as Ext. IRQ, Touch panel ADC, General ADC input	Int. pull-up/pull-down (Programmable)
GPIO_C[13:0]	I/O	General Purpose Input/Output C with Programmable Pull up/down resistor. It can also be select as LCD interface, CSTN interface	Int. pull-up/pull-down (Programmable)
VRC	I	Audio Voltage Regulator Control VRC = 1: Using Internal Voltage Regulator VRC = 0: Using External Reference Voltage	Int. pull-up
SYNC	O	Internal MPU Kernel Sync monitoring signal	–

Name	I/O Type	Description	Note
CLOCK_OUT	O	32KHz / 288KHz / 27MHz System clock out (Depend on TESTN Status)	–
TESTN[2:0]	I	TEST mode (high active) 0x00, 0x07: Normal mode / 32KHz(CLOCK_OUT) 0x01: PLL enable / 32KHz 0x02: Internal test / 27MHz 0x03: RAM self-test / 27MHz 0x04: V_TEST mode with color bar, tone output / 288KHz 0x05, 0x06: Reserved / 27MHz	TESTN.1, TESTN.2 are int. pull-down, **TESTN.0 is floating**
TRST	I	JTAG Test Reset	Int. pull-down
TCK	I	JTAG Test clock input	
TMS	I	JTAG Test mode select	
TDI	I	JTAG Test data in	
TDO	O	JTAG Test data out	–

- **Video/Audio/Analog Pin**

Name	I/O Type	Description	Note
CVO	O	Composite Video Output	–
AOL	O	Audio Left Output	–
AOR	O	Audio Right Output	–
VTOP	I/O	Voltage Top Reference VRC = 1: Output VRC = 0: Tri-state	–
VBOT	I/O	Voltage Bottom Reference VRC = 1: Output VRC = 0: Tri-state	–

■ Bonding Pad Diagram



Note: For the PCB Layout, the IC substrate must be connected to VSS.

Figure 5-1 EMG2000A Bonding Pad Diagram

6 Functional Description

6.1 CPU

The EMG2000A is embedded with a whole new 16-bit high performance RISC DSP developed by ELAN. It provides 57 powerful instructions with efficient DSP features. The majority of instructions execute in two clock cycle, the eDSP achieves throughputs approaching 1 MIPS per 2 MHz allowing the system designer to optimize power consumption versus processing speed.

The eDSP has eight 16-bit general-purpose registers. All the registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. These registers are used as data, addresses or offset registers. They can be addressed up to 64 Kbytes (ROM, RAM) without any segmentation (bank). The registers R0, R1 have some added functions to their general usage. These two registers are treated as a single double-word (32-bit) accumulator called accumulator D that hold operands and results of arithmetic calculations or data manipulations or data division.

The Program Counter is a16-bit wide register that holds the address of the next instruction to be executed. Therefore, the PC can address up to 64K instruction words. However, the eMG2000A addressing ability can be extended to 16MW through banking mechanism.

The Stack Pointer holds the 16-bit address of the last stack location used and will be automatically modified by interrupt processing and subroutine calls and returns. User may reprogram the SP during initialization to any location within the data (RAM) space. The SP also can be used by the user software (PUSH and POP instructions), but user should remember that the CPU also uses the SP.

Besides, there are four registers; Repeat Counter, Loop Counter, Loop Start Address and Loop End Address. They are used as temporary registers when executing repeat or loop instruction. The Repeat and Loop Counter store the repeat times. Furthermore, it needs to store the Start and End address in loop operation.

The EMG2000A CPU runs at a fast speed of 27MHz, therefore, it can run on a maximum speed of 13.5MIPS. Furthermore, the eMG2000A has an embedded 4KW programming SRAM, which is useful for some time critical application to run the program without wait state.

6.2 Interrupt

There are 23 mask-able interrupt sources with 3 non-mask-able interrupts for the eMG2000A. The **IntEn0/IntEn1** (Interrupt Enable) registers can enable (set bit to 1) and disable (set bit to 0) the corresponding mask-able interrupt. The **IntFlg0/IntFlg1** (Interrupt Flag) registers are the interrupt flag bits. These 23 flags can be set by external/internal hardware events, software events, and cleared by ISR entering condition or software. The **ExtIRQ0** has the highest priority in all mask-able interrupts and the HBI2 has the lowest priority. Each priority could be popped up to a higher one by setting the corresponding bit in **IntPri0/IntPri1** (Interrupt Priority).

Interrupt Vector	Priority	Interrupt Source	Description
0x00	Highest	Reset	Hardware Reset (NMI)
0x02		-	Reserved (NMI)
0x04		-	Reserved (NMI)
0x06		ExtIRQ0	External input interrupt source 0
0x08		Timer0	Timer 0 underflow interrupt
0x0A		Timer1	Timer 1 underflow interrupt
0x0C		Timer2	Timer 2 underflow interrupt
0x0E		Timer2_Ov	Timer 2 overflow interrupt
0x10		Timer3	Timer 3 underflow interrupt
0x12		Timer3_Ov	Timer 3 overflow interrupt
0x14		RTC0	RTC0 interrupt
0x16		RTC1	RTC1 interrupt
0x18		RTC2	RTC2 interrupt
0x1A		RTC3	RTC3 interrupt
0x1C		ExtIRQ1	External input interrupt source 1
0x1E		PWM_Duty	PWM duty interrupt
0x20		PWM_Period	PWM period interrupt
0x22		SPI_Rdy	SPI interrupt
0x24		UART_RxRdy	UART receiver ready interrupt
0x26		WDT	Watch dog timer interrupt
0x28		SP_OvLimit	Stack area limit interrupt
0x2A		ADC_DataRdy	ADC transfer end interrupt
0x2C		UART_TxRdy	UART transmit ready interrupt
0x2E		VBI	Vertical blanking interrupt
0x30		HBI0	Horizontal blanking 0 interrupt
0x32		HBI1	Horizontal blanking 1 interrupt
0x34		ExtIRQ2	External input interrupt Source 2
0x36	Lowest	ExtIRQ3	External input interrupt Source 3

6.3 Memory

The eMG2000A uses a modified Harvard architecture, so that memory is organized in two separate fields: Program ROM and Data RAM. As the memory is separated, the central processing unit can read/write data at the same time. Besides, the I/O space has an independent address, which is the I/O map. The different configuration of each domain is shown as follows.

6.3.1 Program ROM and Program RAM

The Program Counter (PC) is dedicated for program address, and is automatically modified by the processing control flow. The eight general purpose registers could be Program ROM pointers.

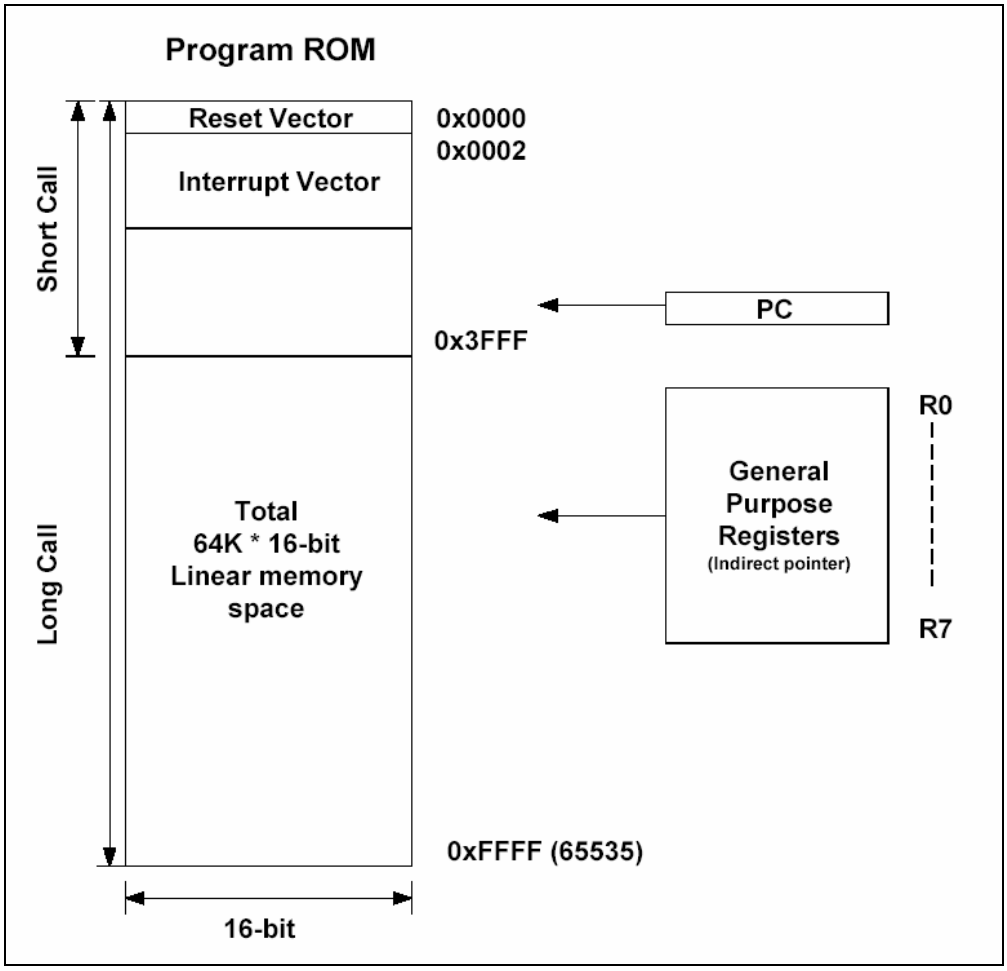
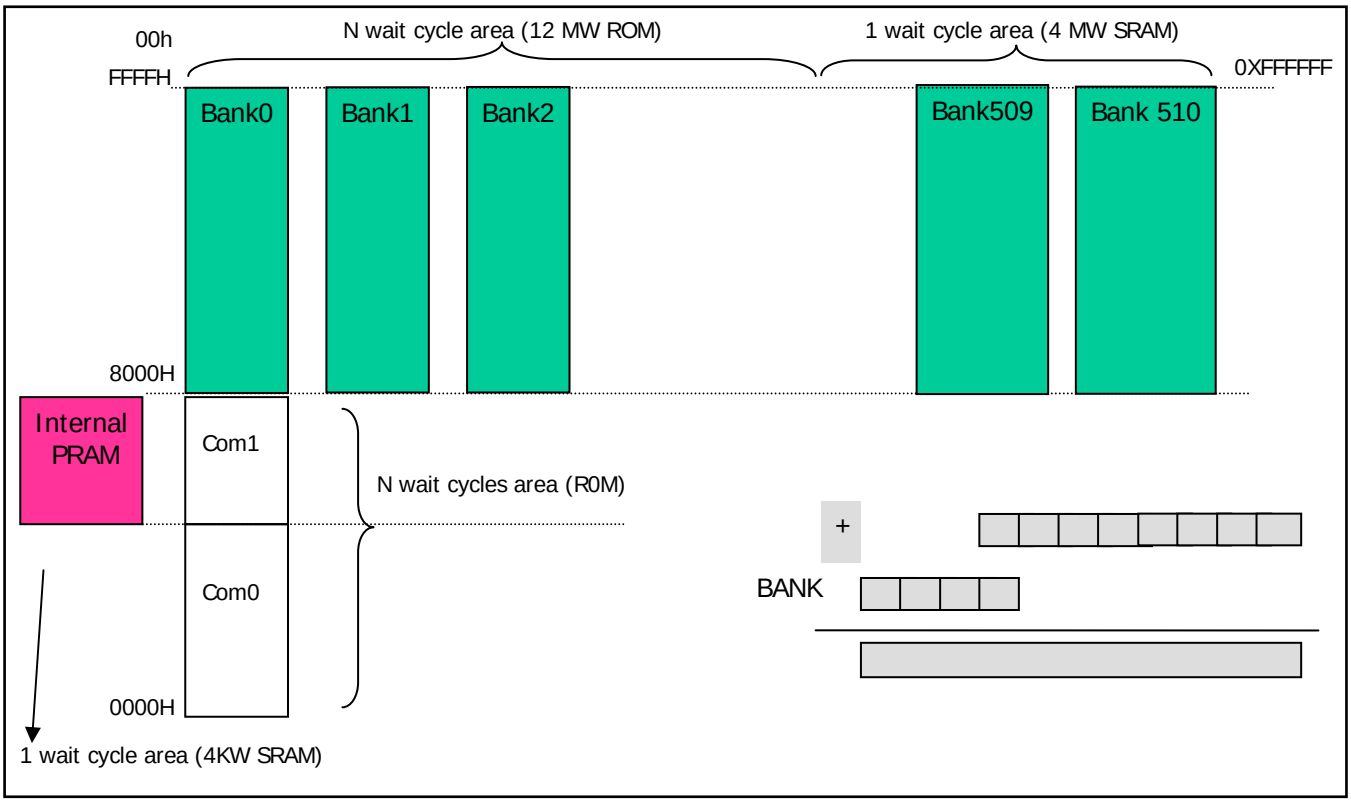
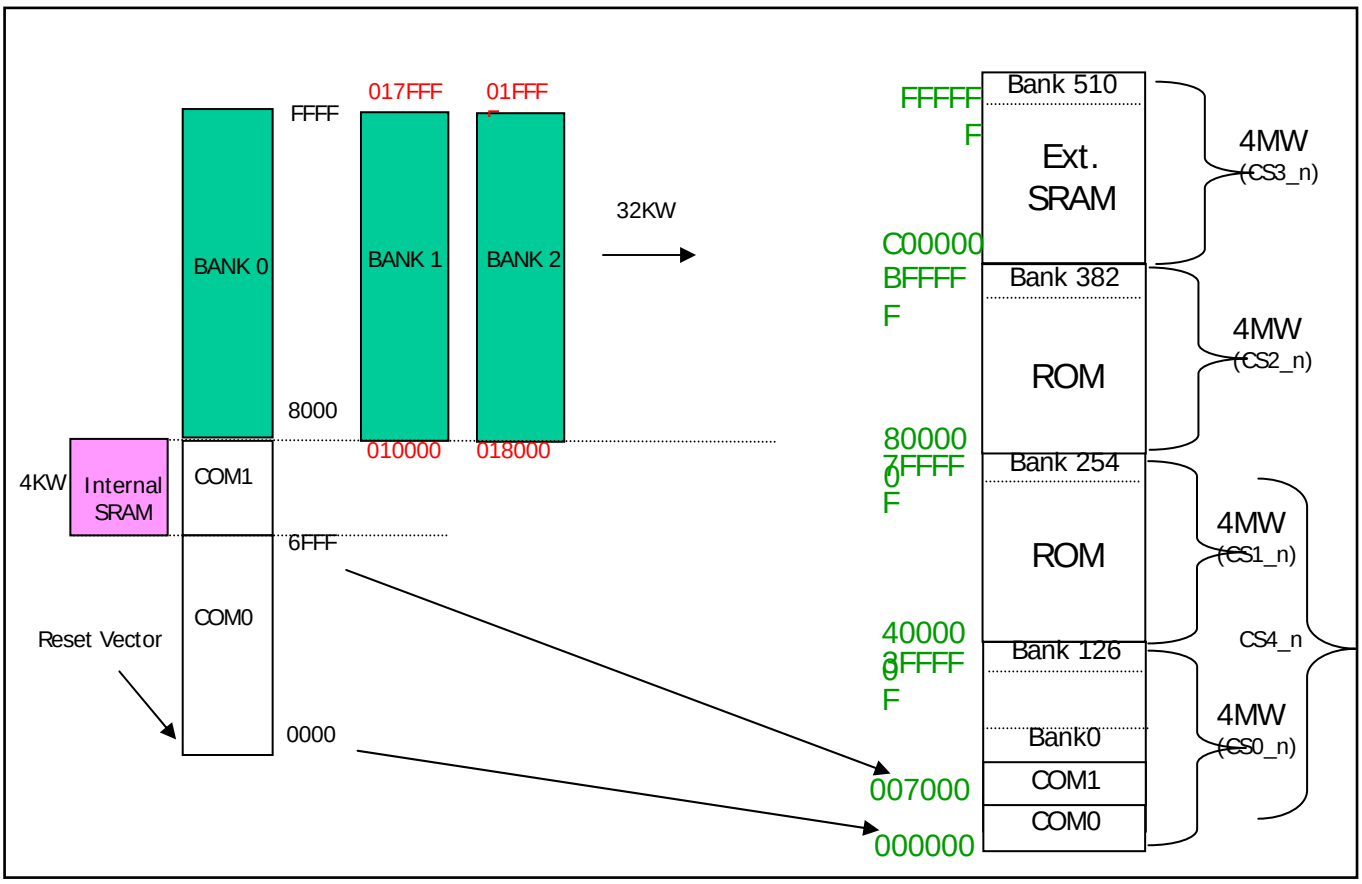


Figure 6-1 EMG2000A Program ROM Memory Diagram

For mass-storage usage, the eMG2000A added a banking methodology for eDSP to access externally a maximum of 16MW program ROM. It can access an external 24 bits address by setting the corresponding bank register, each bank is 32KW. The bank area is from 0x8000H to 0xFFFFH, which is all the same for different banks under logical 16 bits address. The physical 24 bits address can be calculated by bank register with 32KW address offset, which is a common area.

The EMG2000A added an internal program RAM area, which is 4KW, from 0x7000H to 0x8000H. This program RAM area is a full speed area for program, and it is overlapped on the same program ROM area. Therefore, user needs to avoid allocating any data or program in this area when using the program RAM.


00h
FFFFH
N wait cycle area (12 MW ROM)
1 wait cycle area (4 MW SRAM)
0XFFFFFF
Bank0
Bank1
Bank2
Bank509
Bank 510
8000H
Internal PRAM
Com1
Com0
N wait cycles area (R0M)
0000H
1 wait cycle area (4KW SRAM)
+
BANK


017FFF
01FFF
FFFF
BANK 0
BANK 1
BANK 2
32KW
8000
010000
018000
4KW
Internal SRAM
COM1
6FFF
COM0
Reset Vector
0000
FFFFF F
Bank 510
Ext. SRAM
4MW (CS3_n)
C00000
BFFFF F
Bank 382
ROM
4MW (CS2_n)
80000
7FFFF F
Bank 254
ROM
4MW (CS1_n)
40000
3FFFF F
Bank 126
CS4_n
Bank0
4MW (CS0_n)
007000
COM1
000000
COM0

6.3.2 Data RAM

The following Figure shows how the eDSP Data RAM Memory is organized. The six different addressing modes for the data memory are: 16-bit direct, 8-bit direct, Indirect with Displacement, Indirect, Indirect with Post-decrement, and Indirect with Post-increment.

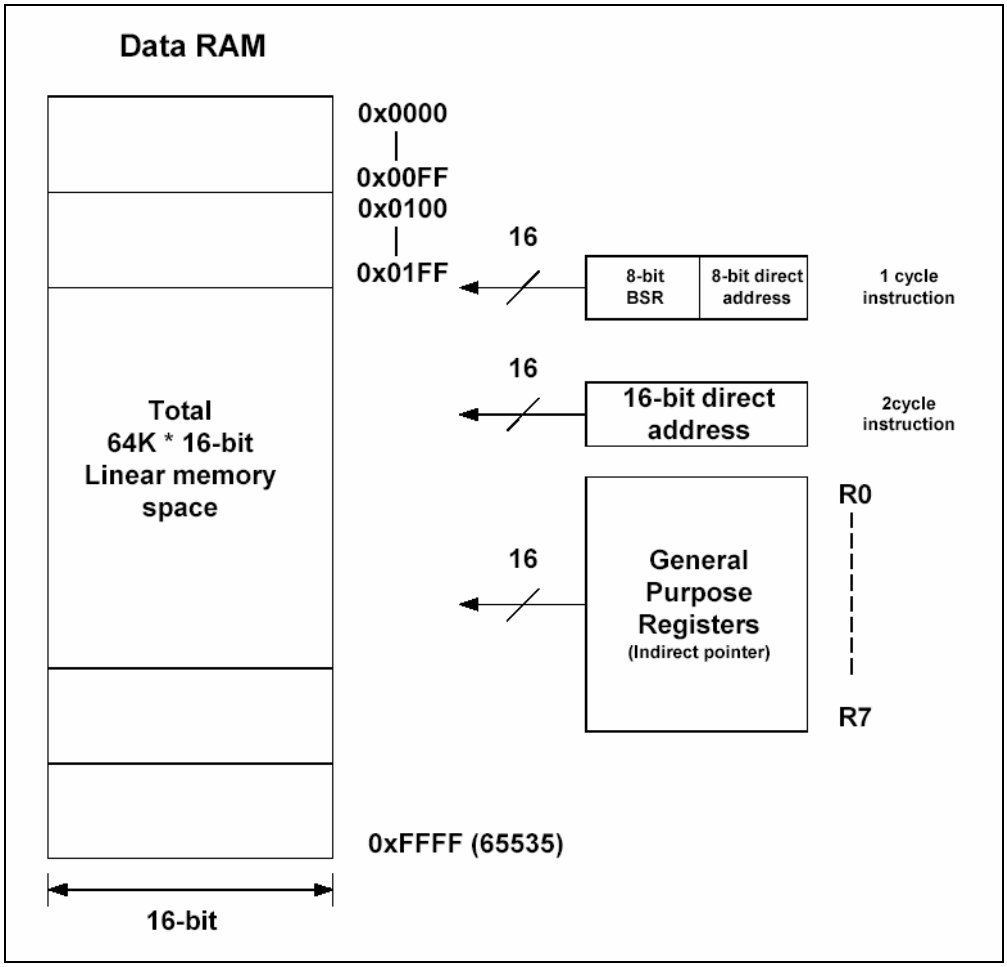


Figure 6-2 EMG2000A Data RAM Memory Diagram

The EMG2000A has an embedded 24KW data RAM; check the next diagram for details on the RAM arrangement.

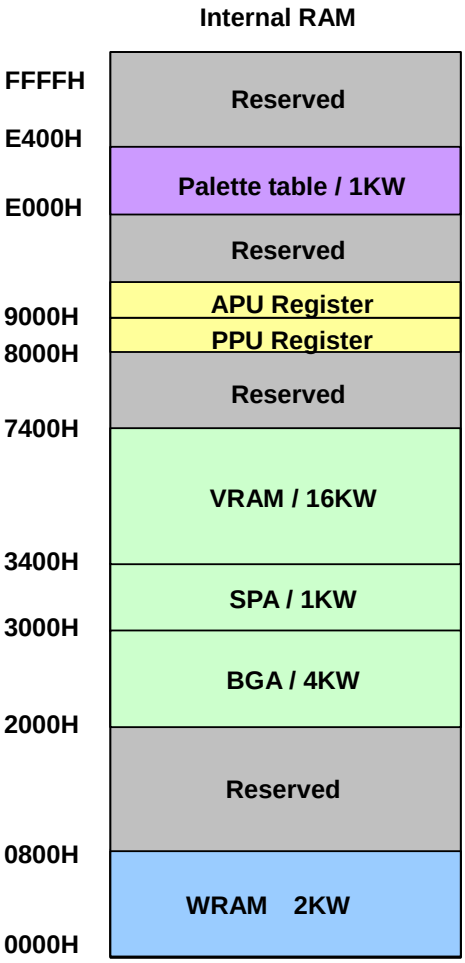


Figure 6-3 EMG2000A Internal Data RAM Memory Diagram

6.3.3 I/O RAM

There are 128 words I/O RAM reserved for the system registers, which could only be accessed by special addressing mode. Besides the original system registers, almost MPU special function registers and TV encoder, ADSR, and DMA special function registers are also allocated in this memory area. For details, refer to the system registers description.

6.4 I/O Ports

The eMG2000A supports three ports, 36 bits multi-function GPIO, Port A is 16 bits, Port B is 8 bits, and Port C is 12 bits. The initial state for multi-function GPIO is GPIO, and all special functions are disabled. The 2nd special function for each GPIO pins is only available when the corresponding function is set correctly with correct GPIO input or output assigned. For example, PA[6] will be RxD, UART receiving data pin, only when UART is enabled and PA[6] is set as input mode. The following is the entire GPIO multi-function reference table.

Port A Multi-Function Reference Table

Port A	Function		I/O Capability				
	First	Second	Pull-up	Pull Down	Option Current	Schmitt	Wake-up
PA[15]	GPIO	SCK	✓	✓	✓	✓	✓
PA[14]	GPIO	MISO	✓	✓	✓	✓	–
PA[13]	GPIO	MOSI	✓	✓	✓	✓	–
PA[12]	GPIO	/SS	✓	✓	✓	✓	–
PA[11]	GPIO	TEXI3	✓	✓	✓	✓	–
PA[10]	GPIO	TEXI2	✓	✓	✓	✓	–
PA[9]	GPIO	TCCP3	✓	✓	✓	✓	✓
PA[8]	GPIO	TCCP2	✓	✓	✓	✓	✓
PA[7]	GPIO	Light_Gun	✓	✓	✓	✓	–
PA[6]	GPIO	RXD	✓	✓	✓	✓	✓
PA[5]	GPIO	TXD	✓	✓	✓	✓	–
PA[4]	GPIO	–	✓	✓	✓	✓	–
PA[3]	GPIO	EXTI1	✓	✓	✓	✓	✓
PA[2]	GPIO	EXTI0	✓	✓	✓	✓	✓
PA[1]	GPIO	PWM1	✓	✓	✓	✓	–
PA[0]	GPIO	PWM0	✓	✓	✓	✓	–

Port B Multi-Function Reference Table

Port B	Function		I/O Capability				
	First	Analog In	Pull Up	Pull Down	Option Current	Schmitt	Wake-up
PB[7]	GPIO	AD[7]	✓	✓	✓	–	✓
PB[6]	GPIO	AD[6]	✓	✓	✓	–	✓
PB[5]	GPIO	AD[5]	✓	✓	✓	–	✓
PB[4]	GPIO	AD[4]	✓	✓	✓	–	✓
PB[3]	GPIO	XP/AD[3]	✓	✓	✓	–	✓
PB[2]	GPIO	XN/AD[2]	✓	✓	✓	–	✓
PB[1]	GPIO	YP/AD[1]	✓	✓	✓	–	✓
PB[0]	GPIO	YN/AD[0]	✓	✓	✓	–	✓

Port C Multi-Function Reference Table

Port C	Function			I/O Capability				
	First	CCIR601	CSTN/Second	Pull Up	Pull Down	Option Current	Schmitt	Wake-up
PC[13]	GPIO	–	EXTI3	✓	✓	✓	✓	✓
PC[12]	GPIO	–	EXTI2	✓	✓	✓	✓	✓
PC[11]	GPIO	CLK27_O	WRB	✓	✓	✓	✓	–
PC[10]	GPIO	HS_O	–	✓	✓	✓	✓	–
PC[9]	GPIO	VS_O	–	✓	✓	✓	✓	–
PC[8]	GPIO	–	–	✓	✓	✓	✓	–
PC[7]	GPIO	VDO[7]	VDO[7]	✓	✓	✓	✓	–
PC[6]	GPIO	VDO[6]	VDO[6]	✓	✓	✓	✓	–
PC[5]	GPIO	VDO[5]	VDO[5]	✓	✓	✓	✓	–
PC[4]	GPIO	VDO[4]	VDO[4]	✓	✓	✓	✓	–
PC[3]	GPIO	VDO[3]	VDO[3]	✓	✓	✓	✓	–
PC[2]	GPIO	VDO[2]	VDO[2]	✓	✓	✓	✓	–
PC[1]	GPIO	VDO[1]	VDO[1]	✓	✓	✓	✓	–
PC[0]	GPIO	VDO[0]	VDO[0]	✓	✓	✓	✓	–

6.5 Watchdog Timer

The eMG2000A has an internal Basic Timer/Watchdog Timer. This kind of timer can be used to resume the controller operation when it is disturbed due to noise, system error, or other kinds of malfunction. To have a Watchdog Timer configuration, the overflow signal from the 4-bit prescaler should be fed to the clock input of the 8-bit Watchdog Timer as shown in the figure below. User can enable or disable the Watchdog Timer by software, i.e., by controlling the configuration in WDTEN bit. If users do not want to use the Watchdog Timer configuration, the 4-bit Basic Timer can only be used as a normal interval timer to request an interrupt service.

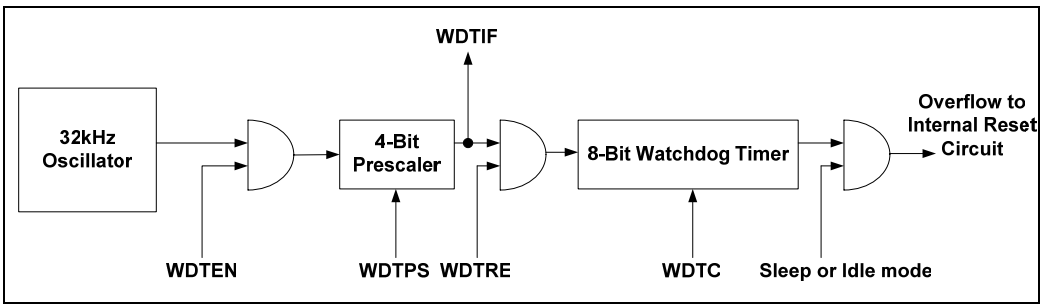


Figure 6-4 EMG2000A Basic Timer/Watchdog Timer Diagram

6.6 Real Time Counter

The Real Time Counter can generate the necessary time delay for a stable clock from 32K oscillator circuit.

- **Real Time Clock and Interrupt**

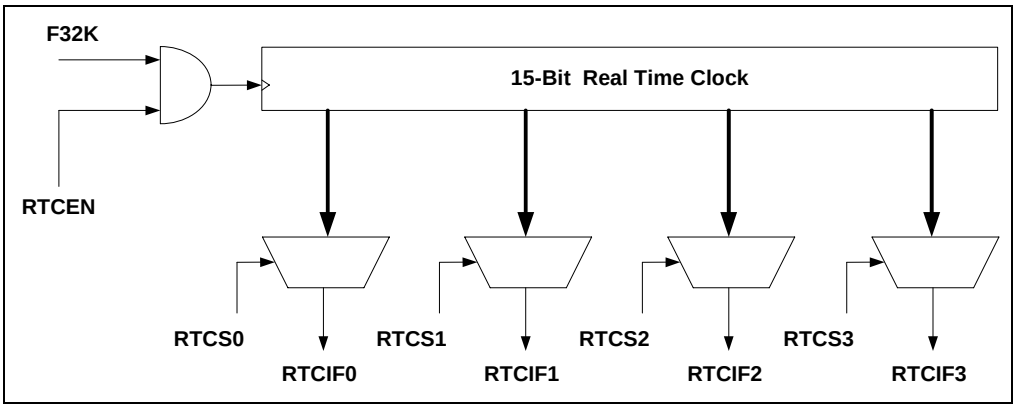


Figure 6-5 EMG2000A Real Time Counter Diagram

6.7 Timer/Counter

Timer 0 and Timer 1 are 8-bit timers that operate in “Auto Reload Mode”. Each timer can be independent with different counting rates. These General timers are used for counting time.

- **Functional Block Diagram:**

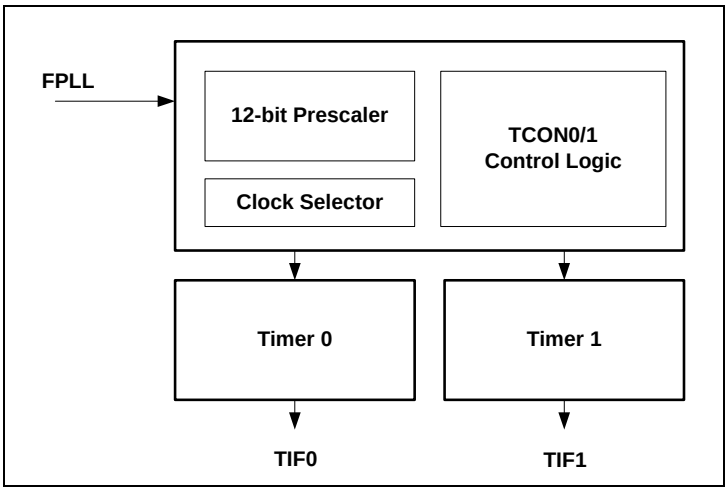


Figure 6-6 EMG2000A Timer/Counter Block Diagram

Timer 2 and Timer 3 are 8-bit timers that operate in Capture and compare mode. Each timer can be independent with different counting rates and operation modes. The two 8-bit timers can be combined to form a 16-bit timer. These Multi-function timers are used for counting events, counting time, measuring frequency (capture function) and generating analog-like outputs (PWM).

- **Block Diagram**

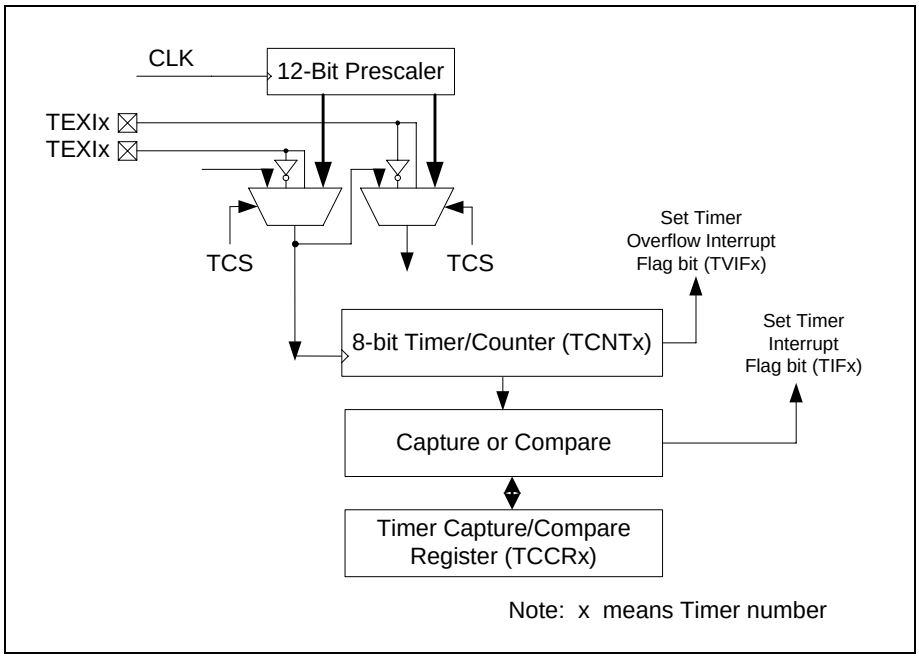


Figure 6-7 EMG2000A Timer/Counter Block Diagram

6.8 Serial Peripheral Interface (SPI)

- **Features**

  - Four external pins: MOSI, MISO, SCK, and /SS. All four pins can be used as GPIO, if the SPI module is not used.
  - Two operational modes: Master and Slave
  - Baud rate: 256 different programmable baud rates
  - Data Word length: 8 or 16 bits. Data must be left-justified when written to transmit buffer register. Data read back from receive buffer register is right-justified.
  - Full duplex: Simultaneous receive and transmit operation
  - Clocking: Four programmable clocking schemes (controlled by clock polarity and clock phase bits)
  - Interrupt/polling: Transmit and receive operations are accomplished through either interrupt-driving or polling.

- **Block Diagram**

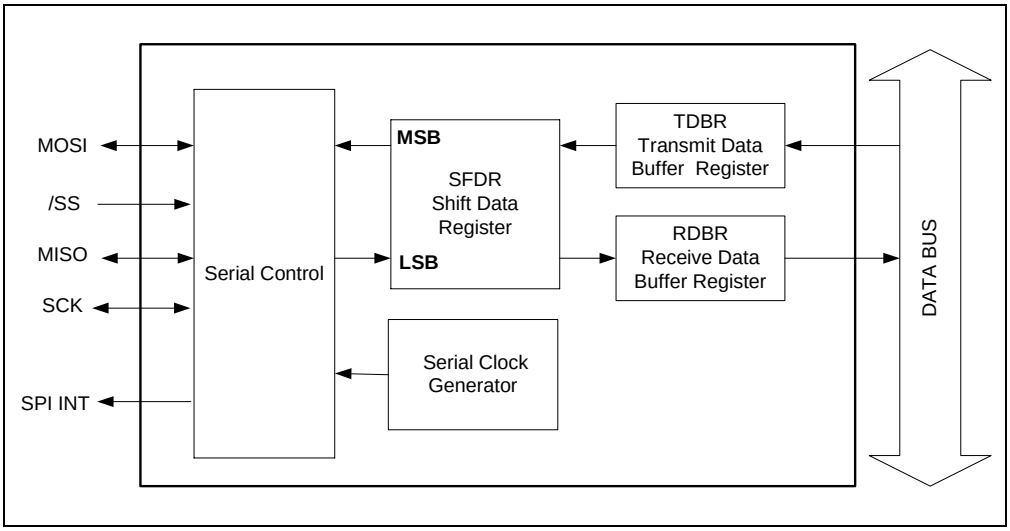


Figure 6-8 EMG2000A SPI Functional Block Diagram

6.9 PPU

The PPU block is designed for graphic data processing. There are two kinds of picture data that needs to be processed. One is the sprite pattern and the other is the background. The data structure of the sprite and background are well defined and can be accessed from the external ROM. The application software determines whether to display one pixel coming from the sprite information or the background information.

6.9.1 Functional Block Diagram

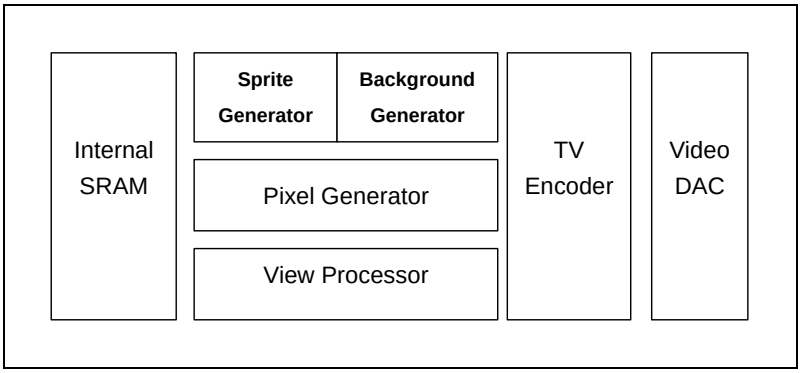


Figure 6-9 EMG2000A PPU Functional Block Diagram

6.9.2 Background Generator

The size of a background picture is 320×240. A single picture is composed of 1200 units. For a picture composed of 1200 units, one unit has 8 (pixels) × 8 (pixels) patterns (tiles). For a picture composed of 300 units, one unit has 16 (pixels) ×16 (pixels) patterns (tiles). The color ability for one screen is 256 colors. The pattern size can be: 8×8 and 16×16.

The color ability for one pattern is programmable. There are two backgrounds for this EMG2000A device. One is text mode and the other can be text mode or graphic mode. The background can be scrolled pixel by pixel in text mode with setting the X and Y coordinate parameters. The scrolling direction is from Up to Down and Left to Right.

The application can divide the background picture to 8 sub-screen areas in text mode for BG1 and 3 sub-screen areas for BG2. User can specify 7/2 Y coordinate value for setting 8/3 sub-screen areas. Each sub-screen can scroll left or scroll right independent with different direction and speed.

6.9.3 Sprite Generator

The sprite pattern is composed of 16 different kinds of pattern sizes: 8×8 to 64×64.

The color ability for the sprite pattern is programmable, but it always uses 8 bits for one pixel. There are a maximum of 31 sprite patterns (8×8 pixels) for each line, and the maximum sprite number on one screen is 256.

Some special effects for the sprite pattern in graphic mode:

a. Mirror: User can make the sprite pattern with left, right, up or down mirror effect
b. Zoom In/Out: User can make the sprite pattern with 16 steps zoom in/out effect.
c. Rotation: User can make the sprite pattern with 24 steps rotation degrees.

There are a total of 8 priorities for different sprite pattern layers (including two background layers).

6.9.4 Pixel Generator

The pixel generator block will receive the sprite pattern characteristics of the sprite generator and the background pattern characteristics of the background generator. The information includes:

a. Palette color

b. Priority

c. Display mode

d. Pattern index,

e. Size

f. Scrolling factor

g. Attribute mode

This block will calculate the exact pixel address information of the ROM depending on these characters.

6.9.5 View Processor

The view processor block processes the display pixel information before issuing the digital color code to TV encoder. There is a color effect processing circuit which can change the final display color. This circuit can change the pixel palette code by specifying a rectangle area. The pixel palette codes in the area can be changed by the MPU application. There are four kinds of methods to change the pixel color:

a. MPU setting a constant value

b. Decrease the saturation and luminance value to one half of the original color code

c. Reverse the polarity of color such as a positive to a negative.

d. Specify a color change to another color

6.9.6 Internal SRAM

There are two kinds of embedded memory for this EMG2000A device. The first is for the MPU program and data memory usage, the accessing space is 2K words. The second is for the PPU and APU usage, it is 22K words.

For the PPU, the usage is target for the:

a. Background buffering

b. Sprite buffering

c. Palette buffering

d. Line buffering

The background and sprite buffer use the same memory as the MPU application memory space. The total size is 24K words.

6.9.7 TV Encoder

After receiving the digital color data from the view processor, the TV encoder will emerge the synchronization signal and the color burst signal for composite video. The sub-carrier generator block will generate the different color burst codes. The two color burst code will match to the two TV systems (NTSC and PAL) with two different color burst frequencies:

a. Color burst of NTSC : 3.58 MHz

b. Color bust of PAL : 4.43 MHz

The sync multiplex block will combine the digital color code with the horizontal sync. The color burst multiplex will combine the color burst signal with the digital color data and the horizontal sync. Considering the PAL line alternative characteristic, the hue reverse circuit covers the line alternative phase change effect.

The digital color data use the YCbCr domain to represent the pixel color information. The TV encoder is designed to combine these three color dimension codes to generate the target composite video. With the waveform ROM block, the digital data can be modulated to analog signal with color burst frequency.

6.9.8 Video DAC

The video DAC will convert the digital composite signal to analog composite signal.

6.10 APU

The APU block is designed for the audio data processing. There are two kinds of audio data that needs to be processed. One is the PCM audio data. The other is the ADSR (Envelope Control) audio data.

The EMG2000A device uses a PCM encoder and decoder to play and record the nature music and voice. The decoded PCM is written on the external ROM device. These will be played back by the MPU application via the adequate starting address setting and the playback length setting. After the material is decided, the left and right DAC will convert the digital PCM audio bit-stream to analog audio signal. The parameters that need to be set are:

a. Channel Starting Address

b. Channel Playback Length

c. Channel Selection

d. Output channel Setting

The analog audio source can be converted by the ADC. Then after setting the MPU proper recording parameters, the converted digital audio data will be encoded by the PCM encoder engine and will be recorded in the external SRAM memory devices.

The ADSR Envelope Control audio source is generated by the MPU application. This ADSR Envelope Control engine provides some parameter registers to let the MPU change these parameters:

e. Envelope Shape Setting

f. Tone Shape Setting

g. Envelop Frequency setting

h. Tone Frequency setting

i. Separate 16 Channel Voice Output Select

6.10.1 Function Block Diagram

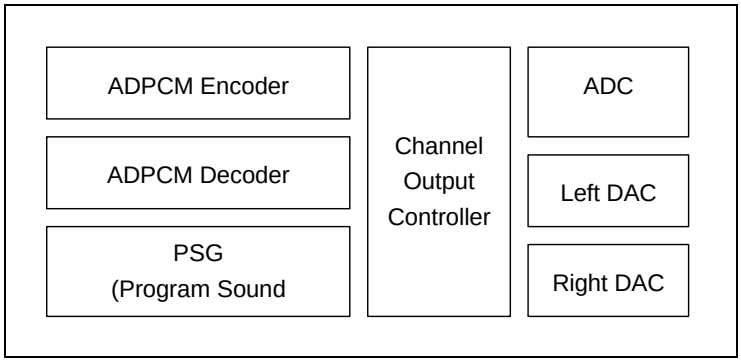


Figure 6-10 EMG2000A APU Functional Block Diagram

6.10.2 PCM Decoder

The PCM decoder decodes the raw PCM audio bit-stream. The PCM bit-stream is 6, 8, 10 bits multi-data bit rate with 8kHz, 12kHz, 16kHz, 20kHz, 24kHz multi-sample rate. That means the data rate is variable.

There are eight PCM decoding channels for the EMG2000A. The MPU can set the starting address for each channel and set the playback length.

This PCM decoder is composed of multi-data rate and multi-sample rate audio bit-stream. There is a buffer for PCM decoder buffering purpose. The eight channels can be set up as left or right channel by the MPU. Each Channel has its own volume control engine to separately control the PCM volume.

6.10.3 PCM Encoder

The PCM encoder encodes the digital PCM data. The encoded bit-stream is 4-bit data rate with 8kHz sampling rate. That means the data rate for the encoded bit-stream is 64Kbps.

There is a starting point detection circuit for audio starting point detection. This will save the external memory device requirement for the case of recoding application. The encoded data can be directly added to the PCM decoding output in digital domain. That means if the encoding function is enabled, the external analog source can be mixed with the internal encoded PCM bit-stream.

6.10.4 ADSR (Envelope Control Generator)

The ADSR is a music generation device. It only requires the MPU to initialize its register array, thus reducing the load on the MPU. Music generation is carried out by the 16 separate ADSR voice generators. This allows for the generation of music, special effects, warnings, and various other types of sounds. All functions of the ADSR are controlled by the internal registers. The MPU need only write data to the internal ADSR registers. The ADSR has its own volume control engine to control the volume of every channel, and the ADSR itself generates the sound.

a. Envelope Shape Generator: Different music waves having different Envelope Shapes are generated for each channel (16 channels).

b. Tone Shape Generator: Different music waves having different Envelope Shapes are generated for each channel (16 channels).

c. Mixer: Separate 16 channels Voice output can be mixed separately to the left or right DAC Audio channels by the mixer.

d. Envelope Frequency Generator: Different music waves having different Envelope Frequency are generated for each channel (16 channels).

e. Tone Frequency Generator: Different music waves having different Tone Frequency are generated for each channel (16 channels).

6.10.5 Channel Output Controller

There are a total of 8 channels for the PCM audio source, 1 channel for the analog source, and the ADSR 16 sound channels. The channel output controller can provide variable channel output combination for the different PCM channel to form two audio channel output. These combinations are dependent on the MPU application setting.

6.10.6 ADC

The ADC is designed for the external analog input signal conversion. There are two applications for this ADC. One is dedicated for the audio PCM encoding purpose. Another is to be used as a general analog device input signal conversion.

There is a built-in analog 8-to-1 MUX for the general analog device application. The MPU can toggle the ADC clock and enable signals by register setting and can also read the ADC digital data input via the data register.

6.10.7 Left DAC and Right DAC

The left DAC and the right DAC are design for conversion of the digital PCM decoded data. These converted data can be a combination of the 8 PCM decoding channels, 1 PCM encoding channel or the 16 ADSR music channels.

7 DC Electrical Characteristics

Condition: D_VDD = V_VDD = A_VDD = 2.4V~3.6V, Ta = -10°C to +80°C, Typical values at TA = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Unit	Conditions	
Clock							
Crystal Oscillator	F_{CLK}	–	27	–	MHz	NTSC	–
		–	27	–	MHz	PAL	–
	F_{CLK}	–	6	–	MHz	NTSC (PLL mode)	–
		–	6	–	MHz	PAL (PLL mode)	–
Digital Input							
Input Voltage High (Programmable)	V_{IH1}	0.8D_VDD	–	D_VDD	V	GPIO_A[15:0], GPIO_B[7:0], GPIO_C[11:0]	–
Input Voltage Low (Programmable)	V_{IL1}	D_VSS	–	0.2D_VDD	V		
Input Threshold Voltage (Schmitt Trigger) (Programmable)	V_{T+}	–	2.1	2.5	V	GPIO_A[15:0], GPIO_B[7:0], GPIO_C[11:0]	–
	V_{T-}	–	0.9	1.2	V		
Input Leakage Current (Programmable)	I_{IN}	–	–	±1	µA	All Input pins (without pull up / pull down resistor), Vin = D_VDD or D_VSS	
Pull-up Resistor	R_{PU}	–	75	–	KΩ	Nrst, VRC, TRST, TCK, TMS, TDI@ D_VDD=3.3	–
Pull-down Resistor	R_{DOWN}	–	75	–	KΩ	TESTN[1:2]@ D_VDD=3.3	–
Pull-up Resistor (Programmable)	R_{PU}	–	75	–	KΩ	GPIO_A[15:0], GPIO_B[7:0] GPIO_C[13:0] @ D_VDD=3.3	–
Pull down Resistor (Programmable)	R_{DOWN}	–	75	–	KΩ	GPIO_A[15:0], GPIO_B[7:0] GPIO_C[13:0] @ D_VDD=3.3	–
Digital Output							
Digital Output Voltage High	V_{OH}	0.8D_VDD	–	D_VDD	V	–	–
Digital Output Voltage Low	V_{OL}	D_VSS	–	0.2D_VDD	V	–	–
Digital Output Current	I_{OH1}	–	-2	–	mA	VOH=2.4V	D_VDD=3.0V nCS[4:0], A[23:0] D[16:0], nRD, nWR, SYNC, CLOCK_OUT, TDO
	I_{OL1}	–	2	–	mA	VOL=0.2V	–
Digital Output Current (Programmable)	I_{OH2}	-4	–	-16	mA	VOH=2.4V	D_VDD=3.0V, GPIO_A[15:0] GPIO_B[7:0] GPIO_C[13:0]
	I_{OL2}	4	–	16	mA	VOL=0.4V	–

Condition: D_VDD = V_VDD = A_VDD = 2.4V~3.6V, Ta = -10°C to +80°C, Typical values at TA = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Unit	Conditions
Analog Input (for 10 bits ADC)						
Input Voltage (Peak to Peak); VTOP-VBOT	V_{PP}	0.9	1.1	1.3	V	–
Input Voltage-Top	V_{TOP}	1.8	1.9	2.0	V	–
Input Voltage-Bottom	V_{BOT}	0.7	0.8	0.9	V	–
Input Leakage Current	I_{IN}	-	-	±1	µA	AI[7:0]=VBOT to VTOP
Analog Output (ALO/ARO/CVO)						
Output Voltage (Peak to Peak); VTOP-VBOT	V_{PP}	0.9	1.1	1.3	V	Full-Scale Output V_VDD=2.2V, RL=5K
Output Voltage-Top	V_{TOP}	1.8	1.9	2.0	V	Full-Scale Output V_VDD=2.2V, RL=5K
Output Voltage-Bottom	V_{BOT}	0.7	0.8	0.9	V	Zero-Scale Output V_VDD=2.2V, RL=5K
Output Leakage Current for Voltage DAC	I_{OUT}	–	–	1	µA	Full-Scale V_VDD=2.2V, PDS = 1; RL=5K
ALO/ARO						
Resolution	N	–	10	–	Bits	–
Integral Nonlinearity	INL	–	±0.25	±1	LSB	–
Differential Nonlinearity	DNL	–	±0.25	±1	LSB	–
Offset Error	–	–	±1	±4	%	Compare to FS*
Full-Scale (Gain) Error	–	–	±2	±6	%	Compare to FS*
CVO						
Resolution	N	–	10	–	Bits	–
Integral Nonlinearity	INL	–	±0.25	±1	LSB	–
Differential Nonlinearity	DNL	–	±0.25	±1	LSB	–
Offset Error	–	–	±1	±4	%	Compare to FS*
Full-Scale (Gain) Error	–	–	±2	±6	%	Compare to FS*
Power Noise Immunity						
Power Noise Immunity (Peak to Peak) (for 10 bits DAC:ALO/ARO)	PNI_{PP1}	0.5	1	2	LSB	A_VDD=A_VDD'+ Single Tone Noise @ 10% A_VDD'; Condition: D[9:0]=256/128/0 Tone=64K/32K/8K/1K/ 100/ 60/50Hz
Power Noise Immunity (Peak to Peak) (for 10 bits DAC : CVO)	PNI_{PP2}	0.1	0.3	0.5	LSB	V_VDD=V_VDD'+ Single Tone Noise @ 10% V_VDD'; Condition: D[9:0]=63/31/0 Tone=5M/1M/50K/5K/50Hz

Note: FS* - Full Scale

Condition: D_VDD = V_VDD = A_VDD = 2.4V~3.6V, Ta = -10°C to +80°C, Typical values at TA = +25°C

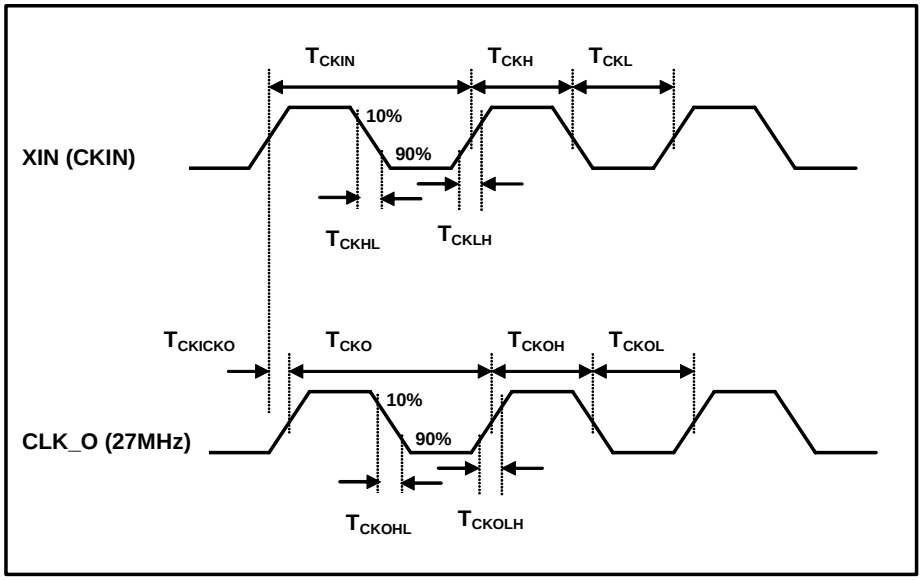
Parameters	Sym.	Min.	Typ.	Max.	Unit	Conditions
Power Requirement						
Analog Power-Supply Voltage (For Video)	V_{VDD}	2.4	3.0	3.6	V	–
Analog Supply Current (For Video)	IV_{VDD}	–	4	5	mA	PDS = 0, V_VDD=3.0 No Loading
Analog Standby Current (For Video)	IV_{STB}	–	0.5	1	µA	Power_Down Mode V_VDD=3.0
Analog Power-Supply Voltage (For Audio)	AVDD	2.4	3.0	3.6	V	–
Analog Supply Current (For Audio)	IAVDD	–	1	2	mA	PDS = 0, A_VDD=3.0 No Loading
Analog Standby Current (For Audio)	IASTB	–	0.5	1	µA	Power_Down Mode A_VDD=3.0
Digital Power-Supply Voltage	DVDD	2.4	3.0	3.6	V	–
Digital Supply Current	IDVDD	–	50	70	mA	PDS = 0, D_VDD=3.0 No Loading
Digital Standby Current	IDSTB	–	4	6	µA	Power_Down Mode D_VDD=3.0

8 AC Electrical Characteristics

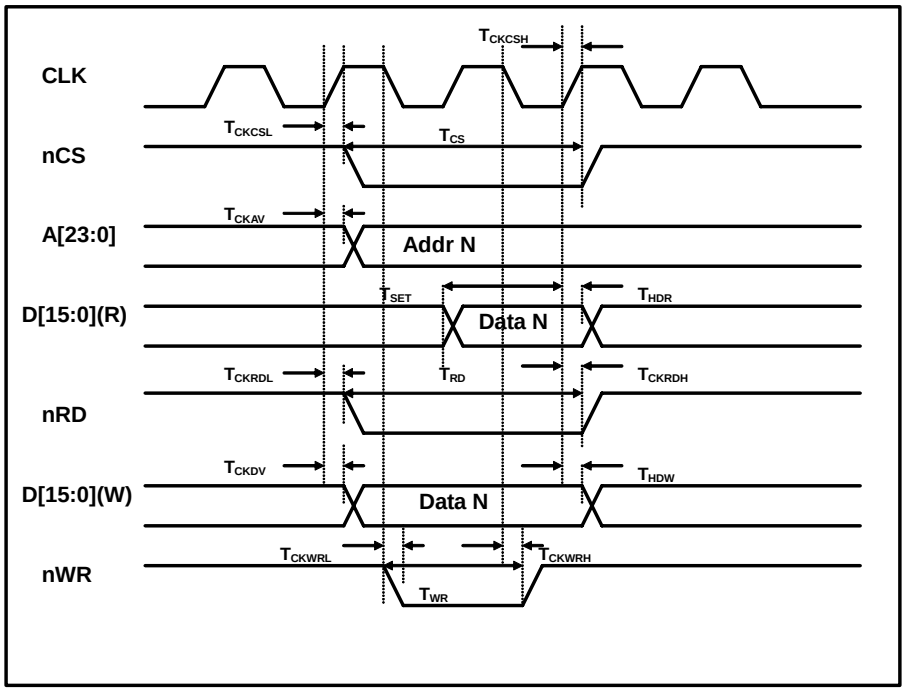
Condition: AVDD = VVDD = DVDD = 3V±0.3, Ta = -10°C to +80°C, Typical values at TA= +25°C

Parameters	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Input (XIN)						
Clock Frequency	Fclk	27M-1K	27	27M+1K	Hz	–
Clock Cycle	TCKIN	37.0	37	37.04	ns	–
Clock High Time	TCKH	14.5	18.5	22.2	ns	–
Clock Low Time	TCKL	14.5	18.5	22.2	ns	–
Clock Output (CLK_O)						
Clock Frequency	FclkO	27M-135	27	27M+135	Hz	27 MHz Output Mode
Clock Cycle	TCKO	37.0	37	37.04	ns	27 MHz Output Mode
Clock Rise Time	TCKOHL	3	5	7	ns	27 MHz Output Mode
Clock Fall Time	TCKOLH	3	5	7	ns	27 MHz Output Mode
Clock High Time	TCKOH	14.5	18.5	22.2	ns	27 MHz Output Mode
Clock Low Time	TCKOL	14.5	18.5	22.2	ns	27 MHz Output Mode
Gated Clock Output Delay	TCKICKO	1	5	10	ns	27 MHz Output Mode
Memory Bus						
Clock High to Chip Select Low	TCKCSL	–	13	18	ns	–
Clock High to Chip Select High	TCKCSH	–	13	18	ns	–
Clock High to Address Valid	TCKAV	–	13	18	ns	–
Chip Select Access Cycle	TCS	74	148	185	ns	Cycle = 2T = 74ns Cycle = 3T = 111ns Cycle = 4T = 148ns Cycle = 5T = 185ns
Read Data Setup Time	TSET	–	3	5	ns	–
Read Data Hold Time	THDR	–	3	5	ns	–
Clock High to Read Strobe Low	TCKRDL	–	13	18	ns	–
Clock High to Read Strobe High	TCKRDH	–	13	18	ns	–
Read Strobe Access Cycle	TRD	74	148	185	ns	Cycle = 2T = 74ns Cycle = 3T = 111ns Cycle = 4T = 148ns Cycle = 5T = 185ns
Clock High to Write Data Valid	TCKDV	–	13	18	ns	–
Write Data Hold Time	THDR	–	3	5	ns	–
Clock High to Write Strobe Low	TCKWRL	–	13	18	ns	–
Clock High to Write Strobe High	TCKRWH	–	13	18	ns	–
Write Strobe Access Cycle	TWR	74	148	185	ns	Cycle = 2T = 74ns Cycle = 3T = 111ns Cycle = 4T = 148ns Cycle = 5T = 185ns

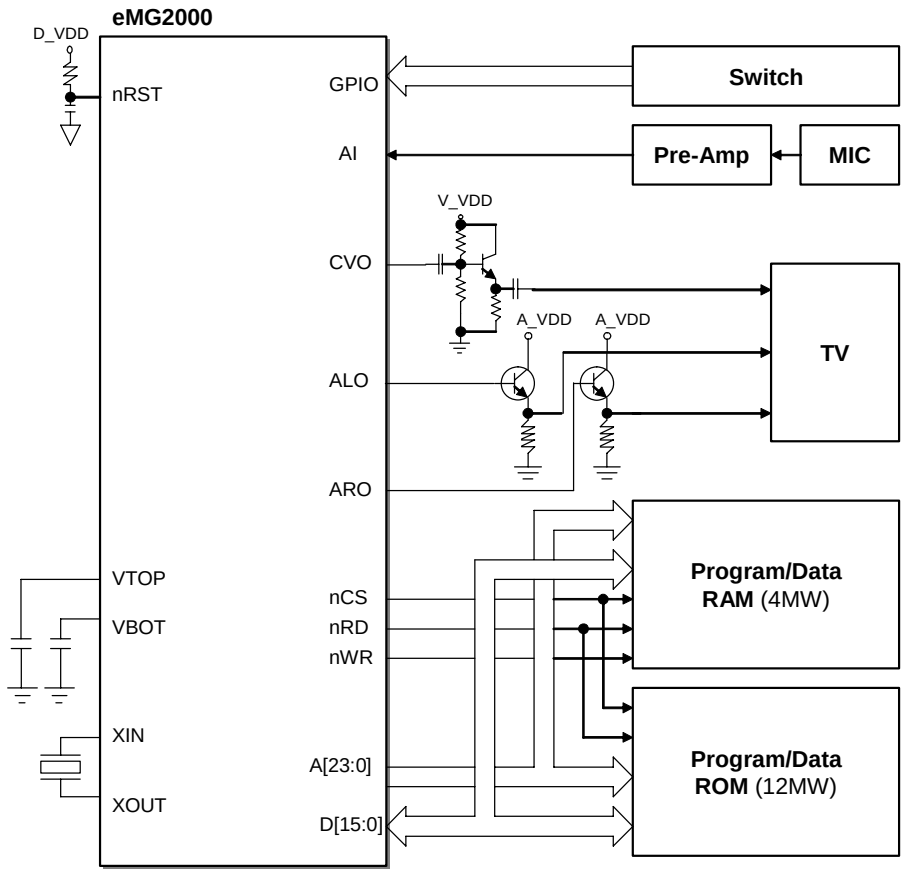
8.1 Clock



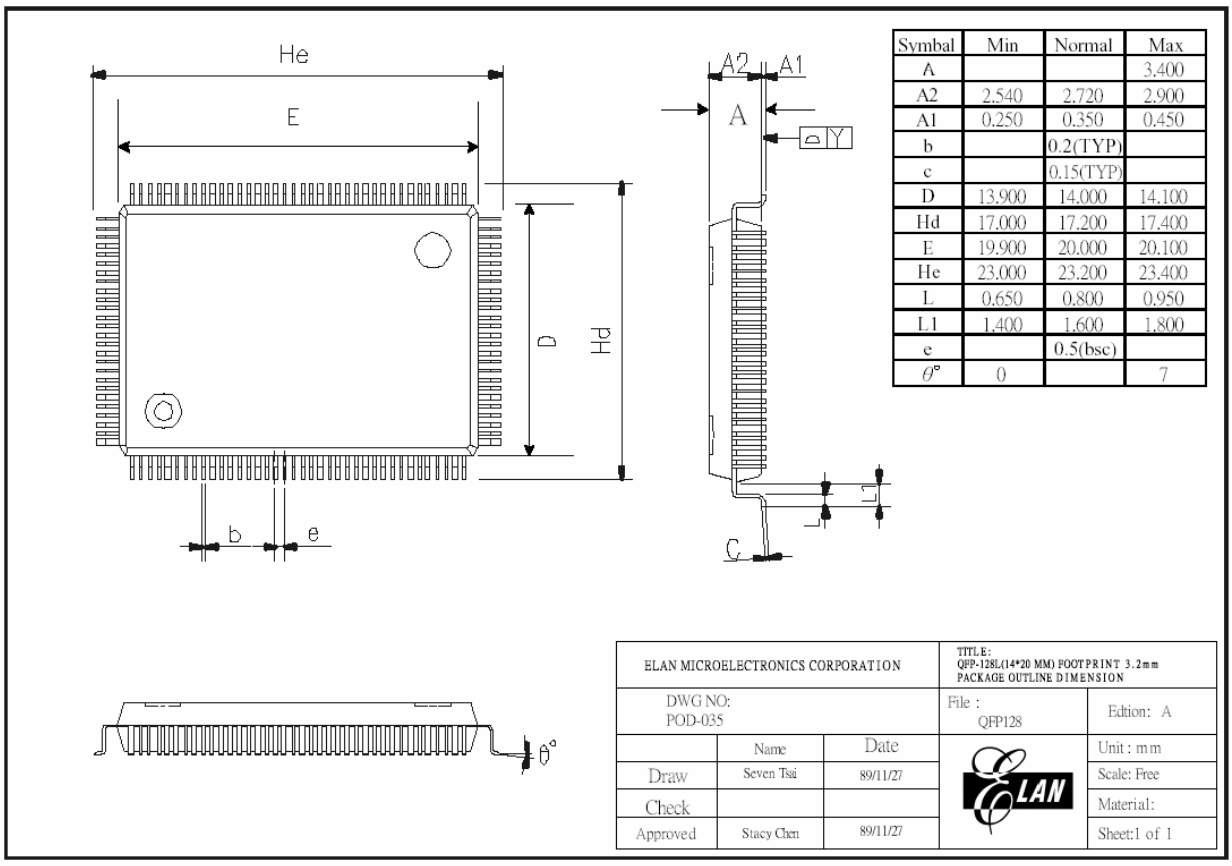
8.2 Memory Access (With 1 Wait Cycle)



9 Application Circuit



10 Package Information



Symbal	Min	Normal	Max
A			3.400
A2	2.540	2.720	2.900
A1	0.250	0.350	0.450
b		0.2(TYP)	
c		0.15(TYP)	
D	13.900	14.000	14.100
Hd	17.000	17.200	17.400
E	19.900	20.000	20.100
He	23.000	23.200	23.400
L	0.650	0.800	0.950
L1	1.400	1.600	1.800
e		0.5(bsc)	
θ°	0		7

ELAN MICROELECTRONICS CORPORATION			TITLE: QFP-128L(14*20 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
DWG NO: POD-035			File : QFP128	Edition: A
	Name	Date		Unit : mm
Draw	Seven Tsai	89/11/27		Scale: Free
Check				Material:
Approved	Stacy Chen	89/11/27		Sheet:1 of 1