ePVP6300

VFD Controller

Product Specification

DOC. VERSION 2.0

ELAN MICROELECTRONICS CORP.

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Contents

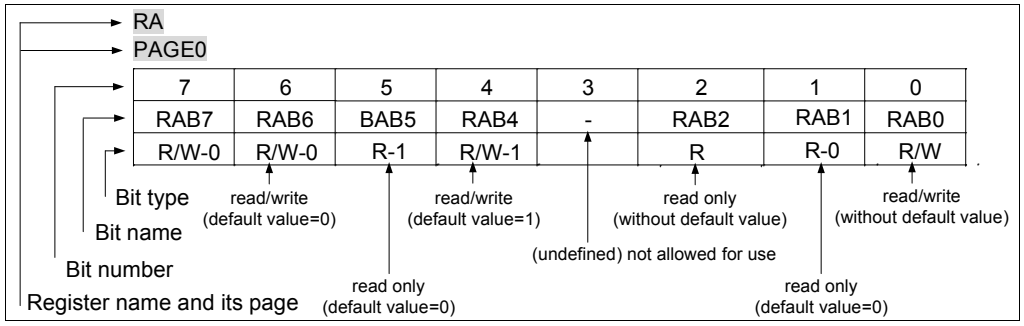
Specification Revision History

Version	Revision Description	Date
1.0	Initial version	2003/6/15
1.4	1. Revised Display control command 2. Revised the external interrupt function (Ports 9, 0 ~ Ports 9, 4)	2004/1/16
1.5	1. Revised the error description 2. Added SPI function timing diagram 3. Revised the display Segment Data Buffers for stored registers	2004/3/24
1.6	1. Revised the error description 2. Added bonding coordinates subsidiary	2004/4/26
1.7	1. Added Relevant Pins on the Pin Assigment section 2.Added Package Information 3. Revised the DC Electrical Characteristics 4. Revised the CPU Feature Description	2004/06/23
1.8	1. Added additional remarks about the SPI function 2. Modified the Package Information	2004/8/10
1.9	1. Added additional remarks on the Application Notes	2004/9/16
1.91	1. Revised the CONT register description 2. Updated the Package Information	2004/9/24
1.92	1. Changed the IC name 2. Revised the Operation Voltage Vs PLL Operation frequency	2004/11/4
1.93	1. Modified the Package Information	2005/1/7
2.0	1. Deleted some information that are not necessary for ePVP6300. 2. Modified the Main Clock max. to 10.747 MHz.	2011/07/05

Read Me First!

Before using the chip, spare a few minutes to take a look at the following important notes.

1. Some bits in the registers are undefined. The values in these bits are unknown and should not be used. These bits are designated with a dash "–" symbol as its bit name in this specification.
2. The following table shows the definitions of the various register designations used to identify bit types, bit name, and bit number. Some definitions will appear quite frequently in the specification.



1 General Description

The ePVP6300 is an 8-bit RISC architecture Vacuum Fluorescent Display (VFD) controller with low power consumption and high speed CMOS technology. This integrated single IC has an on-chip Watchdog Timer (WDT), one-time programmable ROM (OTP), data RAM, programmable real time clock/counter, internal interrupt, power down mode, built-in 4-wire SPI, 10-bit A/D converter, IR detector, and high voltage output for VFD application.

2 Features

2.1 CPU

- Clock source : Crystal Oscillator or RC Oscillator
- Crystal Oscillator : 32.768kHz with external crystal
- RC Oscillator : 32kHz with an external 470 KΩ resistor
- 16k×13 on-chip Program ROM
- 256×8 on-chip Data RAM
- 144×8 General Purpose Registers
- 16-level stacks for subroutine nesting
- 13 interrupt sources : 5 external (IR, INT1~INT4)
  8 internal (SPI, ADC, TCC, Counters 1~5)
- 5 channels 8-bit counters: real time clock/counter (TCC), Counter 1, Counter 3, Counter 4, Counter 5
- 1-channel 16-bit counter : Counter 2
- On-chip Watchdog Timer (WDT)
- Single instruction cycle commands
- Four operating modes : Sleep mode, Idle mode, Green mode, Normal mode

Mode	CPU Status	Main Clock	32.768kHz Clock Status	Description
Sleep mode	Turn off	Turn off	Turn off	RA(6) = 0 RA(7) = 0 + "SLEP" instruction
Idle mode	Turn off	Turn off	Turn on	RA(6) = 0 RA(7) = 1 + "SLEP" instruction
Green mode	Turn on	Turn off	Turn on	RA(6) = 0
Normal mode	Turn on	Turn on	Turn on	RA(6) = 1

* The Main clock can be programmed from 447.829kHz to 10.747 MHz by internal PLL.
* Six main clocks: 447.829K, 895.658K, 1.791M, 3.582M, 7.165M, 10.747M

2.2 SPI

- Serial interface for Clock, Data Input, Data Output, and Strobe pins

2.3 GPIO

- GPIO 9 Port (8-bit): general purpose input/output; LED output; interrupt function
- GPIO B Port (7-bit): general purpose input/output
- GPIO C Port (8-bit): general purpose input/output

2.4 ADC

- 6 channel 10-bit successive approximation A/D converter
- Internal (VDD) or external voltage reference

2.5 VFD

- Multiple display modes (9-segment and 19-digit to 20-segment and 8-digit)
- External resistor not necessary for driver outputs (P-ch open-drain + pull-down resistor output)

2.5 POR

- 2.0V Voltage Detector for Power-on reset

2.6 Package

- 63-pin die
- 64-pin LQFP (14×14 mm)

3 Application

VFD controller

4 Pin Configuration

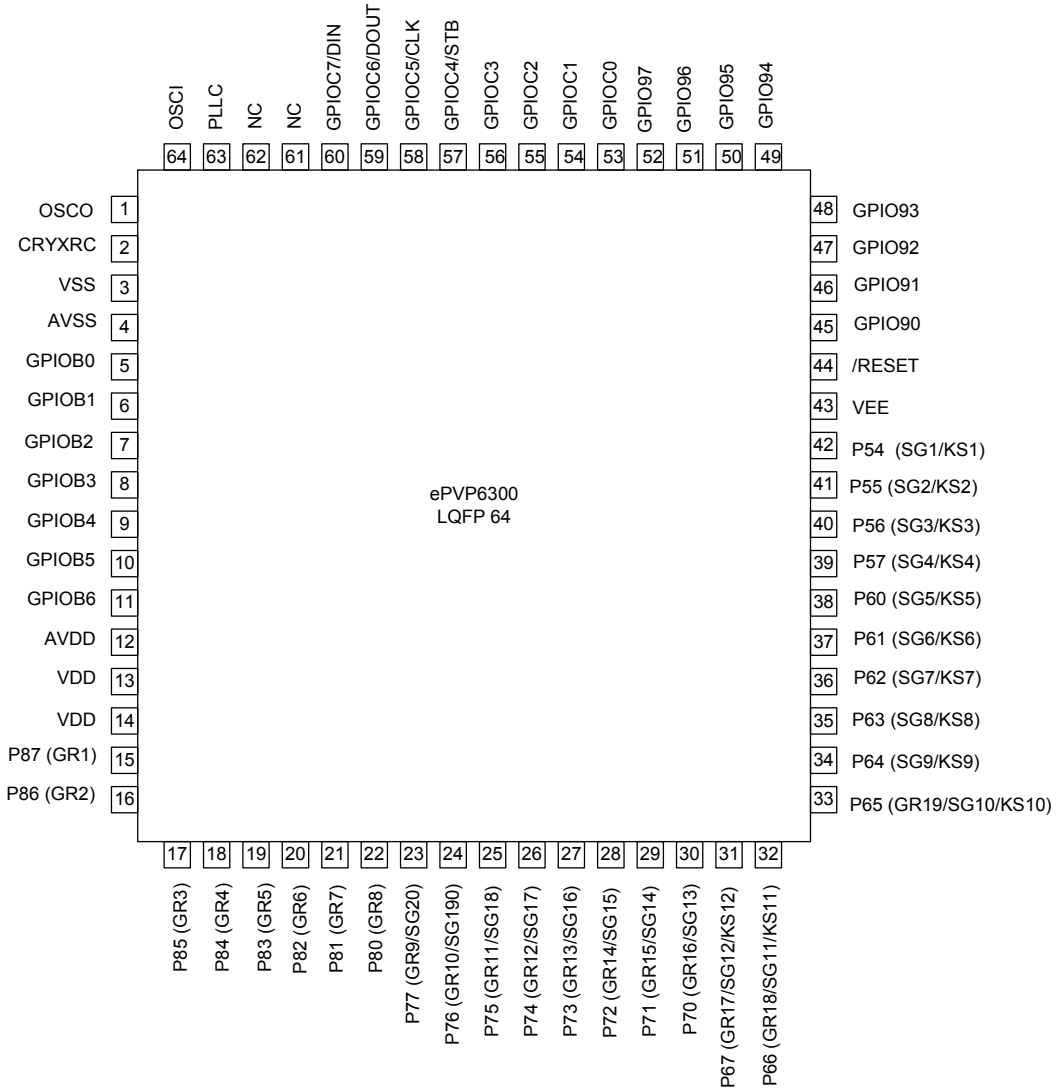


Figure 4 64-pin LQFP ePVP6300 Pin Assignment

5 Functional Block Diagram

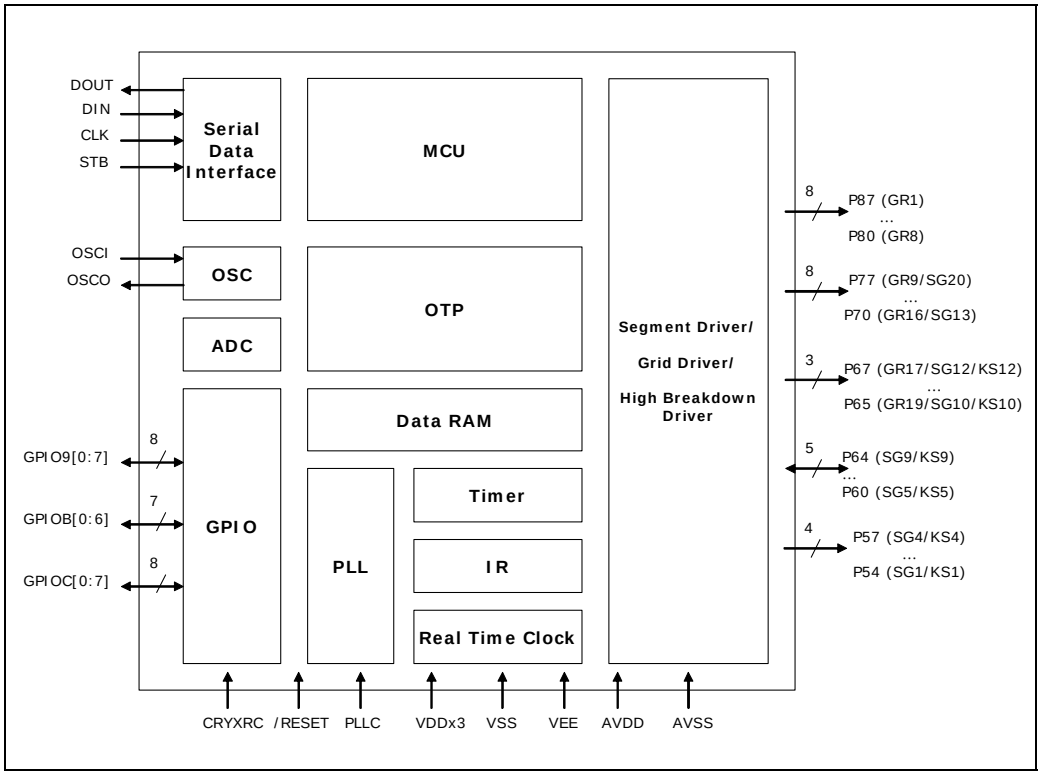


Figure 5-1a Block Diagram

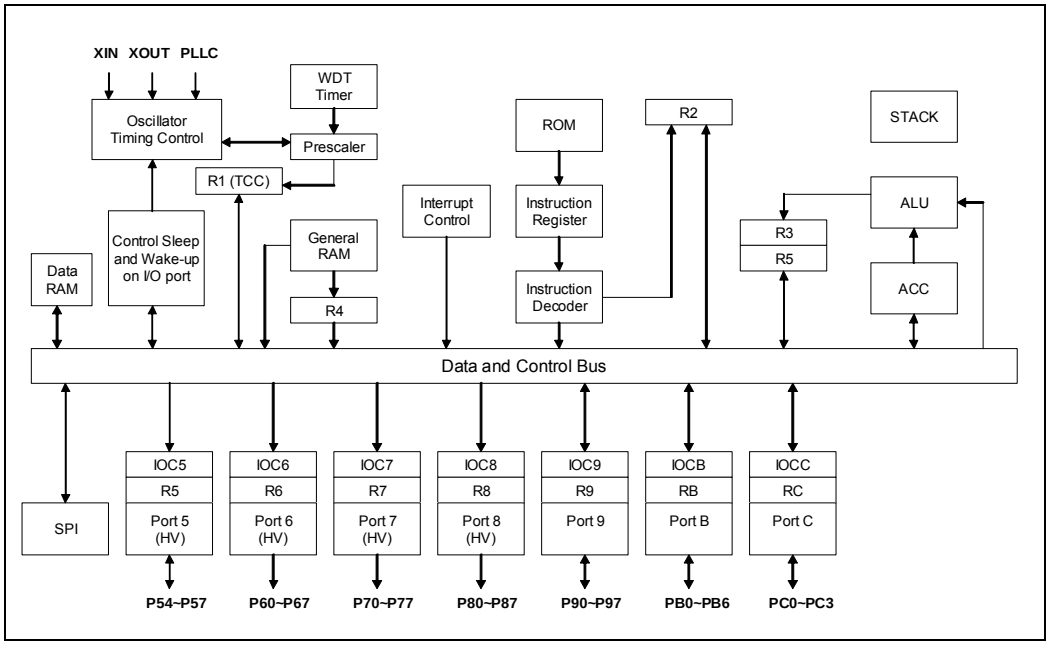


Figure 5-1b Block Diagram

5.1 Port Mapping for HV and GPIO

5.1.1 HV Port Mapping

Port	HV	Port	HV	Port	HV	Port	HV
-		P60	SG5/KS5	P70	GR16/SG13	P80	GR8
-		P61	SG6/KS6	P71	GR15/SG14	P81	GR7
-		P62	SG7/KS7	P72	GR14/SG15	P82	GR6
-		P63	SG8/KS8	P73	GR13/SG16	P83	GR5
P54	SG1/KS1	P64	SG9/KS9	P74	GR12/SG17	P84	GR4
P55	SG2/KS2	P65	GR19/SG10/KS10	P75	GR11/SG18	P85	GR3
P56	SG3/KS3	P66	GR18/SG11/KS11	P76	GR10/SG19	P86	GR2
P57	SG4/KS4	P67	GR17/SG12/KS12	P77	GR9/SG20	P87	GR1

5.1.2 GPIO Port Mapping

Port	GPIO	Port	GPIO	Port	GPIO
P90	GPIO90/LED0/IR	PB0	GPIOB0/VREF	PC0	GPIOC0/Key1
P91	GPIO91/LED1/INT1	PB1	GPIOB1/AD1	PC1	GPIOC1/Key2
P92	GPIO92/LED2/INT2	PB2	GPIOB2/AD2	PC2	GPIOC2/Key3
P93	GPIO93/LED3/INT3	PB3	GPIOB3/AD3	PC3	GPIOC3/Key4
P94	GPIO94/LED4/INT4	PB4	GPIOB4/AD4	PC4	GPIOC4/STB
P95	GPIO95/LED5	PB5	GPIOB5/AD5	PC5	GPIOC5/CLK
P96	GPIO96/LED6	PB6	GPIOB6/AD6	PC6	GPIOC6/DOUT
P97	GPIO97/LED7	-	-	PC7	GPIOC7/ DIN

5.2 Relevant Pins for Programming Mode

OTP Pin Name	Mask ROM Pin Name
VDD	AVDD
VPP	/RESET
DINCK	PC3
ACLK	PC2
PGMB	P92
OEB	P91
DATA	P90
GND	GND

6 Pin Description

Pin #	Pin Name	I/O	Bit	Description	Note
61, 62	NC		2		-
13, 14	VDD	-	2	Logic power supply	-
57	STB/GPIOC4	I/O	1	1. Serial Interface Strobe input pin. While the STB goes low, it will cause an interrupt event. The data input after the STB has fallen is processed as a command. When this pin is "HIGH," CLK is ignored. 2. Programmable Internal pull-high 3. GPIOC4 function	Schmitt Pull-up
58	CLK/GPIOC5	I/O	1	1. Clock input pin. This pin reads serial data at a rising edge and outputs data at a falling edge. 2. Programmable Internal pull-high 3. GPIOC5 function	Schmitt Pull-up
59	DOUT/GPIOC6	I/O	1	1. Data output pin (N-channel, Open-Drain) 2. This pin outputs serial data at a falling edge of the shift clock (starting from the lower bit). 3. Programmable internal pull-high 4. GPIOC6 function	Schmitt Pull-up
60	DIN/GPIOC7	I/O	1	1. Data input pin. This pin inputs serial data at a rising edge of the shift clock (starting from the lower bit.) 2. Programmable Internal pull-high 3. GPIOC7 function	Schmitt Pull-up
53–54	GPIOC0 – GPIOC3	I/O	4	General Purpose I/O pins: 1. Key data input to these pins is latched at the end of a display cycle. 2. These pins constitute a 4-bit general-purpose input/output port. 3. Programmable Internal pull-high 4. Wake-up Function	Schmitt Pull-up
15-22	GR1 – GR8	O	8	High voltage grid output	-
23-30	GR9 /SG20 – GR16 /SG13	O	8	1. High voltage grid output 2. High voltage segment output	-

Pin #	Pin Name	I/O	Bit	Description	Note
31-33	GR17/SG12/KS12 – GR19/SG10/KS10	O	3	1. High voltage grid output 2. High voltage segment output 3. Matrix key scan output	-
34-38	SG9/KS9 – SG5/KS5	O	5	1. High voltage segment output 2. Matrix key scan output	-
39-42	SG4/KS4 – SG1/KS1	I/O	4	1. High voltage segment output 2. Matrix key scan output 3. General Purpose Input pins: P54~P57	-
45–52	GPIO90/LED0 – GPIO97/LED7	I/O	8	1. General Purpose I/O pins 2. LED output pin (20 mA) 3. IR Detector 4. Interrupt Function 5. Programmable Internal pull-high	Schmitt Pull-up
12	AVDD	I	1	Analog Power	-
63	PLLC	I	1	Phase Lock Loop Capacitor (connect a 0.01 to 0.047μ capacitor to the Ground).	-
4	AVSS	I	1	Analog Ground	-
64	OSCI	I	1	Crystal Oscillator input pin (32, 768kHz) or resister input pin for RC Oscillator	-
1	OSCO	O	1	Crystal Oscillator output pin (32, 768kHz)	-
3	VSS	-	1	Connect this pin to GND of the system	-
5-11	GPIOB0 – GPIOB6	I/O	7	1. General Purpose I/O pins 4. ADC/VREF 5. ADC/AD1~AD6	-
2	CRYXRC	I	1	1. Normal (Open)→ select Crystal Oscillator 2. Connect to GND → select RC Oscillator	Pull-up
44	/RESET	I	1	Low active RESET signal input	Schmitt
43	VEE	-	1	Pull-down level [VDD-(-40V)max]	-

7 Functional Description

7.1 Operational Registers Configuration

Addr	R PAGE Registers		
	R PAGE0	R PAGE1	R PAGE2
00	Indirect addressing		
01	TCC		
02	PC		
03	Page, Status		
04	RAM bank, RSR		
05	Port 5 Output data	Program ROM page	
06	Port 6 Output data		SPI data buffer
07	Port 7 Output data	ADC control	Counter 1 data
08	Port 8 Output data	Data RAM address	Counter 2 LB data
09	Port 9 I/O data	Data RAM data buffer	Counter 2 HB data
0A	PLL, Main clock, WDTE	ADC output data buffer	Counter 3 data
0B	Port B I/O data	Port 9 pull-high	Counter 4 data
0C	Port C I/O data	Port C pull-high	Counter 5 data
0D	Interrupt flag		
0E	Interrupt flag, Wake-up control		
0F	Interrupt flag		
10 : 1F	16 bytes Common registers		
20 : 3F	Bank 0 ~ Bank 3 Common registers (32x8 for each bank)		

Addr	IOC PAGE Registers	
	IOC PAGE0	IOC PAGE1
00		
01		
02		
03		
04		
05		Port 5 switch
06		
07		
08		Clock source (CN2, CN1) Prescaler (CN2, CN1)
09	Port 9 I/O control	Clock source (CN4, CN3) Prescaler (CN4, CN3)
0A		Clock source (CN5) Prescaler (CN5)
0B	Port B I/O control	Port B switch
0C	Port C I/O control	Port C switch
0D	Interrupt mask	
0E	Interrupt mask	
0F	Interrupt mask	

7.2 Operational Registers Description

7.2.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as indirect address pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov  A, @0x20    ; store an address at R4 for indirect address
Mov  0x04, A
Mov  A, @0xAA    ; write data 0xAA to R20 at Bank0 through R0
Mov  0x00, A
```

7.2.2 R1 (TCC)

R1 is a TCC data buffer. It is incremented by 16.384kHz or by the instruction cycle clock (controlled by the CONT register).

It is written and read by the program as any other register.

7.2.3 R2 (Program Counter)

The configuration structure generates 16k×13 external ROM addresses to the relative programming instruction codes. The structure is depicted in Figure 7-1.

"JMP" instruction allows direct loading of the low 10 program counter bits.

"CALL" instruction loads the lower 10 bits of the PC and PC+1, and push onto the stack.

"RET" ("RETL k," "RETI") instruction loads the program counter with the contents at the top of the stack.

"MOV R2, A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2, A" allows a relative address to be added to the current PC, and the contents of the ninth and tenth bits are cleared to "0".

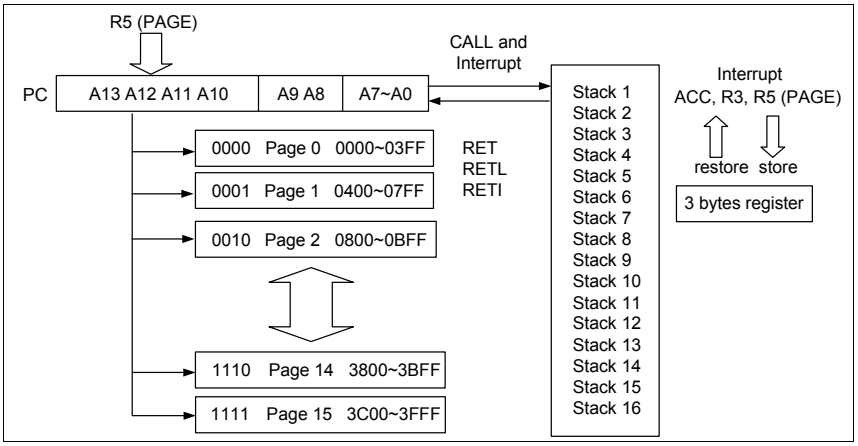


Figure 7-1 Program Counter Organization

"TBL" allows a relative address to be added to the current PC, and the contents of the ninth and tenth bits remain unchanged. The most significant bits (A10~A13) will be loaded with the contents of Bit PS0~PS3 in the status register (R5 Page 1) upon execution of a "JMP," "CALL," "ADD R2, A." or "MOV R2, A" instruction.

If an interrupt is triggered, the Program ROM will jump to Address 0x08 at Page 0. The CPU will automatically store ACC, R3 status, and R5 Page 1, and they will be restored after execution of instruction RETI.

7.2.4 R3 (Status, Page Selection)

Status Flag, Page Selection Bits

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RPAGE1	**RPAGE0**	IOCPAGE	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R	R	R/W	R/W	R/W

Bit 0 (C): Carry flag

The carry flag is affected by the following operation:

a. **Addition**: CF as a carry out indicator, when the addition operation has a carry-out, CF will be "1", in other words, if the operation has no carry-out, CF will be "0".

b. **Subtraction**: CF as a borrow-in indicator, when the subtraction operation has a borrow-in, the CF will be "0", in other words, if there is no borrow-in, CF will be "1".

c. **Comparison**: CF is as a borrow-in indicator for Comparison operation is the same as subtraction operation.

d. **Rotation**: CF shifts into the empty bit of the accumulator for the rotation and holds the shift out data after rotation.

Bit 1 (DC): Auxiliary carry flag

Bit 2 (Z): Zero flag

ZF is affected by the result of ALU, if the ALU operation generates a "0" result, ZF will be "1", otherwise, ZF will be "0".

Bit 3 (P): Power down bit

Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T): Time-out bit

Set to 1 by the "SLEP" and "WDTC" commands or during power up and reset to 0 by WDT timeout.

Event	T	P	Remarks
WDT wake-up from sleep mode	0	0	–
WDT time out (not sleep mode)	0	1	–
/RESET wake-up from sleep	1	0	–
Power up	1	1	–
Low pulse on /RESET	×	×	×: don't care

Bit 5 (IOCPAGE): Change IOC5 ~ IOCE to another page

"0": IOC Page 0

"1": IOC Page 1

Bit 6 (RPAGE0 ~ RPAGE1): Change R5 ~ RC to another page (for details see Section 7.1 *Operation Registers Configuration*)

(RPAGE1, RPAGE0)	R Page # Selected
(0, 0)	R Page 0
(0, 1)	R Page 1
(1, x)	R Page 2

7.2.5 R4 (RAM Selection for Common Registers R20 ~ R3F)

RAM Selection Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 5 (RSR0 ~ RSR5): Indirect address for common Registers R20 ~ R3F.

The RSR bits are used to select up to 32 registers (R20 to R3F) in indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1): Bank selection bits for common Registers R20 ~ R3F.

These selection bits are used to determine which bank is activated among the four banks of the 32 register (R20 to R3F).

Refer to Section 7.1 *Operation Registers Configuration* for details.

7.2.6 R5 (Port 5 Output Data, Program Page Selection)

Page 0 (Port 5 Output Data Register for HV or General Purpose Input pins)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	-	-	-	-
W-0	W-0	W-0	W-0	-	-	-	-

Page 1 (Program ROM Page Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD9	AD8	-	-	PS3	PS2	PS1	PS0
R	R	-	-	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (PS0 ~ PS3): Program page selection bits

PS3	PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	1	1	0	Page 2
0	1	1	1	Page 3
:	:	:	:	:
:	:	:	:	:
1	1	1	0	Page 14
1	1	1	1	Page 15

PAGE instruction is used to select the program page to be accessed. The selected program page is maintained by Elan compiler. PAGE instruction will change user's program by inserting the instruction within the program.

7.2.7 R6 (Port 6 Output Data, SPI Data Buffer)

Page 0 (Port 6 Output Data Register for HV)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

Page 2 (SPI Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7): SPI data buffer

If user writes data to this register, the data will be written to the SPIW register. If user reads this data, it will read the data from the SPIR register. Refer to the following figure.

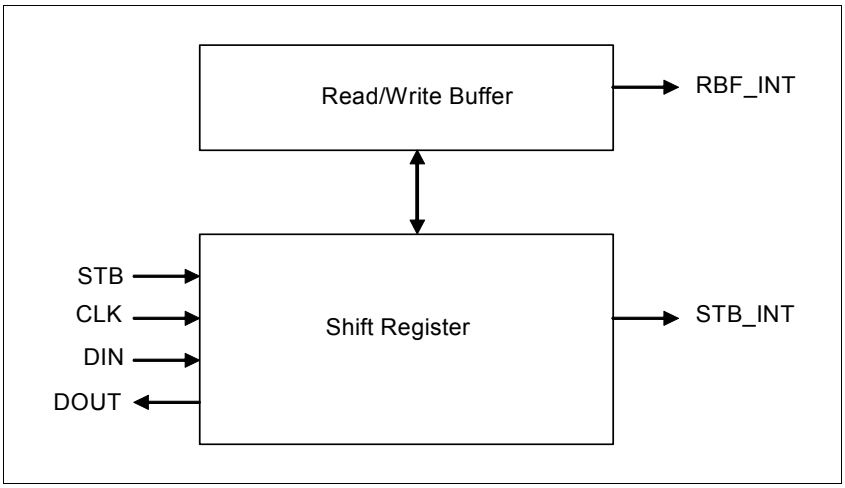


Figure 7-2a SPI Block Diagram

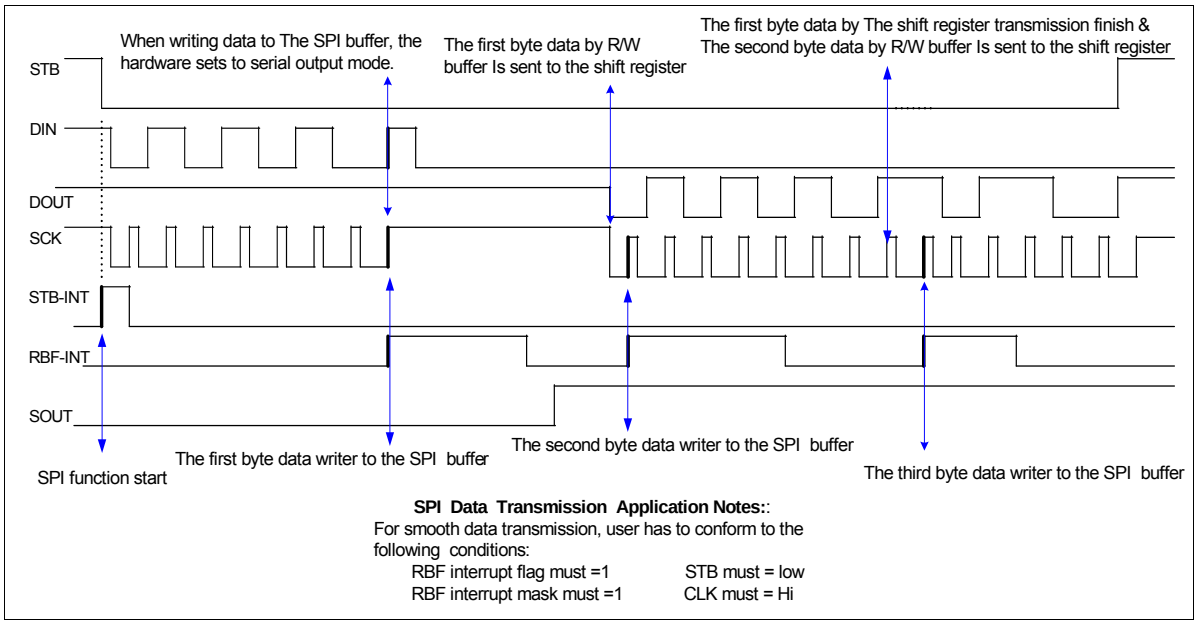


Figure 7-2b SPI Timing Diagram

7.2.8 R7 (Port 7 Output Data, Counter 1 Data)

Page 0 (Port 7 Output Data Register for HV)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

Page 1 (ADC Control Bit)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN2	IN1	IN0	ADCLK1	ADCLK0	ADPWR	ADRES	ADST
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (ADST): AD converter start to sample

By setting to "1," the AD will start to sample the data. This bit is automatically cleared by hardware after a sampling.

Bit 1 (ADRES): Resolution selection for ADC

0 → ADC is an 8-bit resolution

When 8-bit resolution is selected, the most significant (MSB) 8-bit data output of the internal 10-bit ADC will be mapped to RA PAGE1. Therefore, R5 PAGE1 Bit 6 ~ 7 will be of no use.

1 → ADC is 10-bit resolution

When 10-bit resolution is selected, 10-bit data output of the internal 10-bit ADC will be exactly mapped to RA PAGE1 and R5 PAGE1 Bit 6 ~7.

Bit 2 (ADPWR): AD converter power control

0 → disable

1 → enable

Bit 3 ~ Bit 4 (ADCLK0 ~ ADCLK1): AD circuit's sampling clock source

For PLL Clock = 895.658kHz ~ 14.33 MHz (CLK2~CLK0 = 001 ~ 110)

ADCLK1	ADCLK0	Sampling Rate	Operation Voltage
0	0	**74.6K**	≥ 3.5V
0	1	**37.4K**	≥ 3.0V
1	0	**18.7K**	≥ 2.5V
1	1	**9.3K**	≥ 2.5V

For PLL Clock = 447.829kHz (CLK2~CLK0 = 000)

ADCLK1	ADCLK0	Sampling Rate	Operation Voltage
0	0	**37.4K**	≥ 3.0V
0	1	**18.7K**	≥ 3.0V
1	0	**9.3K**	≥ 2.5V
1	1	**4.7K**	≥ 2.5V

This is a CMOS multi-channel 10-bit successive approximation A/D converter.

Features**:**

- 74.6kHz maximum conversion speed at 5V
- Adjusted full scale input
- External reference voltage input or internal (VDD) reference voltage
- 6 analog inputs multiplexed into one A/D converter
- Power down mode for power saving
- A/D conversion complete interrupt
- Interrupt register, A/D control and status register, and A/D data register

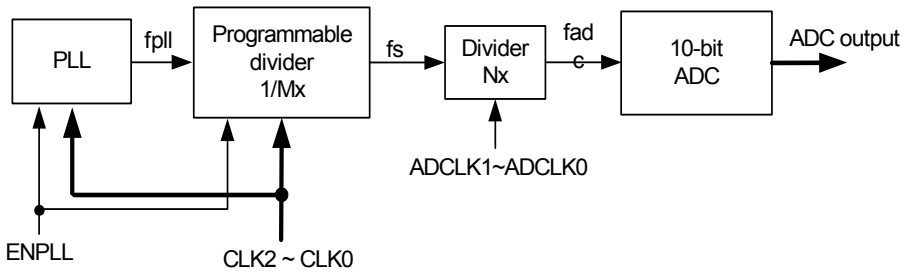


Figure 7-3 ADC Voltage Control Logic

fpll	Mx	fs	fadcon = fadc / 12			
			Nx = 1	Nx = 2	Nx = 4	Nx = 8
10.747MHz	12	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
7.165MHz	8	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
3.582MHz	4	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
1.791MHz	2	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
895.658kHz	1	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
447.829kHz	1	447.829kHz	37.391kHz	18.659khz	9.329kHz	4.665kHz

Bit 5 ~ Bit 7 (IN0 ~ IN2): Input channel selection of AD converter

These two bits can choose one of the three AD inputs.

IN2	IN1	IN0	Input
0	0	0	AD1
0	0	1	AD2
0	1	0	AD3
0	1	1	AD4
1	0	0	AD5
1	0	1	AD6

Page 2 (Counter 1 Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN10 ~ CN17): Counter 1 buffer that you can read and write.

Counter 1 is an 8-bit up-counter with 8-bit prescaler that allows user to use R7 Page 2 to preset and read the counter (write → preset). After an interrupt, it will reload the preset value.

7.2.9 R8 (Port 8 Output Data, Data RAM Address), Counter 2_LB Data

Page 0 (Port 8 Output Data Register for HV)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

Page 1 (Data RAM Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (RAM_A0 ~ RAM_A7): Data RAM address

Page 2 (Counter 2 Low Byte Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CN20 ~ CN27): Counter 2_LB's buffer that user can read and write.

Counter 2 is a 16-bit up-counter with 8-bit prescaler that allows user to use R8 Page 2 to preset and read the counter (write → preset). After an interrupt, it will reload the preset value.

7.2.10 R9 (Port 9 I/O Data, Data RAM Data Buffer), Counter 2_HB Data

Page 0 (Port 9 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P90 ~ P97): 8-bit Port 9 (0~7) I/O data register

User can use the IOC register to define each bit as input or output, and to define the pull-high condition.

Bit 0:

1. P90 : can be defined as Input/Output
2. LED0 : can be defined as Output
3. IR Input : can be defined as Input and IR is enabled (when IOCF Bit 7 is set to 1)

Bit 1 ~ Bit 4:

1. P91~P94 : can be defined as Input/Output
2. LED1~LED4 : can be defined as Output
3. INT1~INT4 : can be defined as Input

Bit 5 ~ Bit 7:

1. P95~P97 : can be defined as Input/Output
2. LED5~LED7 : can be defined as Output

Page 1 (Data RAM Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (RAM_D0 ~ RAM_D7): Data RAM's data

Page 2 (Counter 2 High Byte Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN215	CN214	CN213	CN212	CN211	CN210	CN29	CN28
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CN28 ~ CN215): Counter 2_HB's buffer that user can read and write.

Counter 2 is a 16-bit up-counter with 8-bit prescaler that allows user to use R9 Page 2 to preset and read the counter (write → preset). After an interrupt, it will reload the preset value.

7.2.11 RA (PLL, Main Clock Selection, Watchdog Timer), Counter 3 Data

Page 0 (PLL Enable Bit, Main Clock Selection Bits, Watchdog Timer Enable Bit)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDLE	PLLEN	CLK2	CLK1	CLK0	-	-	WDTEN
R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	-	-	R/W-0

Bit 0 (WDTEN): Watchdog control bit

User can use the WDTC instruction to clear the watchdog counter. The counter clock source is 32768/2 Hz. If the prescaler is assigned to TCC, the Watchdog timer will time out by (1/32768) × 2 × 256 = 15.625 ms. If the prescaler is assigned to WDT, the time out interval will be longer, depending on the prescaler ratio.

"0": disable

"1": enable

Bit 1 ~ Bit 2: Unused

Bit 3 ~ Bit 5 (CLK0 ~ CLK2): Main clock selection bits

User can select different frequencies for the main clock with CLK1 and CLK2. All the available clock selections are listed below.

PLLEN	CLK2	CLK1	CLK0	Sub Clock	Main Clock	CPU Clock
1	0	0	0	32.768kHz	447.829kHz	447.829kHz (Normal mode)
1	0	0	1	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	0	32.768kHz	1.791 MHz	1.791 MHz (Normal mode)
1	0	1	1	32.768kHz	3.582 MHz	3.582 MHz (Normal mode)
1	1	0	0	32.768kHz	7.165 MHz	7.165 MHz (Normal mode)
1	1	0	1	32.768kHz	10.747 MHz	10.747 MHz (Normal mode)
1	1	1	0	32.768kHz	×	(Don't use)
1	1	1	1	32.768kHz	×	(Don't use)
0	Don't care	Don't care	Don't care	32.768kHz	Don't care	32.768kHz (Green mode)

Bit 6 (PLLEN): PLL's power control bit which is a CPU mode control register

"0": disable PLL

"1": enable PLL

If PLL is enabled, the CPU will operate at normal mode (high frequency). Otherwise, it will run at green mode (low frequency, 32768Hz).

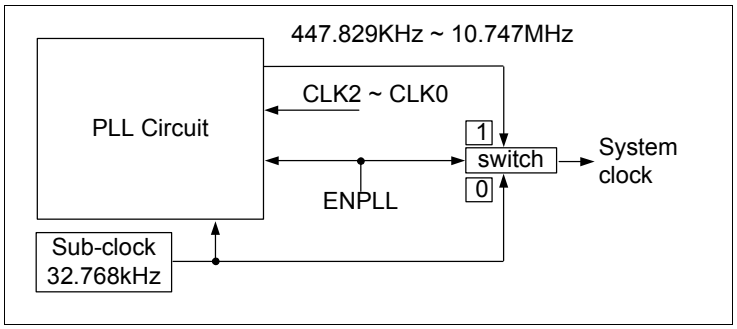


Figure 7-3 Correlation between 32.768kHz and PLL

Bit 7 (IDLE): Sleep or Idle mode control as set by SLEP instruction.

"0": Sleep mode

"1": Idle mode

This bit allows the SLEP instruction to determine which power saving mode to execute. The status after wake-up and the wake-up source list is shown below.

Wake-up Signal	Sleep Mode	Idle Mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP
TCC time out IOCF Bit 0=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
Counter 1 time out IOCF Bit 1=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
Counter 2 time out IOCF Bit 2=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
Counter 3 time out IOCD Bit 0=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
Counter 4 time out IOCD Bit 1=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
Counter 5 time out IOCD Bit 2=1	No function	1) Wake-up 2) Jump to next instruction after SLEP
Port 90 (IR function) IOCF Bit 3=1	Reset and jump to Address 0	1) Wake-up 2) Jump to next instruction after SLEP
WDT time out	Reset and jump to Address 0	1) Wake-up 2) Next instruction
Port C (0~3)(Key1~Key4) RE PAGE 0 Bit 0 or Bit 1 or Bit 2 or Bit 3 = 1	Reset and Jump to Address 0	1) Wake-up 2) Jump to next instruction after SLEP
Port 9 (1~4) IOCF Bit 4 or Bit 5 or Bit 6 =1 or Bit 7=1	Reset and Jump to Address 0	1) Wake-up 2) Jump to next instruction after SLEP

Notes:
1. *Port 90 wake-up function is controlled by IOCF Bit 3. It is a falling edge or rising edge triggered (controlled by CONT register Bit 7).*
2. *Port 91 wake-up function is controlled by IOCF Bit 4. It is a falling edge triggered.*
3. *Port 92 ~ Port 94 wake-up functions are controlled by IOCF. They are falling edge triggered.*
4. *Port C0 ~ Port C3 wake-up functions are controlled by RE PAGE0 Bit 0 ~ Bit 3. They are falling edge triggered.*

Page 1 (ADC Output Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (AD0~ AD7): These 8 bits are full ADC data buffer

Page 2 (Counter 3 Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN37	CN36	CN35	CN34	CN33	CN32	CN31	CN30
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN30 ~ CN37): Counter 3's buffer that user can read and write.

Counter 3 is an 8-bit up-counter with 8-bit prescaler that allows user to use RA Page 2 to preset and read the counter (write → preset). After an interrupt, it will reload the preset value.

7.2.12 RB (Port B I/O Data Buffer, Port 9 Switches)

Page 0 (Port B I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R-0	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 6 (PB0 ~ PB6): 7-bit Port B (0~6) I/O data register

User can use the IOC register to define each bit as input or output.

When Port B is switched to ADC–

Bit 0: is defined as VREF

Bit 1 ~ Bit 6: is defined as AD1~AD6

Page 1 (Port 9, Pull High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH97	PH96	PH95	PH94	PH93	PH92	PH91	PH90
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (PH90 ~ PH97): Port 9 Bit 0 ~ Bit 7 pull-high control register

"0": disable pull-high function

"1": enable pull-high function

Page 2 (Counter 4 Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN47	CN46	CN45	CN44	CN43	CN42	CN41	CN40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN40 ~ CN47): Counter 4 buffer that user can read and write.

Counter 4 is an 8-bit up-counter with 8-bit prescaler that allows user to use RB Page 2 to preset and read the counter (write → preset). After an interrupt, it will reload the preset value.

7.2.13 RC (Port C I/O Data, Counter 5 Data)

Page 0 I/O Data Buffer/Serial Signal

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 3: 1. PC0 ~ PC3 are defined as Input/Output

2. KEY1 ~ KEY4 are defined as Keyscan Input

Bit 4: 1. PC4 is defined as Input/Output

2. STB = Serial strobe signal

Bit 5: 1. PC5 is defined as Input/Output

2. CLK = Serial clock signal

Bit 6: 1. PC6 is defined as Input/Output

2. SDO = Serial data out

Bit 7: 1. PC7 is defined as Input/Output

2. SDI = Serial data in

Page 1 (Port C, Pull High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PHC7	PHC6	PHC5	PHC4	PHC3	PHC2	PHC1	PHC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (PHC0 ~ PHC7): Port C Bit 0 ~ Bit 7 pull-high control register

"0": disable pull-high function

"1": enable pull-high function

Page 2 (Counter 5 Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN57	CN56	CN55	CN54	CN53	CN52	CN51	CN50
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN50 ~ CN57): Counter 5 buffer that user can read and write.

Counter 5 is an 8-bit up-counter with 8-bit prescaler that allows user to use RC Page 2 to preset and read the counter (write → preset). After an interrupt, it will reload the preset value.

7.2.14 RD (Interrupt Flag)

Page 0 (Interrupt Flags Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	CNT5	CNT4	CNT3
-	-	-	-	-	R/W-0	R/W-0	R/W-0

Note: "1" means with interrupt request **"0"** means no interrupt

Bit 0 (CNT3): Counter 3 timer overflow interrupt flag. Set when Counter 3 timer overflows.

Bit 1 (CNT4): Counter 4 timer overflow interrupt flag. Set when Counter 4 timer overflows.

Bit 2 (CNT5): Counter 5 timer overflow interrupt flag. Set when Counter 5 timer overflows.

7.2.15 RE (Interrupt Flags, Wake-up)

Page 0 (Interrupt Flags, Wake-up Control Bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	RBF	ADI	STB	/WUPC3	/WUPC2	/WUPC1	/WUPC0
-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (/WUPC0): Port C0 wake-up control

"0": disable PC0 pin wake-up function

"1": enable PC0 pin wake-up function

Bit 1 (/WUPC1): Port C1 wake-up control

"0": disable PC1 pin wake-up function

"1": enable PC1 pin wake-up function

Bit 2 (/WUPC2): Port C2 wake-up control

"0": disable PC2 pin wake-up function

"1": enable PC2 pin wake-up function

Bit 3 (/WUPC3): Port C3 wake-up control

"0": disable PC3 pin wake-up function

"1": enable PC3 pin wake-up function

Bit 4 (STB): SPI data transfer start interrupt.

While the STB signal goes low, it will issue this interrupt.

Bit 5 (ADI): ADC Interrupt flag after sampling

Bit 6 (RBF): SPI data transfer complete interrupt

If the SPI RBF signal contains a rising edge signal, the CPU will set this bit (RBF set to "1" after data are completely transferred).

Bit 7 (-): Not used

7.2.16 RF (Interrupt Flags)

Page 0 (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT4	INT3	INT2	INT1	IR	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Note: "1" = means interrupt request **"0"** = means non-interrupt

Bit 0 (TCIF): TCC timer overflow interrupt flag. Set when the TCC timer overflows.

Bit 1 (CNT1): Counter 1 timer overflow interrupt flag. Set when Counter 1 timer overflows.

Bit 2 (CNT2): Counter 2 timer overflow interrupt flag. Set when Counter 2 timer overflows.

Bit 3 (IR): External IR pin interrupt flag. If Port 90 contains a falling / rising edge (controlled by CONT register) trigger signal, the CPU will set this bit.

Bit 4 (INT1): External INT1 interrupt flag. If Port 91 contains a falling edge trigger signal, the CPU will set this bit.

Bit 5 (INT2): External INT2 pin interrupt flag. If Port 92 has a falling edge trigger signal, the CPU will set this bit.

Bit 6 (INT3): External INT3 pin interrupt flag. If Port 93 has a falling edge trigger signal, the CPU will set this bit.

Bit 7 (INT4): External INT4 pin interrupt flag, If Port 94 has a falling edge trigger signal, the CPU will set this bit.

Trigger edge is shown below:

Signal	Trigger
TCC	Time out
Counter 1	Time out
Counter 2	Time out
Counter 3	Time out
Counter 4	Time out
Counter 5	Time out
IR	Falling Rising edge
INT1	Falling edge
INT2	Falling edge
INT3	Falling edge
INT4	Falling edge

7.2.17 R10~R3F (General Purpose Registers)

R10 ~ R1F, R20 ~ R3F (Banks 0 ~ 3)**:** all are general purpose registers.

7.3 Special Purpose Registers

7.3.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

7.3.2 CONT (Control Register)

CONT register is readable (CONTR) and writable (CONTW).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P90EG	INT	TS	RETBK	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB): Prescaler assignED bit

"0": TCC

"1": WDT

When in WDT mode (Bit 3 = 1), the prescaler is cleared by the WDTC and SLEP instructions. Likewise, when in TCC mode (Bit 3 = 0), the prescaler **cannot** be cleared by SLEP instructions.

An 8-bit counter is provided as prescaler for the TCC or WDT. The prescaler is available for the TCC only or for the WDT only, one at a given time.

An 8-bit counter is made available for the TCC or WDT as determined by the status of Bit 3 (PAB) of the CONT register.

Both TCC and prescaler are cleared each time a write to TCC instruction is executed. (See the table above for the prescaler ratio under CONT register and Figure 7-4 below for the TCC/WDT block diagram.)

Bit 4 (RETBK): Return value backup control for interrupt routine

"0": disable

"1": enable

When this bit is set to 1, the CPU will store ACC, R3 status, and R5 Page 1 automatically after an interrupt is triggered. It will be restored after instruction RETI. When this bit is set to 0, user needs to store ACC, R3, and R5 Page 1 in the program.

Bit 5 (TS): TCC signal source

"0": internal instruction cycle clock

$$\textbf{\textit{Timing}} = \left(\frac{2}{System\ Clock} \right) \times \Pr escaler \times \left(Counter\ Value \right)$$

"1": 16.384kHz

$$\textbf{\textit{Timing}} = \left(\frac{1}{16.384k} \right) \times \Pr escaler \times \left(Counter\ Value \right)$$

Bit 6 (INT): INT enable flag

"0": interrupt masked by DISI or hardware interrupt

"1": interrupt enabled by ENI/RETI instructions

Bit 7 (P90EG): Interrupt edge type of P90

"0": P90, interrupt source is a rising edge signal

"1": P90, interrupt source is a falling edge signal

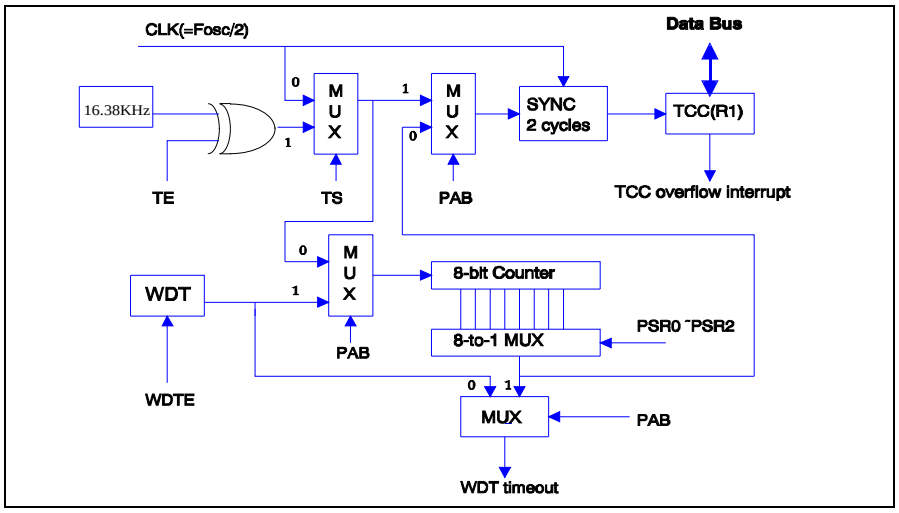


Figure 7-4 TCC and WDT Block Diagram

7.3.3 IOC 5 (Port 5 Switches)

Page 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57S	P56S	P55S	P54S	–	–	–	–
R/W-0	R/W-0	R/W-0	R/W-0	–	–	–	–

Bit 4 ~ Bit 7 (P54S~P57S): Port 5 I/O direction control register

"0": set the relative I/O pin as output HV

"1": set the relative I/O pin into high impedance

7.3.4 IOC 8

Page 1 (Clock Source and Prescaler for Counter 1 and Counter 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C1_PSC0 ~ C1_PSC2): Counter 1 prescaler ratio

C1_PSC0	C1_PSC2	C1_PSC1	Counter 1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S): Counter 1 clock source

"0": 16.384kHz

$$\textbf{\textit{Timing}} = \left(\frac{1}{16.384k}\right) \times \Pr escaler \times \left(Counter\ Value\right)$$

"1": System clock

$$\textbf{\textit{Timing}} = \left(\frac{2}{System\ Clock}\right) \times \Pr escaler \times \left(Counter\ Value\right)$$

Bit 4 ~ Bit 6 (C2_PSC0 ~ C2_PSC2): Counter 2 prescaler ratio

C2_PSC2	C2_PSC1	C2_PSC0	Counter 2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7 (CNT2S): Counter 2 Clock Source

"0": 16.384kHz

$$\textbf{\textit{Timing}} = \left(\frac{1}{16.384k}\right) \times \Pr escaler \times \left(Counter\ Value\right)$$

"1": System clock

$$\textbf{\textit{Timing}} = \left(\frac{2}{System\ Clock}\right) \times \Pr escaler \times \left(Counter\ Value\right)$$

7.3.5 IOC9 (Port 9 I/O Control)

Page 0 (Port 9 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97): Port 9 (0~7) I/O Direction Control Register

"0": set the relative I/O pin as output

"1": set the relative I/O pin into high impedance

Page 1 (Clock Source and Prescaler for Counter 3 and Counter 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT4S	C4_PSC2	C4_PSC1	C4_PSC0	CNT3S	C3_PSC2	C3_PSC1	C3_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C3_PSC0 ~ C3_PSC2): Counter 3 prescaler ratio

C3_PSC2	C3_PSC1	C3_PSC0	Counter 3
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT3S): Counter 3 clock source

"0": 16.384kHz

$$\textbf{\textit{Timing}} = \left(\frac{1}{16.384k}\right) \times \Pr escaler \times \left(Counter\ Value\right)$$

"1": System clock

$$\textbf{\textit{Timing}} = \left(\frac{2}{System\ Clock}\right) \times \Pr escaler \times \left(Counter\ Value\right)$$

Bit 4 ~ Bit 6 (C4_PSC0 ~ C4_PSC2): Counter 4 prescaler ratio

C4_PSC2	C4_PSC1	C4_PSC0	Counter 4
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7 (CNT4S): Counter 4 clock source

"0": 16.384kHz

$$\textbf{\textit{Timing}} = \left(\frac{1}{16.384k}\right) \times \Pr escaler \times \left(Counter\ Value\right)$$

"1": System clock

$$\textbf{\textit{Timing}} = \left(\frac{2}{System\ Clock} \right) \times \Pr escaler \times \left(Counter\ Value \right)$$

7.3.6 IOCA

Page 1 (Clock Source and Prescaler for Counter 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	CNT5S	C5_PSC2	C5_PSC1	C5_PSC0
-	-	-	-	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C5_PSC0 ~ C5_PSC2): Counter 5 prescaler ratio

C5_PSC2	C5_PSC1	C5_PSC0	Counter 4
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT5S): Counter 5 clock source

"0": 16.384kHz

$$\textbf{\textit{Timing}} = \left(\frac{1}{16.384k} \right) \times \Pr escaler \times \left(Counter\ Value \right)$$

"1": System clock

$$\textbf{\textit{Timing}} = \left(\frac{2}{System\ Clock} \right) \times \Pr escaler \times \left(Counter\ Value \right)$$

7.3.7 IOCB (Port B I/O Control, Port B Switch)

Page 0 (Port B I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 6 (IOCB0 ~ IOCB6): Port B (0~6) I/O direction control register

"0": set the relative I/O pin as output

"1": set the relative I/O pin into high impedance

Page 1 (Port B Switch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PB6S	PB5S	PB4S	PB3S	PB2S	PB1S	PB0S
-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (PB0S): Select between AD Voltage Reference pin or I/O Port B0 pin

"0": PB0 (I/O Port B0) pin is selected and ADC reference voltage sourced from internal VDD

"1": VREF (ADC external reference voltage input) pin is selected

Bit 1 (PB1S): Select between normal I/O Port B1 pin or ADC Channel 1 input AD1 pin

"0": PB1 (I/O Port B1) pin is selected

"1": AD1 (ADC Channel 1 input) pin is selected

Bit 2 (PB2S): Select between normal I/O Port B2 pin or ADC Channel 2 input AD2 pin

"0": PB2 (I/O Port B2) pin is selected

"1": AD2 (ADC Channel 2 input) pin is selected

Bit 3 (PB3S): Select between normal I/O Port B3 pin or ADC Channel 3 input AD3 pin

"0": PB3 (I/O Port B3) pin is selected

"1": AD3 (ADC Channel 3 input) pin is selected

Bit 4 (PB4S): Select between normal I/O Port B4 pin or ADC Channel 4 input AD4 pin

"0": PB4 (I/O Port B4) pin is selected

"1": AD4 (ADC Channel 4 input) pin is selected

Bit 5 (PB5S): Select between normal I/O Port B5 pin or ADC Channel 5 input AD5 pin

"0": PB5 (I/O Port B5) pin is selected

"1": AD5 (ADC Channel 5 input) pin is selected

Bit 6 (PB6S): Select between normal I/O Port B5 pin or ADC Channel 6 input AD6 pin

"0": PB6 (I/O Port B6) pin is selected

"1": AD6 (ADC Channel 6 input) pin is selected

7.3.8 IOCC (Port C I/O Control)

Page 0 (Port C I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCC7	IOCC6	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOCC0 ~ IOCC7): Port C (0~7) I/O direction control register

"0": set the relative I/O pin as output

"1": set the relative I/O pin into high impedance

Page 1 (Port C Switches)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7S	PC6S	PC5S	PC4S	-	-	-	-
R/W-1	R/W-1	R/W-1	R/W-1	-	-	-	-

Bit 4 (PC4S): Select STB or I/O Port C4 pin

"0": PC4 (I/O Port C4) pin is selected

"1": STB pin is selected

Bit 5 (PC5S): Select CLK or I/O Port C5 pin

"0": PC5 (I/O Port C5) pin is selected

"1": CLK pin is selected

Bit 6 (PC6S): Select DOUT or I/O Port C6 pin

"0": PC6 (I/O Port C6) pin is selected

"1": DOUT pin is selected (N-channel, Open-drain)

Bit 7 (PC7S): Select DIN or I/O Port C7 pin

"0": PC7 (I/O Port C7) pin is selected

"1": DIN pin is selected

7.3.9 IOCD (Interrupt Mask, Prescaler of CN3 ~ CN5)

Page 0 (Interrupt Mask)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	CNT5	CNT4	CNT3
-	-	-	-	-	R/W-0	R/W-0	R/W-0

Bits 0 ~ 3 (CNT3 ~ CNT5): Interrupt enable bit

"0": disable interrupt

"1": enable interrupt

7.3.10 IOCE (Interrupt Mask)

Page 0 (Interrupt Mask)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	RBF	ADI	STB	-	-	-	-
-	R/W-0	R/W-0	R/W-0	-	-	-	-

Bit 4 (STB): STB goes LOW interrupt mask.

"0": disable interrupt

"1": enable interrupt

Bit 5 (ADI): ADI interrupt flag after a sampling.

"0": disable interrupt

"1": enable interrupt

Bit 6 (RBF): SPI's RBF interrupt mask

"0": disable interrupt

"1": enable interrupt

7.3.11 IOCF (Interrupt Mask)

Page 0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT4	INT3	INT2	INT1	IR	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bits 0 ~ 7: Interrupt enable bit

"0": disable interrupt

"1": enable interrupt

The status after interrupt and the interrupt source list are as shown in the table below.

Interrupt Signal	Idle Mode	Green Mode	Normal Mode
	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out IOCF Bit0=1 And "ENI"	1) Wake-up 2) Interrupt (Jump to Address 8 on Page 0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)
Counter 1 time out IOCF Bit1=1 And "ENI"	1) Wake-up 2) Interrupt (Jump to Address 8 on Page 0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)

(Continuation)

Interrupt Signal	Idle Mode	Green Mode	Normal Mode
Counter 2 time out IOCF Bit2=2 And "ENI"	1) Wake-up 2) Interrupt (Jump to Address 8 on Page 0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (Jump to Address 8 on Page0)	Interrupt (Jump to Address 8 on Page0)
Counter 3 time out IOCD Bit0=1 And "ENI"	1) Wake-up 2) Interrupt (Jump to Address 8 on Page 0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)
Counter 4 time out IOCD Bit1=1 And "ENI"	1) Wake-up 2) Interrupt (Jump to Address 8 on Page 0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (Jump to Address 8 on Page0)	Interrupt (Jump to Address 8 on Page 0)
Counter 5 time out IOCD Bit2=1 And "ENI"	1) Wake-up 2) Interrupt (Jump to Address 8 on Page 0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)
INT1~4 IOCF Bit4=1 or IOCF Bit5=1 IOCF Bit6 = 1 or IOCF Bit7= 1 And “ENI	1) Wake-up 2) Interrupt (Jump to Address 8 on Page 0) 3) after RETI instruction, jump to SLEP Next instruction	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)
IR IOCF Bit3= 1 And “ENI	1) Wake-up 2) Interrupt (Jump to Address 8 on Page 0) 3) After RETI instruction, jump to SLEP Next instruction	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)
ADI IOCE Bit5 = 1 And “ENI	No function	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)
RBF IOCE Bit6 = 1 And “ENI	No function	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)
STB IOCE Bit4 = 1 And “ENI	No function	Interrupt (Jump to Address 8 on Page 0)	Interrupt (Jump to Address 8 on Page 0)

NOTE

1. *Port 9 interrupt function is controlled by IOCF Bit 3. It is falling edge or rising edge triggered (controlled by CONT register Bit 7).*
2. *Port 9 (1~4) interrupt functions are controlled by IOCF Bits 4, 5, 6, and 7). They are falling edge triggered.*
3. *STB interrupt source function is controlled by IOCE Page 0 Bit 4. It is falling edge triggered after the STB goes low.*

7.4 Application Notes

7.4.1 Call-Table Instruction

The call-table instruction can only change the Program Counter Bit 7 ~ Bit 0 one at a time, so only 256 addresses can be searched once. As each program page contains 1024 addresses and each call has 256 addresses as a zone, then each page constitutes four zones.

When a table overlaps two zones, an error will occur during an address search. So user must examine the *.LST file to check for errors. The *.LST file will record the information that the Assembler has generated, such as source code, instruction code, instruction address, error messages, etc.

7.4.2 CPU Operation Requirements

The system frequency must add a latency time (add “NOP” over ten) in order to ensure a stable system operation frequency after the RA register has been set.

7.5 I/O Port

The I/O registers are bidirectional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O data registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Figure 7-5.

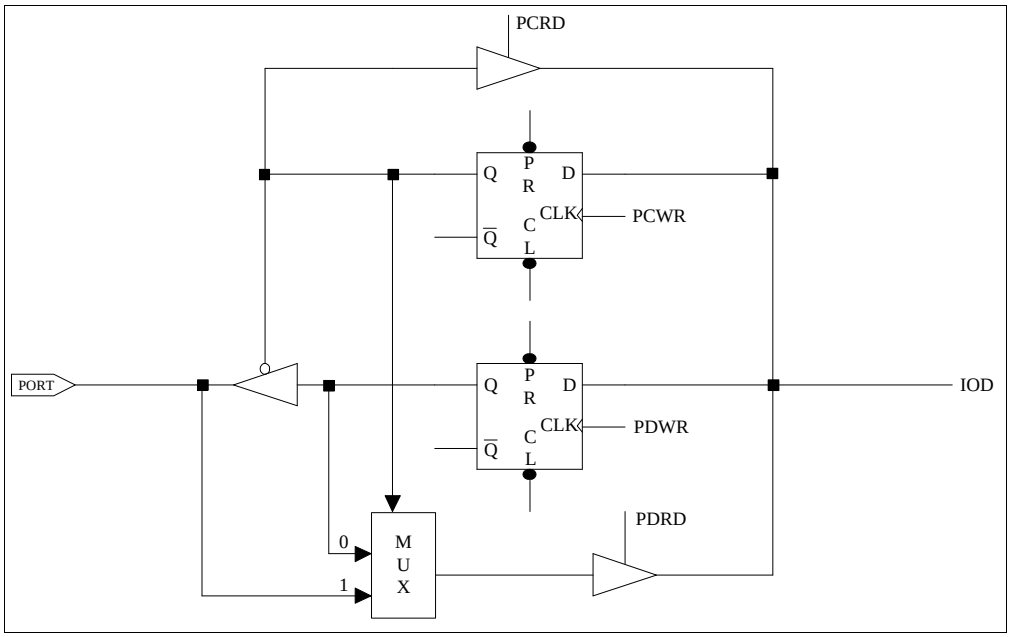


Figure 7-5 Circuit of I/O Port and I/O Control Register

7.6 Reset

A reset can be triggered by any of the following:

1. Power-on reset
2. WDT timeout (if enabled and in Green or Normal mode)
3. /RESET pin pull low

Once a reset occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When in power-on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"

- The other registers' (Bit 7 ~ Bit 0) default values are as follows.

Address	R Register Page 0	R Register Page 1	R Register Page 2	R Register Page 3	IOC Register Page 0	IOC Register Page 1
0x4	00xxxxxx	–	–	–	–	–
0x5	0000xxxx	xxxx0000	00000000	–	–	–
0x6	00000000	–	xxxxxxxx	–	–	–
0x7	00000000	00000000	xxxxxxxx	–	–	–
0x8	00000000	00000000	xxxxxxxx	–	–	00000000
0x9	00000000	xxxxxxxx	xxxxxxxx	–	11111111	00000000
0xA	00011xx0	xxxxxxxx	xxxxxxxx	–	–	00000000
0xB	00000000	00000000	xxxxxxxx	–	00000000	x0000000
0xC	1011xxxx	00000000	xxxxxxxx	–	1111xxxx	1111xxxx
0xD	xxxxx000	–	–	–	xxxxx000	–
0xE	x0000000	–	–	–	x000xxxx	–
0xF	00000000	–	–	–	00000000	–

7.7 Wake-up

The controller features two types of sleep mode for power saving**:**

7.7.1 Sleep Mode, RA(6; 7) = 0 + "SLEP" Instruction

In this mode, the controller turns off all the CPU and crystal. However, other circuits with power control like keytone control or PLL control (with register enabled), has to be turned off through software.

7.7.2 Idle Mode, RA(6; 7) = 1 + "SLEP" Instruction.

In this mode, the controller only turns the CPU off. The crystal remains running.

7.7.3 Wake-up from Sleep Mode

1. WDT time out
2. External interrupt
3. /RESET pull low

Any of these cases will reset the controller and run the program from Address 0. The status is just like the power-on-reset condition. Be sure to enable the circuit after Case 1 or 2 occurs.

7.7.4 Wake up from Idle Mode

1. WDT time out
2. External interrupt
3. Internal interrupt like counters

All these cases require user to enable the circuit before entering Idle mode. All the register values are preserved when "SLEP" instruction is executed and restored after wake-up.

During execution of Case 2 or 3, the controller will wake up and jump to Address 0x08 for interrupt sub-routine. After performing the sub-routine ("RETI" instruction), the program will jump to the next instruction following the "SLEP" instruction.

7.8 Interrupt

RD, RE, and RF are the interrupt status registers which record the interrupt request in flag bit. IOCD, IOCE, and IOCF are their respective interrupt mask registers. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will allow the next instruction to be fetched from Address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in their respective (RD, RE, and RF) registers.

The interrupt flag bit must be cleared by the software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

7.9 Instruction Set

The Instruction set has the following features**:**

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O register can be treated as a general register. That is, the same instruction can operate on the I/O register.

Convention:

R *= Register designator that specifies which one of the 64 registers (including operation and general purpose registers) is to be utilized by the instruction.*
Bits 6 and 7 in R4 determine the selected register bank.

b *= Bit field designator that selects the value for the bit located in register* ***R*** *and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

Binary Instruction	HEX	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 Bits 9,10 do not clear	Z, C, DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC	1

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z	1
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z	1
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None	1
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None	1
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None	1
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z	1
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC	1
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1 1110 100k kkkk	1E8k	PAGE k	K → R5(4:0)	None	1
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC	1

8 RC/Crystal Oscillator

8.1 General Description

This oscillator is designed for the ePVP6300 IC as clock source.

8.2 Features

- Crystal oscillator: 32.768kHz
- RC oscillator: 32kHz
- Operating voltage: 2.2V~5.5V
- Operating temperature: -20°C ~ +70°C

8.3 Block Diagram

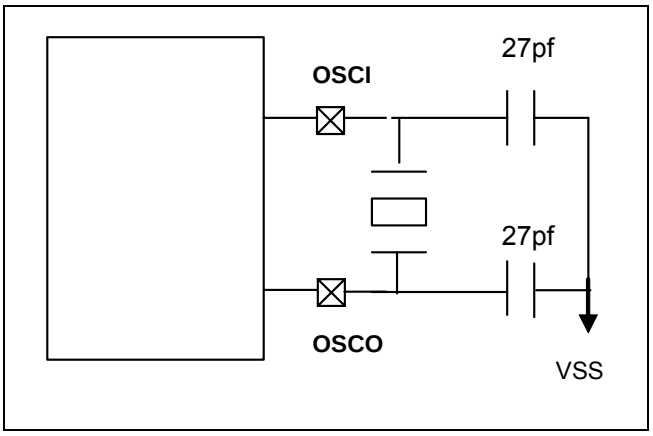


Figure 8-1 Crystal OSC Block Diagram

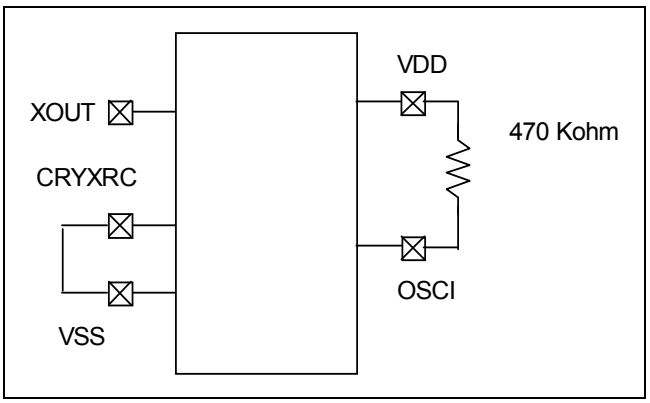


Figure 8-2 RC OSC Block Diagram

8.4 Pin Description

Name	I/O Type	Description	Remarks
OSCI	I	Crystal oscillator connection pin	–
OSCO	O	Crystal oscillator output pin	–
VDD	–	Power supply (+) pin	–
VSS	–	Power supply (–) pin	–

8.5 Electrical Characteristics

Condition: VDD = 4.5 to 5.5V, Ta = -20°C to +70°C

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Starting oscillation voltage	Vs	–	–	2.0	3.2	V
Stable time	Ts	Vdd = 5.0V	–	5	10	clk
Current consumption	Idd	Vdd = 5.0V	–	2	3	mA
Duty cycle	–	–	45	50	55	%
Frequency/Voltage deviation	$\partial f/\partial V$	–	–	1	1.5	%
Frequency/Temperature deviation	Δf	–	–	1	2	%
Frequency vs. Process deviation	–	–	–	±6	±10	%

9 Absolute Maximum Ratings

Ta = 25°C, Vss = 0V

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD}	-0.5 to + 6	V
Driver supply voltage	V_{EE}	VDD +0.5 to VDD - 45	V
Logic input voltage	V_I	-0.5 to VDD +0.5	V
VFD driver output voltage	V_O	VEE -0.5 to VDD +0.5	V
LED driver output current	I_{O1}	+25	mA
VFD driver output current	I_{O2}	-40 (Grid) -15 (Segment)	mA
Operating ambient temperature	T_{opt}	-20 to +70	°C
Storage temperature	T_{stg}	-65 to +150	°C

10 DC Electrical Characteristics

Ta = -20 to +70°C, VDD = 4.5 to 5.5V, Vss = 0V, VEE = VDD - 45V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Digital Input Voltage High	V_{IH}	$0.8V_{DD}$	-	V_{DD}	V	GPIOB
Digital Input Voltage Low	I_{OL}	VSS	-	0.2VDD	V	
Schmitt Trigger Negative Going Threshold Voltage	V_{T-}	1.5	1.8	2.1	V	GPIOC, GPO9, CLK, STB, DIN and /RESET
Schmitt Trigger Positive Going Threshold Voltage	V_{T+}	2.9	3.2	3.5		
Input Leakage Current	I_{IN}	–	–	±1	µA	V_{IN} = V_{DD} or V_{SS}
Pull-up Resistor	R_{PU}	50	75	100	KΩ	GPIOC, GPO9, CLK, STB, DOUT, DIN , CRYXRC and /RESET @ VDD=5V
Digital Output Voltage High	V_{OH}	$0.8V_{DD}$	–	V_{DD}	V	DOUT, GPIOC
Digital Output Voltage Low	V_{OL}	V_{SS}	–	$0.2V_{DD}$	V	
Digital Output High Current	I_{OH1}	-2	-4	-5	mA	V_{OH}=2.4V / DOUT, GPIOB, GPIOC
Digital Output Low Current	I_{OL1}	2	4	5	mA	V_{OL}=0.4V / DOUT, GPIOB, GPIOC
Digital Output High Current	I_{OH2}	-15	-18	-25	mA	V_{OH}=2.4V / GPIO9
Digital Output Low Current	I_{OL2}	15	18	25	mA	V_{OL}=0.4V / GPIO9
HV Output Current	I_{OH1}	-6	-5	-3	mA	Vo = VDD –2V, (VDD=5V) SEG1/KS1 to SEG4/KS4 SG5/KS5 to SG9/KS9
HV Output Current	I_{OH2}	-15	-14	-11	mA	Vo = VDD –2V, (VDD=5V) GR1 to GR8 GR9/SG20 to GR16/SG13 GR17/SG12/KS12 to GR19 /SG10/KS10
HV Leakage current	I_{HVLEAK}	5	8	10	µA	Vo = VDD –45V, driver off
HV Output pull-down resistor	R_L	40	80	120	KΩ	Driver output (VEE= -25V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power down current (Sleep mode) Crystal oscillation operating mode	I_{SB1}	–	–	1.5	μA	VDD =5V, All input and I/O pin at VDD, Output pin floating, WDT disabled
Low clock current (Green mode) Crystal oscillation operating mode	I_{SB2}	–	30	60	μA	VDD =3V CLK=32.768kHz, All analog circuits disabled, All input and I/O pin at VDD, Output pin floating
		–	65	90	μA	VDD =5V CLK=32.768kHz, All analog circuits disabled, All input and I/O pin at VDD, Output pin floating
Low clock current (Idle mode) Crystal oscillation operating mode	I_{SB3}	–	30	45	μA	VDD =3V CLK=32.768kHz, All analog circuits disabled, All input and I/O pin at VDD, Output pin floating
		–	45	60	μA	VDD =5V CLK=32.768kHz, All analog circuits disabled, All input and I/O pin at VDD, Output pin floating
Operating supply current (Normal mode) Crystal oscillation operating mode	I_{CC}	–	1.3	2	mA	/RESET=High, CLK=3.582 MHz, All analog circuits disabled, Output pin floating

11 AC Electrical Characteristics

11.1 CPU Instruction Timing

Ta = -20°C ~ + 70°C, VDD=5V, VSS=0V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk	–	45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.582 MHz	–	60 550	–	μs ns
Device delay hold time	Tdrh	–	–	16	–	ms
TCC input period	Ttcc	Note*	(Tins+20)/N*	–	–	ns
Watchdog timer period	Twdt	Ta = 25°C	–	16	–	ms

Note: *N= selected prescaler ratio*

11.2 AC Timing Characteristics

VDD=5V, Ta=+25°C

Description		Symbol	Min.	Typ.	Max.	Unit
Oscillator timing characteristic						
OSC start up	32.768kHz	Tosc	400	–	1500	ms
	3.579 MHz PLL		–	5	10	µs
SPI timing characteristic (CPU clock 3.58 MHz and Fosc = 3.582 MHz / 2)						
/SS set-up time		Tcss	560	–	–	ns
/SS hold time		Tcsh	250	–	–	–
SCLK high time		Thi	250	–	–	ns
SCLK low time		Tlo	250	–	–	ns
SCLK rising time		Tr	–	15	30	ns
SCLK falling time		Tf	–	15	30	ns
SDI set-up time to the reading edge of SCLK		Tisu	25	–	–	ns
SDI hold time to the reading edge of SCLK		Tihd	25	–	–	ns
SDO disable time		Tdis	–	–	560	ns

11.3 ePVP6300 Operating Voltage vs. Main Clock

(X Axis → Min VDD ; Y Axis → Main CLK)

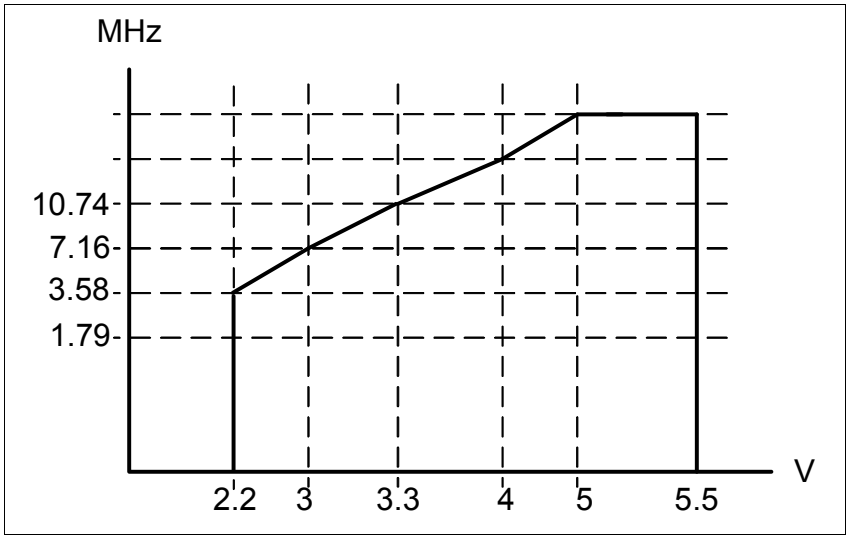
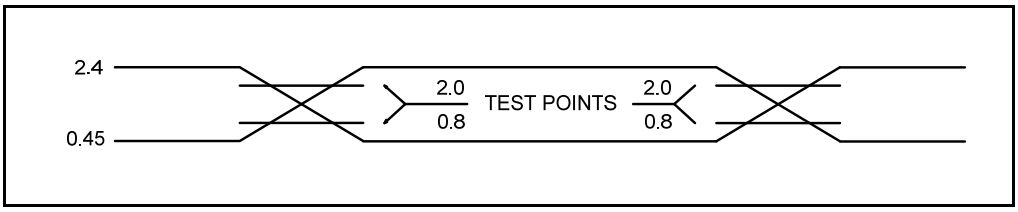


Figure 11-1 Operation Voltage XY Axis

11.4 AC Timing Diagrams

AC Test Input/Output Waveform



Note: *AC Testing: Input are driven at 2.4V for logic "**1**," and 0.45V for logic "**0**"*
*Timing measurements are made at 2.0V for logic "**1**," and 0.8V for logic "**0**"*

Figure 11-2a AC Test Input/Output Waveform Timing Diagram

Reset Timing

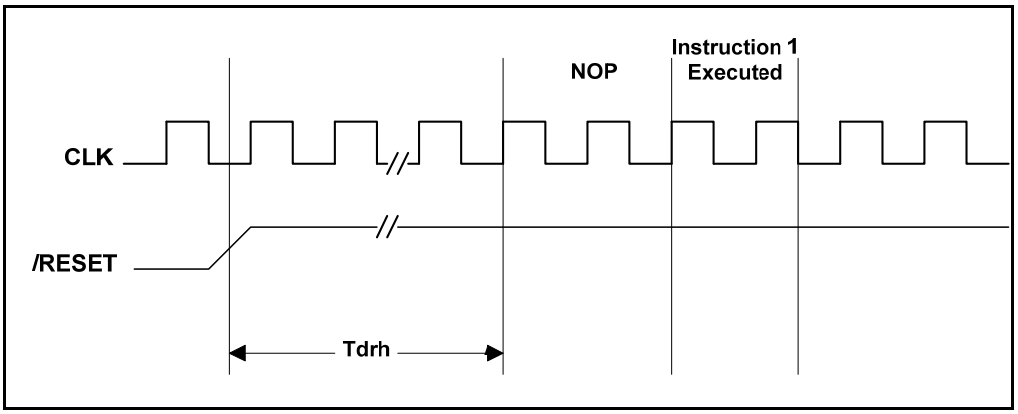


Figure 11-2b Reset Timing Diagram

TCC Input Timing

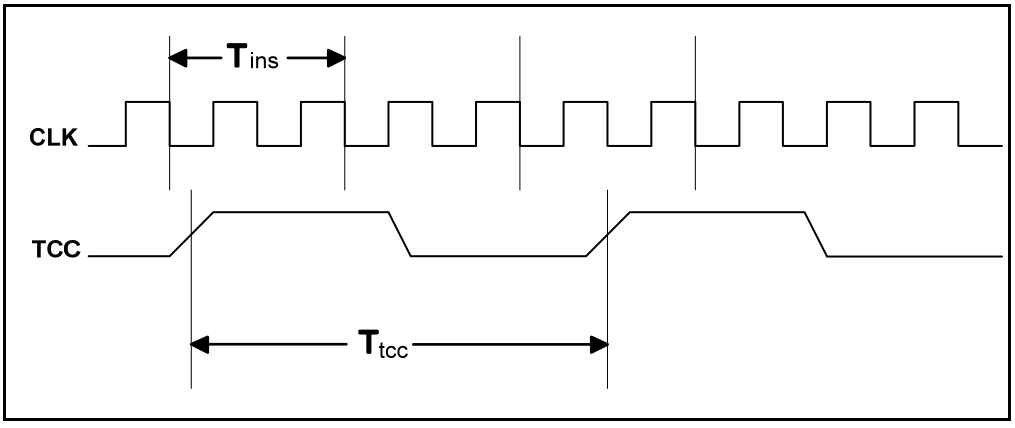


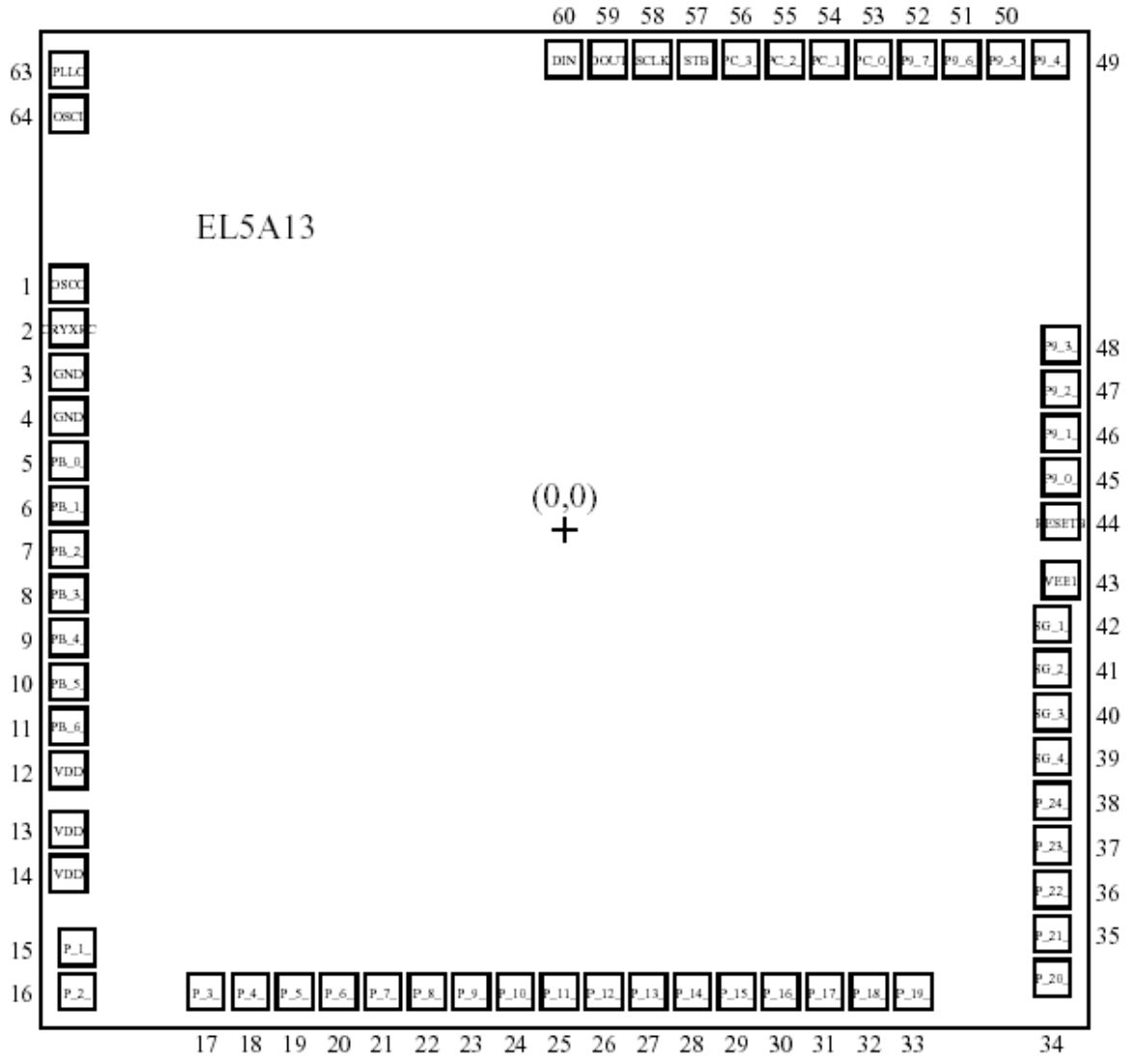
Figure 11-2c TCC Input Timing Diagram

12 Bonding Coordinates Subsidiary

Substrate： P substrate

Chip size ： 2710 *2580 μm

12.1 Pad Configuration



12.2 Pad Name and Coordinates Table

Pin No.	Pad Name	Coordinate (x , y)	Pin No.	Pad Name	Coordinate (x , y)
1	OSCO	-1235.0,611.9	25	P_11 (P75)	12.5,-1148.3
2	CRYXRC	-1235.0,501.9	26	P_12 (P74)	97.5,-1148.3
3	GND	-1235.0,391.8	27	P_13 (P73)	207.5,-1148.3
4	GND	-1235.0,281.9	28	P_14 (P72)	317.6,-1148.3
5	PB_0	-1235.0 ,171.9	29	P_15 (P71)	427.5,-1148.3
6	PB_1	-1235.0 ,61.9	30	P_16 (P70)	537.5,-1148.3
7	PB_2	-1235.0,-48.1	31	P_17 (P67)	647.6,-1148.3
8	PB_3	-1235.0,-158.1	32	P_18 (P66)	757.6,-1148.3
9	PB_4	-1235.0,-268.1	33	P_19 (P65)	867.5,-1148.3
10	PB_5	-1235.0,-378.1	34	P_20 (P64)	1213.3,-1114.0
11	PB_6	-1235.0,-488.1	35	P_21 (P63)	1213.3,-1004.0
12	VDD	-1235.0,-598.1	36	P_22 (P62)	1213.3,-894.0
13	VDD	-1235.0,-744.4	37	P_23 (P61)	1213.3,-784.0
14	VDD	-1235.0,-854.4	38	P_24 (P60)	1213.3,-674.0
15	P_1 (P87)	-1213.3 ,-1038.3	39	SG_4	1213.3,-564.0
16	P_2 (P86)	-1213.3,-1148.3	40	SG_3	1213.3,-454.0
17	P_3 (P85)	-892.5,-1148.3	41	SG_2	1213.3,-344.0
18	P_4 (P84)	-782.5,-1148.3	42	SG_1	1213.3,-234.0
19	P_5 (P83)	-672.5,-1148.3	43	VEE1	1235.0,-124.0
20	P_6 (P82)	-562.5,-1148.3	44	RESETB	1235.0,20.9
21	P_7 (P81)	-452.5,-1148.3	45	P9_0	1235.0,130.9
22	P_8 (P80)	-342.5,-1148.3	46	P9_1	1235.0 ,240.9
23	P_9 (P77)	-232.5,-1148.3	47	P9_2	1235.0,350.9
24	P_10 (P76)	-122.5,-1148.3	48	P9_3	1235.0,460.9

Pin No	Pad Name	Coordinate (x , y)	Pin No	Pad Name	Coordinate (x , y)
49	P9_4	1208.0,1170.0	58	SCLK	218.0,1170.0
50	P9_5	1098.0, 1170.0	59	DOUT	108.0,1170.0
51	P9_6	988.0,1170.0	60	DIN	-2.0,1170.0
52	P9_7	878.0,1170.0	61		
53	PC_0	768.0,1170.0	62		
54	PC_1	658.0,1170.0	63	PLLC	-1235.0,1143.5
55	PC_2	548.0,1170.0	64	OSCI	-1235.0,1033.5
56	PC_3	438.0,1170.0			
57	STB	328.0, 1170.0			

13 Application Circuits

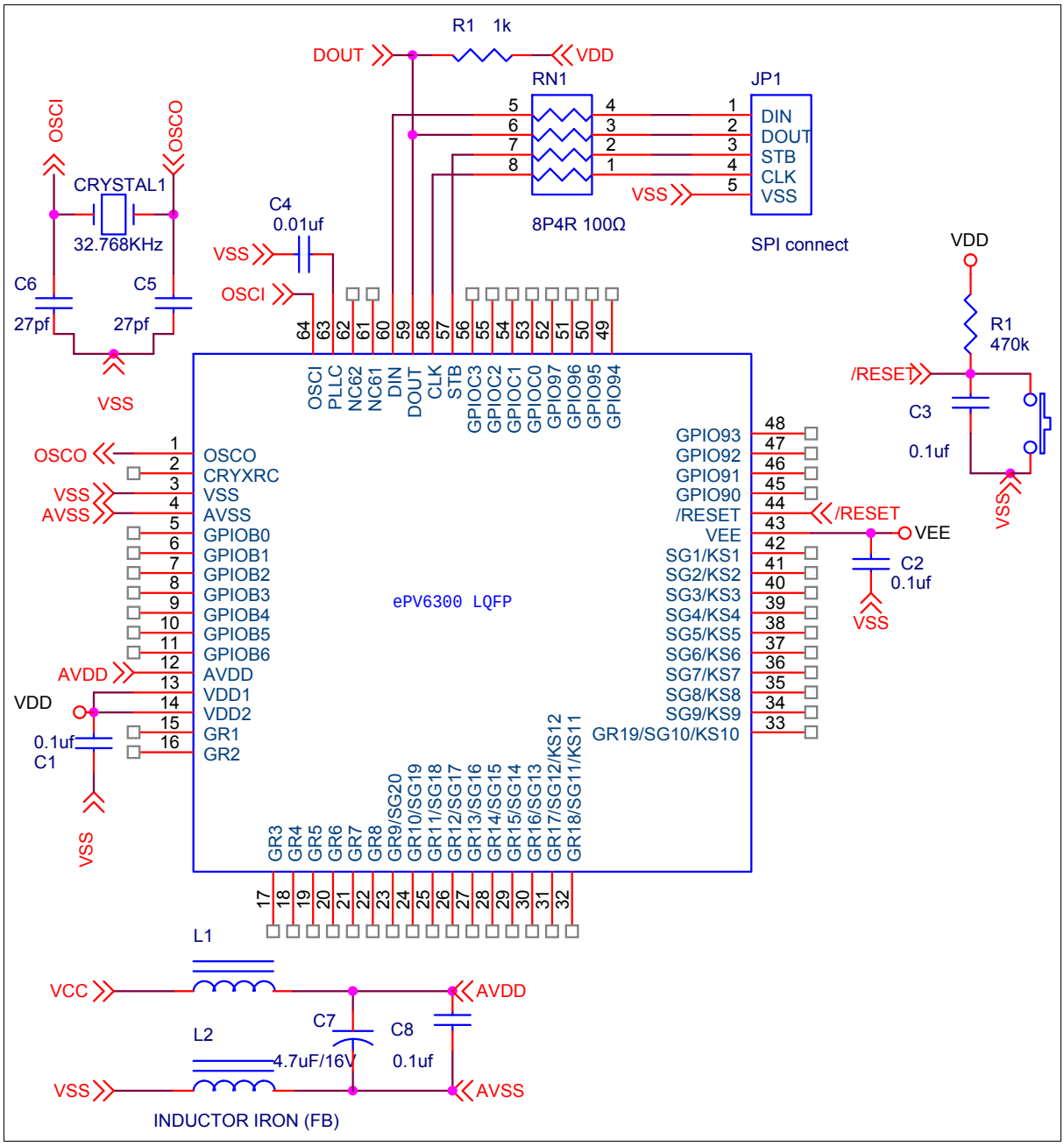
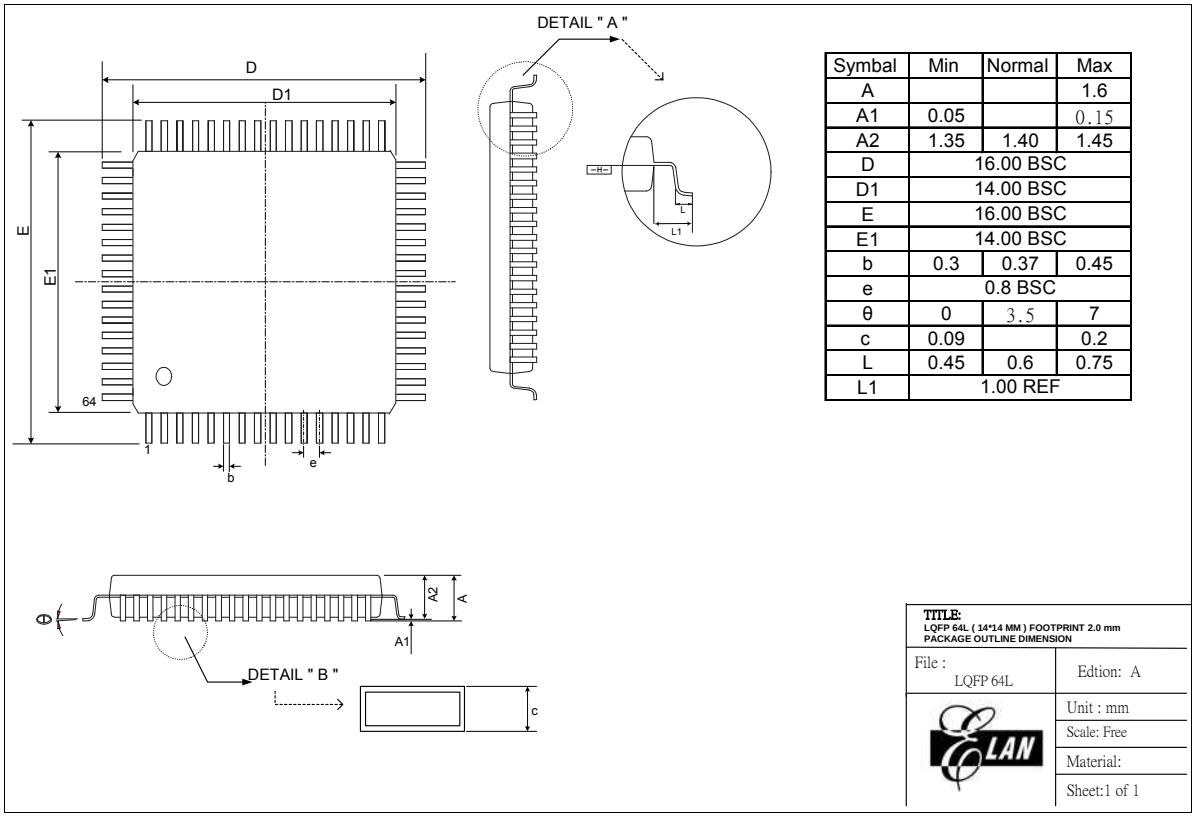


Figure 12-1 ePVP6300 Application Circuits Diagram

14 Package Information

14.1 Package Type: LQFP-64-(14x14)



Symbal	Min	Normal	Max
A			1.6
A1	0.05		0.15
A2	1.35	1.40	1.45
D		16.00 BSC	
D1		14.00 BSC	
E		16.00 BSC	
E1		14.00 BSC	
b	0.3	0.37	0.45
e		0.8 BSC	
θ	0	3.5	7
c	0.09		0.2
L	0.45	0.6	0.75
L1		1.00 REF	

Figure 14-1 LQFP-64 (14×14) Package of ePVP6300