EPD2006

RISC II Series Microcontroller

Product Specification

DOC. VERSION 0.2

ELAN MICROELECTRONICS CORP.

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Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2007/03/27
0.2	1. Added a new circuit on the current consumpiton application. 2. Modified the DC Characteristics for Idle 4 LCD enable condition.	2009/10/14

1 General Description

The **EPD2006** is an 8-bit RISC MCU embedded with the following features**:**

- 10-bit SAR A/D converter with touch screen controller
- Analog front end, 16×56 LCD driver
- Two 8-bit timers and one 16-bit general timer with capture and event counter functions
- Embedded large size user RAM and program/data memory
- Watchdog timer, SPI, UART, and four melody timers
- PWM or current D/A
- IR generator

The **EPD2006** is ideally suitable for educational learning tools application that requires high performance and low cost solution.

The MCU core is ELAN's second generation RISC (RISC II) based IC. The core is specifically designed as a low power and portable device. It supports Fast, Slow, and Idle mode, as well as Sleep mode for low power consumption application.

IMPORTANT NOTES

- *Do not use Register BSR (05h) Bit 7 ~ Bit 3.*
- *Do not use Register BSR1 (07h) Bit 7 ~ Bit 3.*
- *Do not use Special Register (04h).*
- *Do not use Special Register (1Bh).*
- *Do not use Special Register (1Ch).*
- *Do not use Special Register (1Fh).*
- *Do not use Special Register (2Ah).*
- *Do not use Special Register (32h).*
- *Do not use Special Register (33h).*
- *Do not use Special Register (39h).*
- *Do not use Special Register (4Fh).*
- *Do no use LCD RAM Page 00 (18~2Fh, 40h~4Fh, 68~6Fh).*
- *Do not use LCD RAM Page 01 (18~2Fh, 40h~4Fh, 68~6Fh).*
- *Do not use LCD RAM Page 02.*
- *Do not use LCD RAM Page 03.*
- *Do not use LCD RAM Page 04.*
- *Do not use LCD RAM Page 05.*
- *Do not use Port B.3~4.*
- *Do not use Port C.0~1.*
- *Do not use Port D.0~3.*
- *Do not use JDNZ and JINZ at FSR1 (09h) special register.*
- *Do not use Register TABPTRH (0Dh) Bit 6.*

1.1 Applications

- Educational Learning Tools
- Kids PDA, Kids computer
- Electronics book
- Dictionary, Data Bank

2 Features

2.1 MCU Features

- 8 bit RISC MCU
- 8×8 multiplier with controllable signed or unsigned operation
- Operating voltage and speed: 16~11 MHz @ 2.9V~3.6V, 10 MHz @ 2.2V~3.6V
- One Instruction cycle time = 2 × System clock time
- Program ROM addressing: 64K words max.
- Data ROM addressing: 128K words max.
- 128 bytes un-banked RAM including special registers and common registers
- 8×128 bytes banked RAM
- RAM stack has a maximum of 128 levels
- Look-up Table function is fast and highly efficient when implemented with Repeat instruction
- Register-to-Register move instruction
- Compare and Branch in one instruction (2 cycles)
- Single Repeat function (256 repeat times max.)
- Decimal Add and Sub instruction
- Full range Call and Jump capability (2 cycles)

2.2 Peripheral

- One input port (Port A) and 32 general I/O pins (Port B.7~5, Port B.2~0, Port C.7~2, Port D.7~4, Port G ~ Port H)
- 4-channel Melody/Speech Synthesizer
- 16 COM × 56 SEG LCD driver embedded
- 16-bit timer (Timer 0) with capture and event counter functions
- 8-bit timer (Timer 1) with wake-up function
- 8-bit timer (Timer 2) as bit counter for Melody function

- 8-bit IR generator
- 8-bit PWM and a current D/A for melody and speech application
- 8-bit Watchdog Timer
- 10 bits resolution SAR A/D converter with four channels general analog input and two channels for touch panel application
- Key I/O function with 112 keys maximum
- SPI (Serial Peripheral Interface)
- UART (Universal Asynchronous Receiver and Transmitter)

2.3 Internal Specification

- Watchdog Timer with on-chip RC oscillator
- MCU mode: Sleep Mode, Idle Mode, Slow Mode, And Fast Mode
- Supports RC oscillation and crystal oscillation for system clock
- PLL is turned on in Fast Mode, and controlled by the PEN bit when the MCU is in Slow Mode and Idle Mode
- MCU Wake-up function includes input wake up, Timer 1 wake up, touch panel wake up, SPI wake up, and A/D wake up
- MCU interrupt function includes Input port interrupt, touch panel interrupt, Capture interrupt, speech timer interrupt, Timer interrupt (Timers 0~2), A/D interrupt, SPI interrupt and UART interrupt
- MCU reset function includes power-on reset, RSTB pin reset, and Watchdog timer reset

2.4 Elan Software Support (Optional)

- LCD display
- 4-channel Melody or 3-channel Melody + 1-channel Speech
- ADPCM decoder
- ADPCM encoder

3 Block Diagram

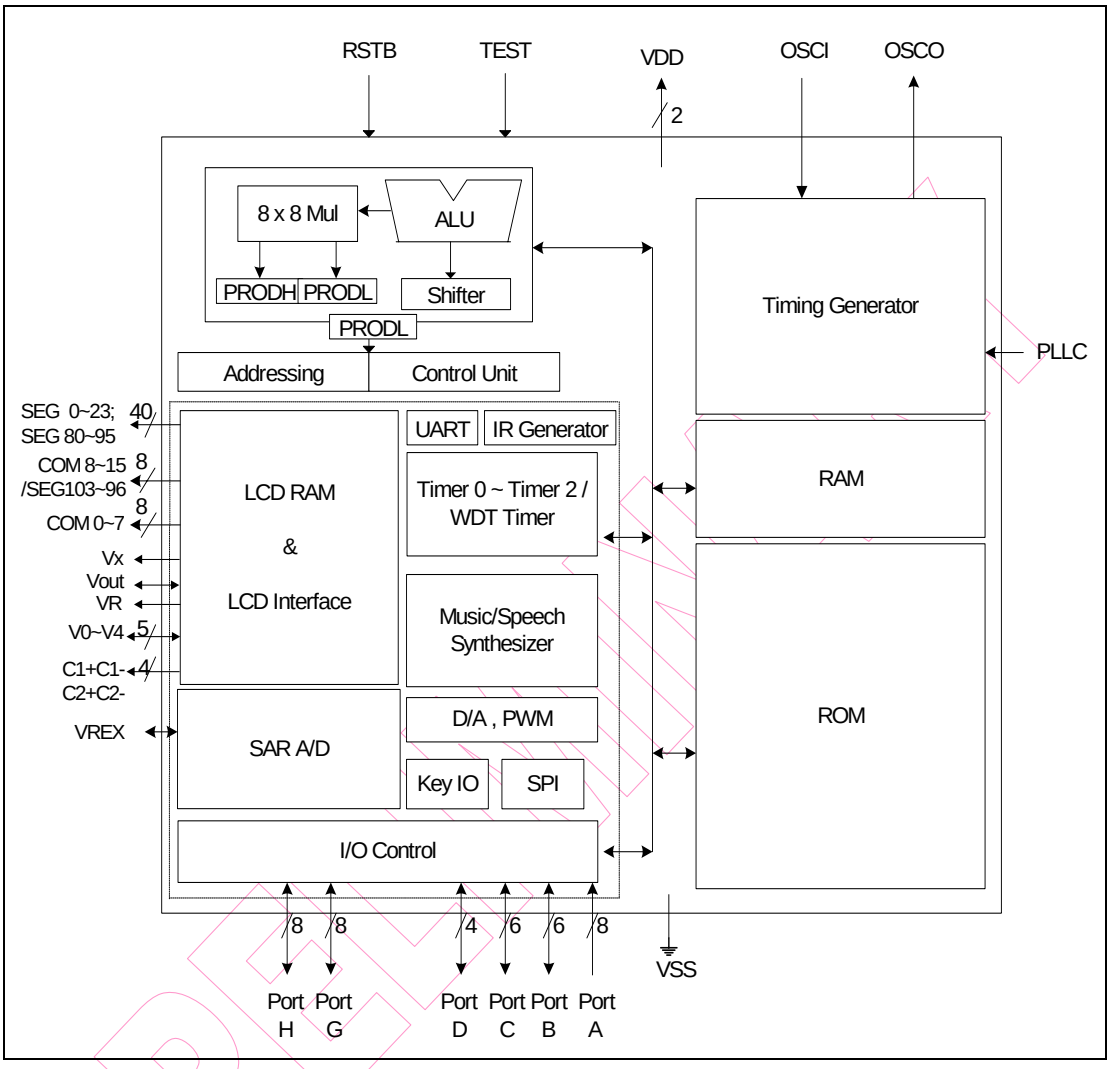
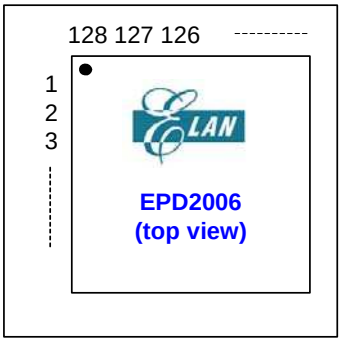


Figure 3-1 EPD2006 Block Diagram

4 Pin Assignment



No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	Port A.0	33	Port B.7 (URXD)	65	N.C.	97	COM4
2	Port A.1	34	Port C.2 (ADIN6)	66	N.C.	98	COM5
3	Port A.2	35	Port C.3 (ADIN5)	67	N.C.	99	COM6
4	Port A.3	36	N.C.	68	N.C.	100	N.C.
5	Port A.4	37	N.C.	69	SEG23	101	N.C.
6	Port A.5	38	N.C.	70	SEG22	102	N.C.
7	Port A.6	39	Port C.4 (ADIN4/YP)	71	SEG21	103	COM7
8	Port A.7	40	Port C.5 (ADIN3/XP)	72	SEG20	104	COM8/SEG103
9	VOUT	41	Port C.6 (YN)	73	SEG19	105	COM9/SEG102
10	C1+	42	Port C.7 (XN)	74	SEG18	106	COM10/SEG101
11	C1-	43	VREX	75	SEG17	107	COM11/SEG100
12	C2+	44	VDD	76	SEG16	108	COM12/SEG99
13	C2-	45	Port D.7 (SPISDI)	77	SEG15 (Strobe 15)	109	COM13/SEG98
14	Vx	46	Port D.6 (SPISDO)	78	SEG14 (Strobe 14)	110	COM14/SEG97
15	VR	47	Port D.5 (SPISCK)	79	SEG13 (Strobe 13)	111	COM15/SEG96
16	V0	48	Port D.4 (SPISS)	80	SEG12 (Strobe 12)	112	SEG80
17	V1	49	Port H.7 (SEG63)	81	SEG11 (Strobe 11)	113	SEG81
18	V2	50	Port H.6 (SEG62)	82	SEG10 (Strobe 10)	114	SEG82
19	V3	51	Port H.5 (SEG61)	83	SEG9 (Strobe 9)	115	SEG83
20	V4	52	Port H.4 (SEG60)	84	SEG8 (Strobe 8)	116	SEG84
21	TEST	53	Port H.3 (SEG59)	85	SEG7 (Strobe 7)	117	SEG85
22	PLLC	54	Port H.2 (SEG58)	86	SEG6 (Strobe 6)	118	SEG86
23	OSCI	55	Port H.1 (SEG57)	87	SEG5 (Strobe 5)	119	SEG87
24	OSCO	56	Port H.0 (SEG56)	88	SEG4 (Strobe 4)	120	SEG88
25	RSTB	57	Port G.7 (SEG55)	89	SEG3 (Strobe 3)	121	SEG89
26	VDD	58	Port G.6 (SEG54)	90	SEG2 (Strobe 2)	122	SEG90
27	Port B.0 (VO2)	59	Port G.5 (SEG53)	91	SEG1 (Strobe 1)	123	SEG91
28	Port B.1 (VO1/DAO)	60	Port G.4 (SEG52)	92	SEG0 (Strobe 0)	124	SEG92
29	VSS	61	Port G.3 (SEG51)	93	COM0	125	SEG93
30	Port B.2 (IROT)	62	Port G.2 (SEG50)	94	COM1	126	SEG94
31	Port B.5 (EVIN/CPIN)	63	Port G.1 (SEG49)	95	COM2	127	SEG95
32	Port B.6 (UTXD)	64	Port G.0 (SEG48)	96	COM3	128	N.C.

5 Pin Description

5.1 MCU System Pins (9 Pins)

Name	I/O/P Type	Description
VDD VSS	P	Digital and Analog positive power supply, ranging from 2.2V~3.6V. Connect to VSS through the 0.1µF capacitor.
RSTB	I	System reset input with built-in pull-up resistor (100KΩ Typical) Low: RESET asserted High: RESET released
TEST	I	Normally connect to VSS, reserved for testing.
OSCI/RC OSCO	I O	RC or Crystal selection by Code Option 32768 Hz oscillator pins. Connect to VSS through the 20pF capacitor. RC oscillator connector pin. Connect to VDD through the 2 MΩ resistor.
PLLC	I	PLL capacitor connector pin. Connect to VSS through the 0.047 µF capacitor.
HOSCI	I	Hi-Speed RC oscillator connecting pin.
VREX	I/O	External or internal reference voltage for A/D converter. Connect to VSS through the 0.1 µF capacitor.

5.2 Embedded LCD Pins (68 Pins)

Name	I/O/P Type	Description
COM0~COM7	O	LCD common/segment signal output pin
COM8~COM15/ SEG103~SEG96	O	LCD common/segment signal output pin Multiplexed: Common and segment pin
SEG0~SEG23 SEG80~SEG95	O	LCD segment signal output pin (SEG0~SEG15 are shared with key strobe)
Vx	-	Clamping circuit output voltage. Ext. C (0.1 µF) to VSS
Vout	-	Charge pump output voltage. Ext. C (0.22 µF) to VSS
VR	-	V0 voltage adjusting pin
V0~V4	O	LCD bias pin. Ext. C (0.1 µF) to VSS
C1+, C1-, C2+, C2-	-	Charge pump capacitor (0.1 µF)

5.3 I/O Ports (40 Pins)

Name	I/O/P Type	Description
Port A	I	General Input port for special functions, i.e., Wake-up and Interrupt Bit 7: ON key input Bits 6~0: Key matrix input pins
Port B (7~5, 2~0)	I/O I O I O O O	General Input/Output port Bit 7: UART Rx pin Bit 6: UART Tx pin Bit 5: Event counter/Capture input pin Bit 2: IR output pin Bit 1: PWM or Current D/A output pin Bit 0: PWM output pin
Port C (7~2)	I/O O O I I I I	General Input/Output port Bit 7: Touch screen X direction negative pin Bit 6: Touch screen Y direction negative pin Bit 5: Touch screen X direction positive pin and A/D Input Channel 3 Bit 4: Touch screen Y direction positive pin and A/D Input Channel 4 Bit 3: A/D input Channel 5 Bit 2: A/D input Channel 6
Port D (7~4)	I/O I O I/O I	General Input/Output port Bit 7: Serial data input pin Bit 6: Serial data output pin Bit 5: Serial clock Input/Output pin Bit 4: /Slave Select pin
Port G	I/O O	General Input/Output port SEG 55~48: LCD segment signal output pins
Port H	I/O O	General Input/Output port SEG 63~56: LCD segment signal output pins

6 Code Option

Located at the address 0x000C~0x0013 of the Program ROM:

- Oscillator (OSCSEL): "RC" oscillator
  "Crystal" oscillator **(Default)**
- Initial mode after reset: "Slow" mode
  "Fast" mode **(Default)**
- Port C.7 function selection bit: "XN for touch panel"
  "General I/O function" **(Default)**
- Port C.6 function selection bit: "YN for touch panel"
  "General I/O function" **(Default)**
- Port C.5 function selection bit: "XP for touch panel/ADIN3"
  "General I/O function" **(Default)**
- Port C.4 function selection bit: "YP for touch panel/ADIN4"
  "General I/O function" **(Default)**
- Port C.3 function selection bit: "ADIN5"
  "General I/O function" **(Default)**
- Port C.2 function selection bit: "ADIN6"
  "General I/O function" **(Default)**
- DAC and PWM function selection bits:

DAC or PWM Function Selection	Port B.0 and Port B.1 Function
DAC is used	Port B.1 is DAO for D/A, Port B.0 is General I/O
PWM is used	Port B.1 is VO1 and Port B.0 is VO2 for PWM
DAC and PWM are prohibited for use	General I/O **(Default)**

- Duty Ratio: Maximum Duty Ratio Option **(1/16, Default)**

COM0~7 ; COM 8-15/SEG 103-96 ; SEG80~95 status setting

Duty Ratio	Display Size (max.)	Common Driver Used		
		COM 0~7	COM 8~15/ SEG 103~96	SEG 95~80
1/4	64 × 4	COM 0~7	SEG103~96	SEG95~80
1/8	64 × 8	COM 0~7	SEG103~96	SEG95~80
1/9	56 × 9	COM 0~15		SEG95~80
1/11	56 × 11	COM 0~15		SEG95~80
1/16	56 × 16	COM 0~15		SEG95~80

- V1; V2; V3 & V4 OP Buffer: "ON (Normal current)" **(Default)**
  "OFF" , "1/3 bias (Small current)"
- V0 OP buffer control bit: "V0 OP buffer turn off"
  "V0 OP buffer turn on" **(Default)**
- Port G low nibble control bits : "LCD segment signal output" **(Default)**
  "General I/O function"
- Port G high nibble control bits : "LCD segment signal output" **(Default)**
  "General I/O function"
- Port H low nibble control bits : "LCD segment signal output" **(Default)**
  "General I/O function"
- Port H high nibble control bits: "LCD segment signal output" **(Default)**
  "General I/O function"
- Select UART standard baud rate: "PLLC frequency is 9.83 MHz" **(Default)**
  "PLLC frequency is 14.745 MHz"
- Read Port A control bit: "Port A connected with LCD-BitST "
  "Port A divided from LCD-BitST" **(Default)**

NOTE

The read Port A control of the code option can be used only on the PMEPD38 or PMEPD33B PM board.

7 MCU System

7.1 Power-up and Reset Timing

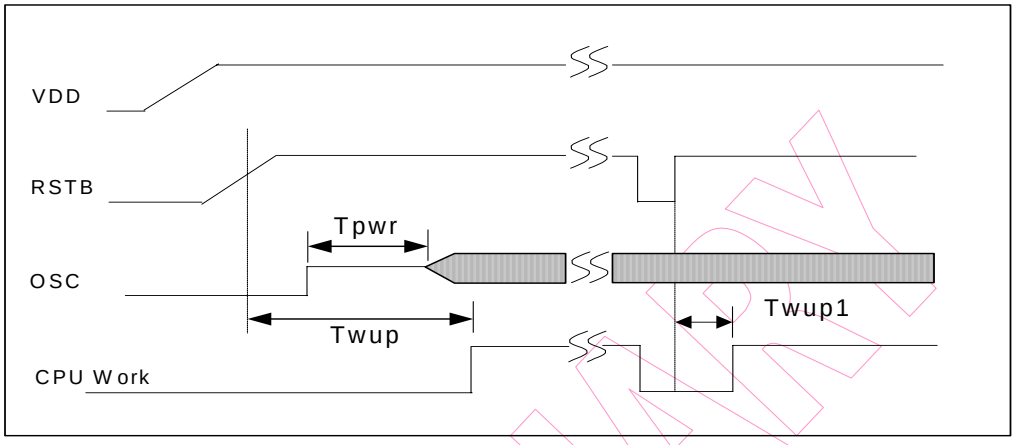


Figure 7-1 Power-up and Reset Timing

Symbol	Characteristics	Min.	Typ.	Max.	Unit
Tpwr	Oscillator start up time	100	226	300	ms
Twup	CPU warm up time	260	340	550	ms
Twup1	CPU reset time	18	22	44	ms

7.2 MCU Operation Timing

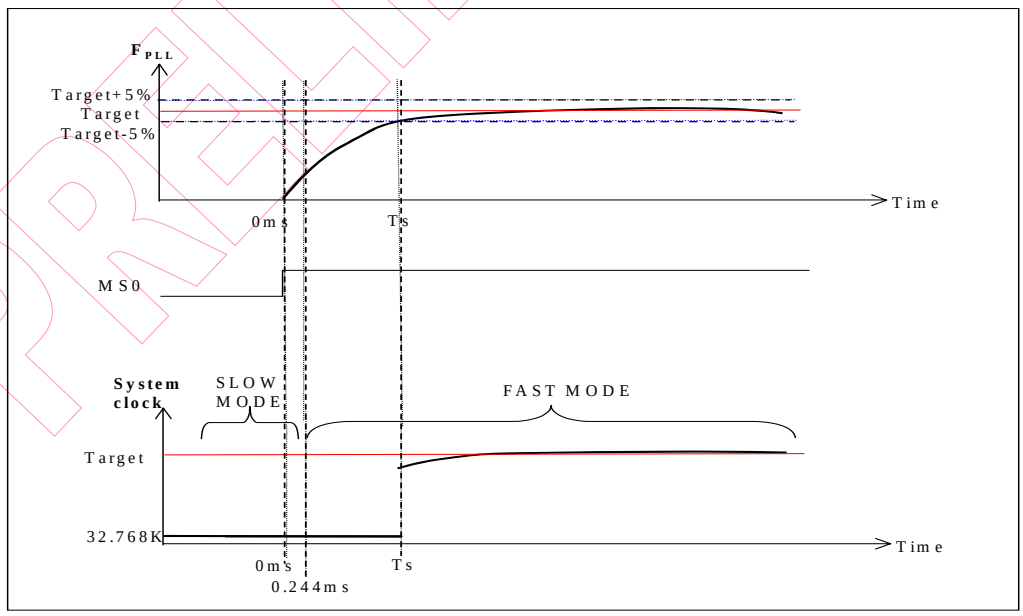


Figure 7-2 MCU Operation Timing Diagram

NOTE

1. *Switch from Slow mode to Fast mode at Time=0ms*
2. *The System clock will switch to FPLL after 8 oscillation clocks, and the system clock will then increase to about hundreds of kHz.*
3. *The PLL frequency will be stable (±5%) at Time=Ts (2ms~5ms).*

8 ROM and RAM

8.1 Program ROM Map

8K Words × 8 Segments = 64K Words	
Address	**Segment**
0000h | 000Bh	Interrupt Vector (12 words)
000Ch | 0013h	Code Option (8 words)
0014h | 001Fh	Test Program (12 words)
0020h | 3FFFh	Segment 0 | Segment 1
4000h | 7FFFh	Segment 2 | Segment 3
8000h | BFFFh	Segment 4 | Segment 5
C000h | FFFFh	Segment 6 | Segment 7

8.2 Data ROM Map

Maximum Size is 128K Words	
Address	
100000h | 11FFFFh	Data ROM (2M bits)

8.3 RAM Map

(RAM Size: 128 Bytes + 8 Banks × 128 Bytes = 1152 Bytes)

■ Other Un-banked Register of RAM:

Address	Un-banked
00h | 1Fh	Special Register
20h | 55h	Control Register
56h | 7Fh	General Purpose RAM

■ Banked Register of RAM: selected by BSR

Address	Bank 0	Bank 1	Bank 2	Bank 3	……..	Bank 7
80h | FFh	General Purpose RAM	General Purpose RAM	General Purpose RAM	General Purpose RAM	……..	General Purpose RAM

8.4 LCD RAM Map

LCD RAM	LCDARH [2:0]	
Address	001 (Page 01)	000 (Page 00)
	COM15~COM8	COM7~COM0
LCDARL	Bit 7 ~ Bit 0	Bit 7 ~ Bit 0
00H (SEG0)		
:		
17H (SEG23)		
18H ~ 2FH	**Not for Use**	
30H (SEG48)		
:		
3FH (SEG63)		
40H ~ 4FH	**Not for Use**	
50H (SEG80)		
:		
67H (SEG103)		

Note: LCDARL = 18F ~ 2F and 40H ~4FH are not for use

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD	-	-0.3 to +3.6	V
Input voltage (general input port)	VIN	-	-0.5 to VDD +0.5	V
Power Dissipation (Topr=70ºC)	PD	-	300	mW
Operating temperature range	TOPR	-	-10 to +70	°C
Storage temperature range	TSTR	-	-55 to +125	°C

9.2 Recommended Operating Conditions

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD	-	2.2 to 3.6	V
	AVDD		2.4 to 3.6	
Input voltage	VIH	-	VDD × 0.9 to VDD	V
	VIL	-	0 to VDD × 0.1	V
A/D full-Scale input span	ADRG	Positive input - Negative input	0 to VREX	V
Operating temperature	TOPR	-	-10 to +70	°C

9.3 DC Electrical Characteristics

Condition: Ta=-10~+70ºC, VDD= 3.0 ± 0.3V

Parameter	Sym.	Condition		Min.	Typ.	Max.	Unit
Clock	Fmain	Main-clock frequency		1	-	16	MHz
	Fsub	Sub-clock frequency	RC OSC	24.6	32.8	41	kHz
			Crystal OSC	-	32.768	-	
Supply Current	Idd1	Sleep mode	VDD = 3V, No load	-	-	1	µA
	Idd2	Idle mode	VDD = 3V RC OSC, LCD disable	-	8	12	
	Idd3		VDD = 3V, Crystal OSC, LCD disable	-	5	8	
	Idd4		Normal current: VDD = 3V, Crystal / RC OSC, LCD enable, Vout = 2VDD, Code Option: V0 and V1~V4 OP On (No load)	-	80	100	
			Small current: VDD = 3V, Crystal / RC OSC, LCD enable (Partial display mode, Vout = VDD) Code Option: V0 OP Off (≤Vdd, external voltage), and V1~ V4 OP On (No load)	-	40	60	
	Idd5	Slow mode	VDD = 3V, LCD disable, RC/Crystal OSC, No load	-	20	30	
	Idd6	Fast mode	VDD = 3V, Fmain = 4 MHz, No load	-	1200	1600	
	Idd7		VDD = 3V, Fmain = 10 MHz, No load	-	2200	2900	
			VDD = 3V, Fmain = 15 MHz, No load	-	3500	4800	
Input Voltage	VIH1	PA[0:7], PB[0:2,5:7], PC[2:7], PD[4:7], PG[0:7] PH[0:7] (as general input port)		VDD×0.7	-	VDD	V
	VIL1			0	-	VDD×0.3	
Input Threshold Voltage (Schmitt)	VT+	RSTB, PB.5 (as EVIN or CPIN)		0.5×VDD	-	0.75×VDD	V
	VT-			0.2×VDD	-	0.4×VDD	

(Continuation)

Parameter	Sym.	Condition		Min.	Typ.	Max.	Unit
Output Current	IOH1	PB[7:6], PB[5], PB[1:0], PC[2:7], PD[7:4] (as general output port),	VDD = 3V, VOH = 2.4V	-1.1	-2.2	-3.3	mA
	IOL1		VDD = 3V, VOL = 0.2V	+1.1	+2.2	+3.3	
	IOH2	PB[1] (as D/A output)	VDD = 3.0V, VOH = 0.7V	-2.5	-3.5	-4.5	
	IOH3	PB[1:0] (as PWM output)	VDD = 3.0V, VOH = 1.5V	-200	-300	-400	
	IOL3		VDD = 3.0V, VOL = 1.5V	+200	+300	+400	
	IOH5	PG[7:0]~PH[0:7]	VDD = 3.0V, VOH = 2.4V	-1.6	-2.6	-3.6	mA
	IOL5		VDD = 3.0V, VOL = 0.2V	+1.1	+2.2	+3.3	mA
	IOH6	PB[2] (as IR output pin)	VDD = 3.0V, VOH = 2.1V	-5	-10	-15	mA
	IOL6		VDD = 3.0V, VOL = 0.9V	+4	+8	+12	mA
Input Leakage Current	IIL	All Input port (without pull up/down resistor) Vin = VDD or GND		-	-	±1	µA
Large Pull up Resistance	RPU1	PA[6:0]	Key high resistance, pulled up by R2, LCD enable (BOOST = 1, normal display mode), Vin = GND, VDD = 3V	100	200	300	KΩ
	RPU3	PA[7], PB[0:2,5:7], PC[2:7], PD[4:7]	Vin = GND, VDD = 3V	300	800	1300	
		PG[7:0]~PH[7:0]	Vin = GND, VDD = 3V	50	150	250	
	RPU5	RSTB	Vin = GND, VDD = 3V	250	500	750	
Small Pull up Resistance	RPU2	PA[6:0]	Key low resistance, pulled up by R1//R2, LCD enable (BOOST = 0, normal display), Vin = GND, VDD = 3V	10	25	40	KΩ
			Key low resistance, pulled up by R1//R2, LCD enable (BOOST = 1, normal display), Vin = GND, VDD = 3V	15	30	45	
	RPU4	PA[7], PB[0:2,5:7], PC[2:7], PD[4:7], PG[0:7], PH[0:7]	Vin = 2V, VDD = 3V	50	100	200	
	RPU6	RSTB	Vin = 2V, VDD = 3V	50	100	200	
Large Pull down Resistance	RPD1	TEST	Vin = VDD, VDD = 3V	250	500	750	KΩ
Small Pull down Resistance	RPD2	TEST	Vin = 1V, VDD = 3V	1.1	2.2	3.3	KΩ
Touch Panel Pull down Resistance	RPD3	DET = 1, Xn pin	Vin = VDD, VDD = 3V	25	50	100	KΩ
Data Retention Voltage	Vret	-		1.6	-	-	V
Power-on Reset Voltage	Vpor	-		1.4	1.5	1.6	V

(Continuation)

Parameter	Sym.	Condition	Min.	Typ.	Max.	Unit
A/D Conversion (VDD = 3.0V, AVDD = 3.0V, Ta = -10 ~ +70℃, Fclk = 12*Fsample)						
Analog Input						
Mux Leakage Current	Imux	On/off leakage current, Vin = 0 or VDD	-	0.1	1	µA
System Performance						
Resolution		-	-	10	-	Bit
Integral Non-Linearity	INL	-	-2	-	+2	LSB
Differential Non-Linearity	DNL	-	-2	-	+2	LSB
Offset Error	OErr	-	-4	-	+4	LSB
Gain Error	GErr	-	-4	-	+4	LSB
Missing Code	MC	-	No missing code			Bit
AVDD Supply Current	Ivdd3	AVDD = 3.0V, VDD = 3.0V, Fsample = 20kHz, ADEN = 1, VRS = 1	-	0.5	0.7	mA
	Ivdd4	ADEN = 0, VRS = 1	-	-	1	µA
Driver Current	IOH	Xp, Yp (VDD = 2.9 ± 0.3V) (Voh = VDD - 0.2V)	-20	-30	-45	mA
Sink Current	IOL	Xn, Yn (VDD = 2.9 ± 0.3V) (Vol = 0.2V)	+20	+30	+45	mA
Reference Voltage						
Internal Reference Voltage	VRIN	AVDD = 3.0 ± 0.3V	1.8	2.0	2.2	V
Internal Reference Supply Current	Ivrin	VDD = 3.0V, AVDD = 3.0V, VRS = 0, VOH = 0.2V	400	500	-	µA
VREX input current	Iref1	ADEN = 1, VRS = 1	-	300	500	µA
	Iref2	ADEN = 0, VRS = 1	-	-	1	µA
LCD Driver						
Reference Voltage	Vref1	Ta = 20℃ *1	2.035	2.12	2.205	V
	Vref2	Ta = 0℃ *1	2.169	2.26	2.351	V
	Vref3	Ta = 40℃ *1	1.900	1.98	2.060	V
Charge Pump Output	Vout	2 times pumping Capacitance of charge pump C1: 0.1µF	2*Vdd-5%	2*Vdd	-	V
		3 times pumping Capacitance of charge pump C1 and C2: 0.1µF	3*Vx-5%	3*Vx	-	V
Clamping Voltage	Vx	BOOST = 0, 2 times pumping	-	Vdd	-	V
		BOOST = 1, 3 times pumping	2.3	2.4	2.5	
Regulated Voltage	V0	VDD = 2.3V~3.3V, Ta = 25℃	V0-10%	V0 *1	V0+10%	V

Parameter	Sym.	Condition		Min	Typ	Max	Unit
LCD Display Output ON-Resistance	ROC	Com[0:15]	VOH=V0±0.2V	1	2	3	KΩ
			VOM=V1±0.2V				
			VOM=V4±0.2V				
			VOL=0.2V				
	ROS	Seg [0:23, 48:63, 80:103]	VOH=V0±0.2V	1	2	3	KΩ
			VOM=V2±0.2V				
			VOM=V3±0.2V				
			VOL=0.2V				
Strobe Output ON-Resistance	ROP	Seg [0:15] (as key strobe)	V=VDD-0.2V	45	70	100	KΩ
	RON		V=0.2V	0.7	1.0	1.5	
Display Frame Frequency	Frame	Sub-Clock : RC OSC		48	-	100.5	Hz
		Sub-Clock : Crystal OSC		64	-	80.4	
Op. Amp Voltage Output of LCD Power Supply	Vout0	V0	No load	-*2	V0 *1	-*2	mV
	Vout1	V1		-*2	V1 *1	-*2	
	Vout2	V2		-*2	V2 *1	-*2	
	Vout3	V3		-*2	V3 *1	-*2	
	Vout4	V4		-*2	V4 *1	-*2	

*1: V0~V4 Theoretical value

*2: The Target value of V1~V4, Vlcd is Theoretical value ± 50mV

Typically regulated voltage for V0 is chosen by software from the following table:

Bias	V0	V1	V2	V3	V4
1/3	V0	2/3 * V0	1/3 * V0	2/3 * V0	1/3 * V0
1/3.5		2.5/3.5 * V0	1.5/3.5 * V0	2/3.5 * V0	1/3.5 * V0
1/4		3/4 * V0	2/4 * V0	2/4 * V0	1/4 * V0
1/4.5		3.5/4.5 * V0	2.5/4.5 * V0	2/4.5 * V0	1/4.5 * V0
1/5		4/5 * V0	3/5 * V0	2/5 * V0	1/5 * V0
1/5.5		4.5/5.5 * V0	3.5/5.5 * V0	2/5.5 * V0	1/5.5 * V0
1/6		5/6 * V0	4/6 * V0	2/6 * V0	1/6 * V0
1/6.5		5.5/6.5 * V0	4.5/6.5 * V0	2/6.5 * V0	1/6.5 * V0

9.4 AC Electrical Characteristics

(Condition: Ta = -10~+70℃, VDD = 3.0 ± 0.3V)

Parameter	Sym.	Condition	Min.	Typ.	Max.	Unit
Instruction Cycle Time	Tcycle	Fmain = 1 MHz	-	2*1	-	μs
		Fmain = 4 MHz	-	0.5*1	-	
		Fmain = 10 MHz	-	0.2*1	-	
		Fmain = 15 MHz	-	0.13*1	-	
A/D Conversion (VDD = 3.0V, AVDD = 3.0V, Ta = -10 ~ + 70℃)						
Throughput Rate	-	VDD = 3.0V, AVDD = 3.0V	-	-	80	ksps
		VDD = 2.4V, AVDD = 2.4V	-	-	60	
Power Supply Rejection Ratio	PSRR1+	Power noise: 1kHz, 100mV	37	40	-	dB
	PSRR1-	Power noise: 1kHz, 100mV	43	46	-	
Signal to Noise Ratio	SNR	-	51	54	-	dB

*1: Instruction cycle time = 2 × System clock time

10 Application Circuits

(1) Elan Product

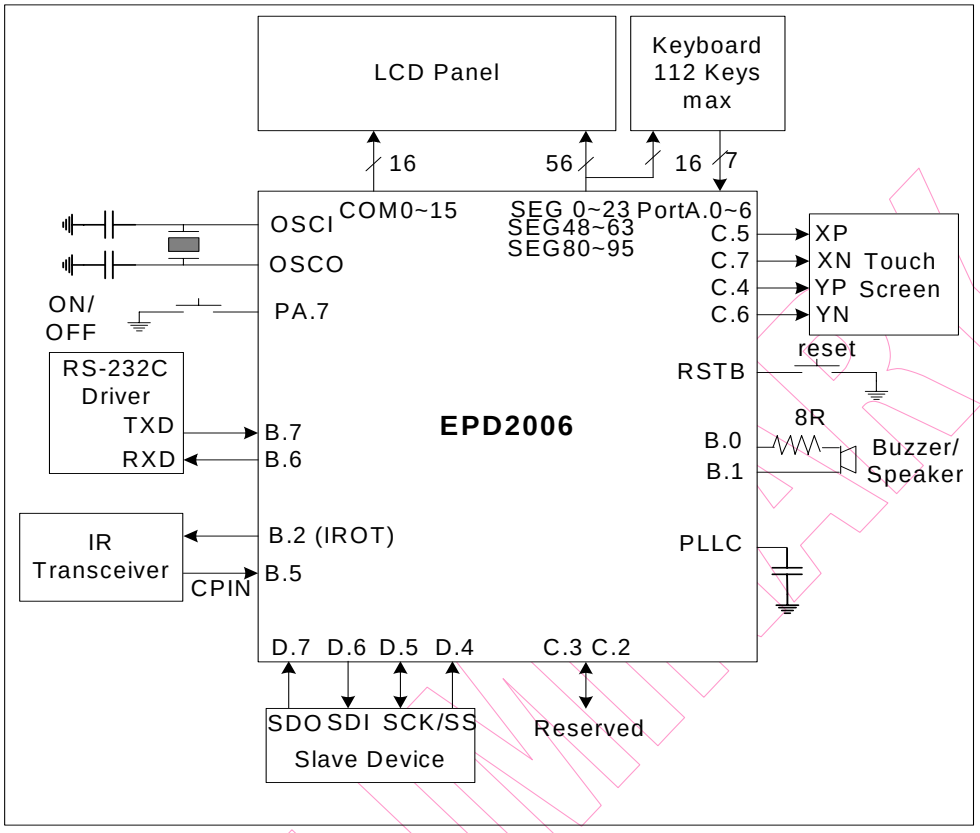


Figure 10-1 Application Circuit Diagram 1

(2) 16×56 pixels driving application circuits (“Single-chip” using internal oscillator)

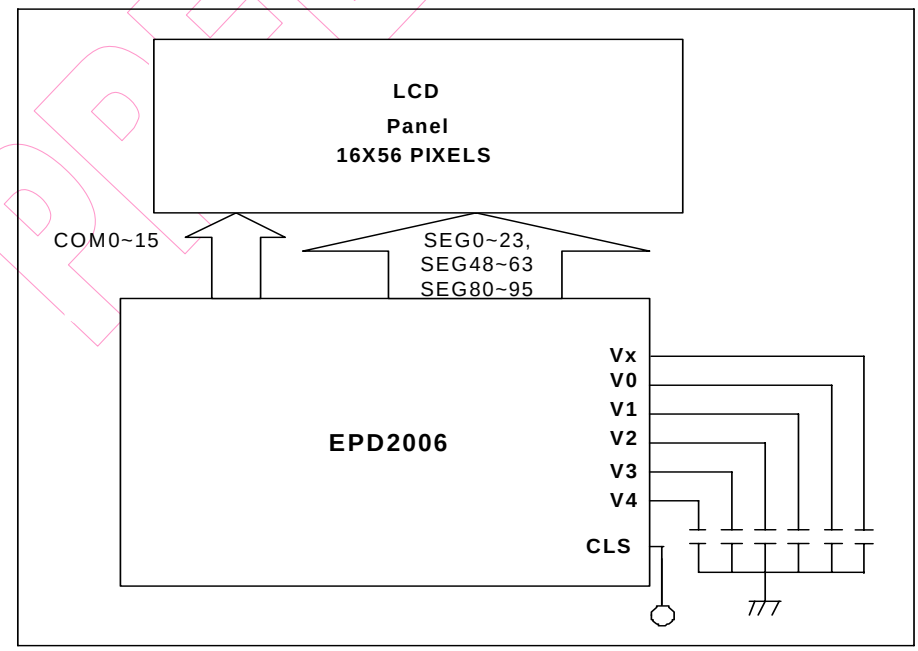


Figure 10-2 Application Circuit Diagram 2