EM78P862A

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.1

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2001/03/02
1.1	Modified the OTP write pin address.	2006/10/12

1 General Description

The EM78P862A is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single chip are on-chip Watchdog Timer (WDT), RAM, ROM, programmable real time clock/counter, internal interrupt, power down mode, LCD driver and tri-state I/O. The EM78P862A provides a single chip solution for designing a Data-Bank message display.

2 Features

CPU

- Operating voltage range: 2.5V ~ 5.5V
- 16K×13 on chip Electrical One Time Programmable Read Only Memory (OTP-ROM)
- 2.2K×8 on chip RAM
- Up to 29 bidirectional tri-state I/O ports
- 8-level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- Two sets of 8 bit counters can be interrupt sources
- Programmable free running on-chip watchdog timer
- Four modes (internal clock: 3.579MHz)
  - Sleep mode: CPU and 3.579 MHz clock turned off, 32.768kHz clock turned off
  - Idle mode: CPU and 3.579 MHz clock turned off, 32.768kHz clock turned on
  - Green mode: 3.579 MHz clock turned off, CPU and 32.768kHz clock turned on
  - Normal mode: 3.579 MHz clock turned on, CPU and 32.768kHz clock turned on
- Input port wake-up function
- Seven interrupt sources: 4 external, 3 internal
- Eight R-option pins
- 100-pin QFP (EM78P862AQ) or 84-pin chip (EM78P862AH)
- Port key scan function
- Clock frequency: 32.768kHz

LCD

- LCD operation voltage is chosen by software
- Common driver pins: 9
- Segment driver pins: 60
- 1/4 bias
- 1/8, 1/9 duty

3 Application

Data bank

Message display box

4 Pin Configuration

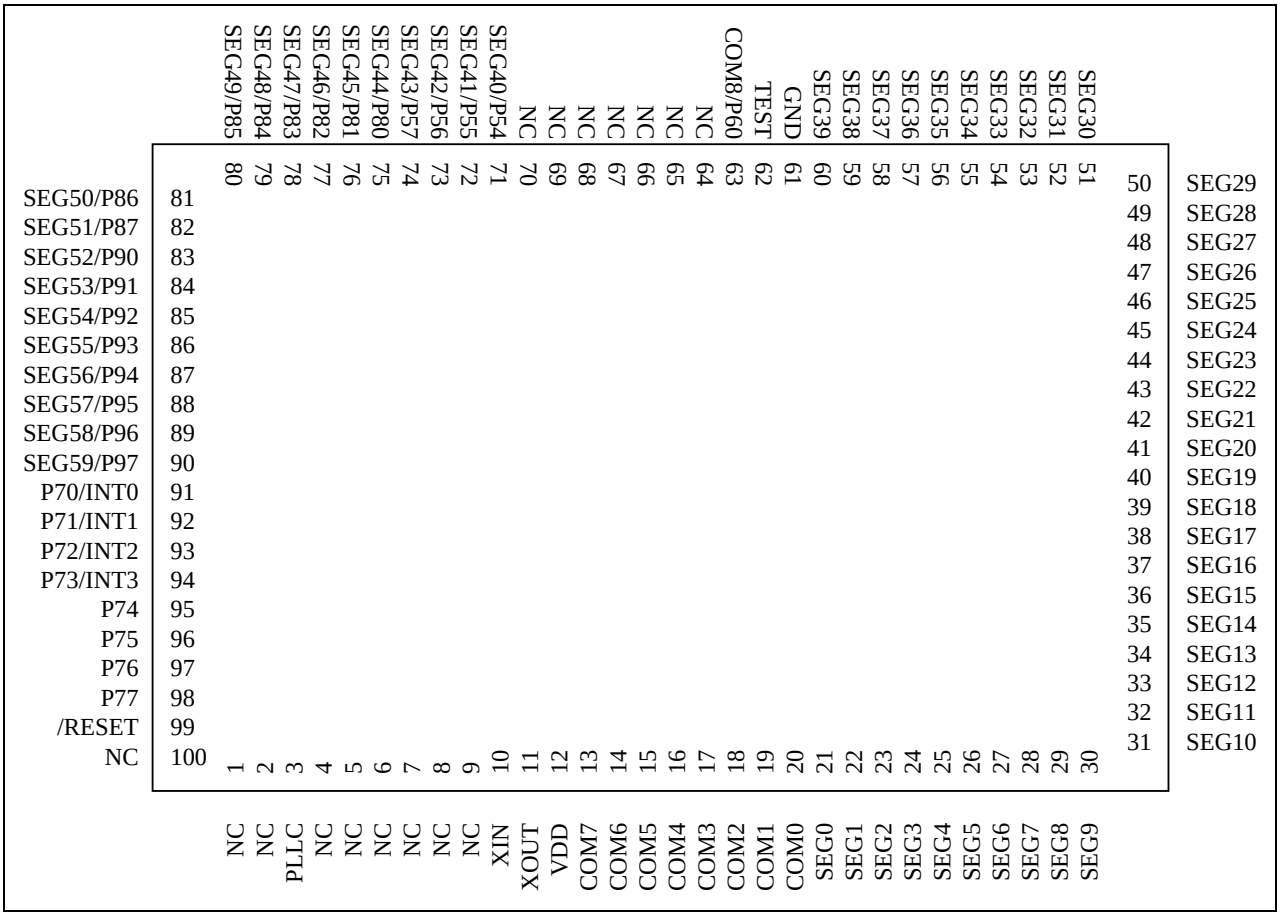


Fig. 4-1 Pin Assignment

OTP Writer Pin Name	Mask ROM Pin Name (Use ELAN writer)	Mask ROM Pin Name (Factory Test, QTP)
1. VDD	VDD	VDD
2. VPP	/RESET	/RESET
3. DINCK	P77	P77
4. ACLK	P76	P76
5. PGMB	P75	P75
6. OEB	P74	P74
7. DATA	P73	P73
8. GND	TEST	GND, TEST

5 Functional Block Diagram

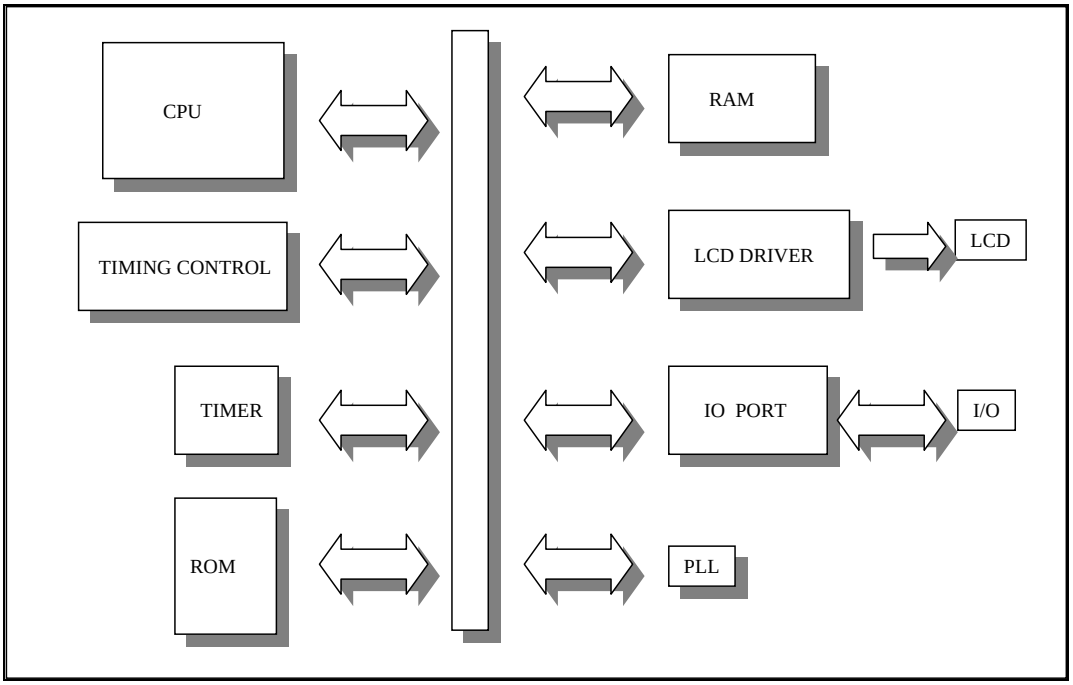


Fig. 5-1 Block Diagram 1

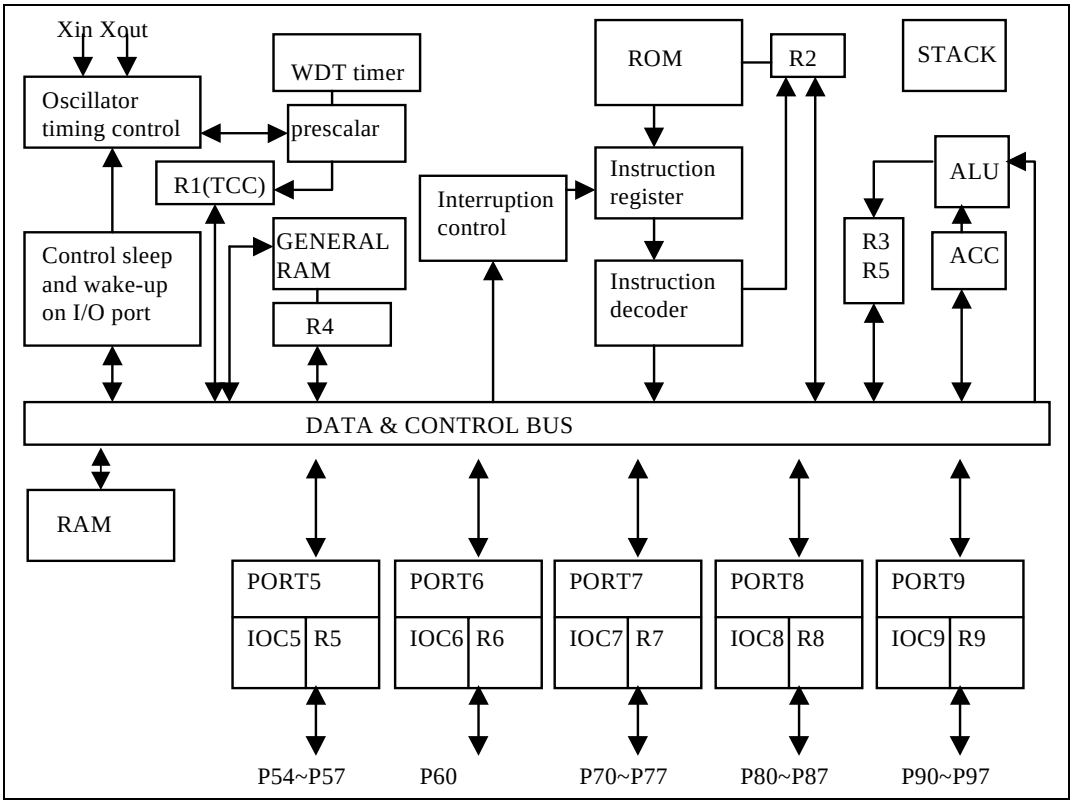


Fig. 5-2 Block Diagram 2

6 Pin Description

Pin	I/O	Description
VDD	Power	Digital power Analog power
GND	Power	Digital ground Analog ground
Xtin	I	Input pin for 32.768 kHz oscillator
Xtout	O	Output pin for 32.768 kHz oscillator
COM0..COM8	O	Common driver pins of LCD drivers
SEG0...SEG43 SEG44..SEG51 SEG52..SEG59	O O (Port 8) O (Port 9)	Segment driver pins of the LCD drivers Port 9 Function Key can wake up the Watchdog Timer.
PLLC	I	Phase lock loop capacitor. Connect a 0.01µ to 0.047µ capacitor with AVSS
INT0 INT1 INT2 INT3	Port 7 (0) Port 7 (1) Port 7 (2) Port 7 (3) Port 7 (4:7)	Port 7 (0) ~ Port 7 (3) signals can be interrupt signals. I/O port
P54 ~P57	Port 5	Each bit in Port 5 can be Input or Output port. These are pin-shared with LCD segment signals.
P60	Port 6	Port 6 can be Input or Output port. These are pin-shared with LCD common signals
P70 ~P77	Port 7	Each bit in Port 7 can be Input or Output port. Internal Pull-high function Key scan function
P80 ~P87	Port 8	Each bit in Port 8 can be Input or Output port. These are pin-shared with LCD segment signals.
P90 ~P97	Port 9	Each bit in Port 9 can be Input or Output port. These can be set to wake up the Watchdog Timer. These are pin-shared with LCD segment signals.
TEST	I	Test pin into test mode, normal low
RESET	I	–

7 Function Description

7.1 Operational Registers

R0 (Indirect Addressing Register)

- R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

R1 (TCC)

- Incremented by an external signal edge (16.384kHz) applied to TCC, or by the instruction cycle clock.
- Written and read by the program as any other register.

R2 (Program Counter)

- The structure is depicted in Fig. 7-1
- Generates 16K×13 on-chip ROM addresses to the relative programming instruction codes
- "JMP" instruction allows direct loading of the low 10 program counter bits
- "CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of the stack.
- "MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".
- * "ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".
- "TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A13) will be loaded with the contents of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

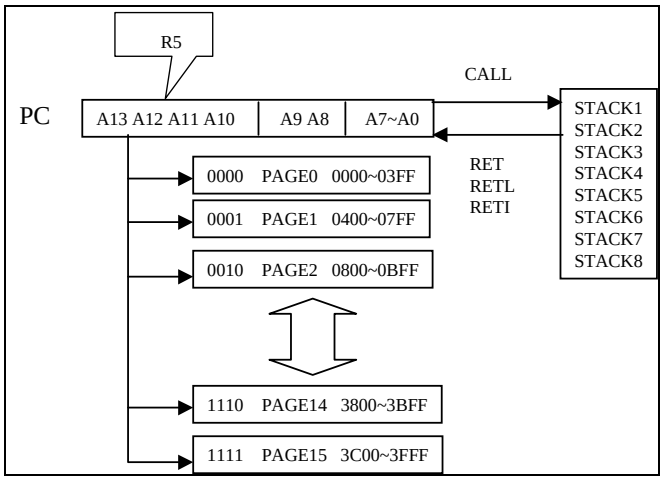


Fig. 7-1 Program Counter Organization

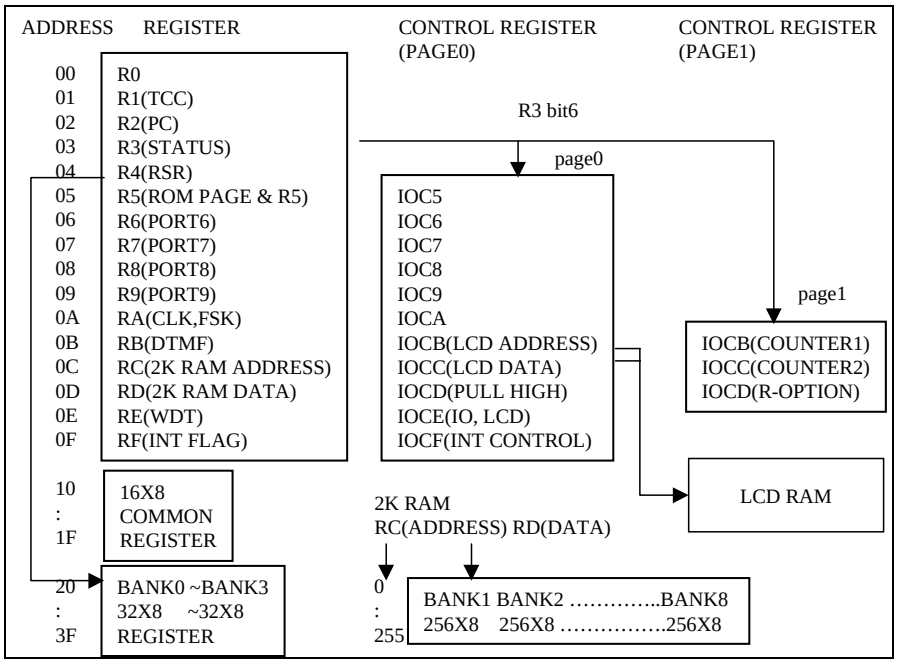


Fig. 7-2 Data Memory Configuration

R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PAGE	-	T	P	Z	DC	C

Bit 0 (C) Carry flag

Bit 1 (DC) Auxiliary carry flag

Bit 2 (Z) Zero flag

Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT timeout.

Event	T	P	Remark
WDT wake up from sleep mode	0	0	–
WDT time out (not sleep mode)	0	1	–
/RESET wake up from sleep	1	0	–
power up	1	1	–
Low pulse on /RESET	x	x	x : don't care

Bit 5 unused

Bit 6 Page: change IOCB ~ IOCE to another page, 0/1 → Page 0 / Page 1

Bit 7 unused

R4 (RAM Select Register)

Bits 0 ~ 5 are used to select up to 32 registers in the indirect addressing mode.

Bits 6 ~ 7 determine which bank is activated among the four banks.

See the data memory configuration in Fig. 7-2.

R5 (Program Page Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R57	R56	R55	R54	PS3	PS2	PS1	PS0

Bit 0 (PS0) ~ 3 (PS3) Page select bits

Page select bits

PS3	PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
:	:	:	:	:
1	1	1	0	Page 14
1	1	1	1	Page 15

User can use the PAGE instruction to change page, or to maintain user's program page. The program page is maintained by ELAN's compiler. It will change user's program by inserting instructions within the program.

Bits 4~7: 4-bit I/O register of Port 5

R6 ~ R9 (Port 6 ~ Port 9): Four 8-bit I/O registers

RA (Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDLE	/358E	**0**	**1**	0	-	-	-

Bit 0 ~Bit 2: unused

Bit 3: reserved, clear this bit to '0'

Bit 4: reserved, set as '1' always

Bit 5: reserved, clear this bit to '0'

Bit 6 (read/write) (PLL enable signal)

0 : Disable

1 : Enable

The relation between 32.768K and 3.579M is shown in Fig.7-3.

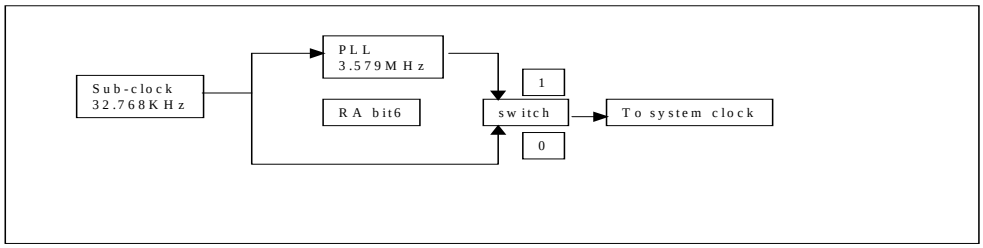


Fig. 7-3 Relation between 32.768kHz and 3.579MHz

Bit 7 Idle: Sleep mode selection bit

0 : Sleep mode

1 : Idle mode. This bit will determine as to which mode will be set using the SLEP instruction.

These two modes can be awakened by TCC clock or Watchdog or Port 9 and run from "SLEP" next instruction.

Wakeup Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
WDT time out	RESET	Wake-up + Next instruction	RESET	RESET
Port 9	RESET	Wake-up + Next instruction	X	X
Ports 70~73	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt

P70 ~ P73's wake-up function is controlled by IOCF (1, 2, 3) and ENI instruction.

P70's wake-up signal is a rising or falling signal defined by Cont Register Bit 7.

Port 9, Port 71, Port 72 and Port 73's wake-up signal is a falling edge signal.

RB (reserved)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	1	1	1	1

Reserved, set to '1' from Bit 7 to Bit 0.

RC (2K RAM's Address) (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAMA7	RAMA6	RAMA5	RAMA4	RAMA3	RAMA2	RAMA1	RAMA0

Bit 0 ~ Bit 7 select data bank RAM address up to 256. IOCA is the register for bank selection.

RD (2K RAM's data, Read/Write)

Bit 0 ~ Bit 8 are 2K RAM's data transfer register.

User can check the IOCA register as to how to select the RAM bank.

RE (LCD Driver, WDT Control, Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	/WDTE	/WUP9H	/WUP9L	0	LCD_C2	LCD_C1	LCD_M

Bit 0 (LCD_M): LCD_M determines the methods, including the duty cycle.

Bit 1~Bit 2 (LCD_C#): LCD_C# determines the LCD display enable or blanking

LCD_C2,LCD_C1	LCD Display Control	LCD_M	Duty Bias
0 0	**Change the duty cycle** **Disable (turn off the LCD)**	**0** **1**	**1/9 1/4** **1/8 1/4**
0 1	Blanking	:	:
1 1	LCD display enable	:	:

Bit 3: Reserved, clear this bit to '0'

Bit 4 (/WUP9L, Port 9 low nibble Wake-up Enable): used to enable the wake-up function of the low nibble in Port 9.

0 : Disable

1 : Enable

Bit 5 (/WUP9H, Port 9 high nibble Wake-up Enable): used to enable the wake-up function of the high nibble in Port 9.

0 : Disable

1 : Enable

Bit 6 (/WDTE, Watchdog Timer Enable)

Control bit used to enable the Watchdog timer.

0 : Disable

1 : Enable

The relation between Bit 4 to Bit 6 is shown in Fig. 7-9.

Bit 7: Reserved, clear this bit to '0'

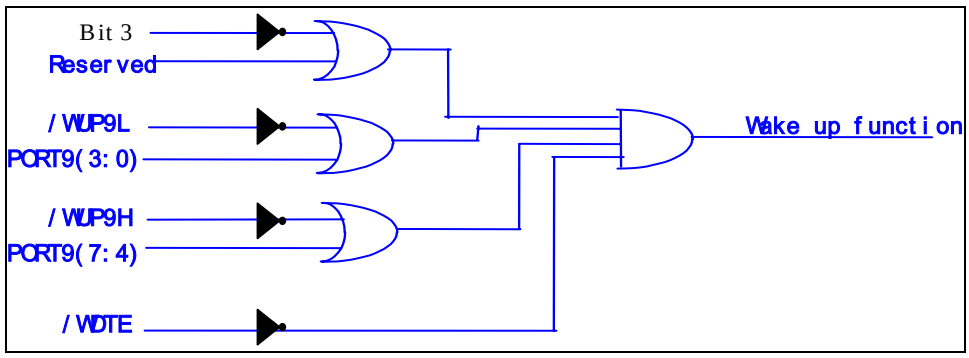


Fig. 7-4 Wake-up Function and Control Signal

RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT3	-	C8_2	C8_1	INT2	INT1	INT0	TCIF

0 : means no interrupt request

1 : means with interrupt request

- **The register can be written with"0" by user only, written with a "1" by hardware when interrupt occurs.**

Bit 0 (TCIF) TCC timer overflow interrupt flag. Set when TCC timer overflows.

Bit 1 (INT0): external INT0 pin interrupt flag

Bit 2 (INT1): external INT1 pin interrupt flag

Bit 3 (INT2): external INT2 pin interrupt flag

Bit 4 (C8_1): internal 8-bit counter interrupt flag

Bit 5 (C8_2): internal 8-bit counter interrupt flag

Bit 6: unused

Bit 7 (INT3): external INT3 pin interrupt flag

NOTE

1. *For High to low edge trigger, refer to Section 7.6 Interrupt.*
2. *IOCF is the interrupt mask register. User can read and clear this bit.*
3. *Don't use the "BC" instruction to clear the interrupt flag in the interrupt subroutine. It is possible to clear other interrupt flag if other interrupts occur at the same time. Use the "MOV" instruction of the following steps:*

In "INT1" interrupt subroutine

```
MOV     A,@0B11111011
MOV     RF,A
```

R10~R3F (General Purpose Register)

R10~R3F (Banks 0~3) all are general purpose registers**.**

7.2 Special Purpose Registers

A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. It is not an addressable register.

CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	–	PAB	PSR2	PSR1	PSR0

Bit 0 (PSR0) ~ Bit 2 (PSR2): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB): Prescaler assignment bit

0 : TCC

1 : WDT

Bit 4 (TE): TCC signal edge. Unused bit.

Bit 5 (TS) TCC signal source

0 : internal instruction cycle clock (System clock/2)

1 : 16.384kHz (32.768kHz/2)

Bit 6 (INT): INT enable flag

0 : interrupt masked by DISI or hardware interrupt

1 : interrupt enabled by ENI/RETI instructions

Bit 7: INT_EDGE

0 : P70 's interrupt source is a rising edge signal

1 : P70 's interrupt source is a falling edge signal

NOTE

The CONT register is readable and writable

T = (2 / System clock) × Prescaler × Count value

IOC5 (I/O Port Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	0	0	0	P5S

Bit 0: P5S is switch register for I/O port or LCD signal switching.

0 : Normal I/O port

1 : Segment output

Bits 1~3: unused

Bit 4 to Bit 7 are Port 5 I/O direction control registers

0 : set the relative I/O pin as output

1 : set the relative I/O pin into high impedance

IOC6 (I/O Port Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	**0**	**0**	**0**	**0**	**0**	**0**	**IOC60**

Bit 0 is I/O direction control register

0 : set the relative I/O pin as output

1 : set the relative I/O pin into high impedance

Bit 1 to Bit 7: Reserved, clear these bits to '0'

NOTE

User can check the IOCE (Bit 5) register on how to switch Port 6 to normal I/O port.

IOC7 ~ IOC9 (I/O Port Control Register): Three I/O direction control registers

0 : set the relative I/O pin as output

1 : set the relative I/O pin into high impedance

NOTE

User can check the IOCA, IOCE (Bits 6, 7) register on how to switch Port 8, Port 9 to normal I/O port.

IOCA (2K RAM, I/O, Page Control Register) (Read/Write, Initial is "00000000")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8SH	P8SL	0	**0**	CALL_3	CALL_2	CALL_1	0

Bit 0: unused

Bit 3~Bit 1: "000" to "111" are eight blocks of 2K RAM area. User can use 2K RAM with RD RAM address**.**

Bit 4: Reserved, clear this bit to 0

Bit 5: unused

Bit 6: Port 8 low nibble switch

0 : normal I/O port

1 : segment output

Bit 7: Port 8 high nibble switch

0 : normal I/O port

1 : segment output

IOCB (LCD Address, Counter 1 Preset Register)

Page 0 : (LCD Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	LCDA6	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

Bit 6 ~ Bit 0 : LCDA6 ~ LCDA0

The LCD display data is stored in the data RAM. The relationship between the data area and the COM/SEG pin is shown below:

COM8	COM7 ~ COM0	
40H (IOCC Bit 0)	00H (IOCC Bit7 ~ Bit0)	**SEG0**
41H	01H	**SEG1**
:	:	**:**
:	:	**:**
:	:	**:**
:	:	**:**
7AH	4AH	**SEG58**
7BH	3BH	**SEG59**
7CH	3CH	**Empty**
:	:	**:**
7FH	3FH	**Empty**

Bit 7 : Unused. Fixed at "0".

NOTE

Writable only when LCD is enabled. Read/Write when disable.

Page 1: (Counter 1 Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C1D7	C1D6	C1D5	C1D4	C1D3	C1D2	C1D1	C1D0

Bit 7 ~ Bit 0: 8 bit up-counter (Counter 1) preset and read out register (write = preset). After an interrupt, it will count from "00".

IOCC (LCD Data, Counter 2)

Page 0: (LCD Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0

Bit 7 ~ Bit 0: LCD RAM data register

Page 1: (Counter 2 Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2D7	C2D6	C2D5	C2D4	C2D3	C2D2	C2D1	C2D0

Bit 7 ~ Bit 0: 8 bit up-counter (Counter 2) preset and read out register (write = preset). After an interrupt, it will count from "00"

IOCD (Pull-high Control Register, R-Option Register)

Page 0: (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70

Bits 0 ~ 7 (PH70~PH77): Control bit used to enable the pull-high of Port 7(#) pin

0 : Disable internal pull-high

1 : Enable internal pull-high

Page 1: (R-Option Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RO7	RO6	RO5	RO4	RO3	RO2	RO1	RO0

Bit 7 ~ 0 (RO7~0): Control bit used to enable the R-Option of Port 97~Port 90 pin

0 : Disable R-Option

1 : Enable R-Option

RO is used for R-Option. Setting RO to '1' will enable the status of R-option pin (P90 ~ P97) to read by controller. Clearing RO will disable the R-option function. If the R-option function is used, user must set the pin as input and connect Port 9 pins to GND by 560K external resister. If the resistor is connected / disconnected, R9 will read as "0/1" when RO is set to '1'.

When R-Option function is enabled, the I/O pin will start a weak pull-high (made of FET). So the current consumption will be less when this I/O pin is pulled low.

The purpose of R-Option function is for selecting one code in a multi-code single chip. The hardware setup on how to select one code includes a determine routine before the main routine or anywhere as designated by user. The hardware cannot automatically jump to some place by R-Option setting.

It is not recommended to set the R-Option as general pull-high, since the R-Option is enabled as a very weak pull-high current and it receives noise easily. Hence, this function should not be used for other application, ex. keyboard matrix, etc.

IOCE (Port 9 GPIO/LCD Segment, Port 6 GPIO/LCD Com, LCD Bias, Scan Key Signal, Port 7 Open Drain, Counter 1 / Counter 2 Clock Source Counter 1 Prescaler Control Register)

Page 0: (Port 9 GPIO/LCD Segment, Port 6 GPIO/LCD Com, LCD Bias, Scan Key Signal Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P9SH	P9SL	P6S	Bias3	Bias2	Bias1	0	SC

Bit 0: SC (Scan Key signal)

0 : Disable

1 : Enable

Once this bit is enabled, all of the LCD signals will have a low pulse during a common period. This pulse has 30μs width. Use the following procedure to implement a key scan function.

a. Set Port 7 as input port.

b. Set IOCD Page 0 Port 7 pull high

c. Enable Key Scan signal

d. Push a key once. Set RA(6)=1 and switch to normal mode.

e. Blank LCD. Disable Key Scan signal

f. Set P9SL = 0, P9SH = 0. Port 9 sends a probe signal to Port 7 and read Port 7. Get the key.

g. Note: A probe signal should delay an instruction at least to another probe signal.

h. Set P9SH = 1, P9SL = 1. Port 9 as LCD signal. Enable the LCD.

NOTE

Port 6 and Port 8 can apply this method.

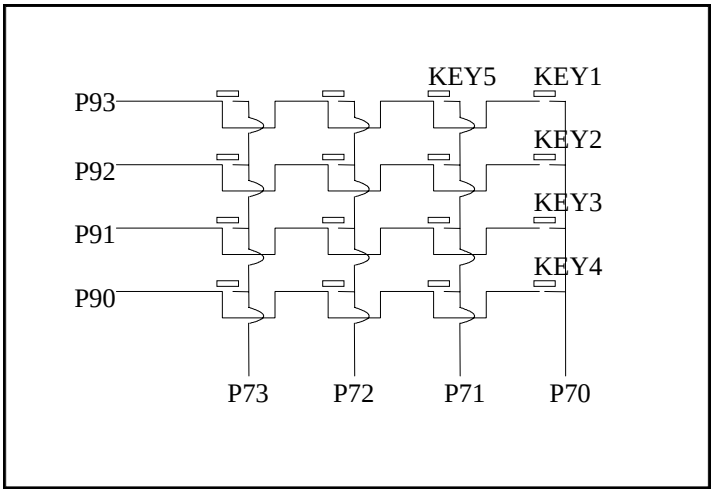


Fig. 7-5 Key Scan Circuit

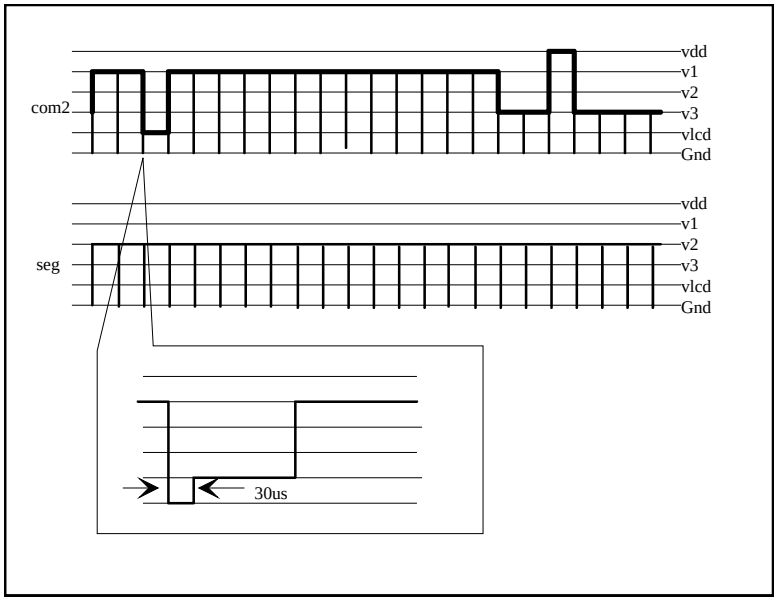


Fig. 7-6 Key Scan Signal

Bit 1: Port 7 Pull-high register option. Use default value.

Bits 2~4 (Bias 1~Bias 3) Control bits used to choose the LCD operation voltage.

LCD Operate Voltage	Vop (VDD 5V)	VDD=5V
000	0.60VDD	3.0V
001	0.66VDD	3.3V
010	0.74VDD	3.7V
011	0.82VDD	4.0V
100	0.87VDD	4.4V
101	0.93VDD	4.7V
110	0.96VDD	4.8V
111	1.00VDD	5.0V

Bit 5: Port 6 switch

0 : normal I/O port

1 : common output

Bit 6: Port 9 low nibble switch

0 : normal I/O port

1 : segment output

Bit 7: Port 9 high nibble switch

0 : normal I/O port

1 : segment output

Page 1: (Port7 Open Drain, Counter 1/2 Clock Source Counter1 Pre-Scaler Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP77	OP76	C2S	C1S	PSC1	PSC0	0	0

Bit 0: unused

Bit 1: unused

Bit 3~Bit 2: Counter 1 prescaler, reset = (0, 0)

PSC1	PSC0	Counter 1 Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	Reserved

Bit 4: Counter 1 source

0 : 32768Hz

1 : 3.579MHz if PLL is enabled, Scale = 1:1 only

Bit 5: Counter 2 source. Scale=1:1 only

0 : 32768Hz

1 : 3.579MHz if enabled PLL

NOTE

1. Counters 1, 2 timing:
T = (1/Freq) × Prescaler × Count value
Counters 1, 2 are 8-bit up counters, so the preset value is (256-Count value)

2. If Counters 1, 2 sources use PLL, the counter cannot work when PLL is disabled.

3. Counter 2 does not have a prescaler, the counter rate is only 1:1.

Bit 6: P76 open drain control

0 : disable

1 : enable

Bit 7: P77 open drain control

0 : disable

1 : enable

IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT3	**0**	C8_2	C8_1	INT2	INT1	INT0	TCIF

Bits 0 ~ 5, Bit 7: Interrupt enable bit

0 : disable interrupt

1 : enable interrupt

Bit 6: Reserved, clear this bit to '0'

NOTE

The IOCF Register is readable and writable.

7.3 TCC/WDT Prescaler

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available only to either the TCC or WDT at a time.

- An 8 bit counter is available for TCC or WDT as determined by the status of Bit 3 (PAB) of the CONT register.
- The prescaler ratio is described in Section 7.2 *Special Purpose Register*, under the subheading *CONT (Control Register)*.
- Fig. 7-7 depicts the Circuit Diagram of TCC/WDT.
- Both TCC and the prescaler will be cleared by instructions each time there's a write operation to TCC.
- The prescaler will be cleared by the WDTC and SLEP instructions, when in WDT mode.
- The prescaler will not be cleared by SLEP instruction, when in TCC mode.

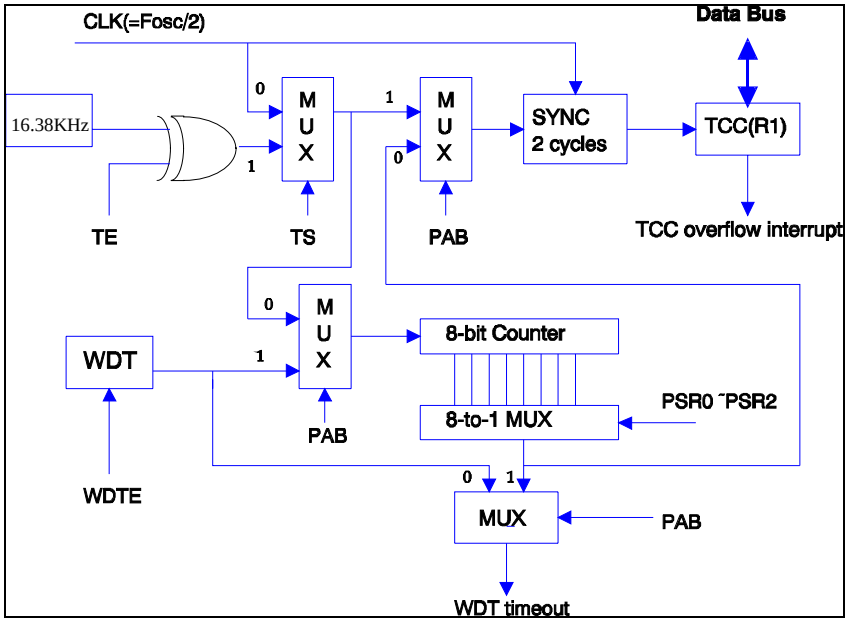


Fig. 7-7 Block Diagram of TCC WDT

7.4 I/O Ports

The I/O registers, (Port 5, Port 6, Port 7, Port 8, and Port 9), are bidirectional tri-state I/O ports. Port 7 can be pulled-high internally by software. Furthermore, P7.6 and P7.7 has its open-drain output also defined through software. Port 9 features an input status changed wake-up function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC9). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits are shown in Fig. 7-8 below.

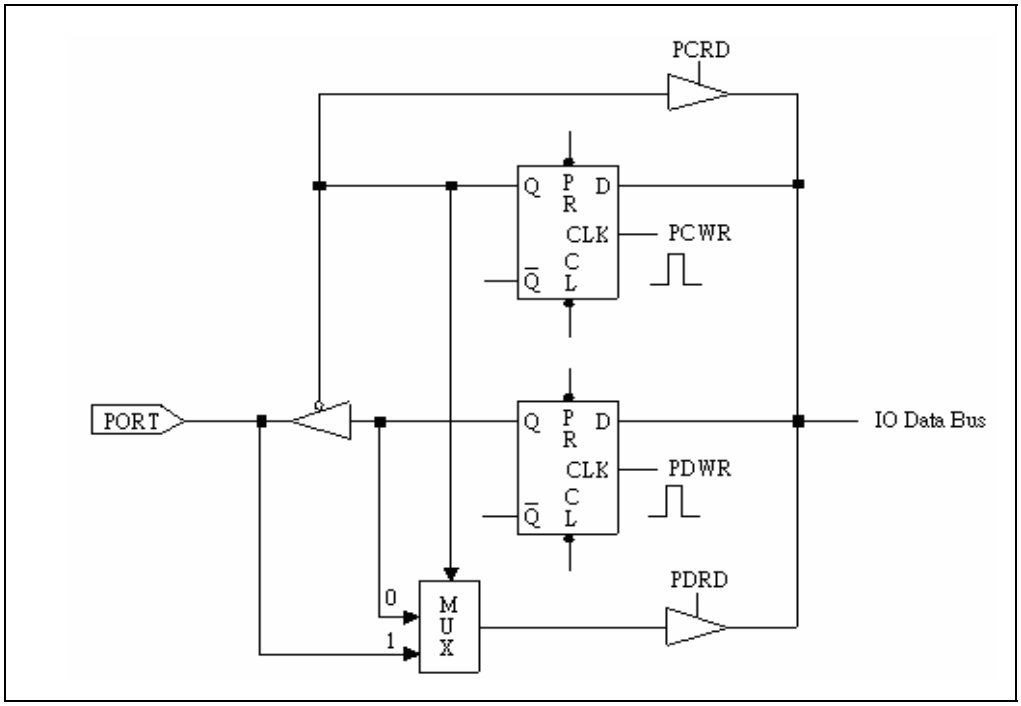


Fig. 7-8 Circuit of I/O Port and I/O Control Register

7.5 Reset and Wake-up

A Reset can be caused by:

(1) Power-on reset, or Voltage detector

(2) WDT timeout (if enabled and in Green or Normal mode)

Note that only Power-on reset, or only Voltage detector in Case (1) is enabled in the system by Code Option bit. If the Voltage detector is disabled, Power-on reset is selected in Case (1). Refer to Fig. 7-9.

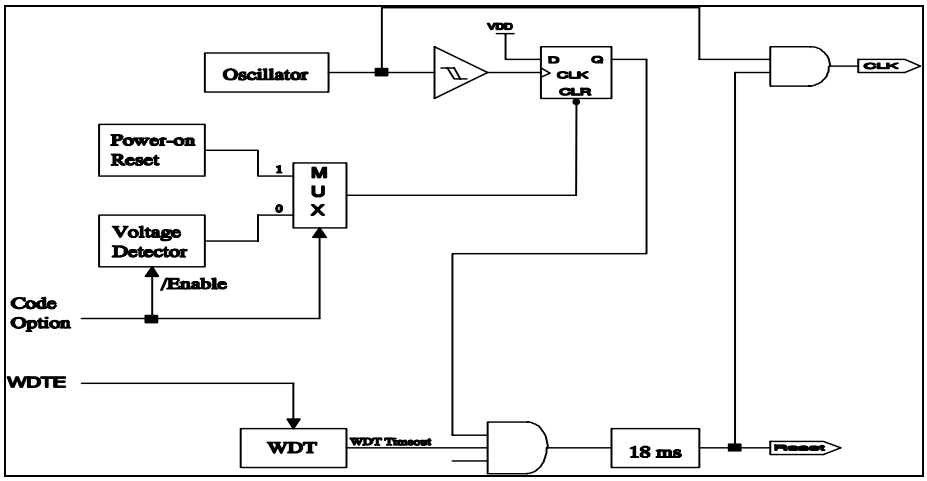


Fig. 7-9 Block Diagram of the Controller Reset

Once a reset occurs, the following functions are performed:

- The oscillator is running, or will be started
- The Program Counter (R2) is set to all "0"
- All I/O port pins are configured to input mode (high-impedance state)
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared
- The TCC/Watchdog timer and prescaler are cleared
- The Watchdog timer is disabled
- The CONT register is set to all "1"
- The other registers (Bit 7~Bit 0)

R5 = Port	**IOC5 = "11110000"**	–
R6 = Port	IOC6 = "11111111"	–
R7 = Port	IOC7 = "11111111"	–
R8 = Port	IOC8 = "11111111"	–
R9 = Port	IOC9 = "11111111"	–
RA = "x00x0xxx	IOCA = "00000000"	–
RB = "11111111"	Page 0 IOCB = "00000000"	Page 1 IOCB = "00000000"
RC = "00000000"	Page 0 IOCC = "0xxxxxxx"	Page 1 IOCC = "00000000"
RD = "xxxxxxxx"	Page 0 IOCD = "00000000"	**Page 1 IOCD = "00000000"**
RE = "00000000"	Page 0 IOCE = "00000000"	Page 1 IOCE = "00000000"
RF = "00000000"	IOCF = "00000000"	–

The controller can be awakened from Sleep mode or Idle mode (execution of "SLEP" instruction, named as Sleep Mode or Idle mode). The wake-up signal list is as follows:

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
_	RA (7, 6)=(0, 0) + SLEP	RA (7, 6)=(1, 0) + SLEP	RA (7, 6)=(x, 0) no SLEP	RA (7, 6)=(x, 1) no SLEP
TCC time out	×	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
WDT time out	RESET	Wake-up + Next instruction	RESET	RESET
Port 9 (Input status change wake-up)	RESET	Wake-up + Next instruction	×	×
Port s 70~73 (INT0~INT3)	×	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt

X means no function

P70 ~ P73's wake-up function is controlled by IOCF (1, 2, 3) and ENI instruction.

P70's wake-up signal is a rising or falling signal defined by CONT Register Bit 7.

Port 9, Port 71, Port 72 and Port 73's wake-up signal is a falling edge signal.

7.6 Interrupt

This IC has internal interrupts which are falling edge triggered, namely,

- TCC timer overflow interrupt (internal)
- Two 8-bit counters overflow interrupt.

If these interrupt sources change signal from high to low, the RF register will generate a '1' flag to the corresponding register if the IOCF register is enabled.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetched from Address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register.

NOTE

- *The interrupt flag bit must be cleared by software before leaving the interrupt service routine and enabling other interrupts to avoid recursive interrupts.*
- *Do not use the "BC" instruction to clear interrupt flag in interrupt subroutine. It is possible to clear other interrupt flags if the other interrupts occur at the same time. Use "MOV" instruction for the following step:*

```
;In "INT1" interrupt subroutine
  MOV   A,@0B11111011
  MOV   RF,A
```

There are four external interrupt pins including INT0, INT1, INT2, INT3, and four internal interrupts available.

- Internal signals include TCC, CNT1, CNT2
- External interrupt INT0, INT1, INT2, INT3 signals are from Port 7, Bit 0 to Bit 3. If IOCF is enable then these signal will cause interrupt, or these signals will be treated as general input data.

After a reset, the next instruction will be fetched from Address 000H and the hardware interrupt is 008H.

TCC will go to Address 0x08 in Green mode or Normal mode after a time out, then proceed with the next instruction from “SLEP” instruction. These two cases will set an RF flag.

It is very important to save ACC,R3 and R5 when processing an interrupt.

Address	Instruction	Note
0x08	DISI	;Disable interrupt
0x09	MOV A_BUFFER,A	;Save ACC
0x0A	SWAP A_BUFFER	
0x0B	SWAPA 0x03	;Save R3 status
0x0C	MOV R3_BUFFER,A	
0x0D	MOV A,0x05	;Save ROM page register
0x0E	MOV R5_BUFFER,A	
:	:	
:	:	
:	MOV A,R5_BUFFER	;Return R5
:	MOV 0X05,A	
:	SWAPA R3_BUFFER	;Return R3
:	MOV 0X03,A	
:	SWAPA A_BUFFER	;Return ACC
:	RETI	

7.7 Instruction Set

Instruction set has the following features:

(1). Every bit of any register can be set, cleared, or tested directly.

(2). The I/O register can be regarded as general register, that is, the same instruction can operate on the I/O register.

Convention:

R = Register designator that specifies which one of the 64 registers (including operation and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Instruction Binary	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None
0 0000 0010 0000	0020	TBL	R2+A → R2 Bits 9,10 do not clear	Z, C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC

Instruction Binary	Hex	Mnemonic	Operation	Status Affected
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None
1 1110 1000 kkkk	1E8k	PAGE k	K->R5(3:0)	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

7.8 Code Option Register

The data bank IC has one Code option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	MCLK

Bit 0: main clock selection

0 : 3.58MHz

1 : 1.84MHz

Bits 1~7: unused, must be set to"0"

7-9 LCD Driver

The data bank IC can drive an LCD directly and has 60 segments and 9 commons that can drive a total of 60×9 dots. The LCD block is made up of LCD driver, display RAM, segment output pins, common output pins and LCD operating power supply pins.

Duty, bias, the number of segments, the number of common and frame frequency are determined by the LCD mode register and LCD control register.

The basic structure contains a timing control which uses the basic frequency 32.768kHz to generate the proper timing for different duty and display access. The RE register is a command register for the LCD driver. The LCD display (disable, enable, blanking) is controlled by LCD_C and the driving duty and bias is determined by LCD_M and the display data is stored in the data RAM of which address and data access is controlled by registers IOCB and IOCC.

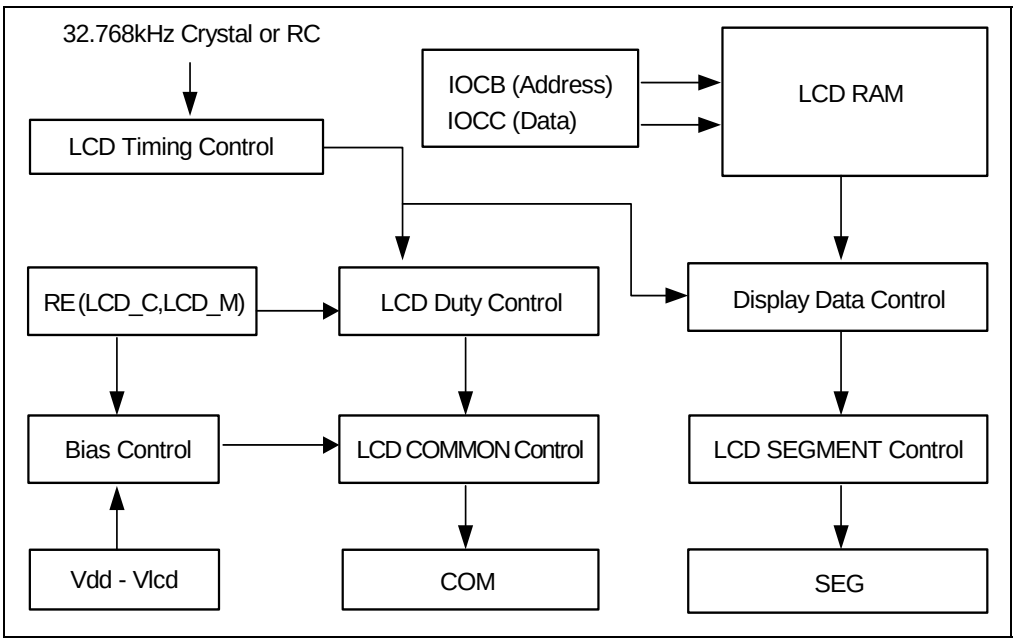


Fig. 7-10 LCD Driver Control

7.9.1 LCD Driver Control

RE (LCD Driver Control, Initial state "00000000")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	LCD_C2	LCD_C1	LCD_M

Bit 0 (LCD_M): LCD_M determines the methods, including duty, bias, and frame frequency.

Bit 1~Bit 2 (LCD_C#): LCD_C# determines the LCD display enable or blanking. In changing the display duty, it is a must to set the LCD_C to "00".

LCD_C2, LCD_C1	LCD Display Control	LCD_M	Duty	Bias
0 0	Change duty Disable (turn off LCD)	0 1	1/9 1/8	1/4 1/4
0 1	Blanking	:	:	
1 1	LCD display enable	:	:	

7.9.2 LCD Display Area

The LCD display data is stored in the data RAM. The relation of data area and COM/SEG pin is as shown below:

COM8	COM7 ~ COM0	
40H (Bit 0)	00H (Bit7 ~ Bit0)	SEG0
41H	01H	SEG1
:	:	:
:	:	:
7BH	3BH	SEG59
7CH	3CH	Empty
7DH	3DH	Empty
7EH	3EH	Empty
7FH	3FH	Empty

IOCB (LCD Display RAM address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	LCDA6	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

Bit 0 ~ Bit 6 select LCD Display RAM address up to 120

The LCD RAM can be written whether in enable or disable mode and can be read only in disable mode.

IOCC (LCD Display data): Bit 0 ~ Bit 8 are LCD data

NOTE

Writable only when LCD is enabled. Read/Write when disabled.

7.9.3 LCD COM and SEG Signal

COM Signal. The number of COM pins varies according to the duty cycle used, as follows: in 1/8 duty mode COM8 must be opened. in 1/9 duty mode COM0~COM8 pins must be used.

	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
1/8	o	o	o	o	o	o	o	o	x
1/9	o	o	o	o	o	o	o	o	o

x : open, **o** :select

SEG signal. The 60 segment signal pins are connected to the corresponding display RAM address 00h to 3Bh. When Duty mode is at 1/8, the required data addresses are only those from Com0 ~ Com7 (located within 00h ~ 3Bh). However, when Duty mode is at 1/9, all data addresses from Com0 ~ Com7 (located within 00h ~ 3Bh) and Com8 (located within 40h ~ 7Bh) are needed.

When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0, a non-select signal is sent to the corresponding segment pin.

The COM, SEG and Select/Non-select signal are shown as follows:

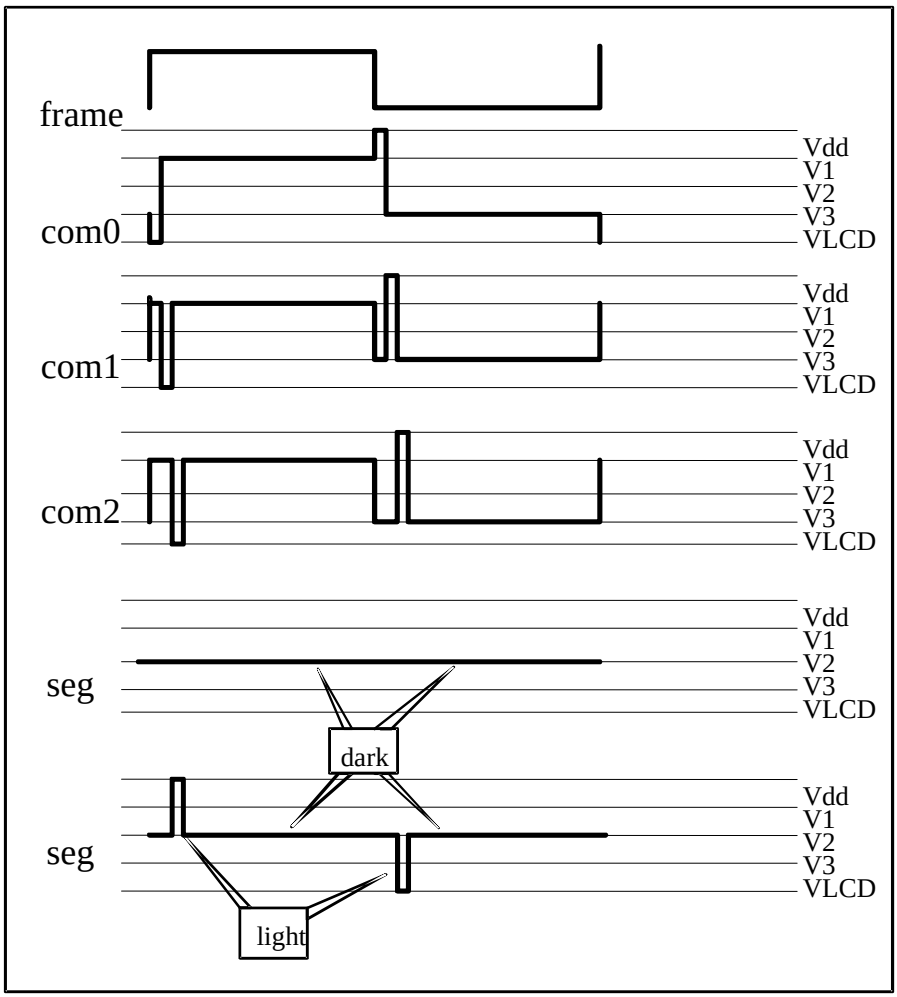


Fig. 7-11 LCD Wave 1/4 Bias

7.9.4 LCD Bias Control

IOCE (Bias Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Bias3	Bias2	Bias1		

Bit 2~4 (Bias1~Bias3) Control bits used to choose LCD operation voltage . For the circuit, refer to Figure 7-12.

LCD Operate Voltage	Vop (VDD 5V)	VDD=5V
000	0.60VDD	3.0V
001	0.66VDD	3.3V
010	0.74VDD	3.7V
011	0.82VDD	4.0V
100	0.87VDD	4.4V
101	0.93VDD	4.7V
110	0.96VDD	4.8V
111	1.00VDD	5.0V

Bits 5~7 unused

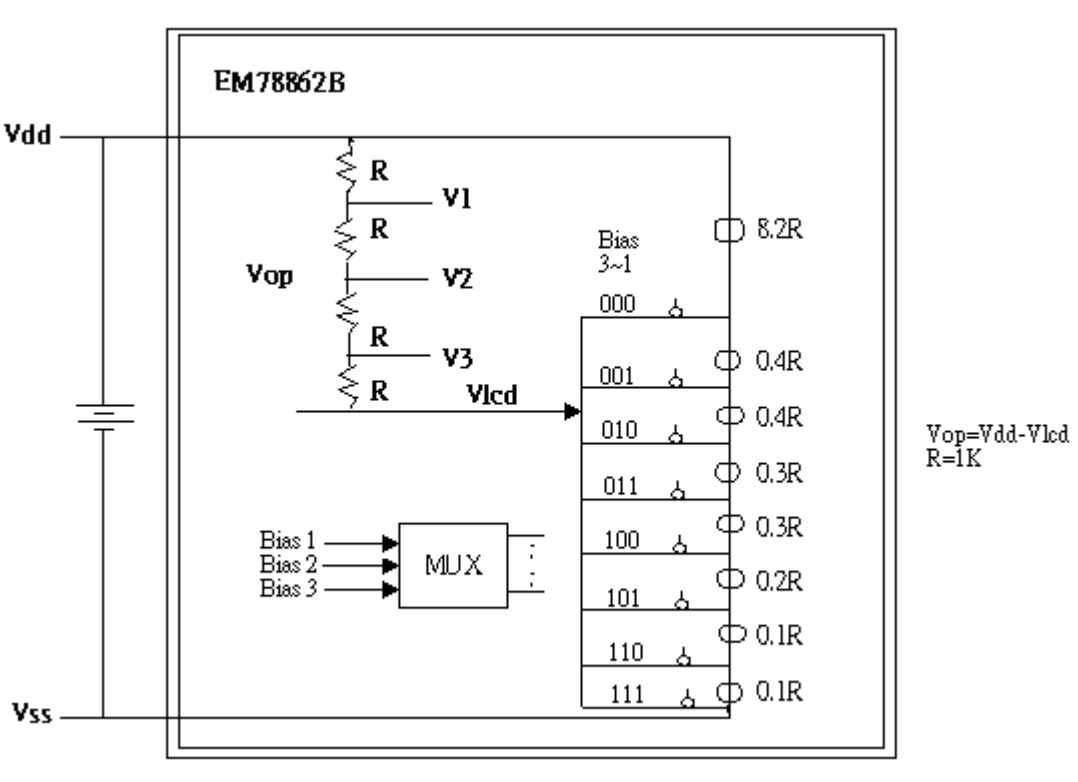


Fig. 7-12 LCD Bias Circuit

8 Absolute Operation Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	Vdd	-0.3 To 6	V
Input Voltage	Vin	-0.5 TO Vdd +0.5	V
Operating Temperature Range	Ta	0 TO 70	℃

9 DC Electrical Characteristic

Ta=0°C ~ 70°C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL1	Input Leakage Current for Input pins	VIN = VDD, VSS	–	–	±1	μA
IIL2	Input Leakage Current for Bidirectional pins	VIN = VDD, VSS	–	–	±1	μA
VIH	Input High Voltage	–	0.8VDD	–	VDD	V
VIL	Input Low Voltage	–	VSS	–	0.2VDD	V
VIHT	Input High Threshold Voltage	/RESET	2.0	–	–	V
VILT	Input Low Threshold Voltage	/RESET	–	–	0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5	–		V
VILX	Clock Input Low Voltage	OSCI	–	–	1.5	V
VHscan	Key scan Input High Voltage	Port 6 for key scan	3.5	–	–	V
VLscan	Key scan Input Low Voltage	Port 6 for key scan	–	–	1.5	V
VOH1	Output High Voltage (Ports 6, 7, 8)	IOH = -1.6mA	0.8VDD	–	VDD	V
	(Port 9)	IOH = -6.0mA	0.8VDD	–	VDD	V
VOL1	Output Low Voltage (Port 6, 7, 8)	IOL = 1.6mA	VSS	–	0.2VDD	V
	(Port 9)	IOL = 6.0mA	VSS	–	0.2VDD	V
Vcom	Com voltage drop	Io=+/- 50 μA	–	–	2.9	V
Vseg	Segment voltage drop	Io=+/- 50 μA	–	-	3.8	V
Vlcd	LCD drive reference voltage	Contrast adjustment	–	–	–	–
IPH	Pull-high current	Pull-high active input pin at VSS	–	-10	-15	μA
ISB1	Power down current (Sleep mode)	All input and I/O pin at VDD, Output pin floating, WDT disabled	–	1	4	μA
ISB2	Power down current (Idle mode)	All input and I/O pin at VDD, Output pin floating, WDT disabled, LCD enabled	–	50	70	μA
ISB3	Low clock current (Green mode)	CLK=32.768kHz, All input and I/O pin at VDD, Output pin floating, WDT disabled, LCD enabled	–	80	100	μA
ICC	Operating supply current (Normal mode)	/RESET=High, CLK=3.579MHz, Output pin floating, LCD enabled	–	1.5	1.9	mA

Ta=0°C ~ 70°C, VDD=3V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ISB1	Power down current (Sleep mode)	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1	2	μA
ISB2	Power down current (Idle mode)	All input and I/O pins at VDD, Output pin floating, WDT disabled, LCD enabled	–	25	35	μA
ISB3	Low clock current (Green mode)	CLK=32.768kHz, All input and I/O pin at VDD, Output pin floating, WDT disabled, LCD enabled	–	35	45	μA
ICC	Operating supply current (Normal mode)	/RESET=High, CLK=3.579MHz, Output pin floating, LCD enabled	–	0.9	1.2	mA

10 AC Electrical Characteristic

Ta=0°C ~ 70°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time	32.768K 3.579M	–	60 550	–	μs ns
Tdrh	Device delay hold time	–	–	18	–	ms
Ttcc	TCC input period	Note [1]	(Tins+20)/N	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	–	18	–	ms

Note: [1] N = selected prescaler ratio

Description	Symbol	Min	Typ	Max	Unit
OSC start up (32.768kHz) (3.579MHz PLL)	Tosc	–	–	2000 10	ms

11 Timing Diagrams

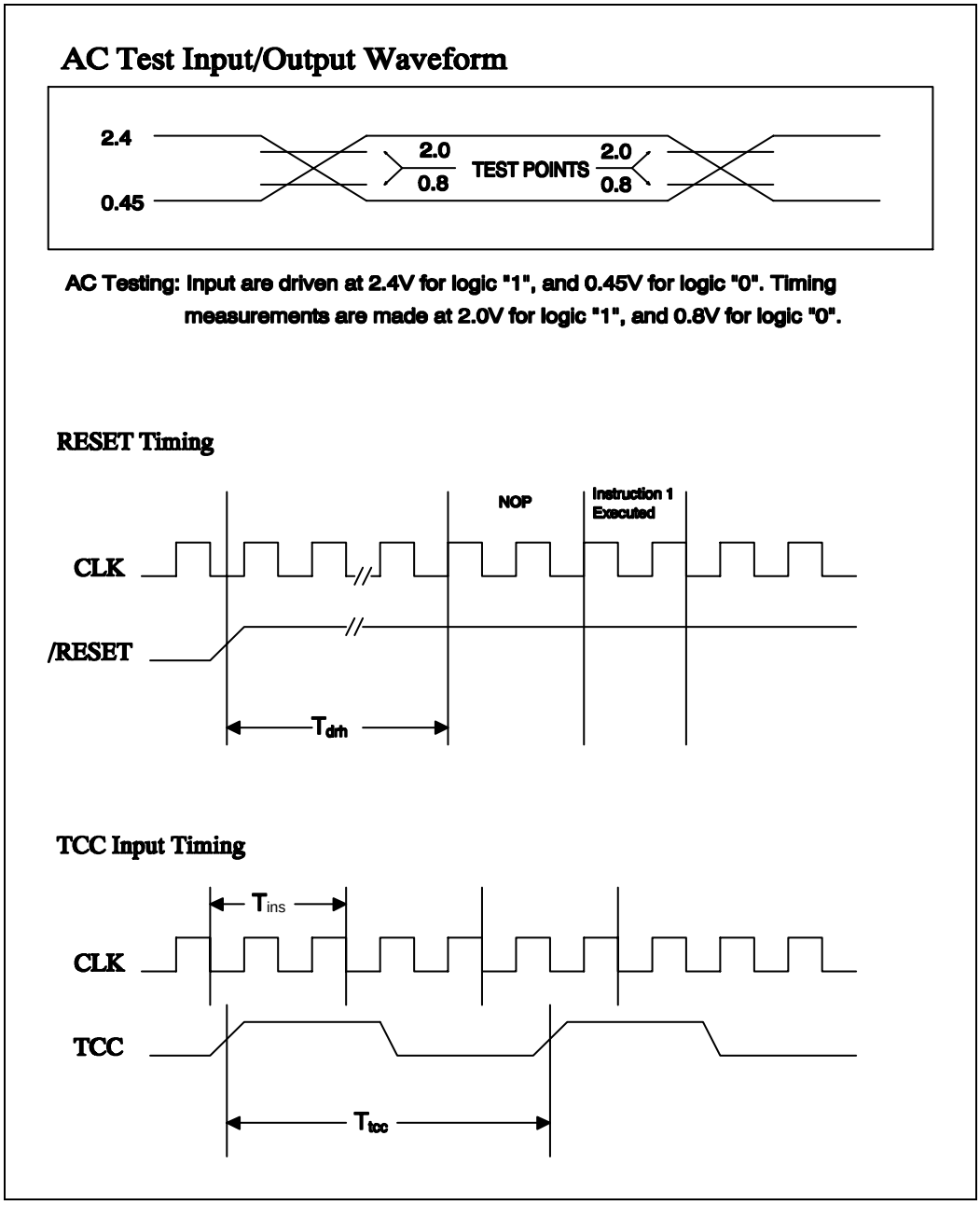


Fig. 11-1 AC Timing

12 Application Circuit

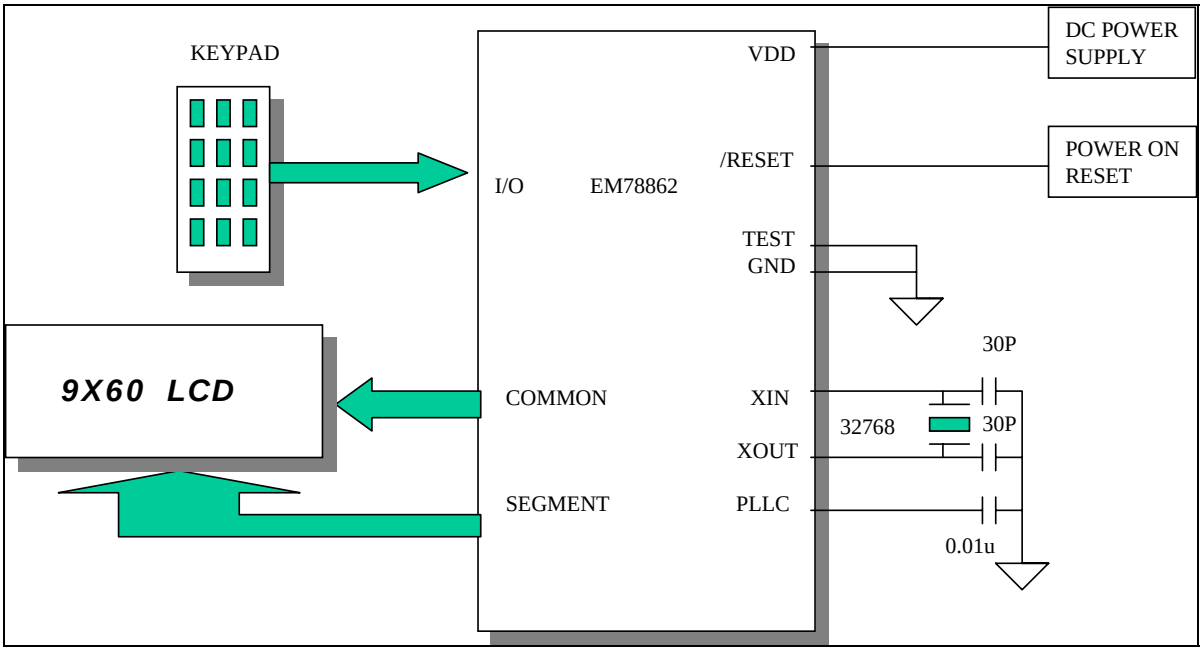
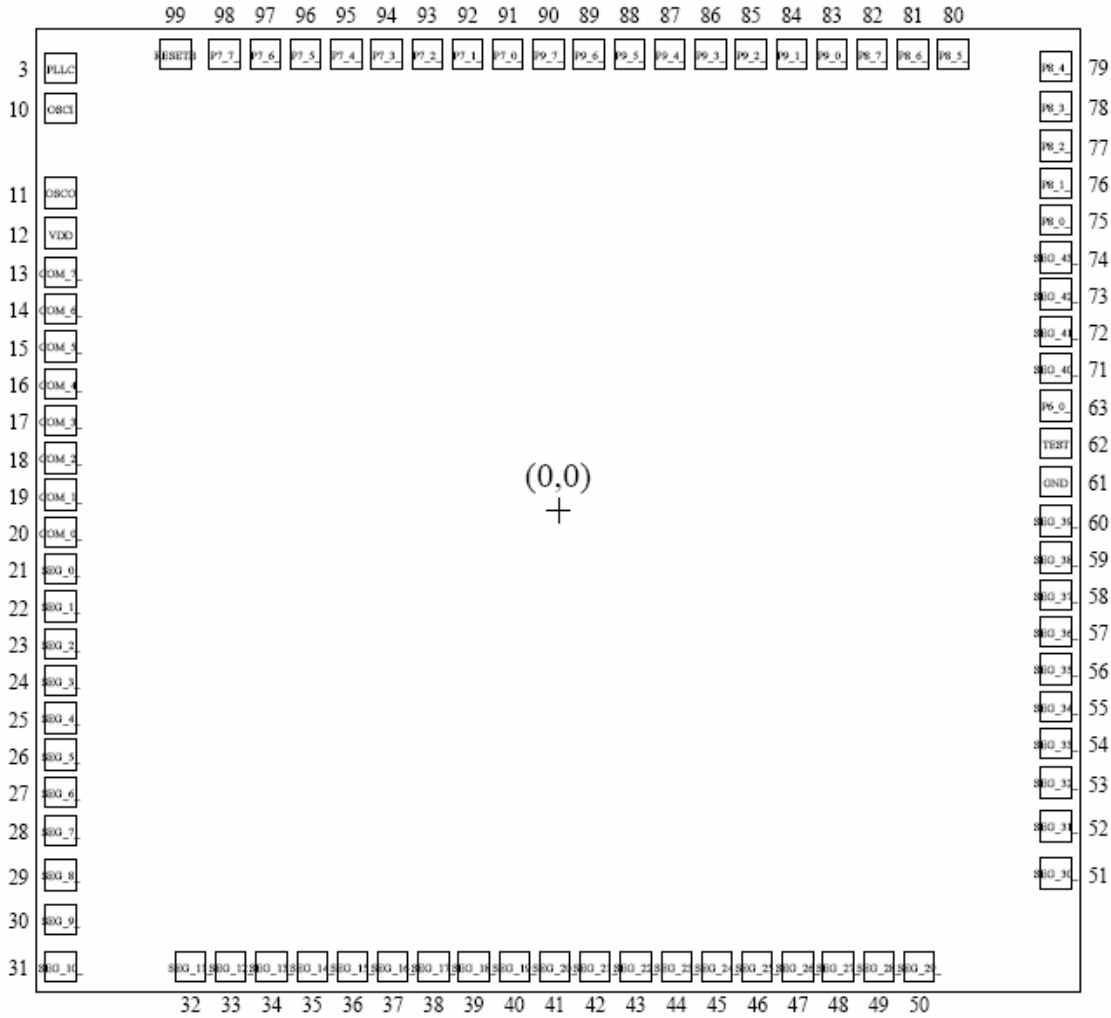


Fig. 12-1 Application Circuit

13 Pad Diagram

(1) HM NO: EM78P862
HC NO: EU5918 Date : Mar 2 2001
Chip Size: 3210 * 2960 UM
(2) Pad Configuration



eu5918 Pad Name & Cordinates Table		
Structure Name: EU5918 Chip Size: 3210 * 2960 UM		
Pin No	Pad Name	Coordinate (X , Y)
1		
2		
3	PLLC	-1475.0 ,1311.0
4		
5		
6		
7		
8		
9		
10	OSCI	-1475.0 ,1191.1
11	OSCO	-1475.0 ,941.0
12	VDD	-1475.0 ,821.0
13	COM_7_	-1475.0 ,706.0
14	COM_6_	-1475.0 ,596.0
15	COM_5_	-1475.0 ,486.0
16	COM_4_	-1475.0 ,376.0
17	COM_3_	-1475.0 ,266.0
18	COM_2_	-1475.0 ,156.0
19	COM_1_	-1475.0 ,46.0
20	COM_0_	-1475.0 ,-64.0
21	SEG_0_	-1475.0 ,-174.0
22	SEG_1_	-1475.0 ,-284.0
23	SEG_2_	-1475.0 ,-394.0
24	SEG_3_	-1475.0 ,-504.0
25	SEG_4_	-1475.0 ,-614.0

eu5918 Pad Name & Cordinates Table		
Structure Name: EU5918 Chip Size: 3210 * 2960 UM		
Pin No	Pad Name	Coordinate (X , Y)
26	SEG_5_	-1475.0 ,-724.0
27	SEG_6_	-1475.0 ,-834.0
28	SEG_7_	-1475.0 ,-949.0
29	SEG_8_	-1475.0 ,-1080.0
30	SEG_9_	-1475.0 ,-1210.0
31	SEG_10_	-1475.0 ,-1350.0
32	SEG_11_	-1090.0 ,-1350.0
33	SEG_12_	-970.0 ,-1350.0
34	SEG_13_	-850.0 ,-1350.0
35	SEG_14_	-730.0 ,-1350.0
36	SEG_15_	-610.0 ,-1350.0
37	SEG_16_	-490.0 ,-1350.0
38	SEG_17_	-370.0 ,-1350.0
39	SEG_18_	-250.0 ,-1350.0
40	SEG_19_	-130.0 ,-1350.0
41	SEG_20_	-10.0 ,-1350.0
42	SEG_21_	110.0 ,-1350.0
43	SEG_22_	230.0 ,-1350.0
44	SEG_23_	350.0 ,-1350.0
45	SEG_24_	470.0 ,-1350.0
46	SEG_25_	590.0 ,-1350.0
47	SEG_26_	710.0 ,-1350.0
48	SEG_27_	830.0 ,-1350.0
49	SEG_28_	950.0 ,-1350.0
50	SEG_29_	1070.0 ,-1350.0

eu5918 Pad Name & Cordinates Table		
Structure Name: EU5918 Chip Size: 3210 * 2960 UM		
Pin No	Pad Name	Coordinate (X , Y)
51	SEG_30_	1475.0 ,-1075.0
52	SEG_31_	1475.0 ,-935.0
53	SEG_32_	1475.0 ,-805.0
54	SEG_33_	1475.0 ,-690.0
55	SEG_34_	1475.0 ,-580.0
56	SEG_35_	1475.0 ,-470.0
57	SEG_36_	1475.0 ,-360.0
58	SEG_37_	1475.0 ,-250.0
59	SEG_38_	1475.0 ,-140.0
60	SEG_39_	1475.0 ,-30.0
61	GND	1475.0 ,85.0
62	TEST	1475.0 ,200.0
63	P6_0_	1475.0 ,310.0
64		
65		
66		
67		
68		
69		
70		
71	SEG_40_	1475.0 ,420.0
72	SEG_41_	1475.0 ,530.0
73	SEG_42_	1475.0 ,640.0
74	SEG_43_	1475.0 ,750.0
75	P8_0_	1475.0 ,860.0

eu5918 Pad Name & Cordinates Table		
Structure Name: EU5918 Chip Size: 3210 * 2960 UM		
Pin No	Pad Name	Coordinate (X , Y)
76	P8_1_	1475.0 ,970.0
77	P8_2_	1475.0 ,1080.0
78	P8_3_	1475.0 ,1195.0
79	P8_4_	1475.0 ,1315.0
80	P8_5_	1171.2 ,1350.0
81	P8_6_	1051.2 ,1350.0
82	P8_7_	931.2 ,1350.0
83	P9_0_	811.2 ,1350.0
84	P9_1_	691.2 ,1350.0
85	P9_2_	571.2 ,1350.0
86	P9_3_	451.2 ,1350.0
87	P9_4_	331.2 ,1350.0
88	P9_5_	211.2 ,1350.0
89	P9_6_	91.2 ,1350.0
90	P9_7_	-28.8 ,1350.0
91	P7_0_	-148.8 ,1350.0
92	P7_1_	-268.8 ,1350.0
93	P7_2_	-388.8 ,1350.0
94	P7_3_	-508.8 ,1350.0
95	P7_4_	-628.8 ,1350.0
96	P7_5_	-748.8 ,1350.0
97	P7_6_	-868.8 ,1350.0
98	P7_7_	-988.8 ,1350.0
99	RESETB	-1135.0 ,1350.0
100		