ESW5221

27MHz FM/FSK Transmitter

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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Specification Revision History

Version	Revision Description	Date
1.0	Initial Release Edition	2000/06/06

1 Introduction

The ESW5221 single-chip solution is an integrated circuit intended for use as a low cost FSK transmitter to establish a frequency-agile RF link. The device is designed to provide a 10-channel transmitter and intended for linear (FM) or digital (FSK) modulated applications in the wireless Mouse and Keyboard. The single chip transmitter operates down to 2.2V minimum and is expressly designed for low power consumption. It offers synthesizer with a typical channel spacing of approximately 30KHz to allow narrow-band applications.

2 Feature Description

- Single-Chip RF Transmitter
- Include oscillation circuit with external X-TAL.
- On-Chip Phase-Locked Loop (PLL)
- Power Down mode
- 2.2 to 5.0V supply range

3 Application

- Wireless Mouse
- Wireless Keyboard
- Wireless Communication Products

4 Block Diagram

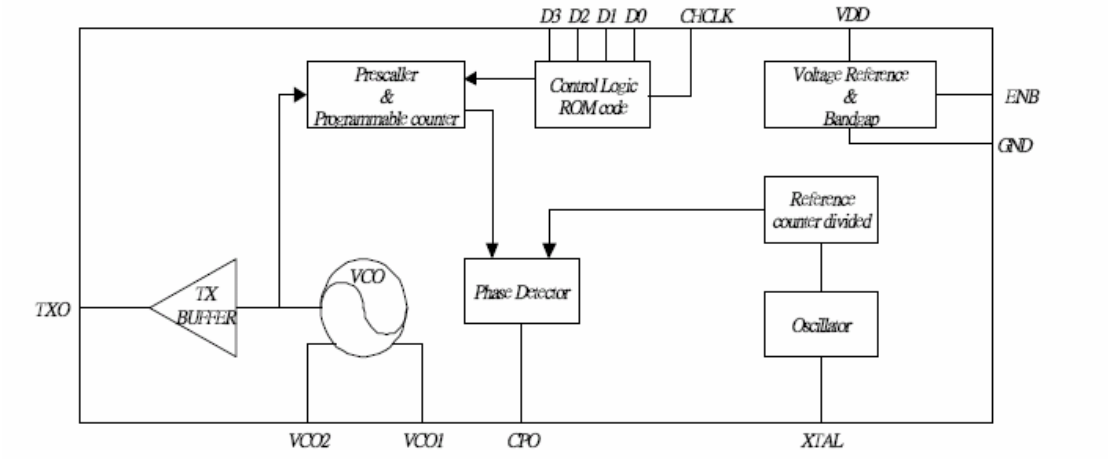


Figure 4-1 ESW5221 Block Diagram

5 Pin Configuration

5.1 Pin Assignment

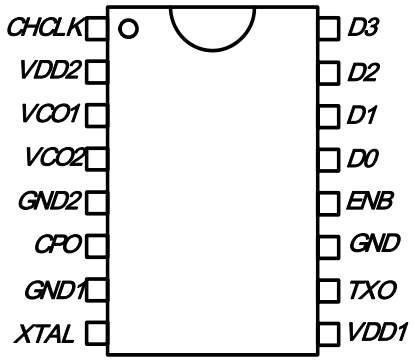


Figure 5-1 ESW5221 SOP-16L (150mil) Package

5.2 Pin Descriptions

Pin No.	Pin Name	Description
2,9	VDD1 VDD2	VDD is supply to this pin. A 0.1μF de-coupling capacitor should be connected as close as possible from this pin to ground.
5,7,11	GND GND1 GND2	This pin should be a low inductance, direct connection to ground.
6	CPO	Phase detector output, connected to external low pass filter.
1	CHCLK	Clock input for channel selection when all parallel BCD (D0~D3) input are left open or connected to ground.
12	ENB	Active Low, enable input.
8	XTAL	Crystal (4MHz) Connection Input.
10	TXO	RF power output
3	VCO1	For external LC tank
4	VCO2	For external LC tank
13	D0	The channel selected pin. The CHCLK pin connects to ground.
14	D1	The channel selected pin. The CHCLK pin connects to ground.
15	D2	The channel selected pin. The CHCLK pin connects to ground.
16	D3	The channel selected pin. The CHCLK pin connects to ground.

6 Function Description

The ESW5221 single-chip solution is a CMOS technology integrated circuit intended for low cost FSK transmitter application and to establish a frequency-agile RF link. The device is capable of providing 10-channel transmitter.

6.1 VCO

The circuit employed an LC-tank structure to achieve low-phase noise characteristic where “L” is an off-chip high-Q inductor, and “C” is provided by a varactor with different tuning ranges and converting baseband data.

6.2 PLL

The PLL includes 64/65 prescaler, charge pump, PFD, N-A swallow counters, and R-counter for the multi-channel applications. The channels, selected via mechanical switches of parallel BCD input or as provided by Pin 1, can be easily set by an input pin CHCLK which directly selects the ROM table addresses.

6.3 D0 – D3/CHCLK

These input pins provide the BCD code for selecting one of the ten channels to be locked in both transmit and receive loop. When the address data other than 1 – 10, are input, the decoding logic defaults to Channel 10. The frequency assignments with reference to CHCLK, connect to ground and D0 – D3 inputs, as shown in the following table, have internal pull up devices.

6.3.1 VCO Frequency and Divider Ratio

Oscillator Frequency 4.0MHz, Ref. Divider 800

Channel	VCO Frequency	TXO Frequency	TX Divider (5.0KHz Ref)	Input			
				D3	D2	D1	D0
1	26.985MHz	26.985MHz	5397	0	0	0	1
2	27.015 MHz	27.015 MHz	5403	0	0	1	0
3	27.045 MHz	27.045 MHz	5409	0	0	1	1
4	27.075MHz	27.075MHz	5415	0	1	0	0
5	27.105 MHz	27.105 MHz	5421	0	1	0	1
6	27.135 MHz	27.135 MHz	5427	0	1	1	0
7	27.165 MHz	27.165 MHz	5433	0	1	1	1
8	27.195 MHz	27.195 MHz	5439	1	0	0	0
9	27.225MHz	27.225MHz	5445	1	0	0	1
10	27.255MHz	27.255MHz	5451	1	0	1	0
-	27.255MHz	27.255MHz	5451	1	0	1	1
-	27.255MHz	27.255MHz	5451	1	1	0	0
-	27.255MHz	27.255MHz	5451	1	1	0	1
-	27.255MHz	27.255MHz	5451	1	1	1	0

NOTE: ***1:*** *open;* ***0:*** *ground*

When all parallel BCD inputs are left open or connected to ground, the channel is set by clock rising edge at Pin 1 (CHCLK) of MCU. The initial or default channel at power on (internal power on reset) is set at Channel 10.

6.4 TX Output Driver

The TX output driver includes a pre-driver and an open-drain output stage. The off-chip loading network can be a parallel RLC tuned resonant circuit which delivers a maximum of 0dBm output to the load at 3V supply.

6.5 Channel Clock Timing

6.5.1 Timing Diagram

Channel DATA by $F_{DIVIDER}$ Clock

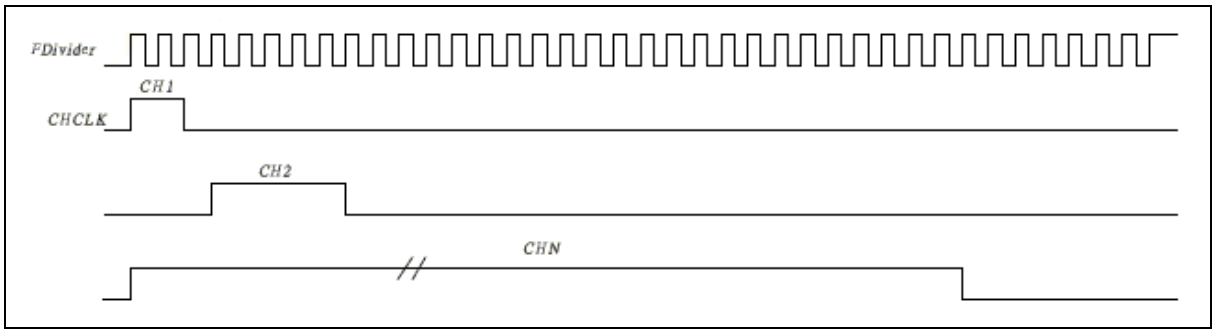


Figure 6-1 ESW5221 Timing Diagram

6.5.2 Channel Clock Timing

The channel clock tolerance of the CHCLK signal should be within ± 150μS.

Channel	CHCLK	Channel	CHCLK
1	600μS	6	3.6mS
2	1.2mS	7	4.2mS
3	1.8mS	8	4.8mS
4	2.4mS	9	5.4mS
5	3.0mS	10	6.0mS

7 Absolute Operation Maximum Ratings

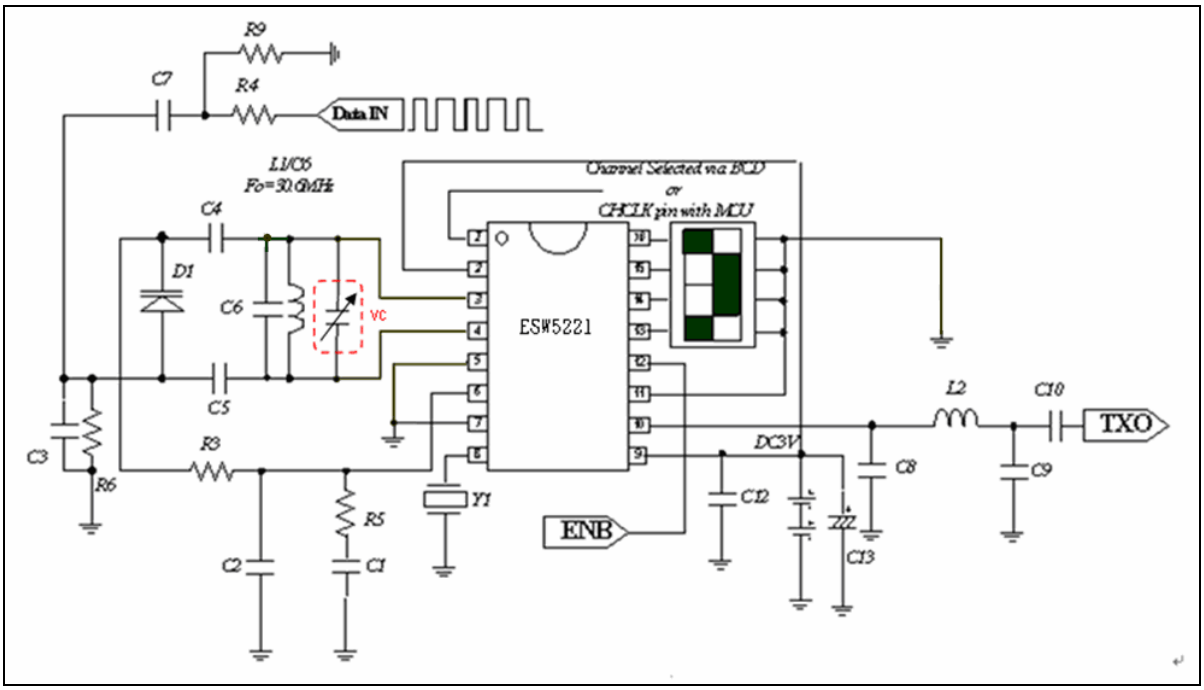
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.3 to 5.5	V
Input Voltage	V_{in}	–0.5 to V_{DD}+0.5	V
Operating Temperature Range	Ta	0 to 70	°C

8 DC/AC Electrical Characteristic

(VDD=3.0V VSS=0V)

Parameter	Min.	Typical	Max.	Unit
Overall				
Operating Voltage	2.2	3.0	5.0	V
Current Consumption: VCO + TX Buffer + PLL Power Down Mode		 8	 10	 mA μA
Frequency Deviation		3		KHz
Transmitter Section				
RF power output @50Ω	-3	0		dBm
RF Output Spurious Suppression	-30			dBc
PLL Section				
PLL Operating Frequency		27		MHz
OSC Operating Frequency		4		MHz
VCO phase noise: 100KHz offset 1MHz offset		 -90 -100		 dBc/Hz
VCO Sensitivity		0.8		MHz/V
Output rise time			200	ns
Output fall time			200	ns
CHCLK				
Input rise time			10	μs
Input fall time			10	μs
BCD Input				
Pull up resistance	300			KΩ

9 Application Circuit



* ***ENB:*** *"Low" for Operating Mode / "High" for Idle Mode*

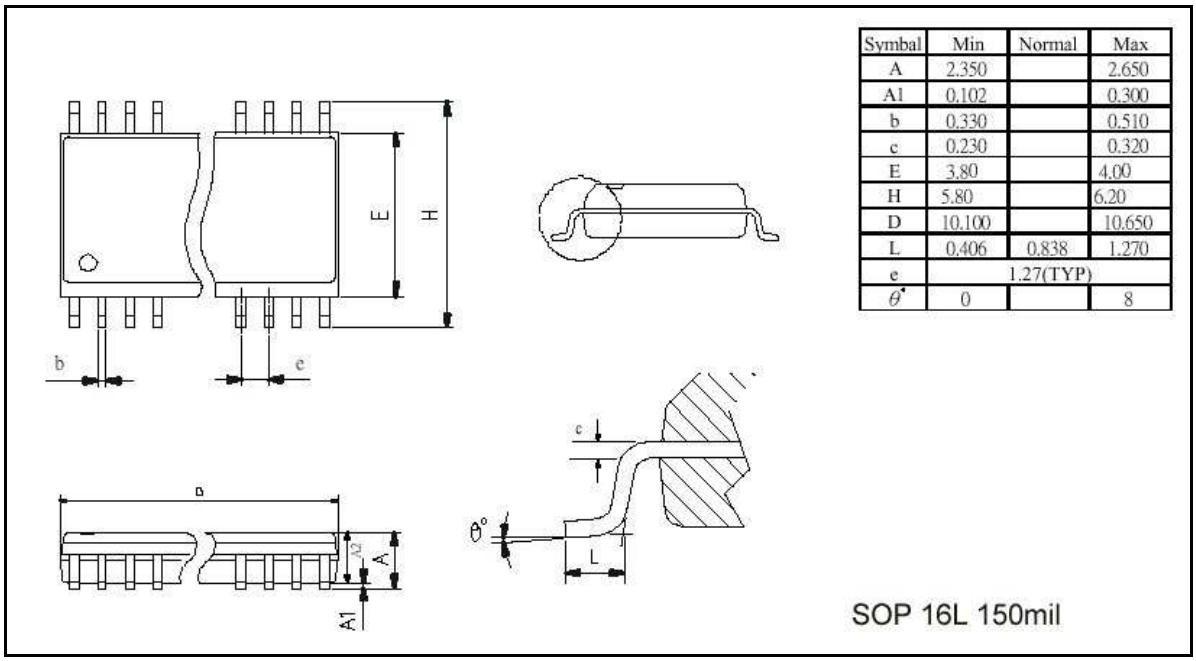
Figure 9-1 ESW5221 Application Circuit

10 Components List

Item	Part Type	Designators	Manufacture	Remark
1	Variable Capacitor 20P	VC		
2	C.F Resistor 1KΩ	R6, R9.		
3	C.F Resistor 39KΩ	R3.		
4	C.F Resistor 22KΩ	R5.		
5	C.F Resistor 100KΩ	R4.		
6	Ceramic Capacitor 33P NPO	C5.		
7	Ceramic Capacitor 120P NPO	C4.C9.C10		
8	Ceramic Capacitor 150P NPO	C8.		
9	Ceramic Capacitor 102 X7R	C3.		
10	Ceramic Capacitor 4n7 X7R	C2		
11	Ceramic Capacitor 0.15UF(154)	C1.		
12	Ceramic Capacitor 0.1UF(104)	C12.		
13	Electrolytic Capacitor 100u 6.3V	C13.		
14	Variable diodes 1SV270	D1.	Toshiba	
15	Inductor 390nH	L2.	King core or WALSIN	
16	Inductor 820nH	L1.	King core or WALSIN	
17	Crystal 4M30P1 49US	Y1.		
18	Dip Switch 4P	SW1.		
19	ESW5221	U1	ELAN	

11 Packaging Reference

- Dimension: mm



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.330		0.510
c	0.230		0.320
E	3.80		4.00
H	5.80		6.20
D	10.100		10.650
L	0.406	0.838	1.270
e		1.27(TYP)	
θ°	0		8

Figure 11-1 ESW5221 SOP Packaging Dimensions

12 Transmitter Demo Board Introduction

12.1 Top View

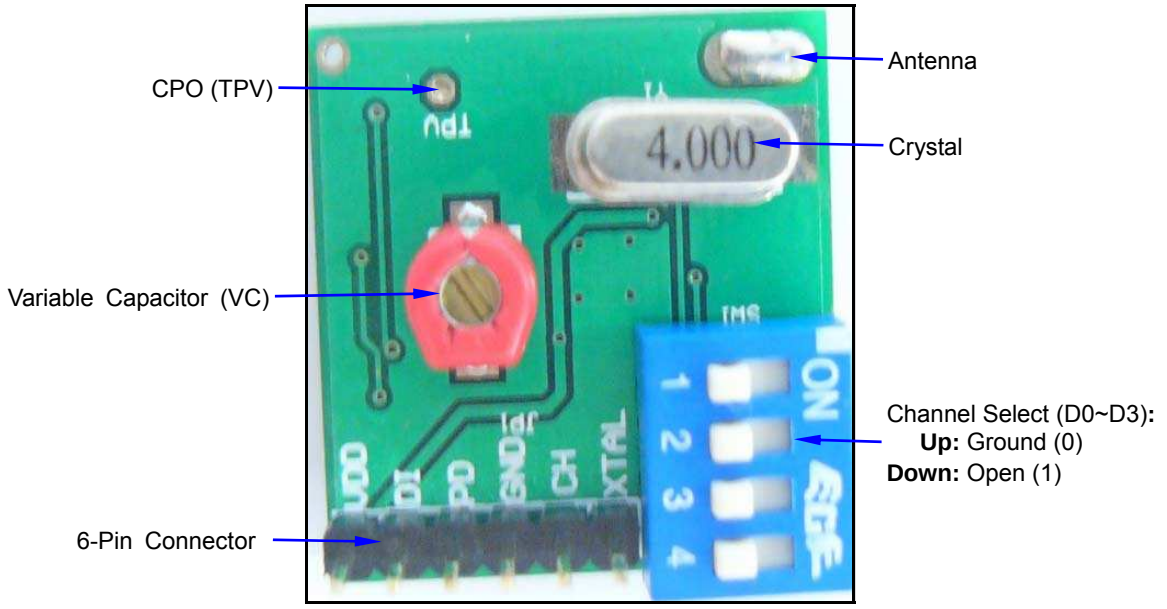


Figure 12-1 ESW5221 TX Board (Top View)

NOTE

1. ***CPO:*** *When Channel-10 is selected, adjust VC until the TPV is at 2 Voltage.*
2. ***ENB:*** *Should be Active Low in order to enable input.*

12.2 Bottom View

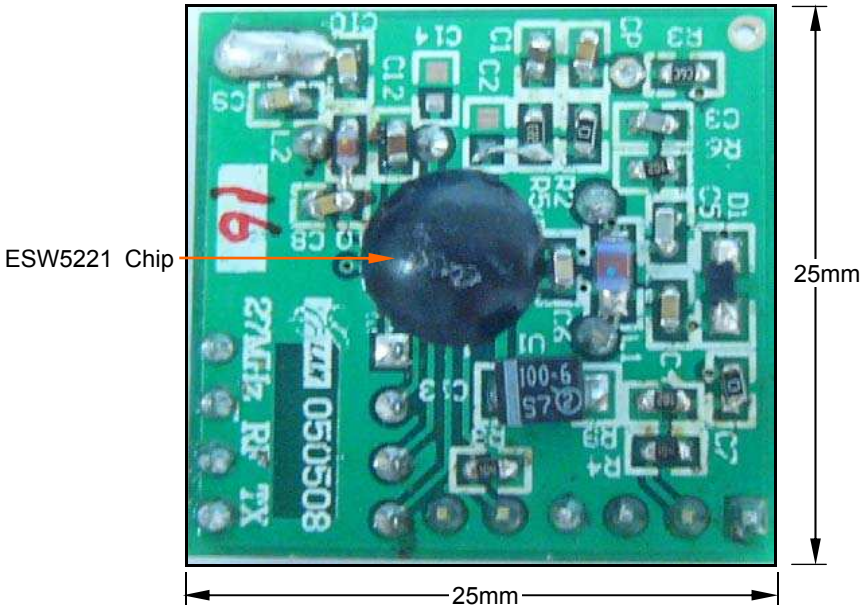


Figure 12-2 ESW5221 TX Board (Bottom View)