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# eSPN03

**Tiny Speech Controller**

# Product Specification

**Doc. VERSION 0.1**

**ELAN MICROELECTRONICS CORP.**


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PRELIMINARY



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# Contents

<b>1</b>	<b>General Description</b>	<b>1</b>
<b>2</b>	<b>Features</b>	<b>1</b>
<b>3</b>	<b>Block Diagram</b>	<b>2</b>
<b>4</b>	<b>Parts List</b>	<b>2</b>
<b>5</b>	<b>PinAssignment and Descriptions</b>	<b>2</b>
<b>6</b>	<b>Arithmetic Logic Unit (ALU)</b>	<b>3</b>
<b>6.1</b>	<b>ALU Instruction Summary</b>	<b>4</b>
6.1.1	Logic Instruction	4
6.1.2	Arithmetic Instruction	4
6.1.3	Data Move Instruction	4
<b>6.2</b>	<b>ALU Related Status Flags</b>	<b>5</b>
6.2.1	Zero Flag Operation	5
6.2.2	Carry Out Flag Operation	5
<b>6.3</b>	<b>Memory Organization</b>	<b>5</b>
6.3.1	Data Memory (RAM)	5
6.3.2	Control Registers	5
6.3.3	ROM Architecture	7
<b>7</b>	<b>Function Description</b>	<b>7</b>
<b>7.1</b>	<b>Control Register Address Map</b>	<b>7</b>
<b>7.2</b>	<b>Control Register Table</b>	<b>8</b>
7.2.1	SR (Status Register)	11
7.2.2	MINF (Channel Interrupt Flag Register)	12
7.2.3	TINF (Timer Interrupt Flag Register)	12
7.2.4	Port1 (Port 1 Control Register)	12
7.2.5	Port2 (Port 2 Control Register)	13
7.2.6	Port3 (Port 3 Control Register)	14
7.2.7	IOC2 (Input/Output Port 2 Direction Control Register)	18
7.2.8	IOC3 (Input/Output Port 3 Direction Control Register)	18
7.2.9	IOC1 (Input/Output Port 1 Direction Control Register)	19
7.2.10	ENTI (Enable Timer Interrupt Control Register)	19
7.2.11	CHPE (Channel Play Enable Control Register)	19
7.2.12	WDTCON (Watchdog Control Register)	20
7.2.13	KCTRL (Key Low Control Register)	21
7.2.14	CTRL3 (ADD/SUB Control Register)	22
7.2.15	PAGE (RAM Page Number Control Register)	24
7.2.16	CTRL1 (IR/Green Mode Control Register)	24
7.2.17	PAV (PinA Value Control Register)	25
7.2.18	VOLH (Volume High Flag Control Register)	25
7.2.19	CTRL2 (Tmsf/Pwmfreq Control Register)	26

<b>7.3 I/O Ports Description</b> .....	<b>27</b>
<b>7.4 System Mode Operation</b> .....	<b>28</b>
7.4.1 Frequency Source .....	29
7.4.2 Normal Mode .....	29
7.4.3 Green (Low ERC) Mode .....	30
<b>7.5 Timer Control</b> .....	<b>31</b>
7.5.1 Timer .....	31
7.5.2 Tmsf (ms Timer Flag) .....	31
7.5.3 Green Mode Timer .....	31
<b>7.6 Interrupt Mode</b> .....	<b>32</b>
<b>8 Instruction Set</b> .....	<b>32</b>
<b>8.1 Introduction</b> .....	<b>32</b>
<b>8.2 Instruction Summary</b> .....	<b>33</b>
8.2.1 Assembly Instruction Set .....	33
8.2.2 Multiple Cycle Instruction .....	35
8.2.3 Speech Macro .....	35
<b>9 Operating Specifications</b> .....	<b>35</b>
<b>9.1 Absolute Maximum Ratings</b> .....	<b>35</b>
<b>9.2 DC Electrical Characteristics</b> .....	<b>36</b>
<b>10 Frequency Deviation</b> .....	<b>36</b>
<b>10.1 Freq. vs. VDD Normal Mode</b> .....	<b>36</b>
<b>10.2 Freq. vs. VDD (Rosc=1M<math>\Omega</math>) Green Mode</b> .....	<b>37</b>
<b>11 Application Circuit Diagram</b> .....	<b>37</b>
<b>11.1 IRC Oscillator in Normal Mode</b> .....	<b>37</b>
<b>11.2 XTAL Oscillator in Normal Mode</b> .....	<b>38</b>
<b>11.3 IRC Oscillator in Green Mode</b> .....	<b>38</b>
<b>11.4 XTAL Oscillator in Green Mode</b> .....	<b>39</b>

### Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial Release of Preliminary Specification	2008/04/11

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## 1 General Description

eSPN03 is a tiny microcontroller-based sound processor IC with single-channel speech audio function that is embedded with an 8k word OTP (One Time Programmable) ROM. The tiny microcontroller incorporates a powerful 4-bit RISC CPU that handles most of the speech functions. It provides a synthesized speech to obtain good quality speech that supports several volume levels. The microcontroller also provides tiny WDT as well as three 4-bit I/O ports. Through programming of the microcontroller, applications, such as section combination, trigger mode, output control, keyboard matrix, and other logic functions can easily put into effect.

In addition to Sleep mode, the eSPN03 also offers Green (IDLE) mode which allows continuous operation under reduced or very low power consumption. Normal operation resumes at a preset time.

These practical features are expected to motivate users in creating a wide variety of new fancy ideas of applications. Moreover, you can take advantage of Elan's Writer and Software simulator to easily program your development code.

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## 2 Features

- System clock:
  - Embedded oscillator (accurate system clock)
    - ⊗ 6MHz @2.5 volts ~ 5.5 volts
  - Crystal Oscillator
    - ⊗ 3.58MHz @2.5 volts ~ 5.5 volts
- 4 bits controller
- Each instruction: 1 or 2 words
- One interrupt entrance
- External interrupt support
- Multiple interrupt source by polling
- Total 2 pages \* 64 nibble (128 nibble) general purpose RAM
- Total of 8 stacks
- Input/Output ports:
  - Three input/output ports (P1 ~ P3)
- Sleep mode for power saving
- Green mode for reduced but continues operation at very low power consumption
- Single ROM with 8K words (maximum) program or voice address
- 1 channel speech only
- Software PCM/eDPCM 6bit/eDPCM 5bit/ ADPCM algorithm for speech synthesis
- 4 steps current control for output pin (Vo1A/Vo1B as general output pin) as well as large current to drive heavy loading components
- 4 steps (1/2, 1/4, 1/8/, and 1/16) light flashing with volume level options
- Watch Dog Timer (WDT)
- Provides Infrared (IR) function and receiver

### 3 Block Diagram

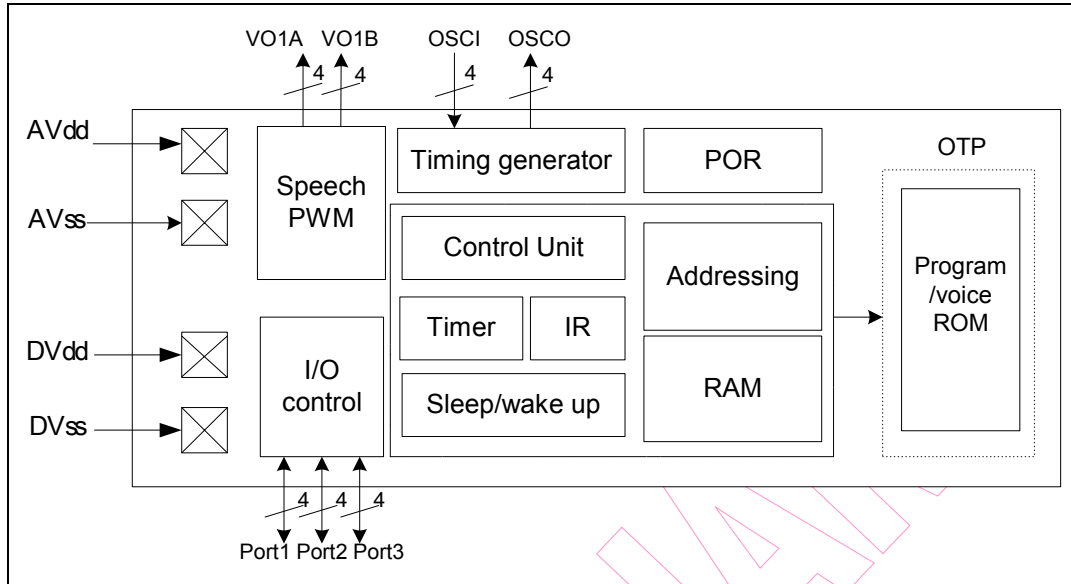


Figure 3-1 eSPN03 Block Diagram

### 4 Parts List

IC Type	Time (Sec)	Stack	Program Size (Words)	ROM (Bits)	RAM (Bits)	I/O (x3)	RC	IR	Channel	PWM
eSPN03	3	8	8K	8K x 16	128 x 4	P1, P2, P3	Yes	Yes	1	1

### 5 Pin Assignment and Descriptions

- 20pin PDIP/SOP package:

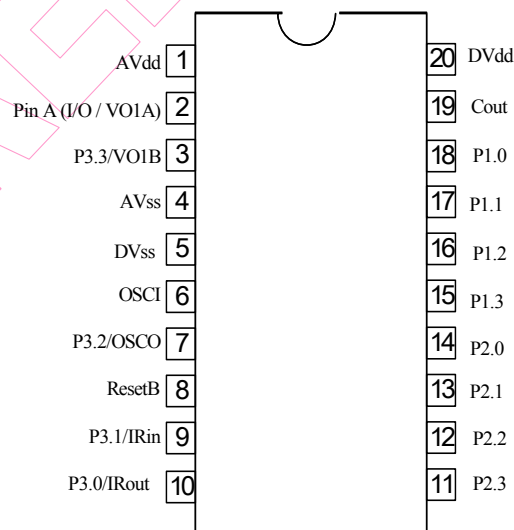


Figure 5-1 eSPN03 Pin Assignment

Symbol	I/O	Function Description
P1.0	I/O	Bit 0 of Port 1
P1.1	I/O	Bit 1 of Port 1
P1.2	I/O	Bit 2 of Port 1
P1.3	I/O	Bit 3 of Port 1 / External interrupt pin (Port1.3 is set as External interrupt pin by Control register)
P2.0	I/O	Bit 0 of Port 2
P2.1	I/O	Bit 1 of Port 2
P2.2	I/O	Bit 2 of Port 2
P2.3	I/O	Bit 3 of Port 2
P3.0/ IRout	I/O	Bit 0 of Port 3 / IR Transmit pad (Port3.0 is set as InfraRed frequency output (IRout) by Control register)
P3.1/ IRin	I/O	Bit 1 of Port 3 / IR Receive pad (Port3.1 is set as InfraRed frequency input (IRin) by Code option)
P3.2/ OSCO	I/O	Bit 2 of Port 3 / Crystal / Ring oscillator input for Green mode (Port3.2 is set as Oscillator by Code option)
P3.3/ VO1B	I/O	Bit 3 of Port 3/ VO1B voice output (Port3.3 be set as VO1B by Code option)
OSCI	I	Crystal(3.58M) oscillator input for Normal mode
AVDD	I	Analog Power
DVDD	I	Digital Power
AVSS	I	Analog Ground
DVSS	I	Digital Ground
PinA (High current I/O /VO1A)	I/O	High current I/O / VO1A voice output (PinA be set as High current I/O or VO1A by Code option)
RESETB	I	Reset pin
Cout	I	Capacitor connection pad*

\* Capacitor value of 4.7uF is recommended

## 6 Arithmetic Logic Unit (ALU)

The eSPN03 provides a 4-bit accumulator and 4-bit arithmetic logic unit that can perform unsigned arithmetic operation, logic operation, data move, etc. There are two flags in the status register to indicate the result of the operations. The following steps occur during an ALU operation:

1. Data is fetched from the source location (such as data memory).
2. Data is then processed by the ALU. If the accumulator is one of the operands, then it will be loaded into the ALU at the same time.
3. Arithmetic instruction can be controlled by the **Instc** register.

Most of the ALU operations have two operands, one must be the accumulator, and the other can either be the constant, memory, or register. In case of just one operand, the data is processed by the ALU itself. For data move operations, the ALU simply passes the source data to its destination.

## 6.1 ALU Instruction Summary

### 6.1.1 Logic Instruction

Instruction	Function	Flag Influenced
AND A, data	Acc ← Acc & data	Z
AND A, Mi (i=0~63)	Acc ← Acc & Mi	Z
OR A, data	Acc ← Acc   data	Z
OR A, Mi (i=0~63)	Acc ← Acc   Mi	Z
XOR A, data	Acc ← Acc ⊕ data	Z
XOR A, Mi (i=0~63)	Acc ← Acc ⊕ Mi	Z

### 6.1.2 Arithmetic Instruction

Instruction	Function	Flag Influenced	
INSTC = 0	ADD A, #data	Acc ← Acc + data	C, Z
	ADD A, Mi (i=0~63)	Acc ← Acc + Mi	C, Z
	SUB A, #data	Acc ← Acc – data	C, Z
	SUB A, Mi (i=0~63)	Acc ← Acc – Mi	C, Z
INSTC = 1	ADD A, #data	Acc ← Acc + data + C	C, Z
	ADD A, Mi (i=0~63)	Acc ← Acc + Mi + C	C, Z
	SUB A, #data	Acc ← Acc – data – (~C) *	C, Z
	SUB A, Mi (i=0~63)	Acc ← Acc – Mi – (~C) *	C, Z
RLCA	{C, Acc[3:0]} = {Acc[3], Acc[2], Acc[1], Acc[0], C}	C, Z	
RRCA	{C, Acc[3:0]} = {Acc[0], C, Acc[3], Acc[2], Acc[1]}	C, Z	

\* (~C) is the inverse of C.

#### NOTE

Refer to item on “INSTC” in Section 7.2.14, CTRL3 (ADD/SUB Control Register) for more details

### 6.1.3 Data Move Instruction

Instruction	Function	Flag Influenced
MOV A, #data	Move data to Accumulator	Z
MOV A, Mi (i=0~63)	Move memory to Accumulator	Z
MOV A, REG	Move register to Accumulator	Z

**NOTE:** “A” under “Instruction” column stands for ACC (accumulator), and “REG” stands for registers, such as I/O ports, or control registers.

## 6.2 ALU Related Status Flags

The ALU related status flags are as follows:

Symbol	Description
C	Carry flag. C=1 if there is carry-out after an ALU operation
Z	Zero flag. Z=1 if the operation is zero

### 6.2.1 Zero Flag Operation

IF Result of Acc ...	Then
Acc = 0	Z = 1
Acc != 0	Z = 0

### 6.2.2 Carry Out Flag Operation

IF	Then	Notice
Acc + #data > 15	C = 1	
15 □ Acc + #data □ 0	C = 0	0 + 0 → C = 0
Acc - #data □ 0	C = 1	0 - 0 or X - X → C = 1
Acc - #data < 0	C = 0	

NOTE: During implementation, subtraction is made by adding 2's complement:  $A - B = A + B + 1$

## 6.3 Memory Organization

The eSPN03 provides 8K words of program/voice ROM and 128 nibbles of data memory (RAM), and 32 nibbles dedicated system control register.

### 6.3.1 Data Memory (RAM)

The eSPN03 data memory has a total of 128 nibbles RAM and 32 nibbles dedicated control register. RAM is partitioned into 2 memory pages. Each memory page contains 64 nibbles.

#### NOTE

The RAM M0~M31 of Pages 0~1 support "BS M, b"; "BC M, b"; "CJBS M, b, Label"; and "CJBC M, b, Label" instructions.

### 6.3.2 Control Registers

A total of 32 nibbles eSPN03 Control Registers are dedicated registers. Their locations (0x0F to 0x15) are partitioned into 6 banks. When using the "banked" area of the Control Register, you must set the bank select register (in the *CHSEL Register*) before accessing the desired register. The following table shows the contents of the "banked" and "unbanked" areas of the Control Register.

Address	Name	
00H	SR	Status register
01H	MINF	Channel interrupt flag register
02H	TINF	Timer interrupt flag register
03H	PORT1	Port 1 input data
04H	PORT2	Port 2 I/O data
05H	PORT3	Port 3 I/O data
06H	Reserved*	
07H	Reserved*	
08H	IOC2	Port 2 direction control
09H	IOC3	Port 3 direction control
0AH	IOC1	Port 1 direction control
0BH	Reserved*	
0CH	ENTI	Timer/External interrupt control register
0DH	CHPE	Channel enable control register
0EH	CHSEL	Channel related control selection register

	CHSEL= 0b0000	CHSEL= 0b0001	CHSEL= 0b0010	CHSEL= 0b0110	CHSEL= 0b0111
0FH	TIH1	TIH2	WDTIH	Reserved*	Reserved*
10H	TIL1	TIL2	WDTIL	Reserved*	Reserved*
11H	Reserved*	Reserved*	Reserved*	Reserved*	DPH
12H	Reserved*	Reserved*	Reserved*	Reserved*	DPM
13H	Reserved*	Reserved*	Reserved*	VOL	DPL
14H	DAOH	Reserved*	Reserved*	Reserved*	DPLL
15H	DAOL	Reserved*	Reserved*	Reserved*	DPLLL

16H	WDTCN	
17H	Reserved*	
18H	KCTRL	Pull-low & wake-up control register
19H	CTRL3	ADD/SUB instruction control register/PinA direction
1AH	PAGE	RAM page selection register
1BH	CTRL1	IR/Green(IDLE) mode control register
1CH	PAV	PinA I/O data
1DH	VOLH	Volume high flag for voice
1EH	Reserved*	
1FH	CTRL2	tmsf/Pwmfreq control register

\* Reserved areas are for ELAN internal use only.

### 6.3.3 ROM Architecture

The eSPN03 provides a program/data/voice single ROM and supports a maximum of 8K words Program ROM. If the ROM is not fully utilized, the remaining space of real chip size can be used as data/voice ROM for speech playback and other user defined applications. The voice ROM can be accessed through hardware or software instruction. Generally, if you want to access the desired data, you need to first write the address of the desired data into the Control Registers and then read the data through READ instruction.

## 7 Function Description

### 7.1 Control Register Address Map

The control register in the eSPN03 is supported by the program counter, hardware stack, interrupts, reset, sleep/wake-up, timer and I/O control. The following sections describe the functions of the components in the control register. The register address map is listed as follows:

Addr	Bits	Name	Bits	Addr	Bits	Name	Bits
00	2	SR	Bit 0: carry Bit 1: zero Bit 2: reserved* Bit 3: reserved*	10	4	TIL / WDTIL	-
01	3	MINF		11	4/1	DPH	-
02	2	TINF	Bit 0: Tinf Bit 1: ExIntF Bit 2: reserved* Bit 3: reserved*	12	4	DPM	-
03	4	Port1	-	13	4/2	DPL/VOL	-
04	4	Port2	-	14	4/4	DAOH/DPLL	-
05	4	Port3	-	15	4/2	DAOL/DPLLL	-
06	(Reserved*)			16	2	WDTCON	Bit0: WDTC Bit1: WDTEN
07	(Reserved*)			17	(Reserved*)		
08	4	IOC2	-	18	4	KCTRL	Bit0: Keyb Bit1: Keylow[0] Bit2: Keylow[1] Bit3: Keylow[2]
09	4	IOC3	-	19	2	CTRL3	Bit0: InstC Bit1: PAIOC Bit2: reserved* Bit3: reserved*
0a	4	IOC1	-	1a	2	Page	Bit0: page number Bit1~2: reserved* Bit3: GreenWKF

\* Reserved bits are for ELAN internal use only

(Continued)

Addr	Bits	Name	Bits	Addr	Bits	Name	Bits
0b	(Reserved*)			1b	3	CTRL1	Bit0: Tx Bit1: reserved* Bit2: GreenWkOpt Bit3: Green
0c	2	ENTI	Bit 0: ENTI Bit 1: EnExtI Bit 2: reserved* Bit 3: reserved*	1c	1	PAV	Bit0: used
0d	3	CHPE		1d	1	VOLH	Bit 0: channel 1
0e	3	CHSEL	Bit2~0: CHSEL Bit 3: reserved*	1e	(Reserved*)		
0f	4	TIH / Timer / WDTIH	-	1f	2	CTRL2	Bit0: reserved* Bit1: tmsf (ms flag) Bit2: Pwmfreq Bit3: reserved*

\* Reserved bits are for ELAN internal use only

## 7.2 Control Register Table

Name	Direction	Bs/Bc	CJBS/ CJBC	Power on	Wake up	Remarks
C	R/W	Yes	Yes	x	u	Carry flag
Z	R/W	Yes	Yes	x	u	Zero flag.
MINF[3:0]	R	No	Yes	0000	0000	channel Interrupt flag Bit 0,1: channel interrupt flag Bit 2: WDT interrupt flag <b>0</b> : channel is not under interrupt mode <b>1</b> : channel is under interrupt mode
TINF	R	No	Yes	0	0	Timer Interrupt flag <b>0</b> : timer interrupt is not under interrupt mode. <b>1</b> : timer interrupt is under interrupt mode.
ExIntF	R	No	Yes	0	0	external Interrupt flag <b>0</b> : external interrupt is not under interrupt mode. <b>1</b> : external interrupt is under interrupt mode.
Port 1[3:0]	R/W	Yes	Yes	xxxx	uuuu	Input/Output Port status <b>1</b> : Provide drive current <b>0</b> : Provide sink current
Port 2[3:0]	R/W	Yes	Yes	xxxx	uuuu	Input/Output Port status <b>1</b> : Provide drive current <b>0</b> : Provide sink current

(Continued)

Name	Direction	Bs/Bc	CJBS/ CJBC	Power on	Wake up	Remarks
Port 3[3:0]	R/W	Yes	Yes	xxxx	uuuu	Input/Output Port status <b>1</b> : Provide drive current <b>0</b> : Provide sink current.
IOC1[3:0]	R/W	Yes	Yes	1111	uuuu	Input/Output Port direction <b>1</b> : Select Port as input <b>0</b> : Select Port as output
IOC2[3:0]	R/W	Yes	Yes	1111	uuuu	Input/Output Port direction <b>1</b> : Select Port as input <b>0</b> : Select Port as output
IOC3[3:0]	R/W	Yes	Yes	1111	uuuu	Input/Output Port direction <b>1</b> : Select Port as input <b>0</b> : Select Port as output
ENTI	R/W	Yes	Yes	0	0	Enable timer interrupt <b>1</b> : Timer interrupt enabled. <b>0</b> : Timer interrupt disabled.
EnExtI	R/W	Yes	Yes	0	u	Enable external interrupt <b>1</b> : external interrupt enabled. <b>0</b> : external interrupt disabled.
CHPE[2:0]	R/W	Yes	Yes	000	000	Channel play / WDT interrupt enable <b>1</b> : interrupt enabled. <b>0</b> : interrupt disabled.
CHSEL[2:0]	R/W	Yes	Yes	xxx	uuu	Channel select register <b>000</b> : channel 0 is selected <b>001</b> : High resolution timer is selected <b>010</b> : WDT is selected <b>110</b> : Volume is selected <b>111</b> : Timer/DP is selected
TIMER[3:0] **	W	No	No	1111	uuuu	Timer parameter register
TIH[3:0] **	W	No	No	xxxx	uuuu	Sample rate integer part high nibble
TIL[3:0] **	W	No	No	xxxx	uuuu	Sample rate integer part low nibble
WDTIH[3:0] **	W	No	No	0100	uuuu	WDT high nibble
WDTIL[3:0] **	W	No	No	0000	uuuu	WDT low nibble
DAOH[3:0] **	W	No	No	0000	0000	DA output high nibble
DAOL[3:0] **	W	No	No	0000	0000	DA output median nibble

\*\* If an attempt is made to read these registers, the random value will result.

(Continued)

Name	Direction	Bs/Bc	CJBS/ CJBC	Power on	Wake up	Remarks
DPH	R/W	Y	Y	x	u	DP address A12
DPM	R/W	Y	Y	xxxx	uuuu	DP address A11 ~ A8
DPL	R/W	Y	Y	xxxx	uuuu	DP address A7 ~ A4
DPLL	R/W	Y	Y	xxxx	uuuu	DP address A3 ~ A0
DPLLL	R/W	Y	Y	xx	uu	Select nibble. Only LSB 2 bits (1, 0) are valid
VOL**	W	No	No	11xx	uuxx	Speech Volume control : 4 steps
WDTC	R/W	Yes	Yes	0	u	Watch dog reset: <b>0</b> : Not effect <b>1</b> : Clear the value of counter (WDTIH/WDTIL)
WDTEN	R/W	Yes	Yes	0	u	Enable Watch dog action
KEYB**	W	No	No	1	u	Port 2 wake-up function enable/disable <b>1</b> : Enable Port2 wake-up. <b>0</b> : Disable Port 2 wake-up.
KeyLow[2:0]**	W	No	No	111	uuu	Port 2 pull low and Port1 and Port 3 pull low/wakeup Bit 0 = Port 1 ( keylow[0] ). Bit 1 = Port 2 ( keylow[1] ). Bit 2 = Port 3 ( keylow[2] ). <b>1</b> : Enable Port2 pull low and Port1&P3 pull low/wake-up <b>0</b> : Disable Port2 pull low and Port1&P3 pull low/wake-up
InstC	R/W	Yes	Yes	0	u	ADD/SUB instruction control register <b>1</b> : Enable add-with-carry/sub-with-borrow function <b>0</b> : Disable add-with-carry/sub-with-borrow function
PAIOC	R/W	Yes	Yes	1	u	Input/Output PinA direction <b>1</b> : Select pin as input <b>0</b> : Select pin as output
PAGE	R/W	No	Yes	x	u	RAM page number
GreenWKF	R	No	Yes	0	u	Green(IDLE) mode timer wake up flag
Tx**	W	Yes	No	0	u	IR output option
GrnWkOpt**	W	Yes	No	0	u	Green(IDLE) mode wake-up option <b>0</b> : I/O, or Timer wake-up <b>1</b> : Only Timer is in wake-up mode

\*\* If an attempt is made to read these registers, the random value will result.

(Continued)

Name	Direction	Bs/Bc	CJBS/CJBC	Power on	Wake up	Remarks
Green**	W	Yes	No	0	0	Green(IDLE) mode register 0: normal mode 1: Green(IDLE) mode
PAV	R/W	Yes	Yes	x	u	Input/Output PinA value 1: Provide drive current 0: Provide sink current.
VOLH	R	No	Yes	x	u	Volume high flag for voice 1: Volume of voice threshold is high 0: Volume of voice threshold is low
tmsf	R/W	Yes	Yes	0	0	Ms timer flag 1: 1.14ms for 3.58MHz 0: 0.68ms for 6MHz
Pwmfreq**	W	Yes	No	0	u	Speech PWM Modulation Freq 0: 48KHz@6MHz 1: 96KHz@6MHz

\*\* If an attempt is made to read these registers, the random value will result.

**Legend:**

- R** : Can be read from the register      **Yes** : BS/BC or CJBS/CJBC instruction enabled      **U** : Unchanged
- W** : Can be written to the register      **No** : BS/BC or CJBS/CJBC instruction disabled      **Z** : High Impedance
- I** : Input type (usually register)      **X** : Unknown or circuit does not need to
- O** : Output type (usually flag)      implement initialization

### 7.2.1 SR (Status Register)

The Status Flag Register contains important status information; including the status of the ALU.

Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Z	C

Bit	Description
Bit 0 (C)	Carry flag
Bit 1 (Z)	Zero flag
Bit 2	Reserved
Bit 3	Reserved

**NOTE**

Refer to Arithmetic Logic Unit (Section 6) and Instruction Set (Section 8) on how to implement the Carry/zero flag.

### 7.2.2 MINF (Channel Interrupt Flag Register)

Channel Interrupt Flag Register represents the interrupt flag occurrence. If bit = 1, the interrupt of relative action will occur. If bit = 0, the interrupt of relative action will not take place.

Bit	Description
Bit 0	Channel interrupt flag
Bit 1	High resolution timer interrupt flag
Bit 2	Watch Dog timer interrupt flag
Bit 3	Reserved

### 7.2.3 TINF (Timer Interrupt Flag Register)

Timer Interrupt Flag Register represents the occurrences of the Timer Interrupt Flag and External Interrupt Flag.

Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	EXINTF	TINF

Bit	Description
Bit 0 (TINF)	Timer interrupt flag bit 0: timer interrupt does not occur 1: timer interrupt occurs
Bit 1 (EXINTF)	External interrupt flag bit 0: external interrupt does not occur 1: external interrupt occur
Bit 2	Reserved
Bit 3	Reserved

### 7.2.4 Port1 (Port 1 Control Register)

Bit	Description
Bit 0	P1.0 input /output value
Bit 1	P1.1 input /output value
Bit 2	P1.2 input /output value
Bit 3	P1.3 input /output value (external interrupt pin)

The Port 1 Control Register is used by IOC1 register to input/output values. Bit “KeyLow[0]” can control the pull-low function of Port 1. If KeyLow[0] = 1, it enables the pull-low and wake-up functions of Port 1. If KeyLow[0] = 0, it disables the pull-low and wake-up functions of Port 1. When “EnExtI” register is set to “1”, the Port 1 (P1.3) 3rd bit becomes the External Interrupt pin. Port 1 also functions as wake-up pin for Sleep/Green mode.

### 7.2.5 Port2 (Port 2 Control Register)

Bit	Description
Bit 0	P2.0 input/output value
Bit 1	P2.1 input/output value
Bit 2	P2.2 input/output value
Bit 3	P2.3 input/output value

The Port 2 Control Register is used by IOC2 register to input/output values. Bit “KeyLow[1]” can control the pull-low function of Port 2. When KeyLow[1] = 1, Port 2 pull-low function is enabled. When KeyLow[1] = 0, it is disabled.

Bit “Keyb” controls the wake-up function. When Port 2 is set as input and Keyb = 1, the Port 2 wake-up function is enabled. If Keyb = 0, wake-up function is disabled.

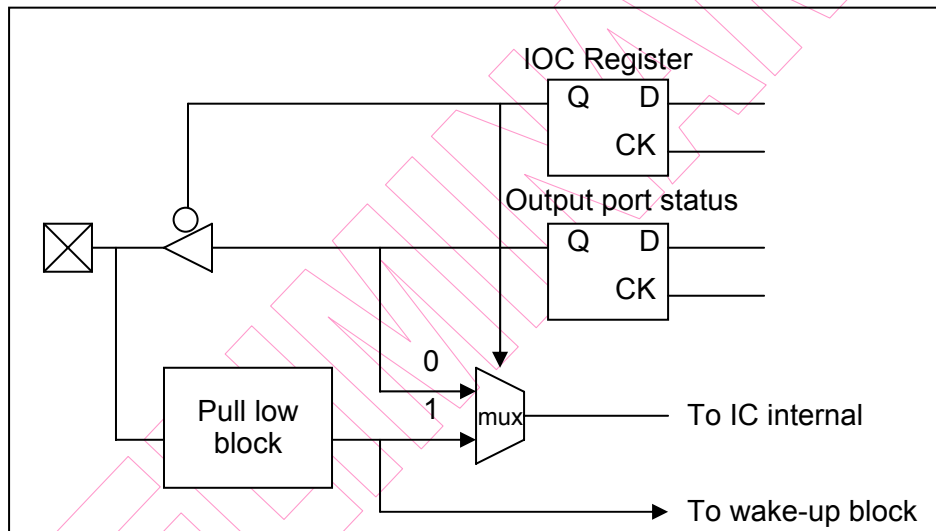


Figure 7-1 Port 2 Block Diagram

### 7.2.6 Port3 (Port 3 Control Register)

Bit	Description
Bit 0	P3.0 input/output value (IRout)
Bit 1	P3.1 input/output value (IRin)
Bit 2	P3.2 input/output value (OSCO pin)
Bit 3	P3.3 input/output value (VO1B pin)

#### ■ GPIO

The Port 3 Control Register is used by the IOC3 register to input/output values. Bit “KeyLow[2]” controls the pull low and wake-up function of Port 3. When Port 3 is set as input and if KeyLow[2] = 1, it enables both the pull low and wake-up functions of Port 3. If KeyLow[2] = 0, it disables both pull low and wake-up functions of Port 3.

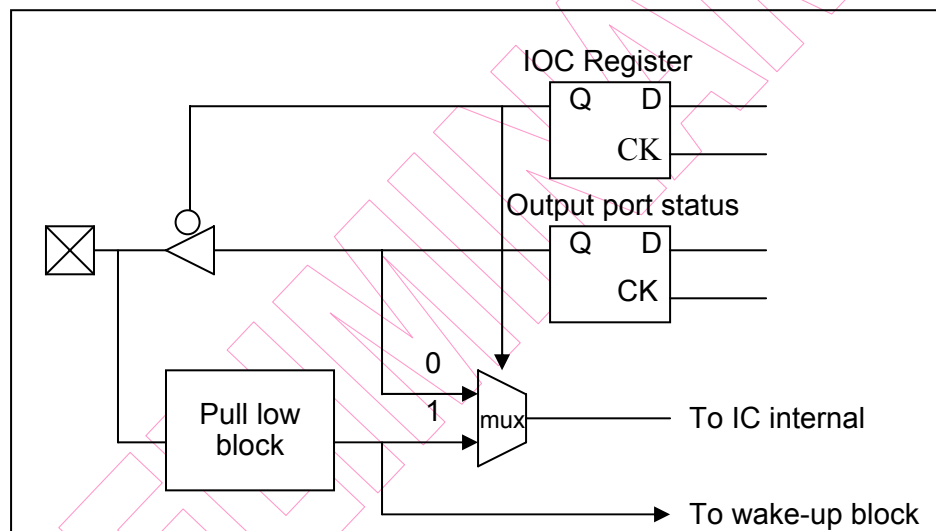


Figure 7-2a Port 3 Block Diagram

In addition to their respective unique functions, all four function pins of PORT3 are also able to offer common GPIO function:

- ◇ P3.0 can serve as GPIO or IRout
- ◇ P3.1 can serve as GPIO or IRin
- ◇ P3.2 can serve as GPIO or OSCO
- ◇ P3.3 can serve as GPIO, VO1B, or high current I/O

Selecting which function to assign for each pin is further discussed in the following sections.

■ **P3.0: GPIO / InfraRed Frequency Output (IRout)**

Port3.0 has two different functions that are selected by Tx control register. One is as GPIO pin, and the other is as IR output. When Port3.0 is used as IR output pin, it generates the Infrared frequency (38kHz) for transmission and the GPIO function is disabled.

**NOTE**  
*Refer to item on "Tx" under Section 7.2.16 (CTRL1) for more details.*

■ **P3.1: GPIO / InfraRed Frequency Input (IRin)**

Port3.1 has two different functions selected through the IDE Code option dialog as illustrated in the figure below. One is as GPIO pin, the other is as IR input pin. When Port3.1 is used as IR input pin, it receives infrared frequency. The GPIO function is disabled.

When P3.1 is used as IRin, it wakes up the chip from GREEN (IDLE) and SLEEP modes.

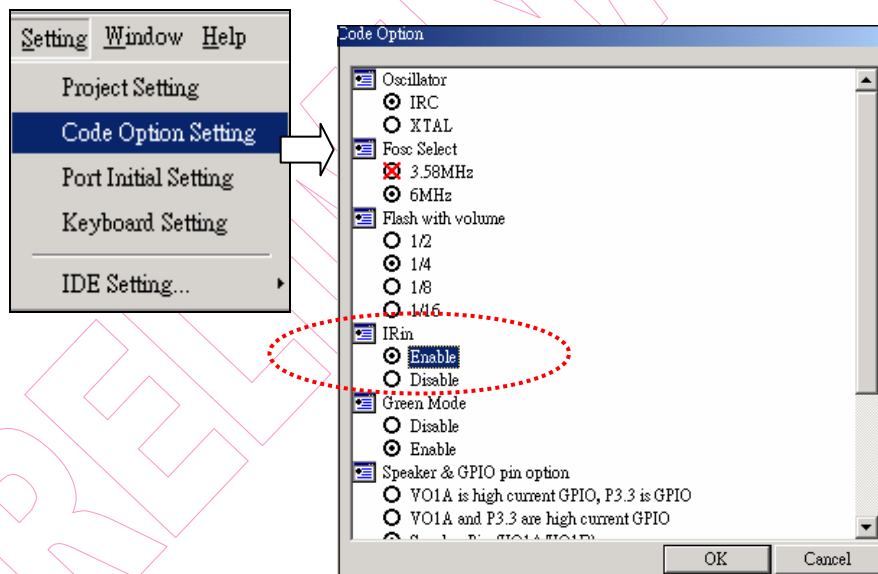


Figure 7-2b Code Option Dialog with "IRin" Option Enabled

■ P3.2: GPIO / OSCO

When the “Green Mode” option buttons of Code Option dialog (see figure below) is set to “Enable”, or the “Oscillator” option buttons is set at “XTAL” in IDE, P3.2 is used as OSCO pin, otherwise, P3.2 is GPIO pin.

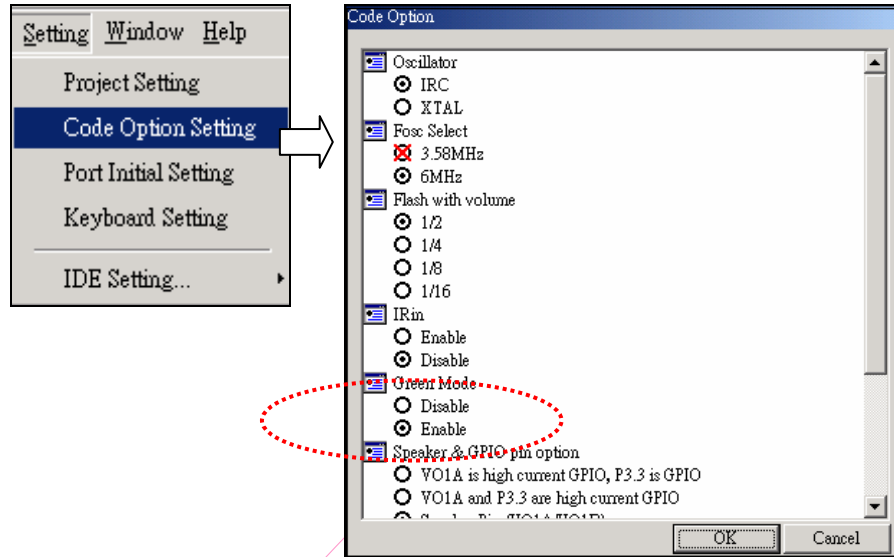


Figure 7-2c Code Option Dialog with “Green Mode” Option Enabled

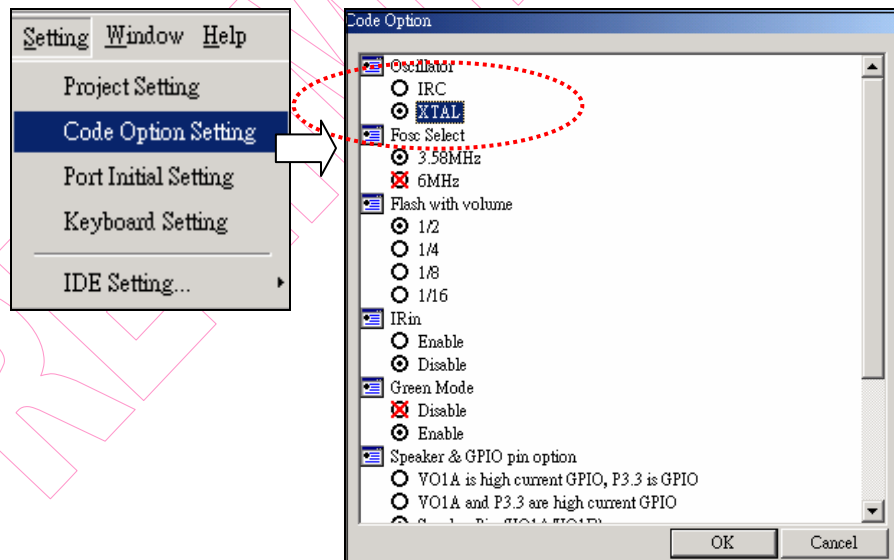


Figure 7-2d Code Option Dialog with “Oscillator” Option Buttons Set at “XTAL”

■ P3.3: GPIO / VO1B / High Current I/O

1. When “Speaker & GPIO pin option” option buttons of Code Option dialog (figure below) is set to “PinA is high current GPIO, P3.3 is GPIO” in IDE, PinA can output 4-step large current (50/100/150/200mA) controlled by VOL register, and P3.3 is used as **GPIO pin**, while both speaker PWM and high current I/O functions are disabled.

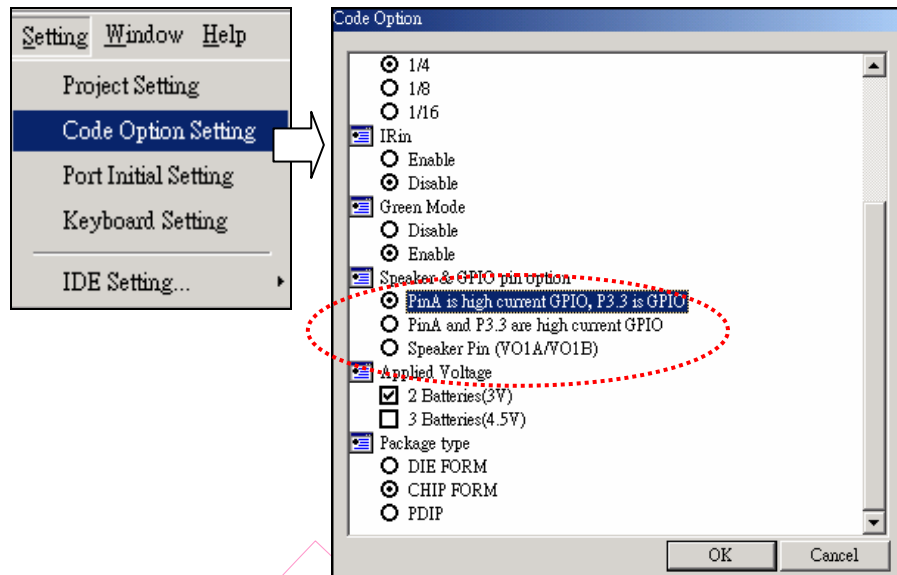


Figure 7-2e Code Option Dialog with “Speaker & GPIO pin option” Option Buttons Set at “PinA is high current GPIO, P3.3 is GPIO”

2. When “Speaker & GPIO pin option” option buttons of Code Option dialog (see figure below) is set to “PinA and P3.3 are high current GPIO” in IDE, P3.3 is used as **high current I/O pin** and both PinA and P3.3 can output 4-step large current (50/100/150 /200mA) controlled by VOL register. Both speaker PWM and GPIO functions are disabled.

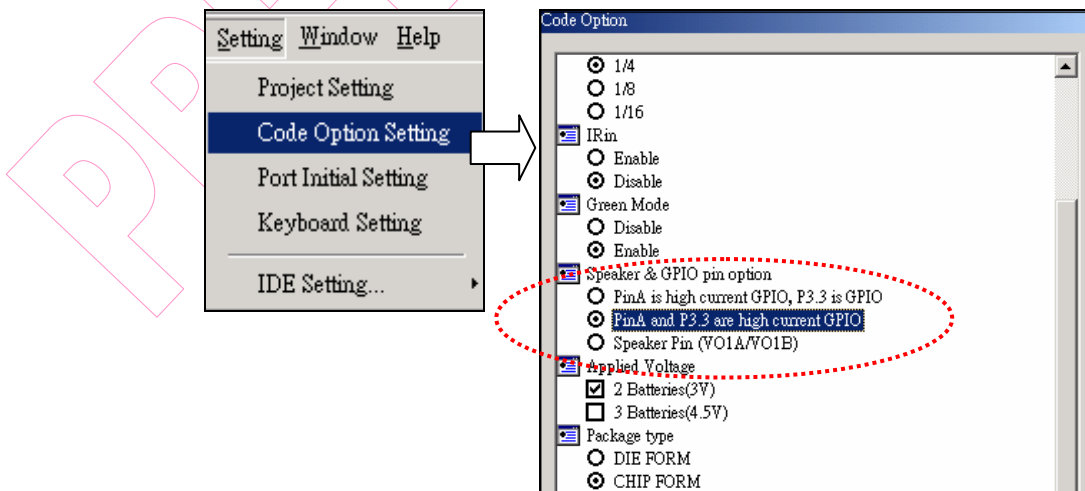


Figure 7-2f Code Option Dialog with “Speaker & GPIO pin option” Option Buttons set at “PinA and P3.3 are high current GPIO”

- When “Speaker & GPIO pin option” option buttons of Code Option dialog (see figure below) is set to “Speaker pin (VO1A/VO1B)” in IDE, P3.3 is used as **VO1B pin** and both PinA and P3.3 can output 4-step large current (50/100/150 /200mA) controlled by VOL register. Both speaker PWM and GPIO functions are disabled.

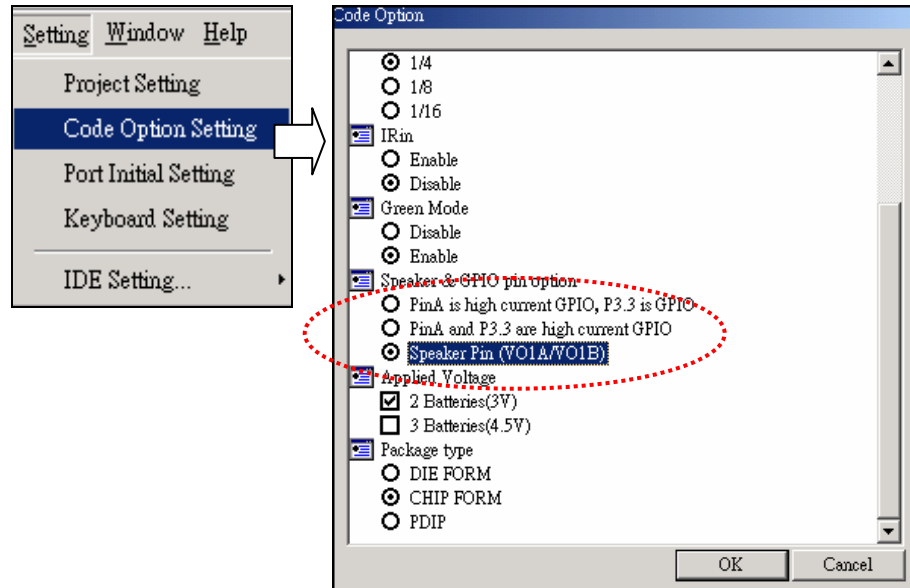


Figure 7-2g Code Option Dialog with “Speaker & GPIO pin option” Option Buttons Set at “Speaker pin (VO1A/VO1B)”

### 7.2.7 IOC2 (Input/Output Port 2 Direction Control Register)

The IOC2 Control Register is used to set Port 2 as input/output port. If Bit = 1, Port 2 is set as input. If Bit = 0, it is set as output.

Bit	Description
Bit 0	Set P2.0 as input/output
Bit 1	Set P2.1 as input/output
Bit 2	Set P2.2 as input/output
Bit 3	Set P2.3 as input/output

### 7.2.8 IOC3 (Input/Output Port 3 Direction Control Register)

The IOC3 Control Register is used to set Port 3 as input/output port. If Bit = 1, Port 3 is set as input. If Bit = 0, it is set as output.

Bit	Description
Bit 0	Set P3.0 as input/output
Bit 1	Set P3.1 as input/output
Bit 2	Set P3.2 as input/output
Bit 3	Set P3.3 as input/output

### 7.2.9 IOC1 (Input/Output Port 1 Direction Control Register)

The IOC1 Control Register is used to set Port 1 as input/output port. If Bit = 1, Port 1 is set as input. If Bit = 0, it is set as output.

Bit	Description
Bit 0	Set P1.0 as input/output
Bit 1	Set P1.1 as input/output
Bit 2	Set P1.2 as input/output
Bit 3	Set P1.3 as input/output

### 7.2.10 ENTI (Enable Timer Interrupt Control Register)

ENTI Control Register enables the Timer or External Interrupt actions.

Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	EnExtI	ENTI

Bit	Description
Bit 0 (ENTI)	Timer interrupt enable bit 0: timer interrupt is disabled 1: timer interrupt is enabled
Bit 1 (EnExtI)	External interrupt enable bit 0: external interrupt is disabled 1: external interrupt is enabled
Bit 2	Reserved
Bit 3	Reserved

### 7.2.11 CHPE (Channel Play Enable Control Register)

This register enables the Channel Play Speech, High Resolution Timer, or Watchdog Timer. If Bit = 1, the corresponding interrupt action is enabled. If Bit = 0, the corresponding interrupt action is disabled. Default is CHPE = x000.

Bit 3	Bit 2	Bit 1	Bit 0
Reserved	CHPE2	CHPE1	CHPE0

Bit	Description
Bit 0	Channel play enabled bit
Bit 1	High resolution timer enabled bit
Bit 2	High resolution timer / watchdog timer enabled bit
Bit 3	Reserved

### 7.2.12 WDTCON (Watchdog Control Register)

The WDT (Watchdog Timer) is used to resume the controller operation after a reset triggered by noise disturbance, system error, or other malfunctions. You can clear WDT counter to avoid reset from occurring through WDTCON setup. The WDT can be set as High Resolution Timer by clearing WDTEN.

Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	WDTEN	WDTCON

Bit	Description
Bit 0	Clear the WDT timer count
Bit 1	Enable watchdog action
Bit 2	Reserved
Bit 3	Reserved

If you want to use WDT or High Resolution Timer function, set CHPE[2] as follows:

- If CHPE[2]=1 and WDTCON[1]=1, WDT function is enabled.
- If CHPE[2]=1 and WDTCON[1]=0, WDT function is disabled but the High Resolution Timer is enabled.
- If CHPE[2]=0, (WDTCON[1] don't care) WDT function and High Resolution Timer are disabled.
- When you want to set WDTCON register to clear WDT counter value, make sure WDTEN and CHPE[2] registers are initially set to "1" (enabled). If one of them is disabled, setting WDTCON register instruction is inaccessible.

When the WDT function is enabled, the clock source will depend on different system frequency; i.e.,:

- If  $F_{High} = 6M$ , the clock source will be about 2.93 KHz.
- If  $F_{High} = 3.58M$ , the WDT clock source will be about 1.75 KHz.

Register	Bit	DIR	Description	Default Value
WDTCON	WDTEN	[1]	R/W Enable or Disable WDT function 0: disable WDT function 1: enable WDT function	0
	WDTCON	[0]	R/W Clear WDT count 1: clear WDT counter value 0: not effect	0
WDTIH	[3:0]	W	WDT high nibble.	0100
WDTIL	[3:0]	W	WDT low nibble.	0000
CHPE	CHPE[2]	[2]	R/W Enable WDT and TIMER control 0: disable 1: enable	0

### 7.2.13 KCTRL (Key Low Control Register)

The eSPN03 provides up to three I/O ports, designated as Port 1 through Port 3. The I/O port configurations are controlled by the I/O mapped registers. The following table summarizes the three ports functions and their respective control register locations:

Port	I/O Type	Pull-Low	Wake-Up	Address	Control Register
Port 1	I/O	Yes	Yes	0x03	IOC1 (0xa)
Port 2	I/O	Yes	Yes	0x04	IOC2 (0x8)
Port 3	I/O	Yes	Yes	0x05	IOC3 (0x9)

Bit	Description
Bit 0	keyb
Bit 1	Port 1 pull low enable/disable
Bit 2	Port 2 pull low enable/disable
Bit 3	Port 3 pull low enable/disable

- Keyb is used to enable/disable Port 2 wake-up function:
  - Keyb = 1:** Enable wake-up function of Port 2.
  - Keyb = 0:** Disable wake-up function of Port 2.
- KeyLow is used to enable/disable pull-low function of Port 1, 2, and 3:
  - KeyLow[0] = 1:** Enable pull-low and wake-up function of Port 1.
  - KeyLow[0] = 0:** Disable pull-low and wake-up function of Port 1.
  - KeyLow[1] = 1:** Enable pull-low function of Port 2.
  - KeyLow[1] = 0:** Disable pull-low function of Port 2.
  - KeyLow[2] = 1:** Enable pull-low and wake-up function of Port 3.
  - KeyLow[2] = 0:** Disable pull-low and wake-up function of Port 3.

The data registers (Port1, Port2, & Port3) latch the high/low status of the I/O ports. The control registers (IOC1, IOC2, & IOC3) determine the direction (input or output) of the bi-directional ports. Note that the bi-directional ports are configured as input ports during a reset and the initial pin status is unknown. You must remember to write the initial values to these ports before configuring them as output ports.

The pull-low control block diagram is shown below:

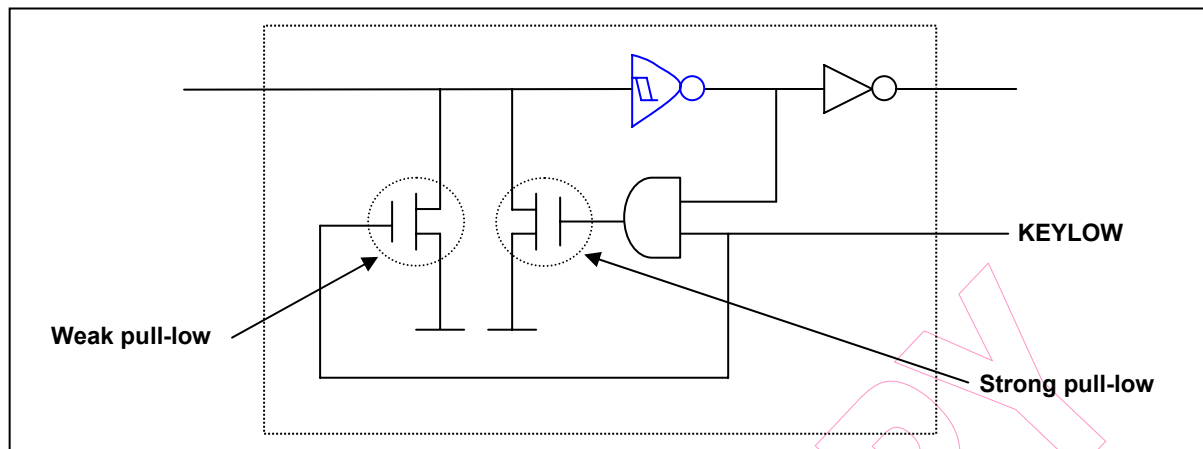


Figure 7-3 Pull-Low Control Block Diagram

When the KeyLow is high, two pull-low devices are enabled, one is a strong pull-low (small impedance), and the other is the weak pull-low (large impedance). When the input goes low, the strong pull-low becomes active, and the pull-low resistor is shunted with these two devices. When the input becomes high, the strong pull-low is disabled, and the weak pull-low (large impedance) will drive a smaller input current.

#### 7.2.14 CTRL3 (ADD/SUB Control Register)

Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	PAIOC	INSTC

##### ■ INSTC

The Bit 0 of INSTC register controls the ADD/SUB instruction function. It can change the ADD/SUB instruction function to ADC/SUBB instruction (ADD with Carry/Sub with Borrow) and use the same instruction name.

■ PAIOC

1. PinA has two different functions. One is as **VO1A pin**, the other is as **high current I/O pin** where it can output 4-step large current (50/100/150/200mA) controlled by VOL register. When PinA is used as **VO1A pin**, speaker PWM function is enabled, otherwise, PinA is used as high current I/O pin and speaker PWM function is disabled. Selection between these two functions is done through the “Code Option” dialog of IDE; i.e., to set PinA as VO1A pin, from IDE Menu bar; click **Setting** → **Code Option Setting** or as illustrated below.

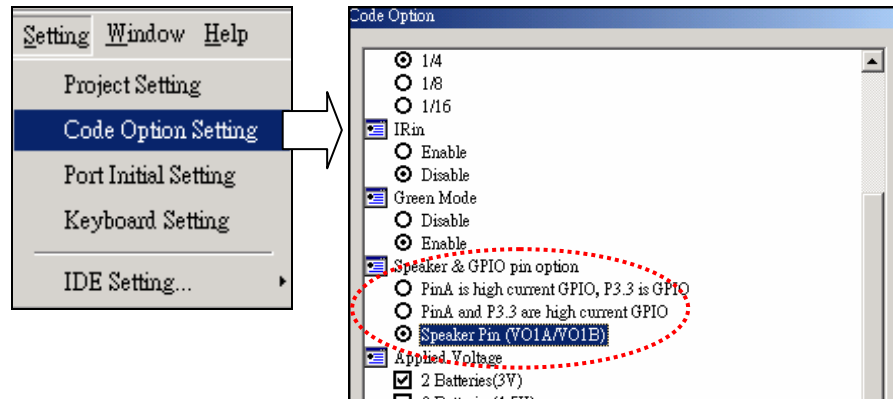


Figure 7-4a Accessing IDE “Code Option” Dialog to Set PinA as VO1A Pin

2. When PinA is used as **high current I/O pin**, it can output 4-step large current (50/100/150/200mA) controlled by VOL register and PAIOC will set PinA as input/output port. If PAIOC=1, PinA is set as input. If PAIOC = 0, PinA is set as output.

To set PinA as high current I/O pin, from IDE Menu bar, click **Setting** → **Code Option Setting** or as illustrated below..

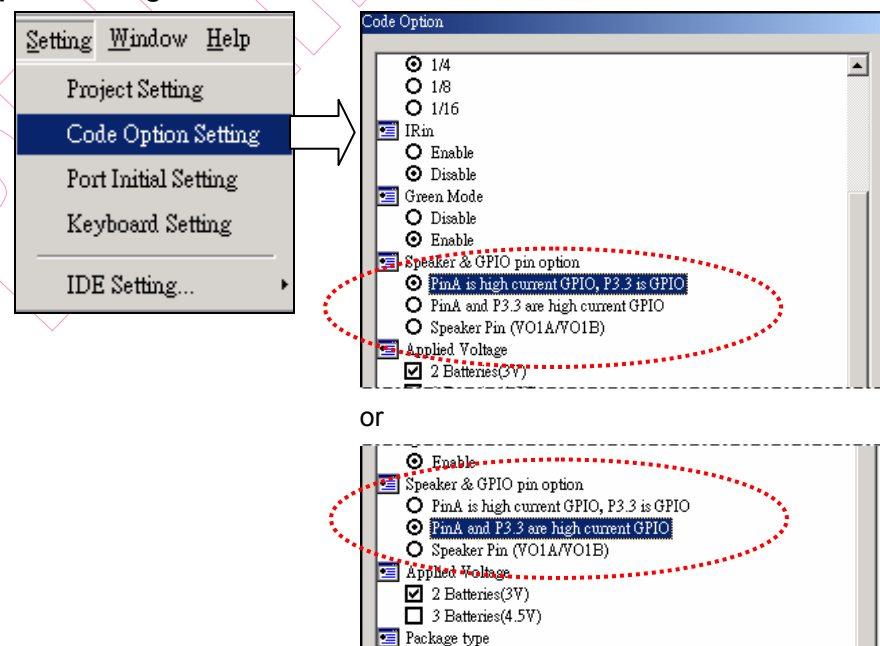


Figure 7-4b Accessing IDE “Code Option” Dialog to Set PinA as High Current I/O Pin

### 7.2.15 PAGE (RAM Page Number Control Register)

Bit 3	Bit 2	Bit 1	Bit 0
GreenWKF	Reserved	Reserved	Page number

#### ■ Page number

Bits 0 of the RAM Page Number Control Register is used to represent the RAM page number.

#### ■ GreenWKF

After Timer wakes up from Green mode, the GreenWKF flag of Page register will be set to "1." You can check the flag to obtain the wakeup source.

### 7.2.16 CTRL1 (IR/Green Mode Control Register)

CTRL1 Control Register is used to enable the IR output mode, Green mode wake-up option, and Green mode enable control. By default, CTRL1 = 00x0.

Bit 3	Bit 2	Bit 1	Bit 0
Green	GrnWkOpt	Reserved	Tx

Bit	Description
Bit 0	IR output option
Bit 1	Reserved
Bit 2 (GrnWkOpt)	Green mode wake-up option bit 0: allow I/O or Timer wake-up from Green mode 1: only the Timer can wake-up from Green mode
Bit 3 (Green)	Green mode bit 0: Normal mode 1: Green mode

#### ■ Tx

Under the IRC mode ( $F_{High} = 6M$ ) or XTAL mode ( $F_{High} = 3.58M$ ), if the Bit 0 of CTRL1 register is "1", the P3.0 becomes **IRout output** that generates the Infrared frequency (38kHz).

If the Bit 0 of CTRL1 is cleared ("0"), the IRout becomes the **GPIO pin (P3.0)** and its value will be in concurrence with Bit 0 of PORT3 register.

■ **GrnWkOpt**

Green mode wakes up through Input Port 1/Port 2/Port 3, or Timer Generator Underflow. The “GrnWkOpt” register will set the wake-up source.

The following is the wake-up option table.

GrnWkopt Register	Green Mode → Normal Mode Wakeup Source
0	All wake-up sources, including I/O (Port 1/Port 2/Port 3) & Timer can wake-up the eSPN03 from Green mode.
1	Only Timer timeout will wake-up the eSPN03 from Green mode.

After Timer wakes up from Green mode, the GreenWKF flag of Page register will set to “1”.

**7.2.17 PAV (PinA Value Control Register)**

Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	PAV

When PinA is defined as high current I/O pin, PAIOC of CTRL3 register is used to set PinA as input/output port. PAV is used to set the PinA value.

**7.2.18 VOLH (Volume High Flag Control Register)**

Volume High Flag Control Register is used to indicate that the corresponding channel is set at high or low volume. If Bit = 1, the volume of the corresponding channel is high. If Bit = 0, volume is low.

Bit	Description
Bit 0	Channel 1 volume flag
Bit 1	Reserved
Bit 2	Reserved
Bit 3	Reserved

**NOTE:** The voice volume level is selected through code option of IDE.

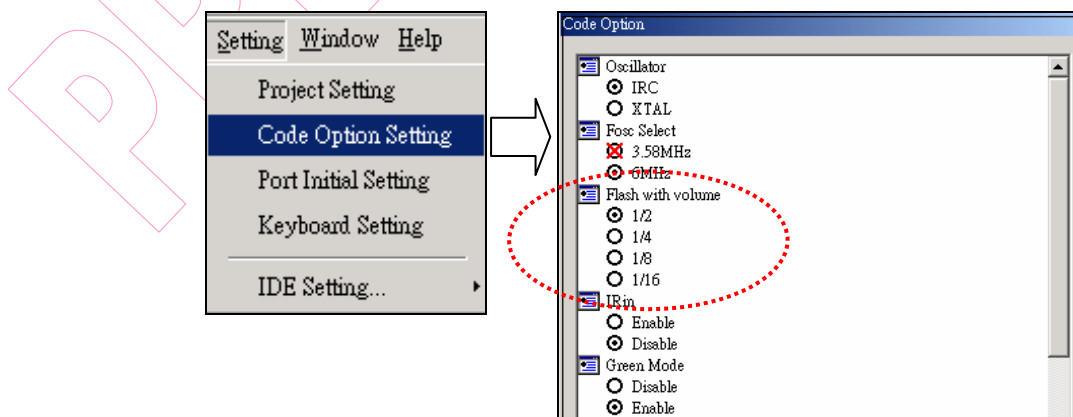


Figure 7-5 Accessing IDE “Code Option” Dialog to Set Voice Volume Level

### 7.2.19 CTRL2 (Tmsf/Pwmfreq Control Register)

CTRL2 register controls the ms timer flag and PWM modulation frequency.

Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Pwmfreq	Tmsf	Reserved

Bit	Description
Bit 0	Reserved
Bit 1	tms timer flag
Bit 2	PWM modulation frequency 0: 48kHz @ 6MHz ; 28.8kHz @ 3.58MHz 1: 96kHz @ 6MHz ; 57.6kHz @ 3.58MHz
Bit 3	Reserved

#### NOTE

*Better speech quality can be obtained by setting Bit2 of CTRL2 to "0"*

When speaker PWM is used to play speech, setting an appropriate frequency could improve the quality of speech playback. You can use macro "**samplerate1**" to set sampling rate. The matching table is listed below.

#### ■ Matching table:

32KHz Pwmfreq=0	3.58MHz	6MHz	64KHz Pwmfreq=1	3.58MHz	6MHz
1	27968	23437	1	27968	23437
2	13984	15625	2	18645	18750
3	9322	11718	3	13984	15625
4	6992	9375	4	11187	13392
5	5593	7812	5	9322	11718
6	4661	6696	6	7991	10416
7	3995	5859	7	6992	9375
8		5208	8	6215	8522
9		4687	9	5593	7812
10		4261	10	5085	7211
			11	4661	6696
			12	4302	6250
			13	3995	5859
			14		5514
			15		5208
			16		4934
			17		4687
			18		4464
			19		4261

#### NOTE

*Refer to Macro on "SampleRate1" under Section 8.2.2 for more details.*

### 7.3 I/O Ports Description

The eSPN03 supports a total of three ports with each port containing 4 bits.

**Port 1:** Available as input or output as defined by the Control Register.

When set to input status, the pull low resistor and wake-up mechanism can be enabled or disabled by the same Control Register.

When set to output status, another register is used to select port to sink or drive outside the circuit.

**Port 2:** Port 2 characteristics are the same as Port 1 except for the pull low resistor and wake-up mechanism which can be enabled or disabled by different Control Register.

**Port 3:** Port 3 characteristics are the same as Port 1.

Each of the port configurations can be summarized as follows:

Port	Available	I/O Direction Controllable	Input Mechanism	
			Pull Low	Wake-up
Port 1	I/O	√ (c)	√ (c)	√ (c)
Port 2	I/O	√ (c)	√ (c)	√ (c)
Port 3	I/O	√ (c)	√ (c)	√ (c)

**Legend:** **I:** input; **I/O:** input/output; **O:** output.

√: Available

(c): Can be enabled/disabled by register.

## 7.4 System Mode Operation

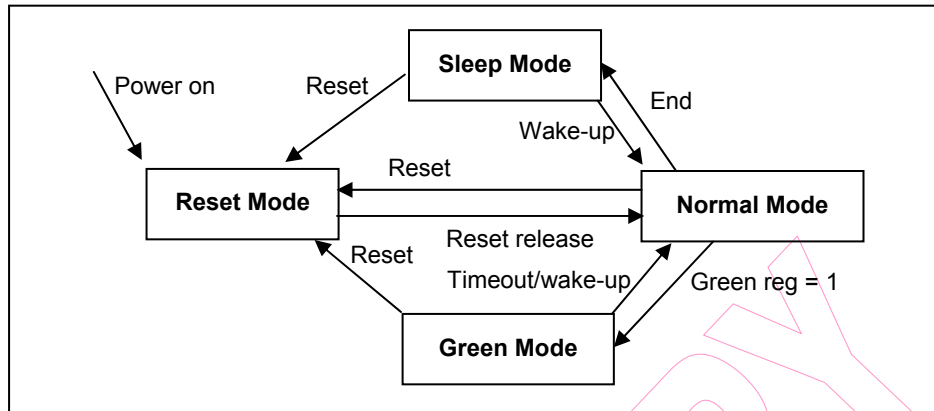


Figure 7-6 System Mode Operation Flow Chart

The Green mode suspends all CPU functions except for the low-frequency clock oscillation and timer generator. The Green mode → Normal mode control register status behavior is the same as the Sleep mode → Normal mode status.

The Timer Generator Interrupt (ENTI) and speech voice (Channel play enable) for Normal mode are disabled under Green mode.

The Green mode will wake-up using the wake-up pin or timer generator. After waking up, the program will run the next instruction following the “Green” register enable instruction, and the Green mode is disabled. When executing “Green” register = 1, the timer generator must reload the timer register again for wake-up countdown.

When “Green” register is enabled, the timer clock source generator will come from  $F_{Low}$ . The timer change must occur at the end of the above instruction execution. Whenever timer changes, i.e., Green mode → Normal mode, the clock source will come from  $F_{High}$ .

Green mode is a very useful feature for conserving power (see table below) and in extending the life span of batteries. With in Green mode, it is possible to achieve continuous operation under reduced or very low power consumption (less than  $15\mu A@3V$ ) and to resume normal operation at a preset time.

Mode	Current Consumption	Suitable Usage Condition
Normal mode	maximum 4 mA@ $V_{DD}=3V$	Complex computing, scenario flow control, high power consumption
Green mode	maximum 15 $\mu A@V_{DD}=3V$	Long (preset) continuous operation but with reduced or very low power consumption
Sleep mode	maximum 4 $\mu A@ V_{DD}=3V$	Sleep (no operation) & wake-up only to conserve power

### 7.4.1 Frequency Source

The eSPN03 offers two (High & Low frequencies) clock sources. High frequency clock is used for Normal mode, and the Low frequency (about 32kHz) clock is used for Green mode. The Low frequency clock shares with OSCO pin.

Mode Operation	Clock Source
Normal mode	F <sub>High</sub> = IRC mode or XTAL mode
Green mode	F <sub>Low</sub> = ERC mode

**NOTE**

*If resistor is not connected to OSCO pin, eSPN03 can NOT perform Green mode function when the IDE Green mode code option is enabled.*

### 7.4.2 Normal Mode

The eSPN03 provides two different oscillator modes for Normal mode operation; i.e., Internal RC oscillator mode (IRC) and XTAL mode. You can select one of them to operate your various applications.

**IRC Mode:** To use the internal RC oscillator mode (IRC), eSPN03 does not need to connect an external resistor to OSCI pin which minimizes external components consumption.

If the IDE code 6M option is selected, the internal RC oscillator will generate the 6M frequency to eSPN03.

**XTAL Mode:** To achieve a more accurate frequency, eSPN03 offers the XTAL mode.

Pin OSCI/OSCO must be connected with a crystal to generate oscillation and use ceramic resonator to as general application to minimize interference. Figure below depicts such circuit for connecting the components. The table that follows the figure provides the recommended value of C1/C2. Since each resonator has its own attributes, you should refer to its specification for appropriate C1/C2 value.

If the IDE XTAL code option is selected, the use of 3.58MHz crystal is highly recommended.

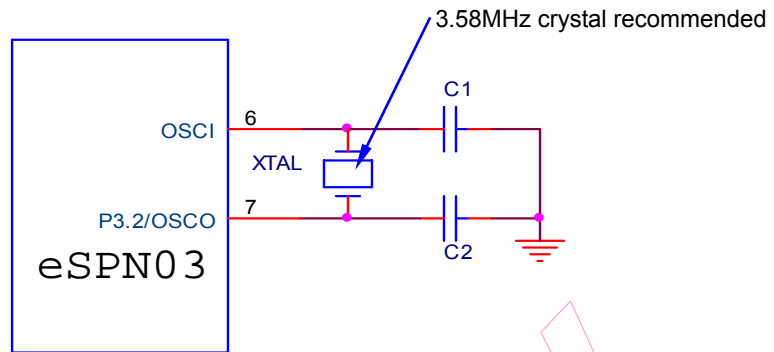


Figure 7-7 Connecting Pin OSCI/OSCO to Crystal and C1/C2 in XTAL (Normal) Mode

Oscillator Type	Frequency	C1(pF)	C2(pF)
Ceramic resonator	3.58M	10~30	10~30
Crystal	3.58M	15	15

**NOTE**

When XTAL is selected as IDE code option, P3.2 will no longer operate as I/O pin.

### 7.4.3 Green (Low ERC) Mode

In addition to XTAL and IRC modes, eSPN03 also provides a Low ERC (External Resistor) mode for low power consumption operation.

To operate in Low ERC (Green) mode, a resistor (R) is required and should only be connected to OSCO pin. In XTAL mode, the applicable 1MΩ oscillator resistor is connected to OSCO as shown in the left figure below. For IRC mode, the applicable 1MΩ oscillator resistor is connected in series with OSCO (see right figure below).

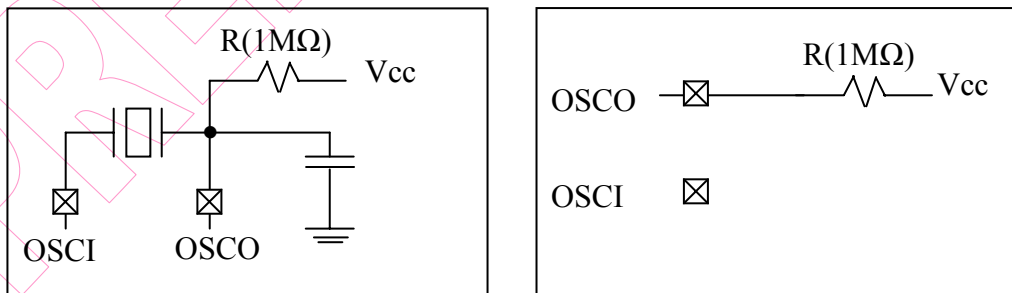


Figure 7-8 Connecting OSCO in Low ERC XTAL Mode (Left) and IRC Mode (Right)

## 7.5 Timer Control

### 7.5.1 Timer

The eSPN03 has a down counter with reload and interrupt functions. The down counter is 4-bit in width. Counter underflow will trigger the Timer Interrupt and automatically reload the Timer Counter value into the TIMER register.

For 6MHz IRC mode, the Timer Counter clock source is 0.341ms. The Timer Counter underflow period is  $0.341 \times (N+1)$  ms, where N is the 4-bit reload value in the TIMER register.

To setup the Timer register, the value of CHSEL register must be #0111.

0	1	2	3	4	5	6	7
0.341ms	0.682ms	1.023ms	1.364ms	1.705ms	2.046ms	2.387ms	2.728ms
8	9	10	11	12	13	14	15
3.069ms	3.41ms	3.751ms	4.092ms	4.433ms	4.774ms	5.115ms	5.456ms

For 3.58MHz XTAL mode, the Timer Counter clock source is 0.572ms. The Timer Counter underflow period is  $0.572 \times (N+1)$  ms, where N is the 4-bit reload value in TIMER register.

0	1	2	3	4	5	6	7
0.572ms	1.144ms	1.716ms	2.288ms	2.86ms	3.432ms	4.004ms	4.576ms
8	9	10	11	12	13	14	15
5.148ms	5.72ms	6.292ms	6.864ms	7.436ms	8.008ms	8.58ms	9.152ms

### 7.5.2 Tmsf (ms Timer Flag)

“TMSF” flag of CTRL2 register is automatically set by hardware every 0.682ms@6MHz or 1.144 ms@3.58MHz. When “TMSF” bit is set, it needs to be cleared by software, otherwise, its state will always remain high. Clearing “TMSF” bit does not reset the counter value.

Example: `BC CTRL2, 1 ; clear tmsf flag`

### 7.5.3 Green Mode Timer

Base on Green mode timer, the timer base clock is 62.5 ms. Different “Timer” register values will produce different clocks under Green mode as detailed below:

0	1	2	3	4	5	6	7
62.5ms	125ms	187.5ms	250ms	312.5ms	375ms	437.5ms	500ms
8	9	10	11	12	13	14	15
562.5ms	625ms	687.5ms	750ms	812.5ms	875ms	937.5ms	1s

To setup the Timer register, the value of CHSEL register must be #0111.

## 7.6 Interrupt Mode

A total of five interrupts are available. Each interrupt can be enabled or disabled and the interrupt status can be checked through their corresponding flags.

They occupy the same interrupt vector. You should check the interrupt flag to see which one invokes interrupt. For each interrupt, it can be enabled and disabled by user's program. To check which interrupt is executed, program should check the corresponding status flag.

Note that once two or more interrupt occur simultaneously, the higher priority interrupts (see table below) are executed first. While an interrupt is executing, other interrupts will hold and wait for it to end.

Priority	Interrupt	Set	Remarks
1	Speech	1	8 bit resolution with pre-load counter
2	High resolution timer	1	8 bit resolution with pre-load counter
3	Watch Dog Timer/ High resolution timer	1	8 bit resolution with pre-load counter (change timer status according to register setting)
4	Timer	1	4 bits pre-load counter
5	External Interrupt	1	Occurs when P1.3 pad has a rising edge change

## 8 Instruction Set

### 8.1 Introduction

The eSPN03 specifies the operation of instruction. The instruction symbols (abbreviations) used in this Series provide powerful instructions and a number of useful macros for speech playback. The instruction symbols and abbreviations used in the instruction set are as follows:

Symbol	Meaning
A	Acc., accumulator
M	RAM
Data*	4-bit constant
b	Specify bit location for bit manipulation instruction
Z	Zero flag
C	Carry flag
k	Binary 0 or 1
Label	Program label
REG	Register
N	Number

\* The immediate value (constant) operand specified by "data" must be prefixed with a "#" sign.

The numeric representation is listed in the following table. The characters are none case-sensitive.

Type	Number			
Decimal	0	1	8	15
Binary	0000B	0001B	1000B	1111B
Hexadecimal	0h	1h	8h	Fh

## 8.2 Instruction Summary

Each instruction cycle takes one system clock. Almost all of the instructions are single instruction cycle except for the following:

- Conditional jump operation: CAJE, CJBS, CJBC, etc. When a conditional jump operation occurs, it will take 3 instruction cycles.
- Bit set/clear operation: BS, BC. These operations take 2 instruction cycles.

### 8.2.1 Assembly Instruction Set

Instruction	Operation	Cycles	Flags Affected
SPA1 *.wav	Play *.wav voice file	2W2C <sup>1</sup>	
LJMP Label	Long jump (full program address space)	2W2C <sup>1</sup>	
JMP Label	Short jump (256 local location)	1W2C <sup>1</sup>	
MOV M, #data	Move data to M (M ← data)	1	
MOV M, A	Move Acc. To M (M ← A)	1	
MOV A, M	Move M to Acc. (A ← M)	1	Z
ADD A, M	Add Acc. With M (Acc. ← Acc. + M)	1	Z, C
	Add Acc. With M and Carry (Acc. ← Acc. + M + C)		
SUB A, M	Subtract M from Acc. (Acc. ← Acc. – M)	1	Z, C
	Subtract M and Carry from Acc. (Acc. ← Acc. – M – (~C))		
AND A, M	“AND” operation (Acc. ← Acc. & M)	1	Z
OR A, M	“OR” operation (Acc. ← Acc.   M)	1	Z
XOR A, M	“XOR” operation (Acc. ← Acc. ⊕ M)	1	Z
BS M, b <sup>2</sup>	Set bit b of M to “1”	1W2C <sup>1</sup>	
BC M, b <sup>2</sup>	Set bit b of M to “0”	1W2C <sup>1</sup>	
BS REG, b	Set bit b of REG to “1”	1W1C <sup>1</sup>	
BC REG, b	Set bit b of REG to “0”	1W1C <sup>1</sup>	
MOV A, REG	Move REG to Acc. (A ← REG)	1	Z
MOV REG, A	Move Acc. To REG (REG ← A)	1	
PAGEN (N = 0 ~ 1)	Set active RAM page	1	

(Continued)

Instruction	Operation	Cycles	Flags Affected
MOV A, #data	Move data to Acc. (A ← data)	1	Z
ADD A, #data	Add Acc. With data (Acc. ← Acc.+ data)	1	Z, C
SUB A, #data	Subtract data from Acc. (Acc. ← Acc. – data)	1	Z, C
AND A, #data	“AND” operation (Acc. ← Acc. & data)	1	Z
OR A, #data	“OR” operation (Acc. ← Acc.   data)	1	Z
XOR A, #data	“XOR” operation (Acc. ← Acc.⊕ data)	1	Z
RETN (N = 0 ~ 7) <sup>1</sup>	PC ← stack N	1W2C <sup>2</sup>	
NOP	No operation	1	
END	Enter power-down mode	1W2C <sup>2</sup>	
PCA	PC ← PC + {Carry, A}	1W2C <sup>2</sup>	
RLCA	Rotate Acc. Left 1 bit through carry {C, A} ← {A[3], A[2], A[1], A[0], C}	1	Z, C
RRCA	Rotate Acc. Right 1 bit through carry {C, A} ← {A[0], C, A[3], A[2], A[1]}	1	Z, C
READ	Read one nibble data from ROM to Acc.	4	Z
CallN Label(N = 0 ~ 7) <sup>1</sup>	Call Nth subroutine at label [stack N] ← PC + 1		
CAJE #data, Label	If A = data, then JMP to label		
CAJE M, Label	If A = M, then JMP to label		
CJBS M, b, Label <sup>3</sup>	If M(b) = 1, then JMP to label		
CJBS REG, b, Label	If REG(b) = 1, then JMP to label		
CJBC M, b, Label <sup>3</sup>	If M(b) = 0, then JMP to label		
CJBC REG, b, Label	If REG(b) = 0, then JMP to label		

**NOTE:** The symbols under “Instruction” column are as explained below:

#data = #0, #1, #2, ...#15

M = M0, M1, M2, ...M63

REG = R0, R1, R2, ...R31

b = 0, 1, 2, & 3

PAGEN = PAGE0, PAGE1

SPAN = SPA1

CallN = Call0, Call2, Call3, ...Call7

RETN = RET0, RET2, RET3, ...RET7

Label = assembly label

W = Words (12 bits)

C = Cycle

<sup>1</sup> The RET7 & Call7 are for ELAN internal speech routine use only. Therefore, do NOT use these parameters for playing voice.

Call1 ~ Call7 are applicable and used to store and return normal call subroutine address, while Call0 is used only to store and return Interrupt address.

<sup>2</sup> In the “Cycles” field, “W” means instruction word and “C” means execution cycle. For example, “1W2C” means this instruction is a 1 word instruction and takes 2 instruction cycles while executing.

<sup>3</sup> The instructions “BS M, b”, “BC M, b”, “CJBS M, b, Label”, & “CJBC M, b, Label” do NOT support RAM M32~M63. These instructions only support RAM M0~M31 of Pages 0~1.

Multiple cycle instructions include **SampleRate1**, **Play1**, and **Volume1**. These instructions can be set as speech frequency or play speech.

The multiple cycle instructions and speech macros used in the instruction set are listed in the following sections.

### 8.2.2 Multiple Cycle Instruction

Multiple Cycle Instruction	Operation
<b>Set Speech Frequency</b>	
SampleRate1 freq	Set sample rate to "freq" for speech
<b>Play Speech</b>	
Play1 file1	Play voice file in Channel 1
Play1 file, freq, volume	Play voice file in Channel 1 by specifying freq, Volume level 0 ~ 3
Volume1	Set Speech volume, Volume level 0 ~ 3

### 8.2.3 Speech Macro

Macro	Operation
<b>Speech Operation</b>	
S1Mute	Mute the speech play (toggle)
S1Pause	Pause the speech play (toggle)
S1Stop	Stop the speech play
S1Check pathname	Check speech play and jump to specific path

**NOTE**

*Using speech macro will result to PAGE register being set "0." Therefore, you need to need backup PAGE register before hand in order to avoid executing incorrect RAM page number.*

## 9 Operating Specifications

### 9.1 Absolute Maximum Ratings

Parameter	Specification		
Supply voltage	V <sub>ss</sub> -0.3V	to	V <sub>DD</sub> +0.3V
Input voltage	V <sub>ss</sub> -0.3V	to	V <sub>DD</sub> +0.3V
Operating Temperature	0°C	to	70°C
Storage Temperature	-55°C	to	125°C

## 9.2 DC Electrical Characteristics

VDD= 2.5 ~5.5V, Vss=0 V, Ta= 25°C unless otherwise specified

Items	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V <sub>DD</sub>	2.5	3.0	5.5	V	
Standby current	I <sub>DDs</sub>	-	-	4	uA	V <sub>DD</sub> =3V
Operating current	I <sub>DDg</sub>		10	15	uA	V <sub>DD</sub> =3V , Green mode (f=32KHz)
	I <sub>DDo</sub>	-	6	8.5	mA	V <sub>DD</sub> =3V, no load, playing stop, f=6MHz.
Drive current of P1, P2, P3	I <sub>OD</sub>	6	8	-	mA	V <sub>DD</sub> =3V, V <sub>O</sub> =2.4V
Sink current of P1, P2, P3	I <sub>OS</sub>	9	12	-	mA	V <sub>DD</sub> =3V, V <sub>O</sub> =0.4V
Input current of P1, P2, P3	I <sub>IH</sub>	-	3.0	5	uA	V <sub>DD</sub> =3V, V <sub>ip</sub> =V <sub>DD</sub> (with internal pull low)
Output current of Vo1A, Vo1B	I <sub>VO</sub>		180		mA	V <sub>DD</sub> =3V, V <sub>O</sub> =1/2 V <sub>DD</sub>
Frequency freq.	F <sub>High</sub>		6		MHz	V <sub>DD</sub> =3.0V
	F <sub>Low</sub>		32		KHz	V <sub>DD</sub> =3.0V

## 10 Frequency Deviation

### 10.1 Freq. vs. VDD Normal Mode

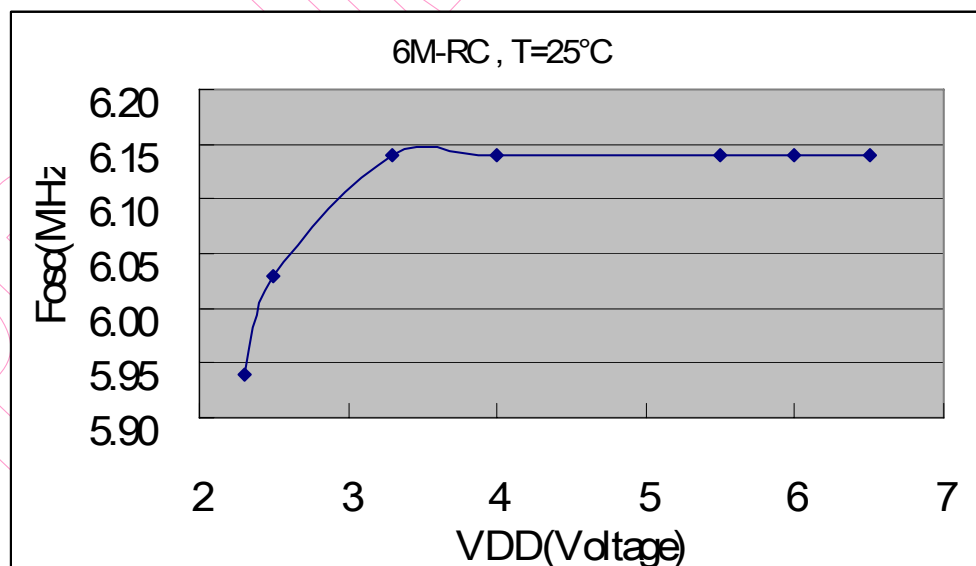


Figure 10-1 Freq. vs. VDD Normal Mode System Frequency Diagram

## 10.2 Freq. vs. VDD (Rosc=1MΩ) Green Mode

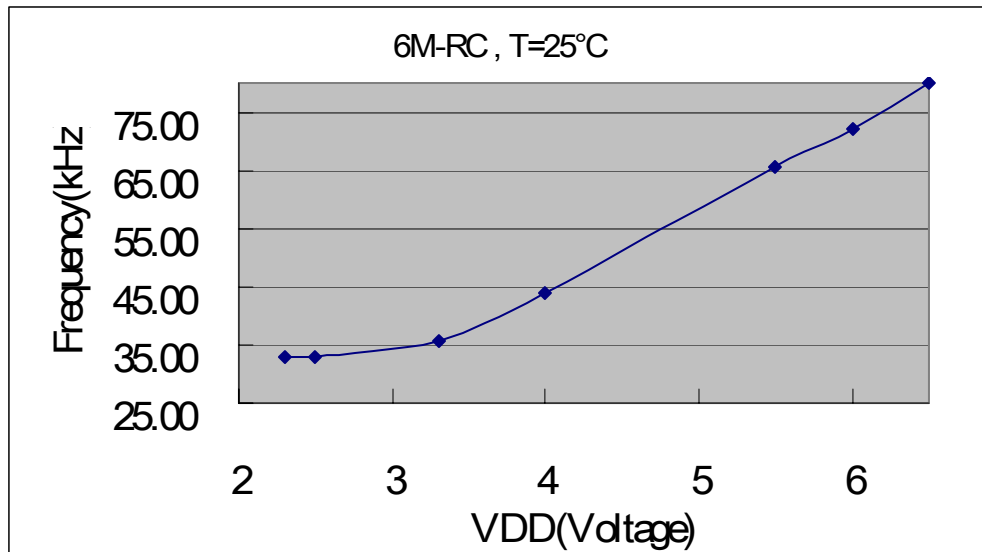


Figure 10-2 Freq. vs. VDD (Rosc=1MΩ) Green Mode System Frequency Diagram

## 11 Application Circuit Diagram

### 11.1 IRC Oscillator in Normal Mode

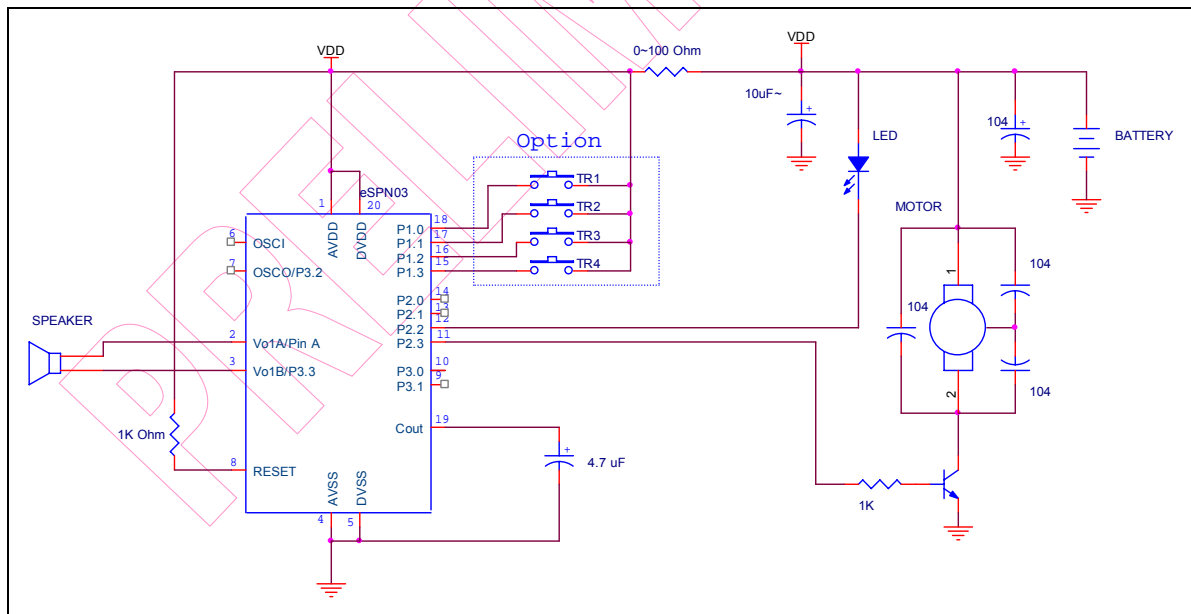


Figure 11-1 eSPN03 with IRC Oscillator (in Normal Mode) Application Circuit Showing Large Loading

## 11.2 XTAL Oscillator in Normal Mode

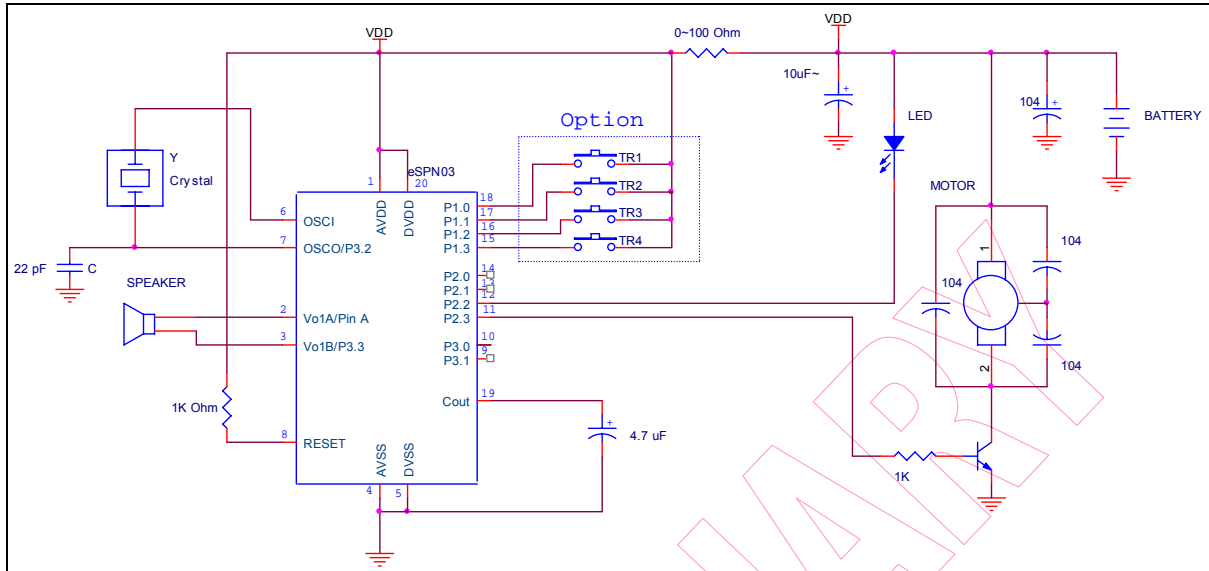


Figure 11-2 eSPN03 with XTAL Oscillator (in Normal Mode) Application Circuit Showing Large Loading

## 11.3 IRC Oscillator in Green Mode

Circuit in Green mode must connect a 1M $\Omega$  resistor to OSCO pin as illustrated below.

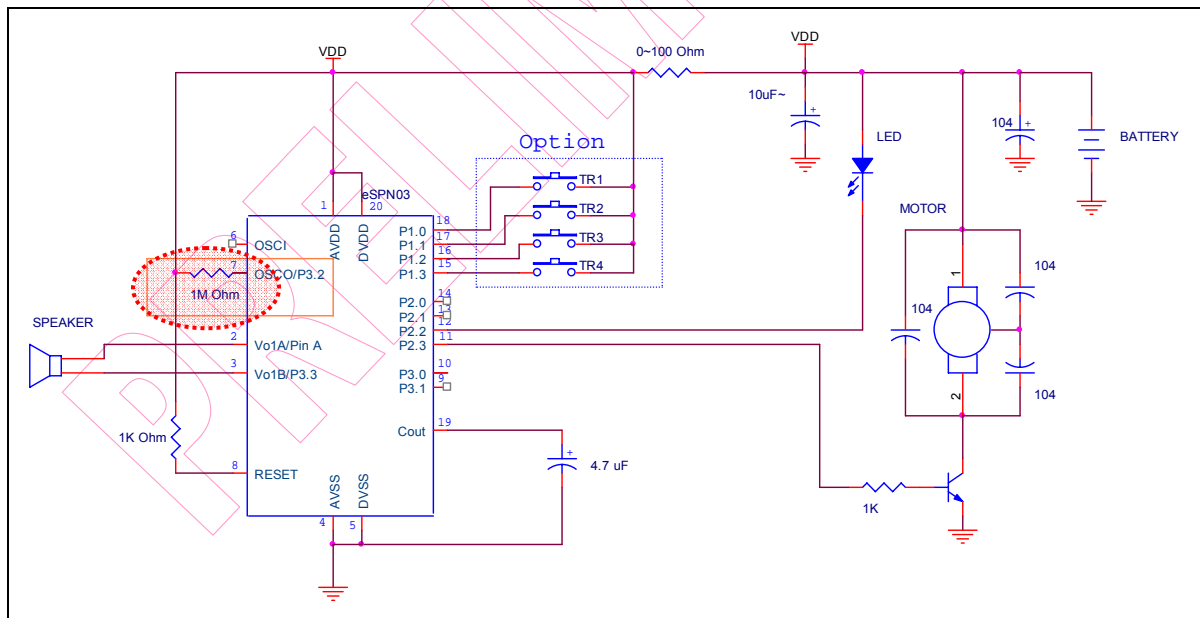


Figure 11-3 eSPN03 with IRC Oscillator (in Green Mode) Application Circuit

## 11.4 XTAL Oscillator in Green Mode

Circuit in Green mode must connect a 1MΩ resistor to OSCO pin as illustrated below.

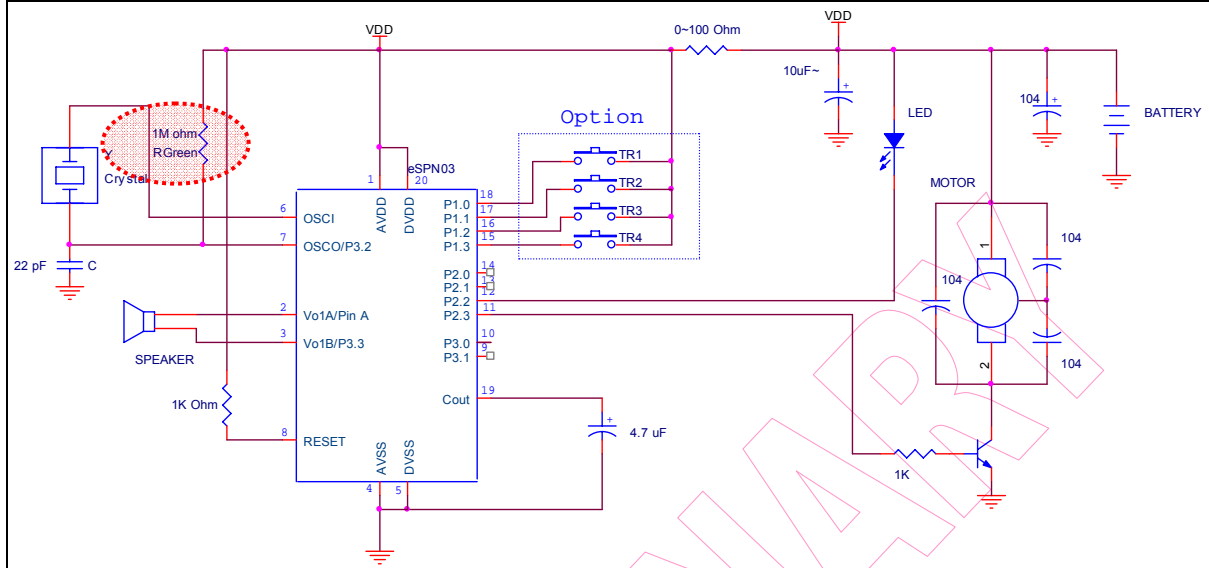


Figure 11-4 eSPN03 with XTAL Oscillator (in Green Mode) Application Circuit

- NOTES:**
1. To prevent noise from power supply, it is recommended to add a ceramic capacitor between VDD and ground with a capacitor value is 0.1μF. Furthermore, adding a 1K ohm ceramic resistor between VDD and RESET pin could further avert power supply interference.
  2. For heavy loading application, adding an electrolytic capacitor between VDD and ground is recommended. The recommended capacitor value for button cell application is 10μF.
  3. To keep power stability level, adding a ceramic capacitor between ground and Cout pin is recommended. The recommended capacitor value is 4.7μF.



PRELIMINARY