EM78P611G

Universal Serial Bus Series Microcontrollers

Product Specification

DOC. VERSION 1.3

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial release version	2010/09/21
1.1	Fixed 40 pin package pin assignment	2011/01/17
1.2	1.Updated standby current 2. Updated D-resister value	2011/05/17
1.3	1.Deleted EM78P611GAP package 2.Deleted P92 P93 PWM function 3.Deleted Port9 LED sink ability	2011/12/08

1 General Description

The EM78P611G is a series of One-Time Programmable (OTP) microcontrollers equipped with 8-bit Universal Serial Bus RISC architecture. It is specifically designed for USB low speed device applications and supports standard devices, such as PS/2 keyboards. It also supports one device address and three endpoints USB device communications. With no firmware involved, these microcontrollers can automatically identify and decode Standard USB Command to Endpoint Zero.

The microcontroller has 8-level stacks and 6 interrupt sources with 144 bytes of General Purpose SRAM and 6K words of OTP ROM. It runs with either an external ceramic resonator with a 6 or 12 MHz or internal high frequency oscillator (IRC) by setting Code Option 11.

2 Features

- Operating voltage**:** 4.0V ~ 5.5V
- All GPIO are 5V
- Low-cost solution for low-speed USB devices, such as keyboard, joystick, and Gamepad
- USB Specification Compliance
  - Universal Serial Bus Specification Version 1.1
  - USB Device Class Definition for Human Interface Device (HID), Firmware Specification Version 1.1
  - Supports one device address and three endpoints
- USB Application
  - P75 (D-) has an internal pull-high resistor (1.4 KΩ)
  - USB protocol handling
  - USB device state handling
  - Identifying and decoding of Standard USB commands to EndPoint Zero
- PS/2 Application Support
  - Built-in PS/2 port interface for keyboard and mouse
- Built-in 8-bit RISC MCU
  - 8-level stacks for subroutine nesting and interrupt
  - 8-bit real time clock/counter (TCC) with overflow interrupt
  - Six available interrupts
  - Built-in free running RC oscillator for Watchdog Timer and Dual Clock mode
  - Two independent programmable prescalers for WDT and TCC

- Two power saving methods:
  1. Power-down mode (Sleep mode)
  2. Dual Clock mode
- Two clocks per instruction cycle
- One-time programmable (OTP)

- I/O Ports
  - Up to 5 LED sink pins
  - Each GPIO pin of Ports 5, 6, 8, P90~P93, P95~97, has an internal programmable pull-high resistor (25KΩ)
  - Each GPIO pin of Port 6, P74 ~ P77 and Port 9 can wake up the MCU from sleep mode by input state change
- Internal Memory
  - Built-in 6K×13 bits Program ROM
  - Built-in 144 bytes general purpose registers (SRAM)
  - Built-in USB Application FIFOs
- Operation Frequency
  - Normal Mode: MCU runs either with an external ceramic resonator of 6 or 12 MHz or internal high frequency oscillator (IRC)
  - Dual Clock Mode: MCU runs at a frequency of 256kHz (or 32kHz, 4kHz, 500Hz), emitted by the internal oscillator with the external ceramic resonator turned off to save power.
- Built-in 3.3V Voltage Regulator
  - Pull-up source for the external USB resistor on D-pin
- Package Types:
  - 44-pin QFP (10×10mm, footprint = 3.2 mm) EM78P611GAQ

3 Application

- USB Keyboard only
- USB and PS/2 both compatible with Keyboard
- USB Keyboard with USB Mouse
- USB Joystick

4 Pin Assignment

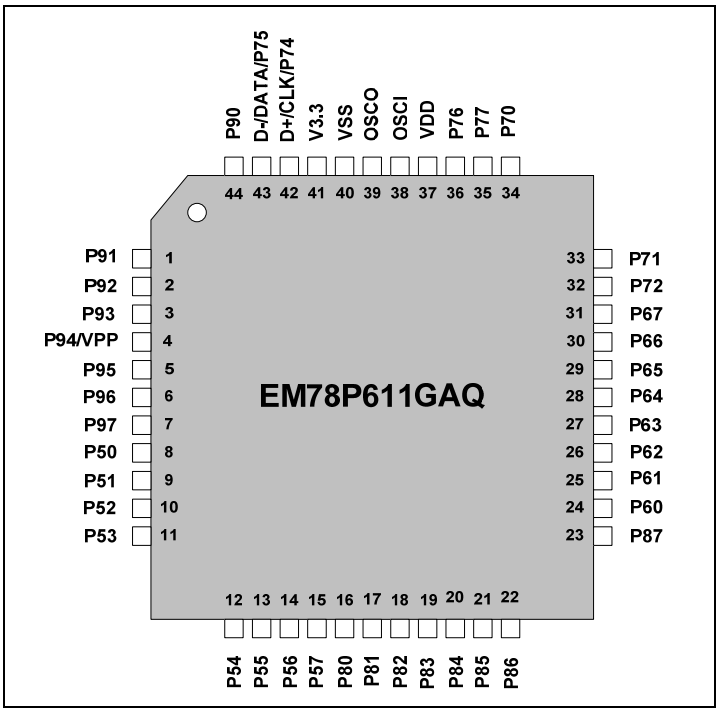


Figure 4-1 EM78P611GAQ (44-Pin QFP)

5 Pin Description

Symbol	I/O	Function
P50 ~ P57	I/O	General 8-bit bidirectional input/output port. All pins on this port can be internally pulled-high by software control.
P60 ~ P67	I/O	General 8-bit bidirectional input/output port. All pins on this port can be internally pulled-high by software control.
P70 ~ P72 P76 ~ P77	I/O	LED sink pins P76 ~ P77 will have an internally pulled-high resistor when the EM78P611G is running in PS/2 mode.
P80 ~ P87	I/O	General 8-bit bidirectional input/output port. All pins on this port can be internally pulled-high by software control.
P90 ~ P93 P95 ~ P97	I/O	General 7-bit bidirectional input/output port. All pins on this port can be internally pulled-high by software control.
P94 / Vpp	I	Input only. OTP program pin.
D+/CLK/P74	I/O	USB plus data line interface or CLK for PS/2 keyboard When the EM78P611G is running in PS/2 mode, this pin will have an internally pulled-high resistor (2.2KΩ), with VDD=5.0V.
D-/DATA/P75	I/O	USB minus data line interface or DATA for PS/2 keyboard When the EM78P611G is running in PS/2 mode, this pin will have an internally pulled-high resistor (2.2KΩ), with VDD=5V. When the EM78P611G is running in USB mode, this pin will have an internally pulled-high resistor (1.4KΩ), with V33=3.3V.
OSCI	I	6 MHz / 12 MHz ceramic resonator input.
OSCO	O	Return path for 6 MHz / 12 MHz ceramic resonator.
V3.3	PWR	3.3V regulator output, This pin has to be tied to a 4.7 µF capacitor.
VDD	PWR	Power supply pin
VSS	GND	Ground pin

NOTE

*Do not confuse interrupt function of EM78P611G with that of **EM78M611, EM78M611E, EM78611, & EM78611E**.*

- ***EM78M611, EM78M611E, & EM78611:** Ports 5, 6, 8, 9 are 3.3V I/O*
- ***EM78P611G, EM78611E:** Ports 5, 6, 8, 9 are 5V I/O*

6 Block Diagram

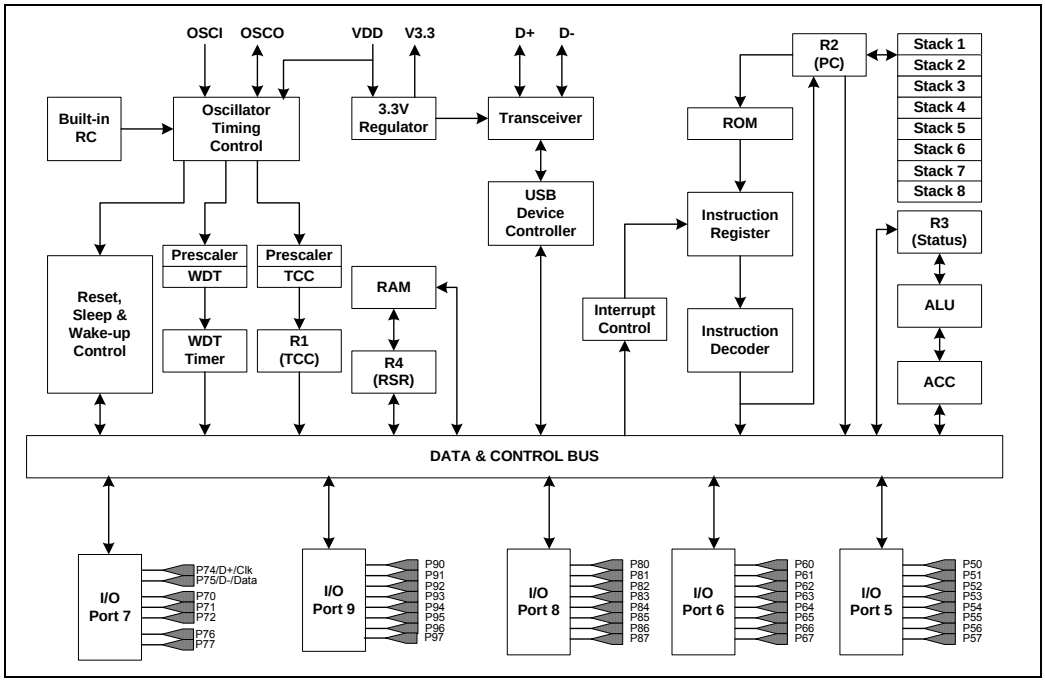


Figure 6-1 EM78P611G Functional Block Diagram

7 Function Description

The EM78P611G memory is organized into three spaces, namely; User Program memory in 6K×13 bits ROM space, Data Memory in 144 bytes SRAM space, and USB Application FIFO's for EndPoint0, EndPoint1, and EndPoint2.

7.1 Program Memory

The program space of the EM78P611G is 6K words, and is divided into six pages. Each page is 1K words long. After a reset, the 13-bit Program Counter (PC) points to location zero of the program space.

The Interrupt Vector is at 0x0001 and accommodates the TCC interrupt, P74~P77 state changed interrupt, EndPoint0 interrupt, USB Suspend interrupt, USB Reset interrupt, and USB Host Resume interrupt.

When an interrupt occurs, the MCU will auto save to the status register (R3 Bits 5~7), RAM Select Register (R4), and the Accumulator (A), then clears PS0~PS2 and fetch the next instruction from the corresponding address as illustrated in the following diagram.

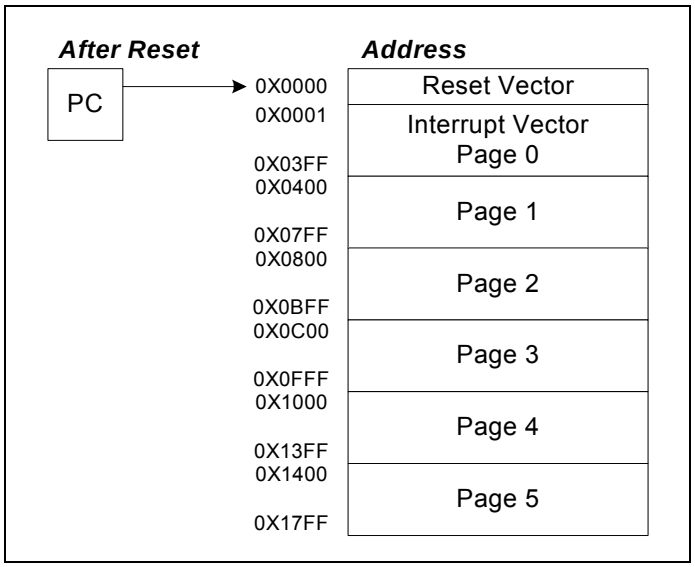


Figure 7-1 Fetching the Next Instruction when Interrupt Occurs

When executing “RETI” instruction, the MCU will pop A, R3 (Bits 5~7), R4, and stack, and then enables an interrupt.

7.2 Data Memory

The Data Memory has 144 bytes SRAM space. It has also an on-chip USB Application FIFO space for USB Application. Figure 7-2 below shows the organization of the Data Memory Space.

7.2.1 Special Purpose Register

When the microcontroller executes instructions, specific registers are implemented to ensure proper operation of essential functions, such as Status Register which records the calculation status, Port I/O Control Registers which control the I/O pins’ direction, etc. Lots of other special purpose registers are provided for various functions.

Note that Special Control Registers can only be read or written to by two instructions; IOR and IOW.

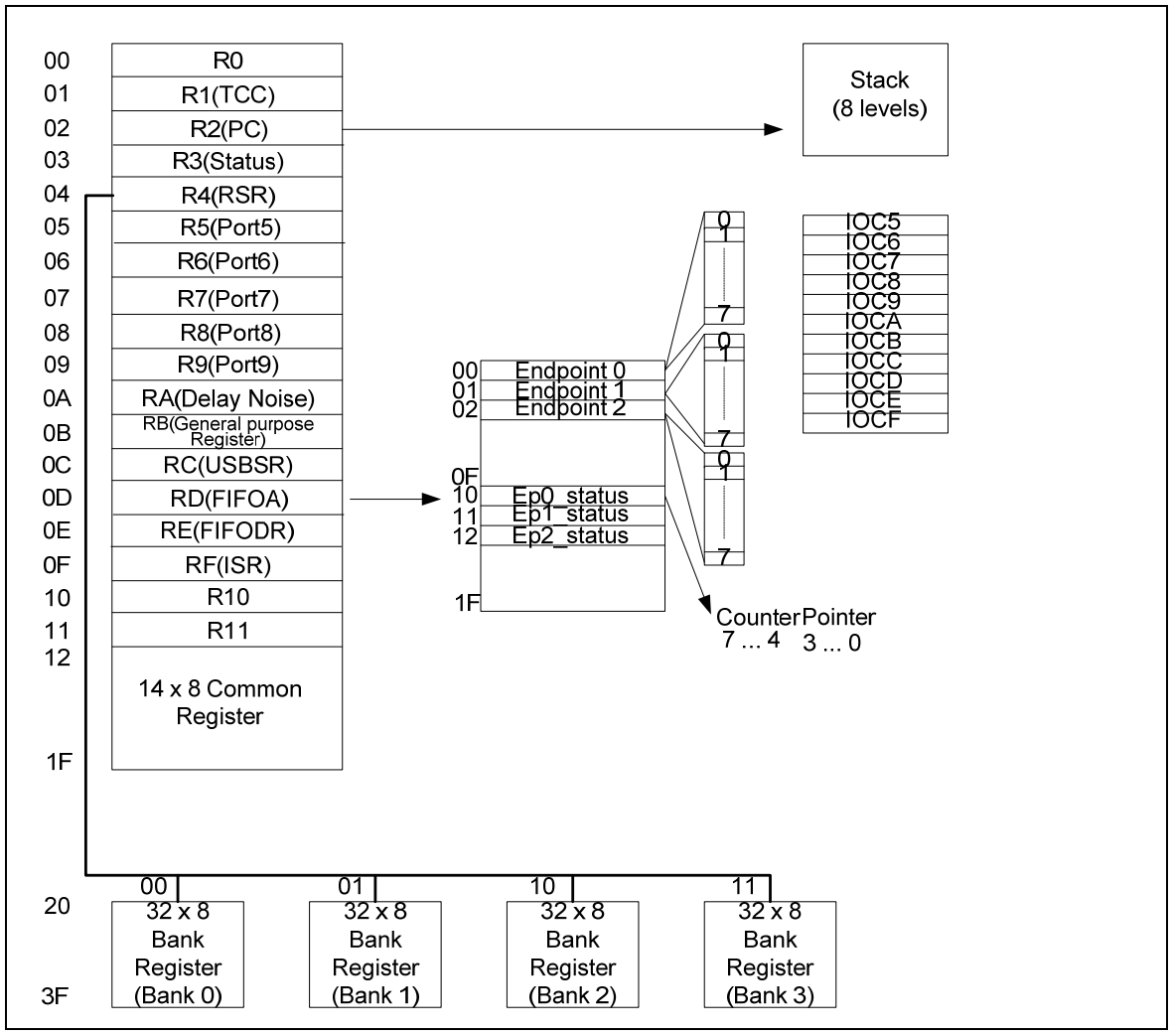


Figure 7-2 EM78P611G Data RAM Organization

7.2.2 Operational Registers

The following subsections describe each of the Operational Registers of the Special Purpose Registers. The Operational Registers are arranged according to the order of the registers' address. Note that some registers are read only, while others are both readable and writable.

7.2.2.1 R0 (Indirect Addressing Register) *Default Value: (0B_0000_0000)*

R0 is not a physically implemented register. Its major function is to serve as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses the data pointed to by the RAM Select Register (R4).

7.2.2.2 R1 (Timer/Clock Counter) *Default Value: (0B_0000_0000)*

The TCC register is an 8-bit timer or counter. It is readable and writable as any other registers. The Timer module is incremented after execution of every instruction cycles. You can work around this by writing an adjusted value. Timer interrupt is generated when the R1 register overflows from FFh to 00h. This overflow sets bit TCIF (RF[0]). The interrupt can be masked by clearing bit TCIE (IOCF[0]). After Power-on reset and Watchdog reset, the initial value of this register is 0x00.

7.2.2.3 R2 (Program Counter and Stack) *Default Value: (0B_0000_0000)*

The EM78P611G Program Counter is a 13-bit register that allows accessing of the 6k words of the Program Memory with 8-level stacks. The eight LSB bits, A0~A7, are located at R2, while the three MSB bits, A12~A10, are located at R3. The Program Counter is cleared after Power-on reset or Watchdog reset. The first instruction that is executed after a reset is located at Address 00h.

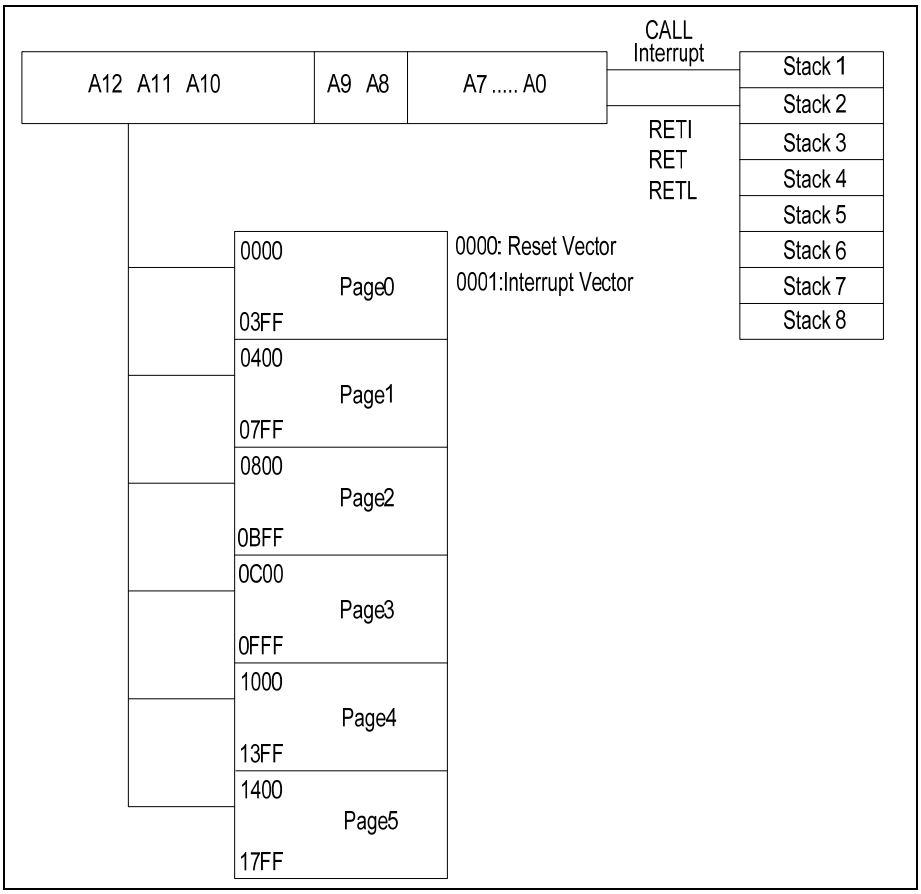


Figure 7-3 EM78P611G Program Counter and Stack

7.2.2.4 R3 (Status Register) *Default Value: (0B_0001_1XXX)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS2	PS1	PS0	T	P	Z	DC	C

R3 [0] Carry / Borrow Flag

0: No carry-out from the result of Most Significant bit

1: A carry-out occurs from the result of Most Significant bit

NOTE

For Borrow, the polarity is reversed. For rotate (RRC, RLC) instructions, this bit is loaded with either high or low-order bit of the source register.

R3 [1] Auxiliary Carry / Borrow Flag (for ADD, SUB Instructions)

0: No carry-out from the result of 4th low-order bit

1: A carry-out occurs from the result of 4th low-order bit of the

NOTE

For Borrow, the polarity is reversed.

R3 [2] Zero Flag. It will be set to "**1**" when the result of an arithmetic or logic operation is zero.

R3 [3] Power-Down Flag. It will be set to "**1**" during Power-on phase or by "WDTC" command and is cleared when the MCU enters into Power down mode. It will remain in its previous state after a Watchdog Reset.

0: Power down

1: Power-on

R3 [4] Time-out flag. It will be set to "**1**" during Power-on phase or by "WDTC" command. It is reset to "**0**" by WDT time-out.

0: Watchdog timer overflow occurs

1: No Watchdog timer overflow

The various states of Power down flag and Time-out flag at different conditions are shown below:

T	P	Condition
1	**1**	Power-on reset
1	**1**	WDTC instruction
0	**P***	WDT time-out
1	**0**	Power down mode
1	**0**	Wake up caused by port change during Power down mode

* **P:** *Previous status before WDT reset*

R3 [5 ~ 7] Page Select Bits

These three bits are used to select the program memory page.

PS2	PS1	PS0	Program Memory Page [Address]
0	0	0	Page 0 [0000-03FF]
0	0	1	Page 1 [0400-07FF]
0	1	0	Page 2 [0800-0BFF]
0	1	1	Page 3 [0C00-0FFF]
1	0	0	Page 4 [1000-13FF]
1	0	1	Page 5 [1400-17FF]

7.2.2.5 R4 (RAM Select Register) *Default Value: (0B_00XX_XXXX)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BK1	BK0	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0

R4 (RAM select register) contains the address of the registers.

R4 [0 ~ 5]: Used to select registers in 0x00h~0x3Fh. The Address 0x00~0x1F is common space. After 0x1Fh, SRAM is divided into four banks, using Bank Select Register.

R4 [6, 7]: Used to select the registers bank (refer to the table below). The following are two examples**:**

1) R4=00001100 and R4=10001100 point to the same Register 0x0Ch. Since 0x0Ch is in the common space, Bit 6 and Bit 7 are meaningless.
2) R4=10111100 points to the Register 0x3C in Bank 2.

R4[7]Bk1	R4[6]Bk0	RAM Bank #
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

7.2.2.6 R5 (Port 5 I/O Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	P53	P52	P51	P50

7.2.2.7 R6 (Port 6 I/O Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

7.2.2.8 R7 (Port 7 I/O Register) *Default Value: (0B_0000_X000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	D- / P75 / DATA	D+ / P74 / CLK	–	P72	P71	P70

7.2.2.9 R8 (Port 8 I/O Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80

7.2.2.10 R9 (Port 9 I/O Register) *Default Value: (0B_000X_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	--	P93	P92	P91	P90

7.2.2.11 RA (Reserved) *Default Value: (0B_0000 0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	Delay noise	-	-	-	-

RA[0 ~ 3; 5 ~ 7]: Reserved

RA [4]: Delay noise. Set by Hardware and cleared by software.

0: VDD noise drops from 5V, but above 3V

1: VDD noise drops from 5V to below 3V

NOTE

When the MCU resets (including power-on and Watchdog resets), the RA[4] is reset to "0".

7.2.2.12 RC (USB Application Status Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP0_W	EP0_R	EP1_R	EP2_R	EP2_W	Host_Suspend	EP0_Busy	Stall

RC [0]: Stall flag. When the MCU receives an unsupported command or invalid parameters from the host, this bit is set to "**1**" by firmware to notify the to return a STALL handshake. When a successful Setup transaction is received, this bit is automatically cleared. This bit is readable and writable.

RC [1]: EP0_Busy flag. When this bit is equal to "**1**," it indicates that the Universal Device Controller (UDC) is writing data into the EP0'FIFO or reading data from it. During this time, the firmware will avoid accessing the FIFO until UDC finishes writing or reading. This bit is read only.

RC [2]: Host Suspend flag. If this bit is equal to "**1**", it indicates that the USB bus has no traffic for a specified period of 3.0 ms. This bit is cleared automatically when there is bus activity. This bit is read only.

RC [3]: EP2_W flag. This bit is set when the UDC receives a successful data from USB Host to EP2. When this bit is equal to "**1**", the firmware will execute a read sequence to the EP2's FIFO, after which this bit is cleared. Otherwise, the subsequent data from the USB Host will not be accepted by the UDC.

RC [4,5,6]: EP0_R / EP1_R / EP2_R flag. These three bits inform the UDC to read the data from the FIFO and automatically send the data to the Host. After the UDC finishes reading the data, this bit is cleared automatically. Therefore, before writing data into FIFO, the firmware will first check this bit to avoid overwriting the data. These three bits can only be set by firmware and cleared by hardware.

RC [7]: EP0_W flag. After the UDC completes writing data to the FIFO, this bit is set automatically. The firmware will clear it as soon as it gets the data from EP0's FIFO. Only when this bit is cleared that the UDC will be able to write a new data into the FIFO. Therefore, before the firmware can write data into the FIFO, this bit must be set first by the firmware to prevent the UDC from writing data at the same time. This bit is both readable and writable.

7.2.2.13 RD (USB Application FIFO Address Register)

Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	UAD4	UAD3	UAD2	UAD1	UAD0

RD [0~4]: USB Application FIFO Address Registers. These five bits are the address pointers of the USB Application FIFO.

RD [5~7]: Undefined registers. The default value is zero.

7.2.2.14 RE (USB Application FIFO Data Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UD7	UD6	UD5	UD4	UD3	UD2	UD1	UD0

RE [0~7]: USB Application FIFO Data Register contains the register data which address is pointed to by RD.

NOTE

For example, if you want to read the fourth byte of EndPoint Zero, you have to use the address of EP0 (0x00) and Data Byte Pointer of EP0 (0x10) to access it.

```
// Read the 4th byte of the EP0 FIFO
// First, assign the data byte pointer of EP0 register (0X10) with 0X03.
  MOV  A, @0X10
  MOV  RD, a       // Move data in A to RD register
  MOV  A, @0X03
  MOV  RE , A      // Move data in A to RE register

// Then read the content from EP0 FIFO (0x00) 4th byte
  MOV  A, @0X00
  MOV  RD, A       // Assign address point to EP0 FIFO
  MOV  A, RE       // Read the fourth byte data (Byte 3) of the EP0
                      FIFO
  MOV  A, 0X0E     // Read the fifth byte data (Byte 4) of the EP0
                      FIFO
```

7.2.2.15 RF (Interrupt Status Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
USB Host Resume_IF	–	–	Port7 state change_IF	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF

RF [0]: TCC Overflow interrupt flag. This bit is set while TCC overflows, and is cleared by firmware.

RF [1]: EndPoint Zero interrupt flag. This is set when the EM78P611G receives a user command to EndPoint Zero and is cleared by firmware.

RF [2]: USB Suspend interrupt flag. This bit is set when the EM78P611G finds the USB Suspend Signal on the USB bus and is cleared by the firmware.

RF [3]: USB Reset interrupt flag. This bit is set when the host issues the USB Reset signal.

RF [4]: P74/P75 (PS2 only) /P76/P77 (USB & PS2) Port state change interrupt flag. This bit sets the voltage level change interrupt flag.

In PS2 Mode, Pins P74, P75, P76, & P77 support the voltage level change interrupt function. Under USB mode, only P76 & P77 support the function.

NOTE

*Do not confuse interrupt function of EM78P611G with that of **EM78M611, EM78M611E, EM78611, & EM78611E**.*

- ***EM78M611 & EM78611:***
  *USB Mode – P74/P75/P76/P77 does **NOT** support interrupt function*
  PS2 Mode – P74/P75/P76/P77 support interrupt function
- ***EM78P611G, EM78M611E, & EM78611E:***
  *USB Mode – P76 and P77 support interrupt function (P74 & P75 **NOT** supported)*
  PS2 Mode – P74/P75/P76/P77 support interrupt function

RF [5, 6]: Reserved

RF [7]: USB Host Resume interrupt flag. This will be set only in Dual Clock mode when the USB suspend signal becomes low.

NOTE

*Do not confuse USB Host Resume_IF function of EM78P611G with that of **EM78M611, EM78M611E, EM78611, & EM78611E**.*

- ***EM78M611 & EM78611:** This bit is always '**1**'. **NOT** accessible for use.*
- ***EM78P611G, EM78M611E, & EM78611E:** This bit is **O.K**. to use.*

7.2.3 Control Registers

Some special purpose registers are available for special control purposes. Except for the Accumulator (ACC), these registers must be read and written with special instructions. One of these registers, CONT, can only be read by the instruction "CONTR" and written by "CONTW" instruction. The other special control registers can be read by the instruction "IOR" and written by the instruction "IOW".

The following sections describe only the general functions of the control registers.

7.2.3.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding, usually involves the temporary storage function of the Accumulator. The Accumulator is an 8-bit register that holds operands and results of arithmetic calculations. It is not addressable. After an interrupt occurs, the Accumulator is auto-saved by hardware.

7.2.3.2 CONT (Control Register) *Default Value: (0B_0011_1111)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LED	/INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0

Except for Bit 6 (Interrupt enable control bit), the CONT register can be read by the instruction "CONTR" and written by the instruction “CONTW".

CONT [0 ~ 2]: Watchdog Timer prescaler bits. These three bits are used as the Watchdog Timer prescaler.

CONT [3 ~ 5]: TCC Timer prescaler bits

The relationship between the prescaler value and these bits are as follows**:**

PSR2/TSR2	PSR1/TSR1	PSR0/TSR0	TCC Rate	WDT Rate
0	**0**	**0**	1: 2	1: 1
0	**0**	**1**	1: 4	1: 2
0	**1**	**0**	1: 8	1: 4
0	**1**	**1**	1: 16	1: 8
1	**0**	**0**	1: 32	1: 16
1	**0**	**1**	1: 64	1: 32
1	**1**	**0**	1: 128	1: 64
1	**1**	**1**	1: 256	1: 128

NOTE

WDT Timing base is 8ms.

Example: Prescaler = 1:128

WDT Overflow Time is: 8 ms $\times 2^{7}$ *= 1024 ms*

CONT [6]: Interrupt enable control bit. This bit toggles the Interrupt function between enable and disable. It is set to "**1**" by the interrupt disable instruction "DISI" and reset by the interrupt enable instructions "ENI" or "RETI."

0: Enable the Interrupt function

1: Disable the Interrupt function

CONT [7]: LED bit. This bit is used to enable the LED sink capacity of P76 and P77.

0: Disable the LED sink capacity of P76, P77

1: Enable the LED sink capacity of P76, P77

7.2.3.3 IOC5 ~IOC9 I/O (Port Direction Control Registers)

Default Value: (0B_1111_1111)

These are I/O port (Port 5 ~ Port 7) direction control registers. Each bit controls the I/O direction of three I/O ports respectively. When these bits are set to "**1**", the relative I/O pins become input pins. Similarly, the I/O pins becomes outputs when the relative control bits are cleared.

0: Output direction

1: Input direction

7.2.3.4 IOCA (Operation Mode Control Register) *Default Value: (0B_1110_0011)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Dual_Frq.1	Dual_Frq.0	/P76,/P77 Pull high	Remote_ Wake up	--	--	PS/2	USB

IOCA [0, 1]: Two bits are used to select the operation mode.

IOCA[1]	IOCA[0]	Operation Mode
0	0	Detect Mode
0	1	USB Mode
1	0	PS/2 Mode
1	1	USB Test Mode

IOCA[2] [3]: Reserved

IOCA[4]: Indicate whether the device is required to support Remote Wake-up or not. The Remote Wake-up field can be modified by SetFeature () and ClearFeature () requests.

0: Do Not support remote wake-up

1: Supports remote wake-up

NOTE

*Do not confuse Remote_Wake-up function of EM78P611G with that of **EM78M611, EM78M611E, EM78611, & EM78611E***

- ***EM78M611 & EM78611:** Do **NOT** support Remote_Wake-up function.*
- ***EM78P611G, EM78M611E, & EM78611E:** Support Remote_Wake-up function.*

IOCA[5]: Pull-high resistor of P76 and P77. Supports USB mode only

0: Pull-high is enabled

1: Pull-high is disabled

NOTE

*Do not confuse P77/P77 Pull-high resistor function of EM78P611G with that of **EM78M611, EM78M611E, EM78611, & EM78611E***

- ***EM78M611 & EM78611:** Do **NOT** support P77/P77 Pull-high resistor function.*
- ***EM78P611G, EM78M611E, & EM78611E:** Support this function but in USB mode only.*

IOCA [6, 7]: Select the operation frequency in Dual Clock Mode. Four frequencies are available for selection in running the MCU program in Dual Clock Mode.

Dual_Frq.1	Dual_Frq.0	Frequency
0	**0**	500Hz
0	**1**	4kHz
1	**0**	32kHz
1	**1**	256kHz

7.2.3.5 IOCB (Port 9 Wake-up Pin Select Register) *Default Value: (0B_X111_1111)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/P97	/P96	/P95	/P94	/P93	/P92	/P91	/P90

IOCB [0 ~ 7]: These bits are used to select which of the Port 9 pins is to be assigned to wake-up the MCU during Power-down mode.

0: Enable the function

1: Disable the function

7.2.3.6 IOCC (Reserved) *Default Value: (0B_000X_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	–

IOCC [0~7]: Reserved

7.2.3.7 IOCD (Port 9 Pull-high Control Register) *Default Value: (0B_111X_1111)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH97	/PH96	/PH95	–	/PH93	/PH92	/PH91	/PH90

IOCD [0 ~ 3, 5 ~ 7]: These bits control the 25KΩ pull-high resistor of the individual pins in Port 9.

0: Enable pull-high

1: Disable pull-high

IOCD [4]: Reserved

7.2.3.8 IOCE (Special Function Control Register) *Default Value: (0B_1101_0111)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/Dual Clock	/WUE	WTE	RUN	Device_Resume	/PU8	/PU6	/PU5

IOCE [0, 1, 2]: Port 5, Port 6, and Port 8 pull-high control bits

0: Enable

1: Disable

IOCE [3]: Setting this bit will allow the UDC to execute resume signaling. This bit is set by firmware to generate a signal to wake-up the USB host and is cleared as soon as the USB Suspend signal is low. It can only be used in Dual Clock mode when the USB suspend signal is low.

NOTE

*Do not confuse Device_Resume function of EM78P611G with that of **EM78M611, EM78M611E, EM78611, & EM78611E.***

- ***EM78M611 & EM78611:** Do **NOT** support this function.*
- ***EM78P611G, EM78M611E, & EM78611E:** Support this Device_Resume function.*

IOCE [4]: Run bit. This bit can be cleared by firmware and set during power-on, or by the hardware at a falling edge of the wake-up signal. When this bit is cleared, the clock system is disabled and the MCU enters into Power-down mode. At the transition of wake-up signal from high to low, this bit is set to enable the clock system.

0: Sleep mode. The EM78P611G is in power-down mode.

1: Run mode. The EM78P611G is in normal working mode.

IOCE [5]: Watchdog Timer enable bit. The bit disables/enables the Watchdog Timer.

0: Disable WDT

1: Enable WDT

IOCE [6]: Enable the wake-up function as triggered by a port-changed. This bit is set by UDC.

0: Enable the wake-up function

1: Disable the wake-up function

IOCE [7]: Dual Clock Control bit. This bit is used to select the frequency of the system clock. When this bit is cleared, the MCU will run in very low frequency for power saving and the UDC will stop working.

0: Select to run in low frequency

1: Select to run in normal frequency.

7.2.3.9 IOCF (Interrupt Mask Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
USB Host Resume_IE	–	–	Port7 state change_1E	USB Reset_IE	USB Suspend_IE	EP0_IE	TCC_IE

IOCF [0~4, 7]: These six bits control the TCC interrupt function, EP0 interrupt, USB Suspend interrupt, USB Reset interrupt, Port 7 State Change interrupt and USB Host Resume interrupt respectively. Individual interrupt is enabled by setting its associated control bit in the IOCF to "**1**."

0: Disable Interrupt

1: Enable Interrupt

Only when the global interrupt is enabled by the ENI instruction will the individual interrupt works. After DISI instruction, any interrupt will not work even if the respective control bits of IOCF are set to "**1**."

The USB Host Resume Interrupt works only in Dual Clock mode. This is because when the MCU is in Sleep mode, it is automatically awaken by the UDC Resume signal.

7.3 USB Application FIFOs

For USB Application, the EM78P611G provides an 8-byte First-In-First-Out (FIFO) buffer for each endpoint. The buffer cannot be accessed directly. However, a corresponding Data Byte Pointer register for each endpoint is made available to address the individual byte of the FIFO buffer. The content of the individual byte will be mapped to a special register (see the following figure).

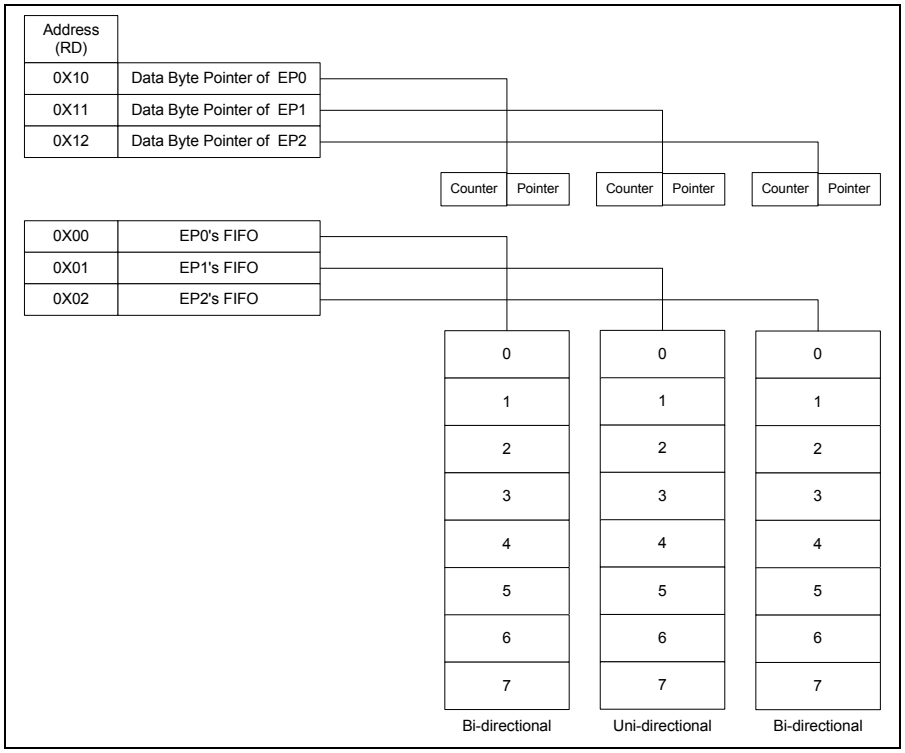


Figure 7-4 EM78P611G USB Application FIFO

7.3.1 USB Application

EM78P611G is designed specially for USB device application and has many powerful functions that support the firmware to free itself from complex situation in various aspects of USB applications.

7.3.2 USB Device Controller

The EM78P611G has a built-in USB Device Controller (UDC) that can interpret the USB standard commands and responds automatically without involving firmware. The embedded Series Interface Engine (SIE) handles the serialization and de-serialization of actual USB transmission. Thus, a developer can concentrate his efforts more in perfecting the device actual functions and spend less effort in dealing with USB internal operations.

The UDC handles and decodes most Standard USB commands defined in the USB Specification Rev 1.1. If the UDC receives an unsupported command, it will set a flag to notify the MCU of the receipt of such command. The standard commands that the EM78P611G supports includes; **Clear Feature, Get Configuration, Get Interface, Get Status, Set Address, Set Configuration, Set Feature, and Set Interface**. Each time the UDC receives a USB command, it writes the command into the EP0's FIFO. Only when it receives unsupported command will the UDC notify the MCU through an interrupt. Hence, the EM78P611G is very flexible under USB application since the developer can freely choose the appropriate decoding method of the USB command as called for by various conditions.

7.3.3 Device Address and Endpoints

EM78P611G supports one device address and three endpoints; EP0 for control endpoint, and EP1 & EP2 for interrupt endpoint. Sending data to USB host with EM78P611G is very easy. Just write data into the EP's FIFO, then set the flag, and the UDC will handle the rest. UDC will then confirm that the USB host has received the correct data from the EM78P611G.

7.4 Reset

The EM78P611G provides three types of reset**:** (1) Power-on Reset, (2) Watchdog Reset, and (3) USB Reset.

7.4.1 Power-on Reset

Power-on Reset occurs when the device is attached to power and a reset signal is initiated. The signal will last until the MCU becomes stable. After a Power-on Reset, the MCU enters into the following predetermined states, and then; it is ready to execute the program.

a. The program counter is cleared.
b. The TCC timer and Watchdog timer are cleared.
c. Special registers and Special Control registers are all set to their initial values.

7.4.2 Watchdog Reset

When the Watchdog Timer (WDT) overflows, it causes the WDT to reset. The program is then executed from start and some registers are reset. The UDC however, remains unaffected.

7.4.3 USB Reset

When the UDC detects a USB Reset signal on the USB bus, an MCU interrupt occurs, after which it proceeds to perform the next specified process. After a USB device is attached to the USB port, it cannot respond to any bus communication until it receives a USB Reset signal from the bus.

7.5 Power Saving Mode

The EM78P611G provides two options of power-saving modes for energy conservation, i.e., Power Down mode and Dual Clock mode.

7.5.1 Power Down Mode

The EM78P611G enters into Power Down mode by clearing the RUN register (IOCE[4]). During this mode, the oscillator is turned off and the MCU goes to sleep. It will wake-up when signal from USB host is resumed, or when a Watchdog Timer reset occurs, or when an input port state changes.

If the MCU wakes up when the I/O port status changes, the direction of the I/O port should be set at input direction, and then read the port status.

■ **Example:**

```
:
// Set Port 6 to input port
MOV      A, @0xFF
IOW       PORT6
// Read the state of Port 6
MOV      PORT6, PORT6
// Clear the RUN bit
IOR       0xE
AND      A, 0B11101111
IOW      0xE
:
:
```

7.5.2 Dual Clock Mode

The EM78P611G has one internal oscillator for power saving application. The clearing Bit IOCE [7] will enable the low frequency oscillator (see Section 7.2.3.8). At the same time, the external oscillator is turned off. Then, the MCU will run under very low frequency to conserve power. Four types of frequency are available for setting Bits IOCA [6, 7] (see Section 7.2.3.4).

The USB Host Resume Interrupt can only be used in this mode. If this interrupt is enabled, the MCU will be interrupted when the USB Host Resume signal is detected on the USB Bus.

7.6 Interrupt

The EM78P611G has one Interrupt Vector in 0x0001. When an interrupt occurs during an MCU program run, it will jump to the Interrupt Vector (0x0001) and execute the instructions sequentially from the interrupt vector. RF is the interrupt status register, which records the interrupt status in the relative flags/bits (see Section 7.2.2.15).

The interrupt condition could be one of the following**:**

■ **TCC Overflow:** When the Timer Clock / Counter Register (R1) overflows, the status flag RF[0] is set to "**1.**" Its Interrupt Vector is 0X0001.

■ **Port 7 State Change:** When the input signals in Port 7 changes, the status flag RF[4] is set to "**1.**". Its Interrupt Vector is 0X0001.

■ **EP0 interrupt:** When the UDC successfully accepts a setup transaction from host to EndPoint0, the status flag RF[1] is set to "**1.**" Its Interrupt Vector is 0X0001.

- **USB suspend:** When the UDC detects a USB Suspend signal on the USB bus, the status flag RF[2] is set to "**1.**" Its Interrupt Vector is 0X0001.
- **USB Reset:** When the UDC detects a USB Reset signal on the USB bus, the status flag R[3] is set to "**1.**" Its Interrupt Vector is 0X0001.
- **USB Host Resume:** When the UDC detects that the USB bus is no longer in Suspend condition and is without Device Resume signal, the status flag R[7] is set to "**1.**" Its Interrupt Vector is 0X0001.

IOCF is an interrupt mask register which can be set bit by bit. While their respective bit is written to "**0**", the hardware interrupt will inhibit, that is, the EM78P611G will not jump to the interrupt vector to execute instructions. But the interrupt status flag still records the conditions no matter whether the interrupt is masked or not. The interrupt status flags must be cleared by firmware before leaving the interrupt service routine and enabling other interrupts.

The global interrupt is enabled by the ENI (RETI) instruction and is disabled by the DISI instruction.

8 Absolute Maximum Ratings

Symbol	Min.	Max.	Unit
Temperature under bias	0	70	ºC
Storage temperature	-65	150	ºC
Input voltage	-0.5	6.0	V
Output voltage	-0.5	6.0	V

9 DC Electrical Characteristics

- T = 25ºC, VDD=5V, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
3.3V Regulator						
V_{Rag}	Output voltage of 3.3V Regulator	V_{DD} = 5V	3.0	3.3	3.6	V
V_{ResetL}	Low Power Reset Detecting Low Voltage	–	–	–	2.2	V
V_{ResetH}	Low Power Reset Detecting High Voltage	–	2.3	–	–	V
Ireg	3.3V Regulator driving capacity	V3.3 = 3.3V	–	–	50	mA
MCU Operation						
I_{IL}	Input Leakage Current for input pins	VIN=VDD, VSS	–	–	±1	µA
V_{IHX}	Clock Input High Voltage	OSCI	2.5	–	–	V
V_{ILX}	Clock Input Low Voltage	OSCI	–	–	1.0	V
I_{CC1}	VDD operating supply current – Normal frequency operation mode	Freq. = 6 MHz	–	–	10	mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{CC2}	VDD operating supply current – Normal frequency operation mode	Freq. = 12 MHz	–	–	20	mA
I_{CC3}	VDD operating supply current – Dual Clock mode	Freq. = 256kHz	–	–	250	µA
I_{SB1}	Operating Supply Current 1 – Power Down mode	WDT disabled	–	–	100	µA
GPIO Pins						
VOH	Output High Voltage	(Ports 5, 6, 8, P7 (P74, 75 in PS2 Mode) and P90~P93, P95~97)	–	Vdd	–	V
VOL	Output Low Voltage	(Port 5, 6, 8, P7 and P90~P93, P95~97)	–	Vss	–	V
V_{IH}	Input High Voltage	Port 5 ~ Port 9	2.0	–	–	V
V_{IL}	Input Low Voltage	Port 5 ~ Port 9	–	–	0.8	V
IOH1	Output High Voltage (P70~P73, P76 and P77)	I_{Sink} = 10.0 mA V_{DD} = 5V	–	10.0	–	mA
IOH2	Output High Voltage (P74, P75)	I_{Sink} = 5.0 mA V_{DD} = 5V	–	5.0	–	mA
IOH3	Output High Voltage (Port 5, Port 6, Port 8 and P90~93, P95~97)	I_{Sink} = 10.0 mA V_{REG} = 5V	–	10.0	–	mA
IOL1	Output Low Voltage (P76 and P77 in normal mode)	I_{Sink} = 10.0 mA V_{DD} = 5V	–	10.0	–	mA
IOL2	Output Low Voltage (P74, P75)	ISink = 10.0 mA VDD = 5V	–	10.0	–	mA
IOL3	Output Low Voltage (P70~P73, P76 and P77 sink LED)	ISink = 10.0 mA VDD = 5V	–	10.0	–	mA
IOL4	Output Low Voltage (P90 ~ P97 in normal mode)	ISink = 10.0 mA VREG = 5V	–	10.0	–	mA
RPH1	Pull-High resistor (Ports 5, 6, 8, 9)	Input pin with pull-high resistor, VREG = 5V	–	25.0	–	KΩ
RPH2	Pull-High resistor (P.74 ~ P.77), (P74/P75) PS2 mode	Input pin with pull-high resistor, VDD = 5V	–	2.2	–	KΩ

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
USB Interface						
V_{OH}	Static Output High	USB operation Mode	2.8	–	3.6	V
V_{OL}	Static Output Low		–	–	0.3	V
V_{DI}	Differential Input Sensitivity		0.2	–	–	V
V_{CM}	Differential Input Command Mode Range		0.8	–	2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8	–	2.0	V
C_{IN}	Transceiver Capacitance		–	–	20	pF
V_{RG}	Output Voltage of Internal Regulator		3.0	–	3.6	V
R_{PH3}	Pull-high resistor (P.75 / D-)		–	1.4	–	KΩ

10 Application Circuits

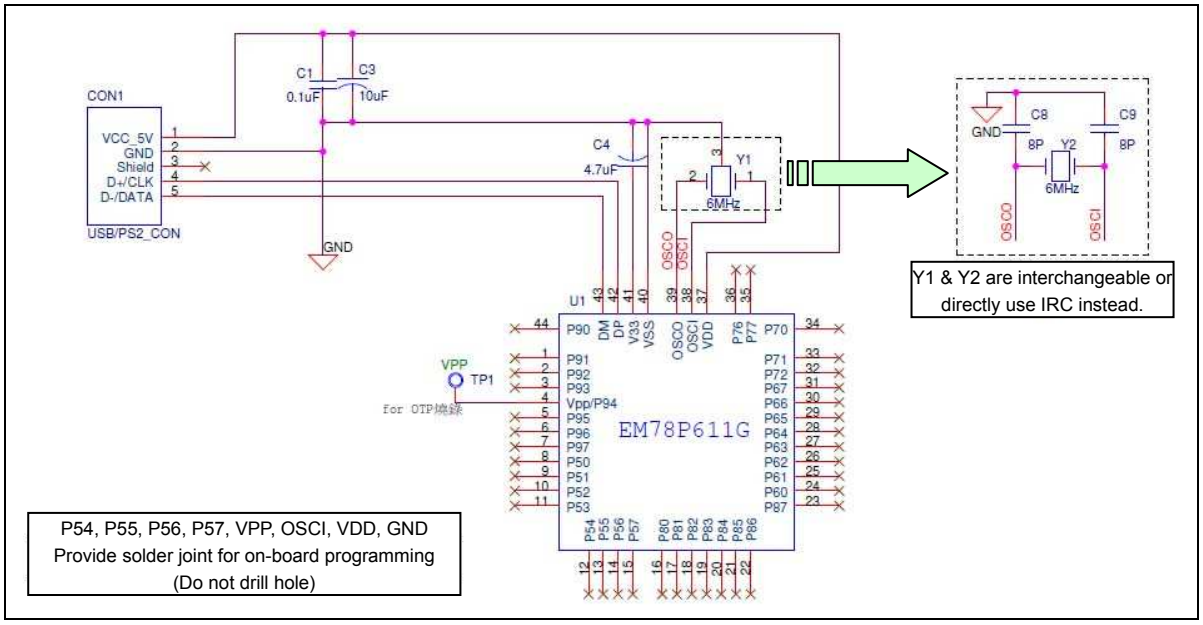


Figure 10-1 EM78P611G Application Circuit

NOTE

*A) **C8, C9:** Load Capacitor*

*B) **C1 C3 (Bypass Capacitor):** Place adjacent to the connector to minimize noise*

*C) **C4 (Power Capacitor):** Place adjacent to the Power source to improve the transient response and ripple rejection.*

APPENDIX

A Special Register Map

A.1 Operational Registers

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0	Default Value
0×00	R0	Indirect Addressing Register								0B_0000_0000
0×01	R1 (TCC)	Timer / Clock Counter								0B_0000_0000
0×02	R2 (PC)	Program Counter								0B_0000_0000
0×03	R3 (Status)	PS2	PS1	PS0	T	P	Z	DC	C	0B_0001_1xxx
0×04	R4 (RSR)	BK1	BK0	Select the register (Address: 00~3F) in Indirect Addressing Mode						
0×05	R5 (Port 5)	P57	P56	P55	P54	P53	P52	P51	P50	0B_0000_0000
0×06	R6 (Port 6)	P67	P66	P65	P64	P63	P62	P61	P60	0B_0000_0000
0×07	R7 (Port 7)	P77	P76	P75/D-/DATA	P74/D+/CLK	*	P72	P71	P70	0B_0000_u000
0×08	R8 (Port 8)	P87	P86	P85	P84	P83	P82	P81	P80	0B_0000_0000
0×09	R9 (Port 9)	P97	P96	P95	*	P93	P92	P91	P90	0B_000u_0000
0×0A	RA	*	*	*	Delay Noise	*	*	*	*	–
0×0B	RB	–	–	–	–	–	–	–	–	0B_0000_0000
0×0C	RC	EP0_W	EP0_R	EP1_R	EP2_R	EP2_W	UDC _SUSPEND	UDC _Writing	STALL	0B_0000_0000
0×0D	RD	USB Application FIFO Address Register								0B_0000_0000
0×0E	RE	USB Application FIFO Data Register								0B_0000_0000
0×0F	RF	USB Host Resume _IF	*	*	Port 7 state change_ 1F	USB Reset_IF	USB Suspend _IF	EP0_IF	TCC_IF	0B_0000_0000

- *Reserved*

A.2 Control Registers

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
-	CONT	S7	INT	TSR2	SR1	TSR0	PSR2	PSR1	PSR0	0B_0011_1111
0×05	IOC5	Port 5 Direction Control Register								0B_1111_1111
0×06	IOC6	Port 6 Direction Control Register								0B_1111_1111
0×07	IOC7	Port 7 Direction Control Register								0B_1111_1111
0×08	IOC8	Port 8 Direction Control Register								0B_1111_1111
0×09	IOC9	Port 9 Direction Control Register								0B_1111_1111
0×0A	IOCA	Dual_ Frq.1	Dual_ Frq.0	/P76, /P77 Pull High	Remote_ Wake-Up	*	*	PS/2	USB	0B_11x0_0000
0×0B	IOCB	/P97	/P96	/P95	/P94	/P93	/P92	/P91	/P90	0B_x111_1111
0×0C	IOCC	P97	P96	P95	*	P93	P92	P91	P90	0B_x00x_0000
0×0D	IOCD	/97	/P96	/P95	*	/P93	/P92	/P91	/P90	0B_x00x_0000
0×0E	IOCE	/Dual clock	/WUE	WTE	RUN	Device_ Resume	/PU8	/PU6	/PU5	0B_1101_0111
0×0F	IOCF	USB Host Resume_ IE	*	*	Port 7 State Change_ 1F	USB Reset_IE	USB Suspend_ IE	EP0_IE	TCC_IE	0B_0000_0000

- *Reserved*

B Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consisting of two oscillator periods), unless the program counter is changed by-

a) Executing the instruction "MOV R2, A", "ADD R2,A", "TBL", or any other instructions that write to R2 (e.g., "SUB R2,A"; "BS R2,6"; "CLR R2", etc.).

b) Execute CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) which were tested to be true.

Under these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

Legend:

R = Register designator that specifies which one of the 64 registers (including operation and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	A, R3, R4
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z, C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC

(Continuation)

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

NOTE: [1] *This instruction is applicable to IOCx only.*
[2] *This instruction is not recommended for RE, RF operation.*

C Code Option Register

The EM78P611G has two Code option registers, which are not part of the normal program memory. The option bits cannot be accessed during normal program execution.

C.1 Address 000:

Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP2 Ena	Clock_source	/R.S	Package_1	Package_0	ID_3	ID_2	ID_1	ID_0	OST_1	OST_0	Freq.	/Protect

Bit 0 (/Protect): Protect program memory address

0: Protect enabled

1: Protect disabled

Bit 1 (Frequency): Frequency Selection

0: MCU runs on 12 MHz

1: MCU runs on 6 MHz

Bits 3 ~ 2 (OST_1 ~ OST_0): Oscillator start-up time

00: 500 µs

01: 2 ms

10: 8 ms

11: 16 ms

Bits 7 ~ 4 (User ID): For user identification use

Bits 9 ~ 8 (Package_1 ~ Package_0): Package type select

00: Not defined

01: Reserved

10: Not defined

11: 44 pins

Bit 10 (/R.S.): D- Pull-up Resistance

0: Connect Resistor Switch

1: Disconnect Resistor Switch

Bit 11 (Clock Source):

1: External oscillator

0: Internal clock (IRC)

Bit 12 (EP2_Enable): Endpoint 2 Enable

0: Disable

1: Enable

C.2 Address 001:

Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	–	–	EP2_ Maxsize_2	EP2_ Maxsize_1	EP2_ Maxsize_0	EP2_ DIR

Bit 0 (EP2_Dir): Endpoint 2 Direction

0: OUT

1: IN

Bits 3 ~ 1 (EP2_Maxsize_2~0): Endpoint 2 maximum size

000: 1 Byte

001: 2 Bytes

010: 3 Bytes

011: 4 Bytes

100: 5 Bytes

101: 6 Bytes

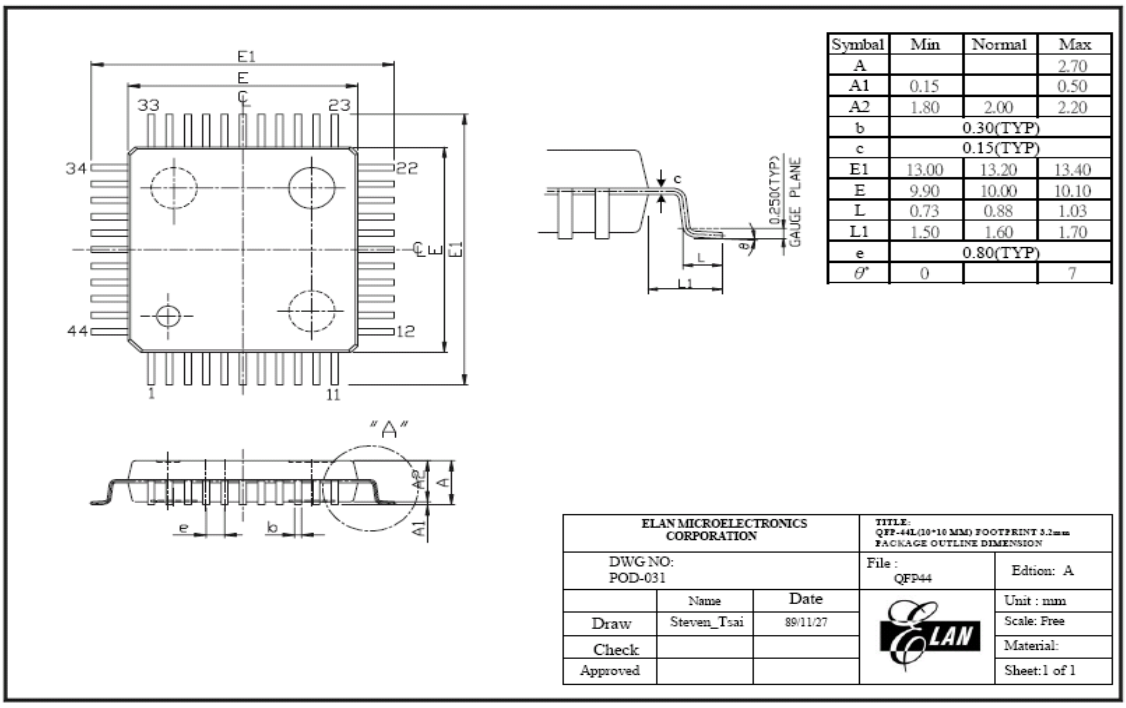
110: 7 Bytes

111: 8 Bytes

Bits 12 ~ 4: Values are fixed

D Package Outline Dimension

- **EM78P611GAQ**



Symbal	Min	Normal	Max
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b		0.30(TYP)	
c		0.15(TYP)	
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e		0.80(TYP)	
θ°	0		7

ELAN MICROELECTRONICS CORPORATION			TITLE: QFP-44L(10*10 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
DWG NO: POD-031			File : QFP44	Edtion: A
	Name	Date		Unit : mm
Draw	Steven_Tsai	89/11/27		Scale: Free
Check				Material:
Approved				Sheet:1 of 1

Figure D-1 EM78P611GAQ Package Outline Dimension

E OTP Program Pin

IC Pin Name	44-pin Package
P94	4
P57	15
P56	14
P55	13
VSS	40
OSCI	38
VDD	37
P54	12