
EM78680

**USB Full Speed
Microcontroller**

**Product
Specification**

DOC. VERSION 1.0


ELAN MICROELECTRONICS CORP.

November 2011



Trademark Acknowledgments:

Windows is a trademark of Microsoft Corporation.

ELAN and ELAN logo  are trademarks of ELAN Microelectronics Corporation.

Copyright © 2008~2011 by **ELAN Microelectronics Corporation**

All Rights Reserved

Printed in Taiwan

The contents of this specification are subject to change without further notice. ELAN Microelectronics assumes no responsibility concerning the accuracy, adequacy, or completeness of this specification. ELAN Microelectronics makes no commitment to update, or to keep current the information and material contained in this specification. Such information and material may change to conform to each confirmed order.

In no event shall ELAN Microelectronics be made responsible for any claims attributed to errors, omissions, or other inaccuracies in the information or material contained in this specification. ELAN Microelectronics shall not be liable for direct, indirect, special incidental, or consequential damages arising from the use of such information or material.

The software (if any) described in this specification is furnished under a license or nondisclosure agreement, and may be used or copied only in accordance with the terms of such agreement.

ELAN Microelectronics products are not intended for use in life support appliances, devices, or systems. Use of ELAN Microelectronics product in such applications is not supported and is prohibited.

NO PART OF THIS SPECIFICATION MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE EXPRESSED WRITTEN PERMISSION OF ELAN MICROELECTRONICS.



ELAN MICROELECTRONICS CORPORATION

Headquarters:

No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
<http://www.emc.com.tw>

Hong Kong:

Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre 95
How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:

Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Korea:**Elan Korea Electronics Company, Ltd.**

301 Dong-A Building
632 Kojan-Dong, Namdong-ku
Incheon City, KOREA
Tel: +82 32 814-7730
Fax: +82 32 813-7730

Shenzhen:**Elan Microelectronics Shenzhen, Ltd.**

3F, SSMEC Bldg., Gaoxin S. Ave. I
Shenzhen Hi-tech Industrial Park
(South Area), Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:**ELAN Microelectronics Shanghai, Ltd.**

Rm101, #3 Lane 289, Bisheng Rd.,
Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai,
CHINA 201204
Tel: +86 21 5080-3866
Fax: +86 21 5080-0273
elan-sh@elanic.com.cn

Contents

| | | |
|----------|--|----------|
| 1 | General Description | 1 |
| 2 | Features | 1 |
| 3 | PIN DESCRIPTION | 4 |
| 4 | Block Diagram | 5 |
| 5 | Function Description | 5 |
| 5.1 | Program Memory..... | 5 |
| 5.2 | Data Memory..... | 6 |
| 5.2.1 | Operational Registers..... | 8 |
| 5.3 | Special Function Registers..... | 18 |
| 5.3.1 | A (Accumulator)..... | 18 |
| 5.3.2 | CONT (Control Register)..... | 18 |
| 5.3.3 | IOC5 ~ IOC9 Port Direction Control Registers..... | 19 |
| 5.3.4 | IOCA (RFCNT: RF Control Register)..... | 19 |
| 5.3.5 | IOCB (PWM_CNT: PWM Controller) Default (0b0000_0001)..... | 19 |
| 5.3.6 | IOCC (T1CON: Timer 1 Control Register)..... | 20 |
| 5.3.7 | IOCD (Port 9 Pull-high Control Register) Default Value: (0B_1111_1111) | 20 |
| 5.3.8 | IOCE (MCU Control Register) Default (0b1101_1111)..... | 21 |
| 5.3.9 | IOCF (Interrupt Mask Register)..... | 21 |
| 5.4 | USB Device Controller | 22 |
| 5.5 | Device Address and Endpoints..... | 23 |
| 5.6 | Reset..... | 23 |
| 5.6.1 | Power-on Reset..... | 23 |
| 5.6.2 | Watchdog Reset..... | 23 |
| 5.6.3 | USB Reset..... | 23 |
| 5.7 | Power Saving Mode | 24 |
| 5.7.1 | Power-down Mode | 24 |
| 5.7.2 | Dual Clock Mode..... | 24 |
| 5.8 | Interrupt..... | 25 |
| 5.9 | Pattern Detect Application (PDA) | 26 |
| 5.9.1 | Function Description..... | 26 |
| 5.9.2 | Control Register | 26 |
| 5.9.3 | Sampling Rate and Debounce Length | 27 |
| 5.10 | Pulse Width Modulation (PWM) | 28 |
| 5.10.1 | Function Description..... | 28 |
| 5.10.2 | Control Register | 29 |
| 5.11 | Analog-To-Digital Converter (ADC) | 29 |
| 5.11.1 | Function Description..... | 29 |
| 5.11.2 | Control Register | 30 |
| 5.12 | Serial Peripheral Interface Mode..... | 31 |
| 5.12.1 | Overview | 31 |
| 5.12.2 | Features | 31 |



5.12.3 SPI Function Description.....33

5.12.4 SPI Signal and Pin Description35

5.12.5 SPI Control Registers.....36

5.12.6 SPI Mode Timing.....39

5.12.7 SPI Timer 1 Mode.....44

6 Absolute Maximum Ratings 46

7 DC Electrical Characteristic 47

APPENDIX

A Special Register Map 48

B Instruction Set 54

C Code Option..... 56

D Application Circuit 59

Specification Revision History

| Doc. Version | Revision Description | Date |
|--------------|------------------------|------------|
| 0.1 | Preliminary version | 2008/03/19 |
| 1.0 | Remove Pin Assignment. | 2011/11/23 |



1 General Description

The EM78680 is a series of 8-bit Universal Serial Bus (USB), RISC architecture, micro-controller. It is specifically designed for USB full speed device application. The EM78680 also supports one device address and six endpoints.

The EM78680 has 8-level stacks and four sets of interrupt sources. It has a maximum of 38 General Input/Output pins with the capacity of sinking large current. Each device has 272 bytes of general purpose SRAM, 6K bytes of program ROM.

These series of ICs have special features that meet user's requirements. Such features are:

- Dual Clock mode which allows the device to run on very low power.
- Pattern Detect Application function which is used in serial transmission to count waveform width.
- Pulse Width Modulation that can generate a duty-cycle-programmable signal
- 24-channel AD converter with up to 10 bits resolution
- Serial Peripheral Interface

2 Features

- Operating voltage: 4.0V ~ 5.5V (24MHz operation voltage: 5.0~5.5V)
- USB Specification Compliance
 - Universal Serial Bus Specification Version 1.1
 - USB Device Class Definition for Human Interface Device (HID), Firmware Specification Version 1.1
 - Supports one device address and six endpoints
- USB Application
 - P74 (D+) has an internal pull-high resistor (1.5K Ω)
 - USB protocol handling
 - USB device state handling
 - Identifies and decodes Standard USB commands to Endpoint Zero
- Built-in 8-bit RISC MCU
 - 8-level stacks for subroutine testing, and interrupt
 - Auto saving R3, R4 and RA Bit 7 when interrupt occurs
 - 4 sets of interrupts
 - 8-bit real time clock/counter (TCC) with overflow interrupt
 - Built-in RC oscillator free running for Watchdog Timer and Dual clock mode
 - Two independent programmable prescalers for WDT and TCC



- Two methods of power saving:
 - Power-down mode (Sleep mode)
 - Dual clock mode
- Two clocks per instruction cycle
- Multi-time programmable
- Set 1 INT : (jump to 0x08)
 - TCC overflow interrupt
 - EP0 command in interrupt
 - USB suspend interrupt
 - USB reset interrupt
 - USB HOST resume interrupt
- Set 2 INT : (jump to 0x10)
 - RF1 low pattern interrupt
 - RF1 high pattern interrupt
 - RF2 low pattern interrupt
 - RF2 high pattern interrupt
- Set 3 INT : (jump to 0x18)
 - P77 port change interrupt
 - P76 port change interrupt
 - SPI Timer 1 comparator completed interrupt (Note 1)
 - SPI transmission completed interrupt (Note 1).

Note1: When use this interrupt please set code option bit 65 as “0”.
- Set 4 INT : (jump to 0x20)
- EP1~5 output Endpoint received O.K interrupt
- I/O Ports
 - 3 LED sink pins
 - Each GPIO pin in Ports 5, 6, 8, 9, P70~P72 and P76~P77 has an internal programmable pull-high resistor (25 K Ω)
 - Ports 5, 6, 8, 9 are 3.3V I/O, Port 7: 5V I/O
 - Each GPIO pin of Port 6, Ports 90~93 can wake-up the MCU from sleep mode by input state change
- Internal Memory
 - Built-in 6K \times 13 bits Program ROM
 - Built-in 272 bytes general purpose registers (SRAM)
 - Built-in USB Application FIFOs
- Operation Frequency

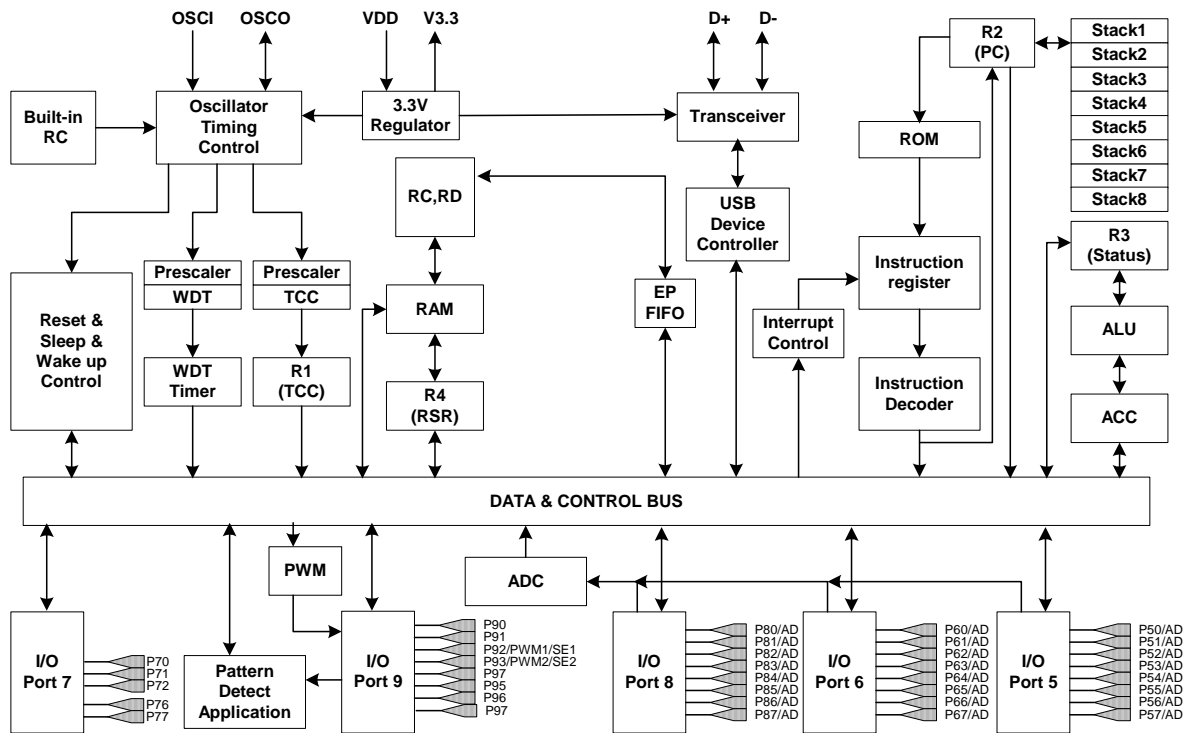


- Normal Mode: MCU runs on an external oscillator frequency of 4MHz, Internal system frequency of 8MHz, 16MHz or 24MHz
- Dual Clock Mode: MCU runs at a frequency of 256kHz (or 32kHz, 4kHz, 500Hz), using an internal oscillator with an external crystal resonator turned off to save power
- Built-in Pattern Detecting Application for serial signal transmission
- Built-in Pulse Width Modulation (PWM)
 - 2 channels PWM function on P.92 (PWM1) and P.93 (PWM2)
 - 8-bit resolution of PWM output
 - 8 selections of duty cycles
- Built-in 24-Channel Analog-to-Digital Converter (ADC)
 - Built-in AD Converter with 10-bit resolution
 - 4 types of ADC clock source selection: 256K/128K/64K/32K
- Built-in Serial Peripheral Interface (SPI)
 - Operation in either Master mode or Slave mode
 - Programmable baud rates of communication
 - Up to 8 MHz bit frequency
- Built-in 3.3V Voltage Regulator
 - For UDC power supply
 - Pull-up source for the external USB resistor on D+ pin

3 Pin Description

| Symbol | I/O | Function |
|------------------------|-----|--|
| P50 ~ P57 | I/O | General 8-bit bidirectional input/output port. All pins on this port can be internally pulled-high by register IOCE Bit 0. All Port 5 input/output pins can be used for ADC function. (Code Option Bit 65=0) and SPI function enable => P57: SPI /SS bit P56: SCK , P55:SDO , P54:SDI |
| P60 ~ P67 | I/O | General 8-bit bidirectional input/output port. All pins on this port can be internally pulled-high by register IOCE Bit 1. All Port 6 input/output pins can be used for ADC function. |
| P70 ~ P72 P76 ~ P77 | I/O | General 5-bit bidirectional input/output port. All pins on this port can be internally pulled-high by register IOCE Bit 3. The sink current of P70 ~ P72 are used for driving the LED. |
| P80 ~ P87 | I/O | General 8-bit bidirectional input/output port. All pins on this port can be internally pulled-high by register IOCE Bit 2. All Port 8 input/output pins can be used for ADC function. |
| P90~P97 | I/O | General 8-bit bidirectional input/output port. Each pin can be internally pulled-high by register IOCD. P92 ~ P93 can be used for PWM (pulse width modulation) or PDA (serial signal transmission application) function. |
| USB D+ | I/O | USB D+ pin. Built-in internal 1.5K pulled-high resistor to V3.3 |
| USB D- | I/O | USB D- pin |
| OSCI | I | 4 MHz crystal input |
| OSCO | I/O | Return path for 4 MHz crystal |
| V3.3 | O | 3.3V DC voltage output from an internal regulator. This pin has to be tied to a 4.7 μ F capacitor. |
| VDD | - | Connect to the USB power source or to a nominal 5V-power supply. Actual VDD range can vary between 4.4V and 5.25V. |
| VSS | - | Connect to ground. |

4 Block Diagram



5 Function Description

The EM78680 memory is organized into four spaces, namely; User Program memory in 6K×13 bits ROM space, Data Memory in 272 bytes SRAM space, and USB Application FIFOs for Endpoint 0, Endpoint 1, Endpoint 2, Endpoint 3, Endpoint 4, Endpoint 5. Furthermore, several registers are used for special purposes.

5.1 Program Memory

The program space of the EM78680 is 6K bytes, and is divided into six pages. Each page is 1K bytes long. After a Reset, the 13-bit Program Counter (PC) points to location zero of the program space.

The Interrupt Vectors are at 0x0008 (USB and TCC interrupts), 0x0010 (RF function interrupt), 0x0018 (P76 P77 port change and SPI interrupt) and 0x020 (EP1~5 output endpoint interrupt).

When interrupt occurs, the MCU will auto save the Status Register (R3), RA,7, RAM Select Register (R4 Bits 6, 7), Accumulator (A) then clear PS0~PS2 and fetch the instruction from the interrupt vector address. The interrupt vector address is illustrated in the following diagram.

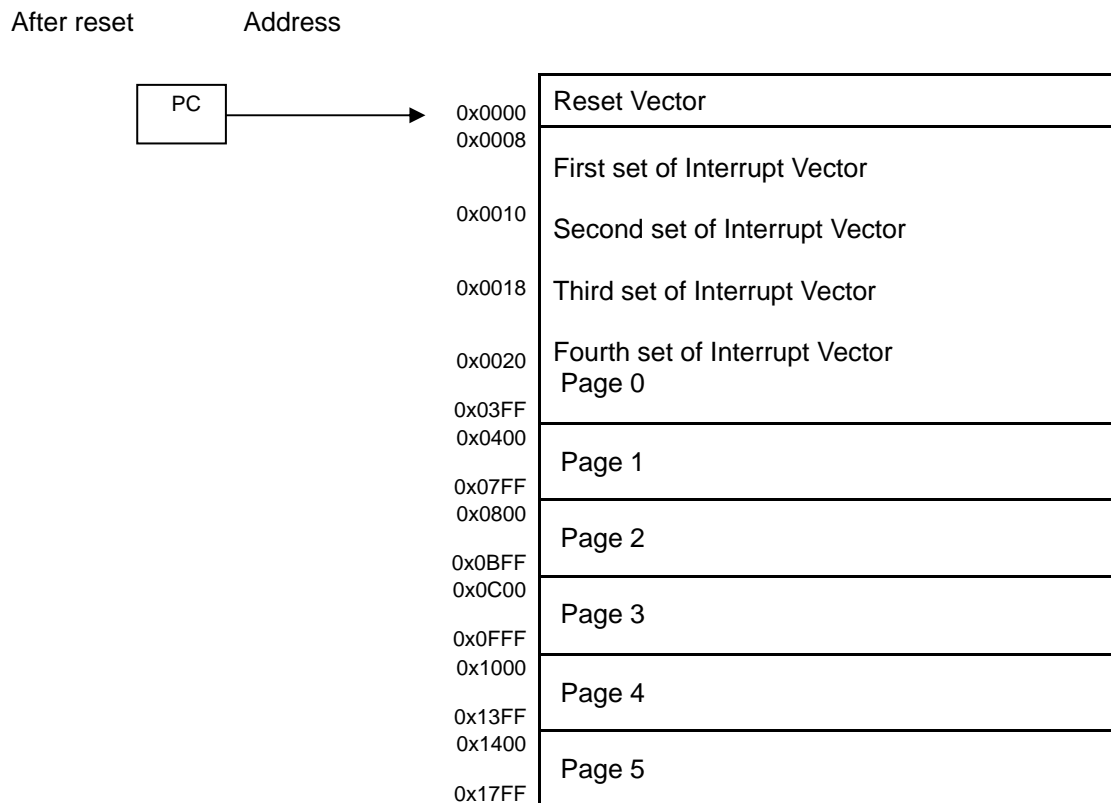


Figure 5-1 EM78680 Data RAM Organization

5.2 Data Memory

The Data Memory has 272 bytes SRAM space. It is also equipped with USB Application FIFO space for USB Application. Figure 5-2 shows the organization of the Data Memory Space.

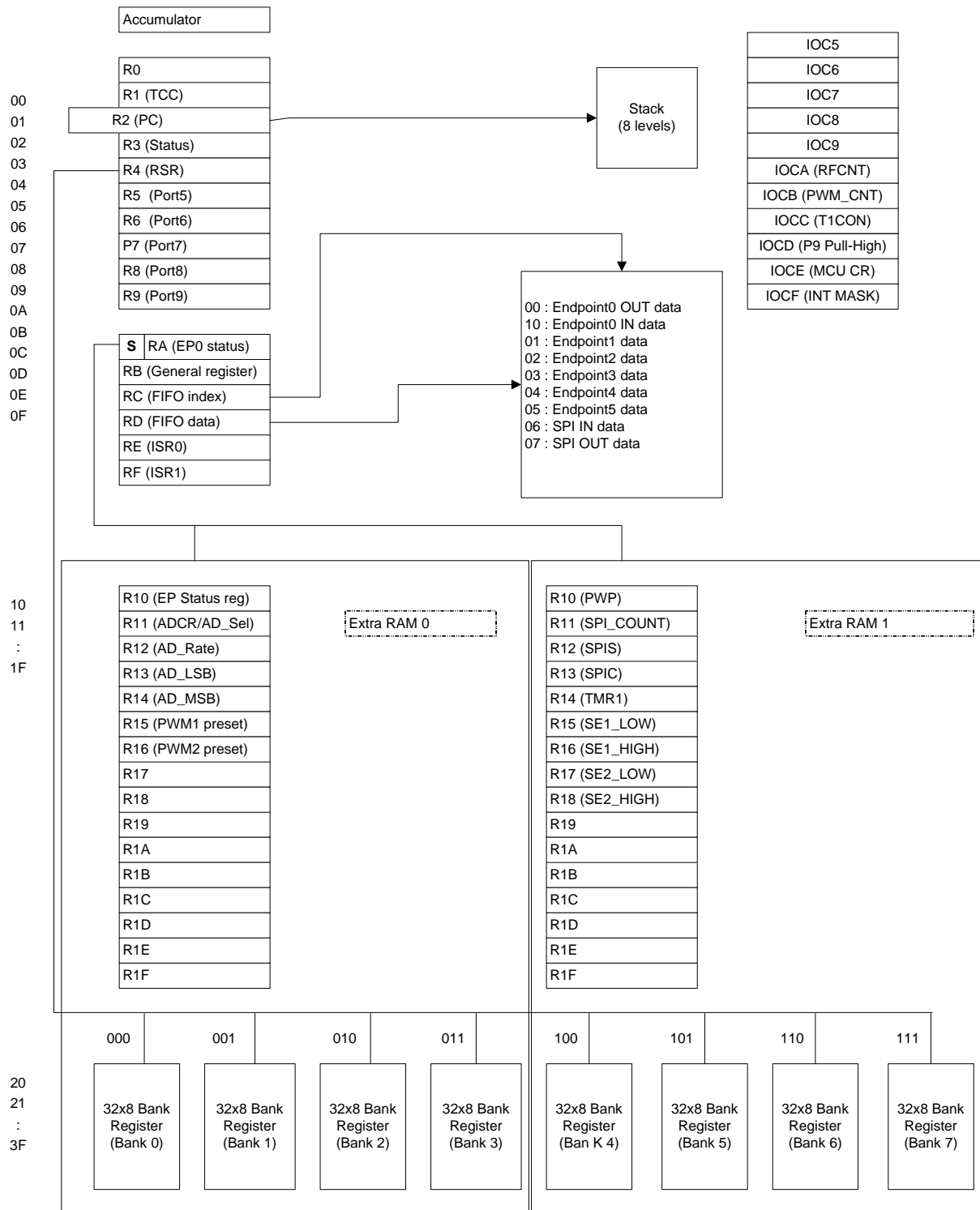


Figure 5-2 Data Memory Configuration



5.2.1 Operational Registers

5.2.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

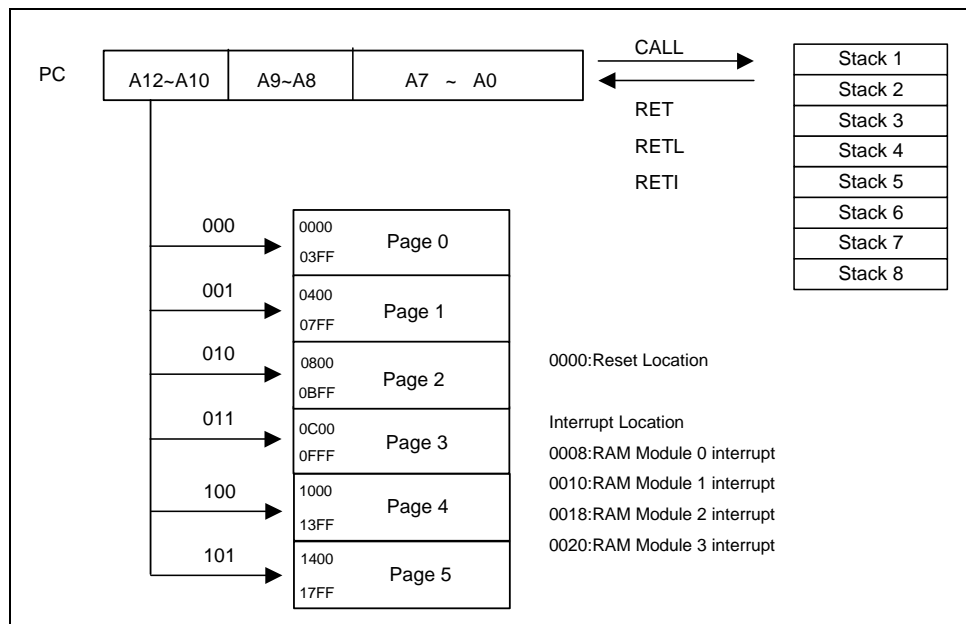
5.2.1.2 R1 (Timer/Clock Counter, TCC)

This register TCC, is an 8-bit timer or counter. It is incremented by the instruction cycle clock, and is readable and writable as any other register.

5.2.1.3 R2 (Program Counter and Stack)

- R2 and the hardware stacks are 13 bits wide.
- The structure is depicted in Figure 5-3.
- Generates 6K×13 on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- All the R2 bits are set to "0"s when a reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows jump to any location on one page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
- "MOV R2, A" allows the loading of an address from the "A" register to the lower 8 bits of PC, and the ninth and tenth bits (A8~A9) of PC are cleared.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and tenth bits of PC are cleared.
- Any instruction that is written to R2 (e.g. "ADD R2, A", "MOV R2, A", "BC R2,6", etc-), except "TBL" will cause the ninth and tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- "TBL" allows a relative address to be added to the current PC (R2+A→R2), and the contents of the ninth and tenth bits (A8~A9) of the PC are not changed. Thus, the computed jump can be on the second (third, or 4th) 256 locations on one program page.
- For the EM78680, the most significant bits (A10~A12) will be loaded with the contents of bits PS0~PS2 in the status register (R3) upon the execution of a "JMP", "CALL", or any other instructions which writes to R2.

- All instructions are single instruction cycle except for the instruction that would change the contents R2. Such instruction will need one more instruction cycle.



5.2.1.4 R3 (Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PS2 | PS1 | PS0 | T | P | Z | DC | C |

After an interrupt occurs, the MCU will save R3 Bits 5~7 first and clear automatically PS0~PS2.

R3 [0] Carry flag

R3 [1] Auxiliary carry flag

R3 [2] Zero flag. It will be set to 1 when the result of an arithmetic or logic operation is zero.

R3 [3] Power down flag. It will be set to 1 during Power-on phase or by “WDTC” command and cleared when the MCU enters into Power-down mode. It remains in its previous state after a Watchdog Reset.

“0”: Power-down mode

“1”: Power on

Values of RST, T and P after a Reset

| Reset Type | T | P |
|---|---|---|
| Power on | 1 | 1 |
| WDT during Operation mode | 0 | P |
| WDT wake-up during Sleep 1 mode | 0 | 0 |
| WDT wake-up during Sleep 2 mode | 0 | P |
| Wake-up on pin change during Sleep 2 mode | P | P |

*P: Previous value before reset



Status of RST, T and P Being Affected by Events

| Event | T | P |
|---|---|----|
| Power on | 1 | 1 |
| WDTC instruction | 1 | 1 |
| WDT time-out | 0 | *P |
| SLEP instruction | 1 | 0 |
| Wake-up on pin change during Sleep 2 mode | P | P |

*P: Previous value before reset

R3 [4] Time-out flag. It will be set to 1 during Power-on phase or by “WDTC” command. It is reset to 0 by WDT time-out.

“0”: Watchdog timer with overflow

“1”: Watchdog timer without overflow

R3 [5~7] Page select bits. These three bits are used to select the program memory page.

| PS2 | PS1 | PS0 | Program Memory Page [Address] |
|-----|-----|-----|-------------------------------|
| 0 | 0 | 0 | Page 0 [000-3FF] |
| 0 | 0 | 1 | Page 1 [400-7FF] |
| 0 | 1 | 0 | Page 2 [800-BFF] |
| 0 | 1 | 1 | Page 3 [C00-FFF] |
| 1 | 0 | 0 | Page 4 [1000-13FF] |
| 1 | 0 | 1 | Page 5 [1400-17FF] |

5.2.1.5 R4 (RAM Select Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| BK1 | BK0 | Ad5 | Ad4 | Ad3 | Ad2 | Ad1 | Ad0 |

R4 (RAM select register) contains the address of the registers. When interrupt occurs , the MCU will save R4 value automatically.

R4 [0~5] are used to select registers (Address: 0x00h~0x3Fh) in indirect addressing mode.

R4 [6~7]are used to determine which bank is activated among the 8 banks. To select a register bank, refer to the table below:

| R4[7]BK1 | R4[6]BK0 | RAM Bank # |
|----------|----------|------------|
| 0 | 0 | Bank 0 |
| 0 | 1 | Bank 1 |
| 1 | 0 | Bank 2 |
| 1 | 1 | Bank 3 |

5.2.1.6 R5 (Port 5 I/O Register) Default Value: (0B_0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |



5.2.1.7 R6 (Port 6 I/O Register) Default Value: (0B_0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| P67 | P66 | P65 | P64 | P63 | P62 | P61 | P60 |

5.2.1.8 R7 (Port 7 I/O Register) Default Value: (0B_0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|--------|--------|-------|-------|-------|-------|
| P77 | P76 | D-/P75 | D+/P74 | – | P72 | P71 | P70 |

5.2.1.9 R8 (Port 8 I/O Register) Default Value: (0B_0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| P87 | P86 | P85 | P84 | P83 | P82 | P81 | P80 |

5.2.1.10 R9 (Port 9 I/O Register) Default Value: (0B_0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| P97 | P96 | P95 | P94 | P93 | P92 | P91 | P90 |

5.2.1.11 RA (USB Endpoint 0 Status Register) Default Value: (0B0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------------|-------|-------|------------|-------------|-------------|-------|
| Extr_R | Remote Status | EP0_W | EP0_R | Dev_Resume | UDC_Suspend | UDC_Writing | STALL |

RA [0] STALL flag. When the MCU receives an unsupported command or invalid parameters from host, this bit will be set to 1 by the firmware to notify the UDC to return a STALL handshake. When a successful setup transaction is received, this bit is cleared automatically. This bit is both readable and writable.

RA [1] UDC Writing flag. Read only. When this bit is equal to “1,” it indicates that the UDC is writing data into the EP0’s FIFO or reading data from it. During this time, the firmware will avoid accessing the FIFO until the UDC finishes writing or reading. This bit is readable only.

1: EP0’s FIFO is busy

0: EP0’s FIFO is free for data transition. ACK, NAK are reset.

RA [2] UDC Suspend flag. If this bit is equal to 1, it indicates that the USB bus has no traffic for a specified period of 3.0 ms. This bit will also be cleared automatically when a bus activity takes place. This bit is readable only.

RA [3] Device resume flag. This bit is set by firmware to generate a signal to wake up the USB host and is cleared as soon as the USB Suspend signal becomes low. This bit can only be set by firmware and cleared by hardware. It can only be used in dual mode. This bit is both readable and writable.

RA [4] EP0_R flag. This bit informs the UDC to read the data written by the firmware from the FIFO. Then the UDC will automatically send the data to the Host. After the UDC finishes reading the data from the FIFO, this bit will be cleared automatically.



Therefore, before writing data into FIFO, the firmware will first check this bit to avoid overwriting the data. This bit can only be set by the firmware and cleared by the hardware.

RA [5] EP0_W. After the UDC completes writing data to the FIFO, this bit will be set automatically. The firmware will clear it as soon as it gets the data from EP0's FIFO. Only when this bit is cleared will the UDC be able to write a new data into the FIFO.

Therefore, before the firmware can write a data into the FIFO, this bit must first be set by the firmware to prevent the UDC from writing data at the same time. This bit is both readable and writable.

RA [6] Remote wake-up status. Pass device remote wake-up setting from the PC.

RA [7] Extra RAM switch. RAM block switch

0: Switch to Bank 0~Bank 3 and external RAM 0

1: Switch to Bank 4~Bank 7 and external RAM 1

5.2.1.12 RC (FIFO Indirect Index Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | UAD4 | UAD3 | UAD2 | UAD1 | UAD0 |

RC [0~4] Application FIFO address registers. These five bits are the address pointer of the Application FIFO.

RC [5~7] Undefined registers.

5.2.1.13 RD (FIFO Indirect Data Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| UAD7 | UAD6 | UAD5 | UAD4 | UAD3 | UAD2 | UAD1 | UAD0 |

RD (Application FIFO data register) contains the data in the register of which address is pointed by RC.

5.2.1.14 RE (Interrupt Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|-------|-------|----------|---------|----------|---------|
| P77_IF | P76_IF | TM1IF | SPIIF | RF2_High | RF2_Low | RF1_High | RF1_Low |

RE [0] RF1_Low flag: Pattern Detection interrupt flag. RF1 low pattern compare flag.

RE [1] RF1_High flag: Pattern Detection interrupt flag. RF1 high pattern compare flag.

RE [2] RF2_Low flag: Pattern Detection interrupt flag. RF2 low pattern compare flag.

RE [3] RF2_High flag: Pattern Detection interrupt flag. RF2 high pattern compare flag.

RE [4] SPI interrupt flag. Set by data transmission complete, flag is cleared by software. The interrupt is created after the SPI data is saved to SRAM.



RE [5] Timer 1 interrupt flag. Set by the comparator at Timer 1 application, flag cleared by software.

RE [6] P76_IF: P76 State Change interrupt flag.

RE [7] P77_IF: P77 State Change interrupt flag. The Interrupt Vector is in Address 0x0018.

5.2.1.15 RF (Interrupt Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-----------|-------------|------------|--------|--------|
| OUT_EP_IF | – | – | Resume_IF | USBReset_IF | Suspend_IF | EP0_IF | TCC_IF |

RF [0] TCC timer overflow interrupt flag. It will be set while TCC timer overflows, and is cleared by the firmware.

RF [1] EndPoint Zero interrupt flag. It will be set when the EM78680 receives Vendor /Customer Command to EndPoint Zero. This bit is cleared by the firmware.

RF [2] USB Suspend interrupt flag: It will be set when the EM78680 finds the USB Suspend Signal on USB bus. This bit is cleared by the firmware.

RF [3] USB Reset interrupt flag. It will be set when the Host issues the USB Reset signal.

RF [4] USB Host Resume interrupt flag. It will be set only under Dual clock mode when the USB suspend signal becomes low.

RF [5~6] Not used and read as “0”.

RF [7] OUT Endpoint interrupt flag. It will be set when the FIFO of Out Endpoint has received data from host.

Extra RAM0:

5.2.1.16 R10 (USB Endpoint Status Register) Default (0b0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------|--------|--------|--------|--------|
| – | – | – | EP5_ST | EP4_ST | EP3_ST | EP2_ST | EP1_ST |

R10 [0~4] EPx_ST: End point state flag.

For IN Endpoint: Set to “1” by firmware when buffer o.k. This bit is reset after UDC sends data to Host and gets ACK from Host. Before writing data into FIFO, user must check this bit to prevent overwriting the data. This is readable and writable.

For OUT Endpoint: Set 1 by UDC when buffer o.k. Set 0 by firmware when buffer is read.

After an out token finish, and the UDC completes writing data to the FIFO, this bit will be set automatically, and run into Interrupt Vector 0x0020. The firmware should clear it as soon as it gets the data from OUT Endpoint's FIFO. Only when this bit is cleared, the UDC is able to write a new data into the FIFO.



When Code Option Bit 65=0, user can reset the FIFO pointer and counter by setting the EPX_ST bit from high to low.

5.2.1.17 R11 (AD Controller/AD Selection Pin) Default (0b0001_1111)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|
| AD_start | AD_R1 | AD_R0 | AD_A4 | AD_A3 | AD_A2 | AD_A1 | AD_A0 |

R11 [0~4] AD channel selector: If the AD number is from 0 to 0x17, the AD converter will be powered on. Otherwise, it will be powered off.

| | | | | |
|-----------|-------|-------|-------|-------|
| AD number | 00000 | 00001 | 00010 | 00011 |
| AD pin | AD0 | AD1 | AD2 | AD3 |
| AD number | 00100 | 00101 | 00110 | 00111 |
| AD pin | AD4 | AD5 | AD6 | AD7 |
| AD number | 01000 | 01001 | 01010 | 01011 |
| AD pin | AD8 | AD9 | AD10 | AD11 |
| AD number | 01100 | 01101 | 01110 | 01111 |
| AD pin | AD12 | AD13 | AD14 | AD15 |
| AD number | 10000 | 10001 | 10010 | 10011 |
| AD pin | AD16 | AD17 | AD18 | AD19 |
| AD number | 10100 | 10101 | 10110 | 10111 |
| AD pin | AD20 | AD21 | AD22 | AD23 |

R11 [5~6] AD conversion clock source

00: 256K

01: 128K

10: 64K

11: 32K

R11 [7] AD Converter ready flag

0 → 1: Start AD Conversion (set by firmware).

1 → 0: When AD finishes converting and has moved the digital data into the AD Data Register, this bit will be reset by hardware.

NOTE

Hardware can enable this function only at the AD Channel Selector of the functional I/O port. After Power-on reset, the initial value of this register is 0b0001 1111.

5.2.1.18 R12 (Dual Mode Control) Default (0b0000_1000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-----------|---------|---------|-----------|-------|-------|-------|
| - | USB-Token | LOW FR1 | LOW FR0 | /LOW FREQ | - | - | - |

R12 [3]: /LOW FREQ: Dual Clock Control bit. This bit is used to select the system clock frequency. When this bit is set to 0, the MCU will run on very slow frequency for power saving purposes and the UDC will stop working.

0: Slow frequency (500Hz~256kHz)

1: Normal frequency

R12 [4~5]: LOW FR0 ~ LOW FR1: Low Frequency Switches. These bits select the operation frequency in Dual Clock Mode. Four frequencies are available and can be chosen as Dual Clock Mode for running the MCU program.

| Low FR1 | Low FR0 | Frequency |
|---------|---------|-----------|
| 0 | 0 | 500Hz |
| 0 | 1 | 4kHz |
| 1 | 0 | 32kHz |
| 1 | 1 | 256kHz |

R12[6] (USB_Token): Set when USB Token from Host. Reset when end of the Token.

5.2.1.19 R13 R14 (ADC Output Data for Selecting Pin) Default (0b0000_0000)

Read Only

When the A/D conversion is completed, the result is loaded to R13 and R14.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADB1 | ADB0 | -- | -- | -- | -- | -- | -- |

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADB9 | ADB8 | ADB7 | ADB6 | ADB5 | ADB4 | ADB3 | ADB2 |

R15: High level time of the 1st PWM module that outputs to P92 (If PWM function is enabled).

R16: The high level time of the 2nd PWM module that outputs to P93 (If PWM function is enabled).

R15~R16 can be a general purpose register if the PWM function is disabled.

5.2.1.20 R17~R1F (General Purpose Register)

R17~R1F are general-purpose registers.

5.2.1.21 R20~R3F (General Purpose Register)

R20~R3F (including Banks 0~3) are general-purpose registers.

Extra RAM1:

R10 ~ R14 (Note that only when Code Option Bit 65 is selected as “0”, these registers are valid. If user sets the Code Option Bit 65 as “1”, R10~R14 of extra RAM1 is not available).

5.2.1.22 R10 (PWP: Pulse Width Preset Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PWP7 | PWP6 | PWP5 | PWP4 | PWP3 | PWP2 | PWP1 | PWP0 |

R10 [0~7] PWP7~PWP0 is bit set of pulse width preset in advance for the desired width of the baud clock.

$$Pulse\ Width = (PWP + 1) \times TMR$$

5.2.1.23 R11 (SPI Byte Number Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | SPIC7 | SPIC6 | SPIC5 | SPIC4 | - | - | - |

R11 [0~2]: Reserved

R11 [3~6]: SPI byte number: For setting the SPI byte number. The maximum number is 8 bytes

R11 [7]: Reserved

5.2.1.24 R12 (SPIS: SPI Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|----------|-------|-------|-------|-------|-------|-------|
| Lstatus1 | Lstatus0 | M/LSB | -- | OD3 | OD4 | - | RBF |

R12[0] RBF: Read Buffer Full flag

0: Receiving not completed yet, and SPIRB (SPI Read Buffer) has not fully exchanged

1: Receiving completed; SPIRB (SPI Read Buffer) is fully exchanged.

R12 [1]: Reserved

R12 [2] OD4: Open-Drain Control bit:

0: Open-drain disable for SCK

1: Open-drain enable for SCK

R12 [3] OD3: Open-Drain Control bit:

0: Open-drain disable for SDO

1: Open-drain enable for SDO

R12 [4]: Reserved

R12 [5] M/LSB: The first bit of SPI Shift.

0: LSB

1: MSB



R12 [6~7] Lstatus0~ Lstatus1:

- 00: The SDO will keep status after transfer over.
- 01: The SDO will pull-down after transfer over.
- 10: The SDO will pull-high after transfer over.
- 11: No defined.

5.2.1.25 R13 (SPIC: SPI Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CES | SPIE | SRO | SSE | -- | SBR2 | SBR1 | SBR0 |

R13 [0~2] SBR0~2: SPI Baud Rate Select bits

SPI baud rate table is illustrated in SPI section in the subsequent pages.

R13 [3]: Reserved

R13 [4] SSE: SPI Shift Enable bit

- 0: Reset as soon as the shifting is complete, and the next transmission is ready to shift.
- 1: Start to shift, and keep on 1 while the current transmissions still being transmitted.

NOTE

This bit will reset to 0 at every transmission by the hardware

R13 [5] SRO: SPI Read Overflow bit

- 0: No overflow
- 1: A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in SPIS register will be destroyed.

NOTE

This can only occur in slave mode.

R13 [6] SPIE: SPI Enable bit

- 0: Disable SPI mode
- 1: Enable SPI mode

R13 [7] CES: Clock Edge Select bit

- 0: Data shifts out on rising edge, and shifts in on falling edge. Data is on hold during the low level.
- 1: Data shifts out on falling edge, and shifts in on rising edge. Data is on hold during the high level.



5.2.1.26 R14 (TMR1: Timer 1 Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TMR17 | TMR16 | TMR15 | TMR14 | TMR13 | TMR12 | TMR11 | TMR10 |

R14 [0~7] TMR: TMR is bit set of Timer 1 register and it increases until the value matches PWP and then resets to 0.

R15 (SE1_LOW): Low signal counter of the 1st RF module that is input from P92.

R16 (SE1_HIGH): High signal counter of the 1st RF module that is input from P92.

R17 (SE2_LOW): Low signal counter of the 2nd RF module that is input from P93.

R18 (SE2_HIGH): High signal counter of the 2nd RF module that is input from P93.

R15 ~ R18 are RF Timing counter registers if RF function is enabled by setting Bit 2 or Bit 3 of IOCF. Otherwise, they are general registers.

R19~R1F (General Purpose Registers)

R19~R1F are general-purpose registers.

R20~R3F (General Purpose Registers)

R20~R3F (including Banks 4~7) are general-purpose registers.

5.3 Special Function Registers

5.3.1 A (Accumulator)

The accumulator is an 8-bit register that holds operands and results of arithmetic calculations. It is not addressable. After an interrupt occurs, the Accumulator is auto-saved by hardware.

5.3.2 CONT (Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| – | INT | TSR2 | TSR1 | TSR0 | PSR2 | PSR1 | PSR0 |

Except for Bit 6 (Interrupt enable control bit), the CONT register can be read by the instruction "CONTR" and written to by the instruction "CONTW".

CONT [6] INT: An interrupt enable flag cannot be written by the CONTW instruction.

CONT [3~5] TSR0 ~ TSR2: TCC prescaler bits

CONT [0~2] PSR0 ~ PSR2: WDT prescaler bits



| PSR2 | PSR1 | PSR0 | TCC Rate (Base Freq: Fosc/2) | WDT Rate |
|------|------|------|------------------------------|----------|
| 0 | 0 | 0 | 1:2 | 1:1 |
| 0 | 0 | 1 | 1:4 | 1:2 |
| 0 | 1 | 0 | 1:8 | 1:4 |
| 0 | 1 | 1 | 1:16 | 1:8 |
| 1 | 0 | 0 | 1:32 | 1:16 |
| 1 | 0 | 1 | 1:64 | 1:32 |
| 1 | 1 | 0 | 1:128 | 1:64 |
| 1 | 1 | 1 | 1:256 | 1:128 |

5.3.3 IOC5 ~ IOC9 Port Direction Control Registers

These are I/O port (Port5 ~ Port9) direction control registers. Each bit controls the I/O direction of three I/O ports respectively. When these bits are set to 1, the relative I/O pins become input pins. Similarly, the I/O pins becomes output when the relative control bits are cleared.

0: Output direction

1: Input direction

5.3.4 IOCA (RFCNT: RF Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|---------|---------|---------|
| – | – | RF2 | RF1 | RF0 | RF_DBN2 | RF_DBN1 | RF_DBN0 |

IOCA [0~2] RF_DBN0 ~ RF_DBN2: These are used for defining debounce times in RF pattern detecting application.

IOCA [3~5] RF0 ~ RF2: RF Timing prescaler bits. Base on the MCU frequency.

| RF2 | RF1 | RF0 | Timing Rate | 8MHz System Clock (Time(Cnt.)) | 256kHz RC Mode (Time (Cnt.)) |
|-----|-----|-----|-------------|---|--|
| 0 | 0 | 0 | 1:1 | 0.125 μ s (1), 31.875 μ s (255) | 3.91 μ s (1), 996.1 μ s (255) |
| 0 | 0 | 1 | 1:2 | 0.25 μ s (1), 63.75 μ s (255) | 7.81 μ s (1), 1992 μ s (255) |
| 0 | 1 | 0 | 1:4 | 0.5 μ s (1), 127.5 μ s (255) | 15.625 μ s (1), 3984 μ s (255) |
| 0 | 1 | 1 | 1:8 | 1 μ s (1), 255 μ s (255) | 31.25 μ s (1), 7969 μ s (255) |
| 1 | 0 | 0 | 1:16 | 2 μ s (1), 510 μ s (255) | 62.5 μ s (1), 15.938 ms (255) |
| 1 | 0 | 1 | 1:32 | 4 μ s (1), 1020 μ s (255) | 125 μ s (1), 31.875 ms (255) |
| 1 | 1 | 0 | 1:64 | 8 μ s (1), 2040 μ s (255) | 250 μ s (1), 63.75 ms (255) |
| 1 | 1 | 1 | 1:128 | 16 μ s (1), 4080 μ s (255) | 500 μ s (1), 127.5 ms (255) |

5.3.5 IOCB (PWM_CNT: PWM Controller) Default (0b0000_0001)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|---------|---------|---------|
| PW2_E | PW1_E | – | – | – | PWM_SR2 | PWM_SR1 | PWM_SR0 |

IOCB [0~2] PWM_SR0 ~ PWM_SR2: PWM clock prescaler

Base on MCU frequency



| PWM_SR2 | PWM_SR1 | PWM_SR0 | Clock (Hz) |
|---------|---------|---------|------------|
| 0 | 0 | 0 | Fosc / 2 |
| 0 | 0 | 1 | Fosc / 4 |
| 0 | 1 | 0 | Fosc / 8 |
| 0 | 1 | 1 | Fosc / 16 |
| 1 | 0 | 0 | Fosc / 32 |
| 1 | 0 | 1 | Fosc / 64 |
| 1 | 1 | 0 | Fosc / 128 |
| 1 | 1 | 1 | Fosc / 256 |

IOCB [6] (PW1_E): PW1 Enable. The 1st PWM (P92) module enable bit.

0: Disable the PWM function of the 1st module

1: Enable the PWM function of the 1st module

IOCB [7] (PW2_E): PWM2 Enable: The 2nd PWM (P93) module enable bit.

0: Disable the PWM function of the 2nd module

1: Enable the PWM function of the 2nd module

5.3.6 IOCC (T1CON: Timer 1 Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | TM1E | TM1P1 | TM1P0 |

IOCC[0~1]: Timer 1 Prescaler bit

Timer 1 prescaler table for FOSC will be illustrated in the Section on Timer 1 in the subsequent pages.

IOCC[2]: Timer 1 Function Enable bit

0: Disable Timer 1 function as default

1: Enable Timer 1 function.

5.3.7 IOCD (Port 9 Pull-high Control Register) Default Value: (0B_1111_1111)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| /PH97 | /PH96 | /PH95 | /PH94 | /PH93 | /PH92 | /PH91 | /PH90 |

IOCD [0~6] /PH90 ~ /PH97: These bits control the 25KΩ pull-high resistor of the individual pins in Port 9. If the I/O port is set as output, the pull-high function is disabled.

0: Enable the pull-high function

1: Disable the pull-high function



5.3.8 IOCE (MCU Control Register) Default (0b1101_1111)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| S7 | /WUE | WTE | SLPC | /PU7 | /PU8 | /PU6 | /PU5 |

IOCE [0~3] /PU5~/PU8: Pull-high Control register. Default=1, Disable the pull high function. If the I/O port is set as output, the pull-high function is disabled.

0: Enable the pull-high function

1: Disable the pull-high function

IOCE [4] SLPC: This bit can be cleared by the firmware and set during power-on, or by the hardware at a falling edge of the wake-up signal. When this bit is cleared, the system clock is disabled and the MCU enters into Power down mode. At the transition of a wake-up signal from high to low, this bit is set to enable the system clock.

0: Sleep mode. The device is in power down mode.

1: Run mode. The device is working normally.

IOCE [5] WTE: Watchdog timer enable bit. WDT is disabled/enabled by the WTE bit.

0: Disable WDT

1: Enable WDT

IOCE [6] /WUE: Enable the wake-up function as triggered by a port change.

0: Enable the wake-up function

1: Disable the wake-up function

IOCE [7] S7 Bit: S7 defines the driving ability of P70-P72

0: Normal output

1: Enhance the driving ability of the LED

5.3.9 IOCF (Interrupt Mask Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|------------|--------|-----------|--------|--------|--------|--------|
| OUTEP_IE | P76/P77_IE | SPI_IE | Resume_IE | RF2_IE | RF1_IE | USB_IE | TCC_IE |

IOCF [0] TCC_IE: TCIF interrupt enable bit

0: Disable TCIF interrupt

1: Enable TCIF interrupt

IOCF [1] USB_IE: USB interrupt enable bit. Bits 1, 2, 3 of RF interrupt will be enabled while this bit is set.

0: Disable USB_IE interrupt

1: Enable USB_IE interrupt



IOCF [2] RF1_IE: RF1 pattern compare interrupt enable bit. Bits 0, 1 of the RE interrupt will be enabled while this bit is set.

0: Disable RF1_IE interrupt

1: Enable RF1_IE interrupt

IOCF [3] RF2_IE: RF2 pattern compare interrupt enable bit. Bits 2, 3 of the RE interrupt will be enabled while this bit is set.

0: Disable RF2_IE interrupt

1: Enable RF2_IE interrupt

IOCF [4] Resume_IE: USB Resume interrupt enable bit

0: Disable Resume_IE interrupt

1: Enable Resume_IE interrupt

IOCF [5] SPI & TM1 interrupt enable bit. Bits 4, 5 of the RE interrupt will be enabled while this bit is set.

0: disable SPI interrupt

1: enable SPI interrupt

IOCF [6] P76/P77_IE: P76/P77 port change interrupt enable bit. Bit 6, 7 of the RE interrupt will be enabled while this bit is set.

0: Disable P76/P77_IE interrupt

1: Enable P76/P77_IE interrupt

IOCF [7] OUTEP_IE: Output Endpoint interrupt enable bit

0: disable OUTEP_IE interrupt

1: enable OUTEP_IE interrupt

Only when the global interrupt is enabled by the ENI instruction will the individual interrupt work. After DISI instruction, any interrupt will not work even if the respective control bits of IOCF are set to 1.

The USB Host Resume Interrupt works only in Dual clock mode. This is because when the MCU is in sleep mode, it will be automatically woken up by the UDC Resume signal.

5.4 USB Device Controller

The USB Device Controller (UDC) built-in in the EM78680 can interpret the USB Standard Command and response automatically without involving firmware. The embedded Series Interface Engine (SIE) handles the serialization and de-serialization of actual USB transmission. Thus, a developer can concentrate his efforts more in perfecting the device actual functions and spend less energy in dealing with USB transaction.



The UDC handles and decodes most Standard USB commands defined in the USB Specification Rev 1.1. If the UDC receives an unsupported command, it will set a flag to notify the MCU the receipt of such command.

Each time the UDC receives a USB command, it writes the command into EP0's FIFO. Only when it receives unsupported command will the UDC notify the MCU through interrupt.

Therefore, the EM78680 is very flexible for USB applications since developers can freely choose the method of decoding the USB command as required by different situations.

5.5 Device Address and Endpoints

The EM78680 supports one device address and six endpoints, EP0 for control endpoint, EP1 ~ EP5 for interrupt/bulk /isochronous endpoints. Sending data to the USB host in EM78680 is very easy. Just write data into the EP's FIFO, then set the flag, and the UDC will handle the rest. It will then confirm that the USB host has received the correct data from the EM78680.

5.6 Reset

The EM78680 provides three types of reset: (1) Power-on Reset, (2) Watchdog Reset, and (3) USB Reset.

5.6.1 Power-on Reset

Power-on Reset occurs when the device is attached to power and a reset signal is initiated. The signal will last until the MCU becomes stable. After a Power-on Reset, the MCU enters the following predetermined states (see below), and then, it is ready to execute the program.

- a. The program counter is cleared.
- b. The TCC timer and Watchdog timer are cleared.
- c. Special registers and Special Control registers are all set to their initial value.

5.6.2 Watchdog Reset

When the Watchdog timer overflows, it causes the Watchdog to reset. After it resets, the program is executed from the beginning and some registers will be reset. The UDC however, remains unaffected.

5.6.3 USB Reset

When the UDC detects a USB Reset signal on the USB Bus, it interrupts the MCU, then proceeds to perform the specified process that follows. After a USB device is attached to the USB port, it cannot respond to any bus transactions until it receives a USB Reset signal from the bus.



5.7 Power Saving Mode

The EM78680 provides two options of power-saving modes for energy conservation, i.e., Power-down mode and Dual clock mode.

5.7.1 Power-down Mode

The EM78680 enters into Power Down mode by clearing the SLPC register (IOCE[4]). During this mode, the oscillator is turned off and the MCU goes to sleep. It will wake up when signal from USB host is resumed, or when the Watchdog resets or the input port state changes.

If the MCU wakes up when the I/O port status changes, the direction of the I/O port should be set to input direction, then read the port status.

For example:

```
:  
// Set the Port 6 to input port  
MOV      A , @0XFF  
IOW      PORT6  
// Read the status of Port 6  
MOV      PORT6, PORT6  
// Clear the RUN bit  
IOR      0XE  
AND      A , 0B11101111  
IOW      0XE  
:  
:
```

If the MCU is awakened by a USB Resume signal, the next instruction will be executed and one flag, IOCE[4] will be set to 1.

5.7.2 Dual Clock Mode

The EM78680 has one internal oscillator for power saving application. Clearing the Bit R12 [3] of ExteraRAM0 will enable the low frequency oscillator. At the same time, the external oscillator will be turned off. Then the MCU will run under very low frequency to conserve power. Four types of frequency are available for selection in setting Bits R12 [4, 5].

The USB Host Resume Interrupt can only be used in this mode. If this interrupt is enabled, the MCU will be interrupted when the USB Resume signal is detected on USB Bus.

5.8 Interrupt

The EM78680 has four Interrupt Vectors 0x0008, 0x0010, 0x0018, 0x0020. When an interrupt occurs during an MCU running program, it will jump to the interrupt vector and execute the instructions sequentially from the interrupt vector. RE and RF are the interrupt status registers.

The interrupt condition could be one of the following:

- Set 1 INT: (jump to 0x08)
- TCC overflow interrupt
- EP0 command in interrupt
- USB suspend interrupt
- USB reset interrupt
- USB HOST resume interrupt
- Set 2 INT: (jump to 0x10)
- RF1 low pattern interrupt
- RF1 high pattern interrupt
- RF2 low pattern interrupt
- RF2 high pattern interrupt
- Set 3 INT: (jump to 0x18)
- P77 port change interrupt
- P76 port change interrupt
- SPI Timer 1 comparator completed interrupt (Note1)
- SPI transmission completed interrupt (See Note).
- Set 4 INT: (jump to 0x20)
- EP5-8 output Endpoint received O.K interrupt

IOCF is an interrupt mask register which can be set bit by bit. While their respective bit is written to 0, the hardware interrupt will inhibit, that is, the EM78680 will not jump to the interrupt vector to execute instructions. But the interrupt status flags still records the conditions no matter whether the interrupt is masked or not. The interrupt status flags must be cleared by firmware before leaving the interrupt service routine and enabling interrupt.

The global interrupt is enabled by the ENI (RETI) instruction and is disabled by the DISI instruction.

Note: When employing this interrupt, user has to set the Code Option Bit 65 to "0".



5.9 Pattern Detect Application (PDA)

5.9.1 Function Description

This function is designed for the serial signal transmission, e.g., the transmission between a wireless device and its receiver box. The EM78680 has two sets of built-in Pattern Detect Application block that ensures the EM78680 is equipped with a compound device, such as the receiver box controller for a wireless keyboard, paired with a wireless mouse.

Pattern Detect Application (PDA) can calculate the length of one pattern and interrupt the MCU while the serial signal is transiting from high to low (or vice-versa). Then the MCU reads the length value from a specified register.

5.9.2 Control Register

The PDA includes two enable control bits, one control register and four length counter registers in 0x15 ~0x18 in ExtraRAM1.

5.9.2.1 IOCF [2~3] PDA Enable Control Bit

When this bit is set, the PDA function starts and the P92 and P93 automatically become input pin to sample the serial signal. (**Note:** Enabling these two bits also enables the interrupt mask of the PDA.)

0: Disable PDA function

1: Enable PDA function

5.9.2.2 IOCA (PDA Control Register) *Default Value: (0B_0000_0000)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| – | – | RF.2 | RF.1 | RF.0 | DB2 | DB1 | DB0 |

This register is used to define two parameters of the PDA function; signal sampling rate and debounce length. When a pattern ends, the value in the counter is loaded into its respective register and the RE[0~4] is set to indicate which channel and which type of pattern (high or low) is at its end or which type of pattern counter is on overflow.

0: low pattern

1: high pattern

5.9.2.3 R15 ExtraRAM1 (P.92 Low Pattern Counter)

This register records the length of P.92 in low status.

5.9.2.4 R16 ExtraRAM1 (P.92 High Pattern Counter)

This register records the length of P.92 in high status.

5.9.2.5 R17 ExtraRAM1 (P.93 Low Pattern Counter)

This register records the length of P.93 in low status



5.9.2.6 R18 ExtraRAM1 (P.93 High Pattern Counter)

This register records the length of P.93 in high status.

R15~R18 function as general registers if this function is not enabled. Once the enabled bit is set, these four registers will be loaded with the value of the pattern counter.

5.9.3 Sampling Rate and Debounce Length

The two pattern detect pins are separate, and each pin has its own pattern counter. Both pins use the same Sampling Rate and Debounce Length parameters.

The PDA samples the serial signal for every fixed interval. The pattern counter will be incremented by one at sampling time if the signal remains unchanged. If the signal is at high state, then the “high pattern counter” will be incremented, otherwise the “low pattern counter” is incremented. As long as the signal state changes, the PDA will debounce the signal and load the value of the pattern counter into the respective register for the firmware to read. For example, if the signal in P.92 is in “low” state, the low counter of P.92 will count continuously until the state of the input signal in P.92 changes. When a state change occurs (in this case, the signal changes from “low” to “high” state), the PDA will take a time break (which is equal to the result of the sampling interval multiplied by the debounce length), to avoid possible noise. After the debounce length time, if the signal remains in high state, the high pattern counter will start to count and load the low pattern counter’s value into R15 ExtraRAM1. At the same time, RE [0] is set to indicate that the low pattern is over.

The correlation between the control register value and debounce time are as follows:

| DB.2 | DB.1 | DB.0 | Debounce Time |
|------|------|------|-------------------|
| 0 | 0 | 0 | No Sampling clock |
| 0 | 0 | 1 | 1 Sampling clock |
| 0 | 1 | 0 | 2 Sampling clocks |
| 0 | 1 | 1 | 3 Sampling clocks |
| 1 | 0 | 0 | 4 Sampling clocks |
| 1 | 0 | 1 | 5 Sampling clocks |
| 1 | 1 | 0 | 6 Sampling clocks |
| 1 | 1 | 1 | 7 Sampling clocks |

Now consider another situation of this case, where the signal of P92 always stays “low”. The low pattern counter of P92 will eventually overflow. Once the counter overflows, the contents of the counter will also be loaded into R15, that is, the register is written to 0xFF, then the counter is reset to count from zero again.

If a PDA function hardware interrupt is enabled, (IOCF[2] is equal to “1”), then the program will go to 0x0010 to execute an interrupt routine while the contents of a pattern counter is loaded into the register.

The correlation between the value of control register and actual sampling rate are as shown below:

| RF2 | RF1 | RF0 | Timing Rate | 8MHz System Clock (Time(Cnt.)) | 256kHz RC Mode (Time (Cnt.)) |
|-----|-----|-----|-------------|---|---|
| 0 | 0 | 0 | 1:1 | 0.125 μ s (1), 31.875 μ s (255) | 3.91 μ s (1), 996.1 μ s (255) |
| 0 | 0 | 1 | 1:2 | 0.25 μ s (1), 63.75 μ s (255) | 7.81 μ s (1), 1992 μ s (255) |
| 0 | 1 | 0 | 1:4 | 0.5 μ s (1), 127.5 μ s (255) | 15.62 5 μ s (1), 3984 μ s (255) |
| 0 | 1 | 1 | 1:8 | 1 μ s (1), 255 μ s (255) | 31.25 μ s (1), 7969 μ s (255) |
| 1 | 0 | 0 | 1:16 | 2 μ s (1), 510 μ s (255) | 62.5 μ s (1), 15.938 ms (255) |
| 1 | 0 | 1 | 1:32 | 4 μ s (1), 1020 μ s (255) | 125 μ s (1), 31.875 ms (255) |
| 1 | 1 | 0 | 1:64 | 8 μ s (1), 2040 μ s (255) | 250 μ s (1), 63.75 ms (255) |
| 1 | 1 | 1 | 1:128 | 1 6 μ s (1), 4080 μ s (255) | 500 μ s (1), 127.5 ms (255) |

User can write a default value to the High Pattern counter register and Low Pattern counter register. Then set the corresponding interrupt enable bit (IOCF [2, 3]). When the counting value of one “H” pattern is bigger than the default value of R15_ExtraRAM1, a Pattern Detecting interrupt will be generated. Similarly, if the counting value of one “L” pattern is bigger than the default value of R16_ExtraRAM1, a Low Pattern Detecting interrupt will occur. Thus, the EM78680 is notified and aware that one effective pattern is received from P.92.

5.10 Pulse Width Modulation (PWM)

5.10.1 Function Description

In PWM mode, both PWM1 (P.92) and PWM2 (P.93) produce plus programmable signal of up to 8 bits resolution.

The PWM Period is defined as $0xFF \times \text{Timer Counter Clock}$. The Timer Counter clock source is controlled by the control register IOCB. For example; if the clock source is 1MHz, then the Period will be 255 μ s. $\text{Period} = 255 \times (1/\text{Timer Counter Clock})$. The PWM duty cycle is defined by writing to the R15/R16 Register of ExtraRAM0 for PWM1/ PWM2.

$$\text{Duty Cycle} = (\text{R15 of ExtraRAM0} / 255) \times 100\% \text{ for PWM1}$$

$$(\text{R16 of ExtraRAM0} / 255) \times 100\% \text{ for PWM2}$$

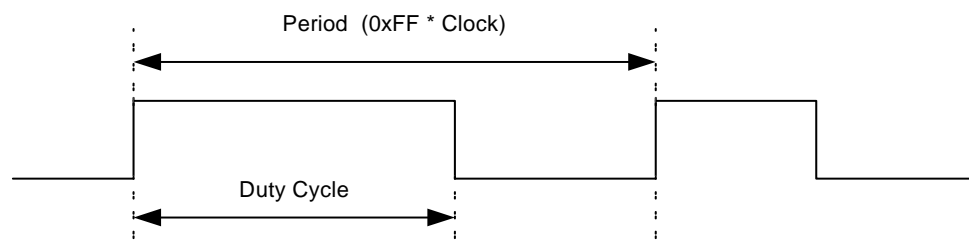


Figure 5-3 PWM Output Timing Diagram

5.10.2 Control Register

5.10.2.1 R15 of Extra RAM0 (PWM1 Duty Period Register)

Duty period setting of PWM1

5.10.2.2 R16 of Extra RAM0 (PWM2 Duty Period Register)

Duty period setting of PWM2

5.10.2.3 IOCB (PWM Control Register) *Default Value: (0B_0000_0001)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|---------|---------|---------|
| PW2_E | PW1_E | – | – | – | PWM_SR2 | PWM_SR1 | PWM_SR0 |

IOCB [0~2] PWM Clock Prescaler

Base on MCU frequency (ex: Fosc = 8 MHz)

| PWM_SR2 | PWM_SR1 | PWM_SR0 | Clock (Hz) | Period / 255 |
|---------|---------|---------|------------|--------------|
| 0 | 0 | 0 | Fosc / 2 | 0.25 μs |
| 0 | 0 | 1 | Fosc / 4 | 0.5 μs |
| 0 | 1 | 0 | Fosc / 8 | 1 μs |
| 0 | 1 | 1 | Fosc / 16 | 2 μs |
| 1 | 0 | 0 | Fosc / 32 | 4 μs |
| 1 | 0 | 1 | Fosc / 64 | 8 μs |
| 1 | 1 | 0 | Fosc / 128 | 16 μs |
| 1 | 1 | 1 | Fosc / 256 | 32 μs |

IOCB [6, 7] PWM1/PWM2 Enable Bit

“0”: Disable

“1”: Enable

5.11 Analog-To-Digital Converter (ADC)

5.11.1 Function Description

The Analog to Digital converter consists of a 5-bit analog multiplexer, one Control Register (R11_ExtraRAM0), and two data registers (R13_ExtraRAM0 ~ R14_ExtraRAM0) for a 10-bit resolution.

The ADC module utilizes successive approximation to convert the unknown analog signal to a digital value. The result is fed to the ADDATA. Input channels are selected by the analog input multiplexer via the ADCR/AD_Sel bits AD0~AD4.

- 10-bit resolution: 0x00-00~0xC0-FF (0b11000000-11111111)
- Start (0x00-00): $0 \text{ Vref} \sim (1/1024) * \text{Vref}$
- Full (0xC0-FF): $(1023/1024) * \text{Vref} \sim \text{Vref}$
- Conversion Time: 12 clock time of the internal clock source



5.11.2 Control Register

5.11.2.1 R11 (AD Channel Select Register0 Default Value: (0B_0001_1111))

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|
| AD_start | AD_R1 | AD_R0 | AD4 | AD3 | AD2 | AD1 | AD0 |

R11 [0~4]: AD Channel Selector

| AD4 | AD3 | AD2 | AD1 | AD0 | Channel | I/O Port |
|-----|-----|-----|-----|-----|---------|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | P50 |
| 0 | 0 | 0 | 0 | 1 | 1 | P51 |
| 0 | 0 | 0 | 1 | 0 | 2 | P52 |
| 0 | 0 | 0 | 1 | 1 | 3 | P53 |
| 0 | 0 | 1 | 0 | 0 | 4 | P54 |
| 0 | 0 | 1 | 0 | 1 | 5 | P55 |
| 0 | 0 | 1 | 1 | 0 | 6 | P56 |
| 0 | 0 | 1 | 1 | 1 | 7 | P57 |
| 0 | 1 | 0 | 0 | 0 | 8 | P80 |
| 0 | 1 | 0 | 0 | 1 | 9 | P81 |
| 0 | 1 | 0 | 1 | 0 | 10 | P82 |
| 0 | 1 | 0 | 1 | 1 | 11 | P83 |
| 0 | 1 | 1 | 0 | 0 | 12 | P84 |
| 0 | 1 | 1 | 0 | 1 | 13 | P85 |
| 0 | 1 | 1 | 1 | 0 | 14 | P86 |
| 0 | 1 | 1 | 1 | 1 | 15 | P87 |
| 1 | 0 | 0 | 0 | 0 | 16 | P60 |
| 1 | 0 | 0 | 0 | 1 | 17 | P61 |
| 1 | 0 | 0 | 1 | 0 | 18 | P62 |
| 1 | 0 | 0 | 1 | 1 | 19 | P63 |
| 1 | 0 | 1 | 0 | 0 | 20 | P64 |
| 1 | 0 | 1 | 0 | 1 | 21 | P65 |
| 1 | 0 | 1 | 1 | 0 | 22 | P66 |
| 1 | 0 | 1 | 1 | 1 | 23 | P67 |

R11 [5 6]: AD Conversion Clock Source

00: 256kHz

01: 128kHz

10: 64kHz

11: 32kHz

R11 [7] AD Converter Start Flag

0 → 1: Start AD Conversion (set by firmware)

1 → 0: When AD finishes converting and has moved the digital data into the AD Data Register, this bit will be reset by hardware.

NOTE

Hardware can enable this function only at the AD Channel Selector of the functional I/O port. After Power-on reset, the Initial Value of this Register is 0b0001 1111.

5.11.2.2 R13 (AD LSB Data Register) Default Value: (0B_0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 1 | Bit 0 | – | – | – | – | – | – |

AD Digital Data LSB 2 bits

5.11.2.3 R14 (AD MSB Data Register) Default Value: (0B_0000_0000)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 |

AD Digital Data MSB 8 bits

5.12 Serial Peripheral Interface Mode

5.12.1 Overview

Figures 5-4, 5-5, and 6-6 show how the EM78680 communicates with other devices through the SPI module. If the EM78680 is a master controller, it sends clock through the SCK pin. A couple of 8-bit multiple data are transmitted and received at the same time. However, if the EM78680 is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge.

5.12.2 Features

- Operation in either Master mode or Slave mode
- Full duplex, 3-wire or 4-wire synchronous communication
- Programmable baud rates of communication
- Programming clock polarity, (ExtraRAM1 R13 Bit 7)
- Interrupt flag available for the read buffer full
- Up to 8 Mbps (maximum baud rates)

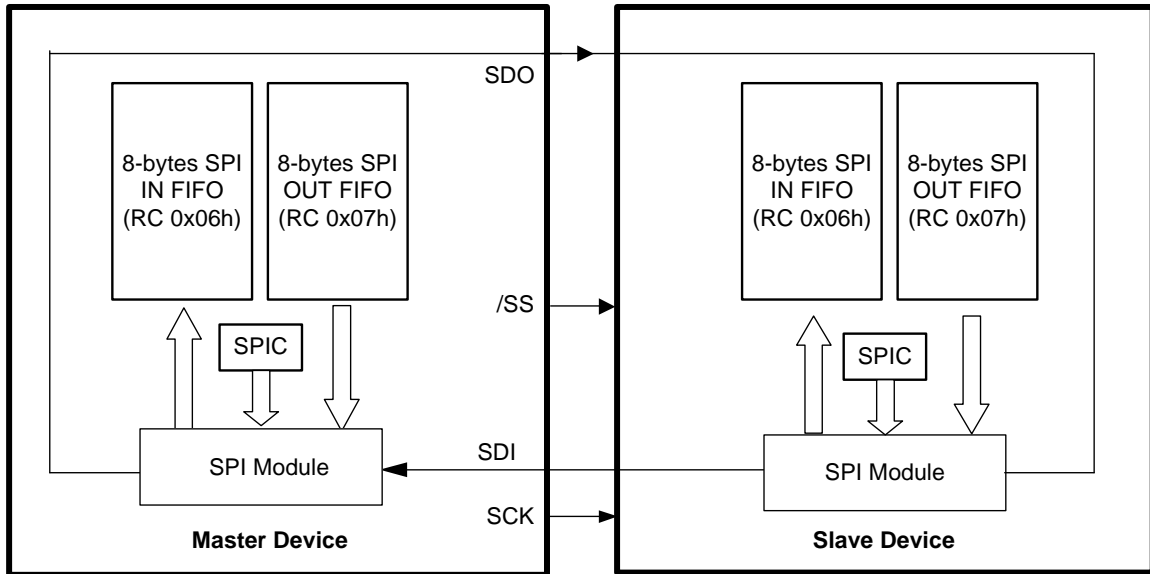


Figure 5-4 SPI Master/Slave Communication

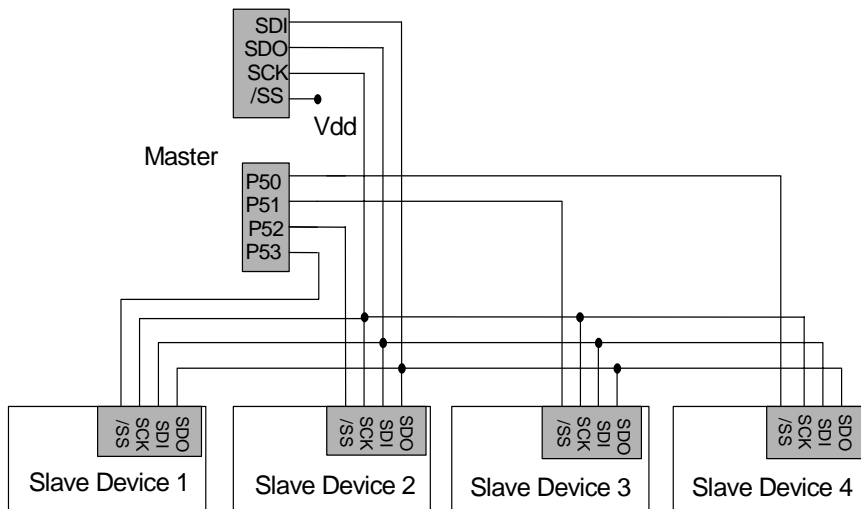


Figure 5-5 SPI Configuration of Single-Master and Multi-Slave

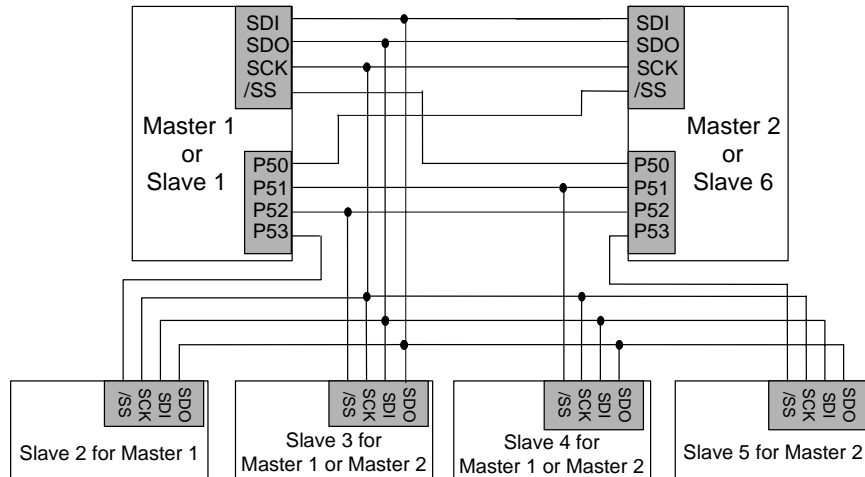


Figure 5-6 SPI Configuration of Single-Master and Multi-Slave

5.12.3 SPI Function Description

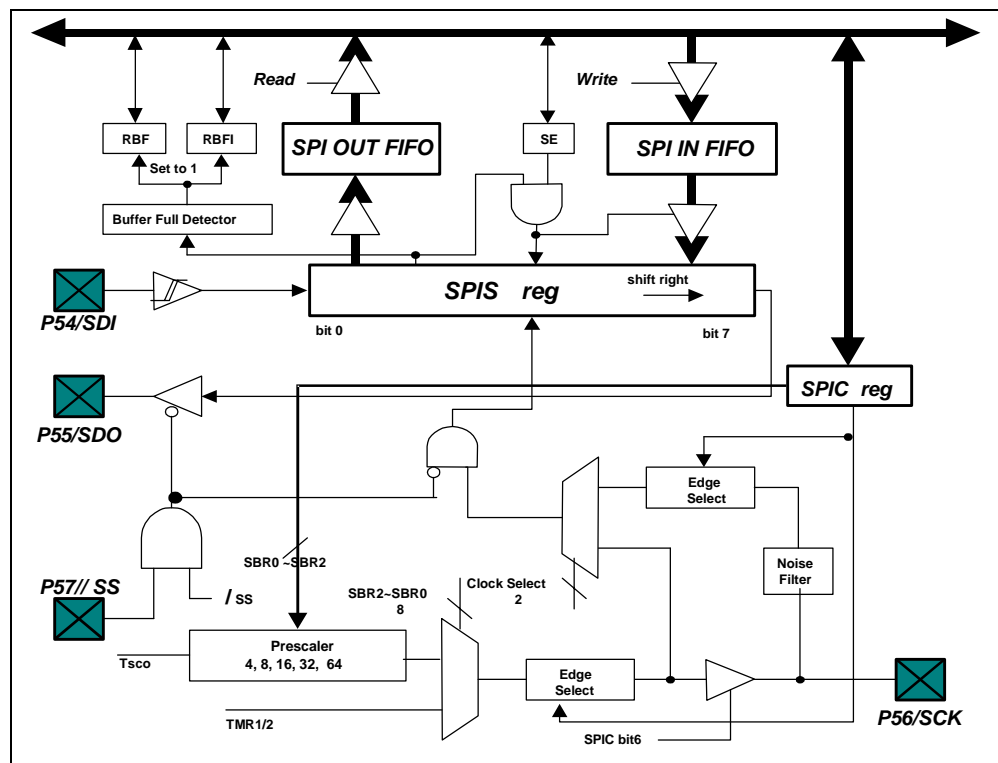


Figure 5-7 SPI Block Diagram

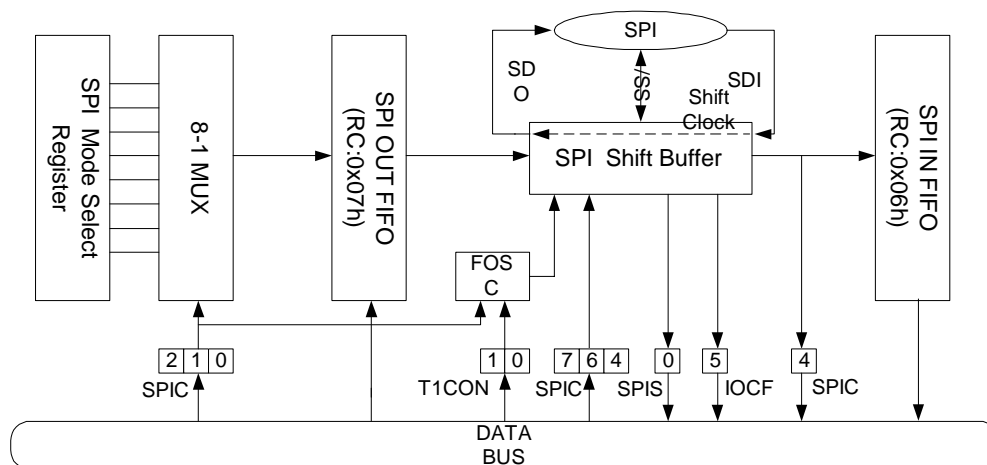


Figure 5-8 The Function Block Diagram of SPI Transmission

The following describes the function of each block and explains how to carry out the SPI communication with the signals depicted in Figure 5-7 and Figure 5-8:

P54/SDI: Serial Data In

P55/SDO: Serial Data Out

P56/SCK: Serial Clock

P57//SS: /Slave Select (Option). This pin (/SS) may be required during a slave mode.

RBF: Set by Buffer Full Detector, and reset by software.

RBFIF: Set by Buffer Full Detector, and reset by software.

SSE: Loads the data in SPIS register, and begin to shift.

SPIS reg.: Shifting byte in and out. The MSB is shifted first. Both the SPI IN FIFO data and the SPI OUT FIFO data are loaded at the same time. Once data are written, SPIS starts transmission / reception. The received data will be moved to the SPI IN FIFO register as the shifting of the 8-bytes data is completed. The RBF (Read Buffer Full) flag and the RBFIF (Read Buffer Full Interrupt) flag are then set.

SPI IN FIFO reg: Read buffer. The buffer will be updated as the 8-byte data shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPI IN FIFO data is read.

SPI OUT FIFO reg: Write buffer. The buffer will deny any attempt to write until the 8-bytes data shifting is completed.

The SSE bit will be kept at 1 if the communication is still undergoing. This flag must be cleared as the shifting is completed.

SBRS2~SBRS0: Programming the clock frequency/rates and sources.

Edge Select: Selecting the appropriate clock edges by programming the CES bit.

5.12.4 SPI Signal and Pin Description

The detailed functions of the four pins, SDI, SDO, SCK, and /SS, which are shown in Figure 5-5, are as follows:

SDI/P54:

- Serial Data In
- Receive serially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Defined as high-impedance, if not selected
- Program the same clock rate and clock edge to latch on both the master and slave devices
- The received byte will update the transmitted byte
- Both the RBF and RBFIF bits (ExtraRAM1 Register 0x12h) will be set as the SPI operation is completed.
- Timing is shown in Figure 5-9 and 5-10.

SDO/P55:

- Serial Data Out
- Transmit serially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Program the same clock rate and clock edge to latch on both the master and slave devices.
- The received byte will update the transmitted byte.
- The CES (ExtraRAM1 Register 0x13h) bit will be reset, as the SPI operation is completed.
- Timing is shown in Figure 5-9 and 5-10.

SCK/P56:

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SDI and SDO pins
- The CES (ExtraRAM1 Register 0x13h) is used to select the edge to communicate.
- The SBR0~SBR2 (ExtraRAM1 Register 0x13h) is used to determine the baud rate of communication.
- The CES, SBR0, SBR1, and SBR2 bits have no effect in the slave mode.
- Timing is shown in Figure 5-9 and 5-10.



/SS/P57:

- Slave Select ; negative logic
- Generated by a master device to signify the slave(s) to receive data.
- Goes low before the first cycle of SCK appears, and remains low until the last (8th) cycle is completed.
- Ignores the data on the SDI and SDO pins while /SS is high, because SDO is no longer driven.
- Timing is shown in Figures 5-9 and 5-10.

5.12.5 SPI Control Registers

As the SPI mode is defined, the related registers involved in this operation are shown in Table 2 and Table 3.

Table 2 Related Control Registers in SPI Mode

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-------|-------|--------|-------|-------|-------|-------|-------|
| 0x13 | SPIC/R13 | CES | SPIE | SRO | SSE | – | SBR2 | SBR1 | SBR0 |
| 0x0F | IOCF | – | – | SPI_IE | – | – | – | – | – |

SPIC: SPI Control Register.

CES (Bit 7): Clock Edge Select bit

0: Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during the low level.

1: Data shifts out on a falling edge, and shifts in on a rising edge. Data is on hold during the high level.

SPIE (Bit 6): SPI Enable bit

0: Disable SPI mode

1: Enable SPI mode

SRO (Bit 5): SPI Read Overflow bit

0: No overflow

1: A new data is received while the previous data is still being on hold in the SPIB register. Under this condition, the data in SPIS register will be destroyed. To avoid setting this bit, users should read the SPIRB (SPI Read Buffer) register even if the transmission is implemented only.

NOTE
This can only occur in slave mode.

SSE (Bit 4): SPI Shift Enable bit

0: Reset as soon as the shifting is completed and the next byte is ready to shift.

1: Start to shift, and stays on 1 while the current byte continues to transmit.

NOTE
This bit can be reset by hardware only.

SBRS (Bits 2~0): SPI Baud Rate Select Bits

| SBRS2 (Bit 2) | SBRS1 (Bit 1) | SBRS0 (Bit 0) | Mode | Baud Rate |
|---------------|---------------|---------------|--------|-------------|
| 0 | 0 | 0 | Master | Fosc/2 |
| 0 | 0 | 1 | Master | Fosc/4 |
| 0 | 1 | 0 | Master | Fosc/8 |
| 0 | 1 | 1 | Master | Fosc/16 |
| 1 | 0 | 0 | Master | Fosc/32 |
| 1 | 0 | 1 | Slave | /SS enable |
| 1 | 1 | 0 | Slave | /SS disable |
| 1 | 1 | 1 | Master | TMR1 / TMR2 |

NOTE

1. In master mode, disable /SS connection.
2. Do not select SRB2~0 as 0, 0, 0 when selecting FOSC as 24 MHz (Baud Rate = 12 MHz), since the SPI maximum baud rate is 8 MHz.

IOCF: Interrupt control register

Bit 5 (SPI_IE): SPI and TM1 interrupt enable bit

0: disable SPI and TM1 interrupt

1: enable SPI and TM1 interrupt

Table 3 Related Status/Data Registers in SPI Mode

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|----------|----------|-------|-------|-------|-------|-------|-------|
| SPIS (0x12) | Lstatus1 | Lstatus0 | M/LSB | – | OD3 | OD4 | – | RBF |

SPIS: SPI Status register

RBF (Bit 0): Read Buffer Full flag

0: Receive is ongoing, SPIB is empty

1: Receive is completed, SPIB is full.

RBFIF (Bit 1): Read Buffer Full Interrupt flag

0: Receive is ongoing, SPIB is empty.

1: Receive is completed, SPIB is full, and an interrupt occurs if enabled.

OD4 (Bit 2): Open Drain-Control bit (P94)

0: Open-drain disable for SCK.



1: Open-drain enable for SCK.

OD3 (Bit 3): Open-Drain Control bit (P93)

0: = Open-drain disable for SDO.

1: Open-drain enable for SDO.

M/LSB (Bit 5): The first bit of SPI Shift.

0: LSB

1: MSB

Lstatus (Bits 6~7):

00: The SDO will keep status after transfer over.

01: The SDO will pull-down after transfer over.

10: The SDO will pull-high after transfer over.

11: Not defined.

Table 4 R11 (SPI Byte Number Register)

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| SPIS(0x11) | - | SPIB3 | SPIB2 | SPIB1 | SPIB0 | - | - | - |

SPI byte counter. For setting SPI byte number. The SPI transfer and receive bytes are based on this register. Max byte number is 8 bytes.

NOTE
Code Option Bits 11~12

5.12.6 SPI Mode Timing

The SCK edge is selected by programming bit CES. The waveform shown in Figure 5-9 is applicable regardless whether the EM78680 is in master or slave mode with /SS disabled. However, the waveform in Figure 5-10 can only be implemented in slave mode with /SS enabled.

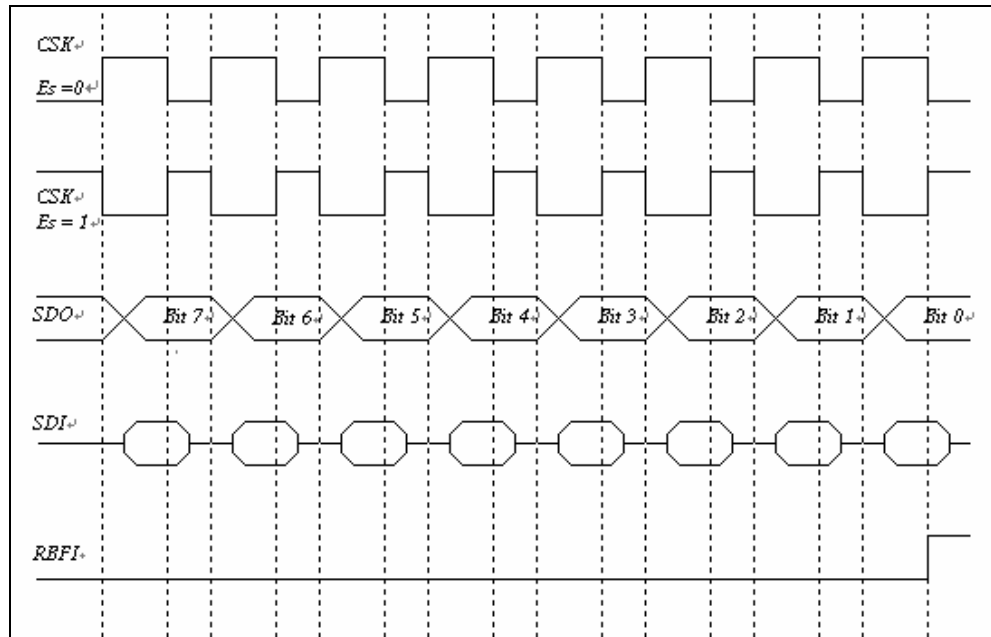


Figure 5-9 SPI Mode with /SS Disabled

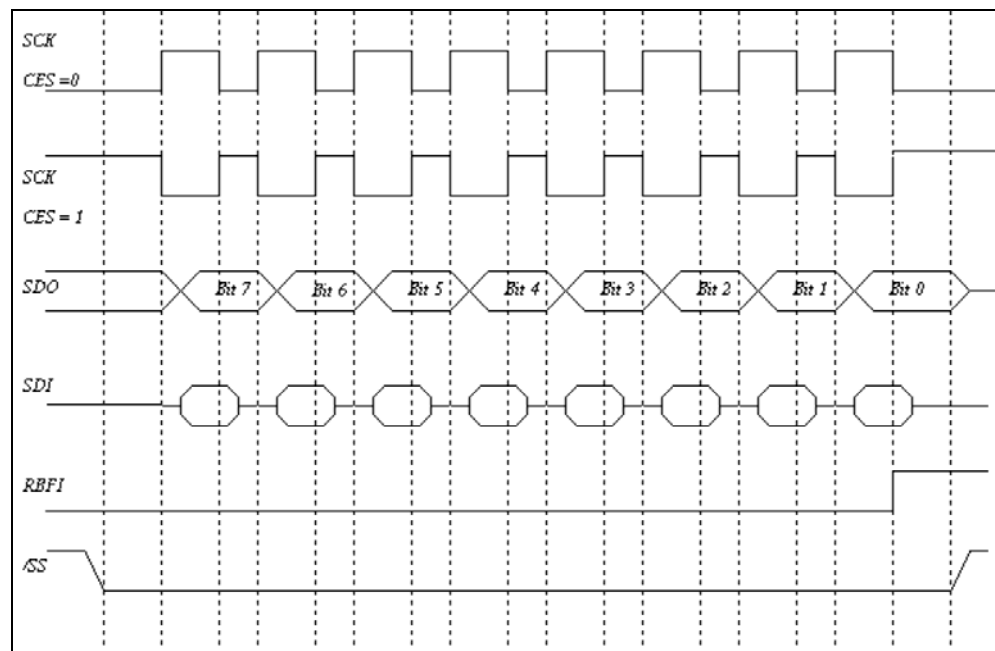


Figure 5-10 SPI Mode with /SS Enabled



Example for SPI:

For Master

```
ORG 0X00
JMP SETTING
ORG 0X0080
SETTING:
    DISI
    CLRA
    IOW 0X08          ; SET PORT 8 OUTPUT
    IOW 0X06          ; SET PORT 6 OUTPUT
    MOV 0X08,A
    MOV A,@0B01010000 ; DISABLE WAKE-UP FUNCTION, DISABLE WATCHDOG
    IOW 0X0E

    MOV A,@0B00000000 ; DISABLE INTERRUPT
    IOW 0X0F

    MOV A,@0X10          ; SDI INPUT AND SDO, SCK OUTPUT
    IOW 0X05

    BS 0XA,7
    MOV A,@0X18
    MOV 0X11, A          ; SET SPI 2 BYTES

    MOV A,@0X00          ; CLEAR RBF AND RBFIF FLAG; SDO KEEP STATUS, MSB
                          ; FIRST
    MOV 0X12,A

    MOV A,@0B11000010   ; SELECT CLOCK EDGE AND ENABLE SPI FUNCTION
    MOV 0X13,A
    BC 0XA,7
START:
    BS 0X0A, 7
    BC 0XE,4            ; CLEAR RBFIF FLAG
    MOV A,@0XFF
    MOV 0X08,A          ; SHOW A SIGNAL AT PORT 8
    MOV A,@0X06          ; POINT TO SPI IN FIFO
    MOV 0XC,A
    MOV A,@0XFF
    MOV 0XD,A          ; MOVE FF AT READ BUFFER

    MOV A,@0X07
    MOV 0XC,A
    MOV A,@0XAA          ; MOVE AA AT WRITE BUFFER
    MOV 0XD,A          ; WRITE 0XAA TO BYTE 0
    MOV 0XD,A          ; WRITE 0XAA TO BYTE 1
    COMA 0XD
    MOV 0XD,A          ; WRITE 0X55 TO BYTE 2
    MOV 0XD,A          ; WRITE 0X55 TO BYTE 3
    NOP
    BS 0X13,4          ; START TO SHIFT SPI DATA
    NOP
    JBC 0X13,4         ; POLLING LOOP FOR CHECKING SPI TRANSMISSION
                          ; COMPLETED
```



```
JMP $-2

BC 0X03,2
CALL DELAY          ; TO CATCH THE DATA FROM SLAVER
MOV A,@0X06
MOV 0XC,A
MOV A,0XD
XOR A,@0X5A        ; COMPARE THE DATA FROM SLAVER
JBS 0X03,2
JMP START
FLAG:
  MOV A,@0X55       ; SHOW 0X55 TO PORT 8 WHEN RECEIVING CORRECT DATA
                    ; FROM SLAVER

  MOV 0X08,A
  CALL DELAY
  JMP START

DELAY:
                    ; (USER'S PROGRAM)

  RET

EOP
ORG 0XFFF
JMP SETTING
```

For Slaver example:

```
ORG 0X0000
JMP START

ORG 0X0018
JMP INT_3_STATE
INT_3_STATE:
  DISI
  CLR RSR
  CLR STATUS
  JBC RE,4
  JMP SPI_INT_STATE
  RETI

SPI_INT_STATE:
  MOV A,@0X06
  MOV RC,A          ; SET SPI FIFO IN INDEX

  MOV A,RD
  MOV 0X19,A        ; READ SPI IN FIFO DATA

  MOV A,@0B00000010
  XOR PORT5,A       ; SPI INTERRUPT FINISH SIGNAL

  MOV A,@0B11101111
  MOV RE,A
  RETI

;=====
;INITIAL
;=====
```



```
INITIAL:
  CLR RSR
  CLRA
  IOW IOCF          ; DISABLE ALL INTERRUPT

  IOR IOCE
  OR A,@0B00000001
  IOW IOCE          ; DISABLE PORT 5 PULL-HIGH

  IOR IOCD
  AND A,@0B11110000
  IOW IOCD

  MOV A,@0B11111111 ; P9 TEST PIN; INPUT PULL HIGH
  IOW IOC9

  CLRA
  MOV PORT6,A
  MOV PORT8,A

  MOV A,@0XFF
  IOW IOC6
  IOR IOCE
  AND A,@0B11111101
  IOW IOCE

  BS RA,7          ; SET EXTRA RAM #1
  MOV A,@0B01000000
  MOV R11,A        ; SPI BYTE NUM = 1

  MOV A,@0B11010000
  IOW IOC5          ; SDI, /SS INPUT & SDO SCLK OUTPUT
  CLR PORT5

  CLR RE           ; CLR SPI AND TMIIF FLAG
  MOV A,@0B00000000 ; BIT5: 1 / 0 = MSB / LSB
  MOV R12,A        ; CLR RBFIF ,SET LSTUS = SAME ,MSB ,DISABLE OP DRAIN

  MOV A,@0B11000110 ; /SS DISABLE
  MOV R13,A        ; SET CES=1 ,SPI ENABLE ,SLAVE MODE WITH /SS
                  ; DISABLE

  BS R13,6

  BS PORT5,3
  MOV A,@0B00100000
  IOW IOCF          ; ENABLE SPI

  MOV A,@0X07      ; POINTER TO SPI OUT FIFO, FILL DATA
  MOV RC,A

  MOV A,@0X5A
  MOV RD,A
  RET
```



```
CLR_RAM:                                ; CLR 0X20~0X3F
    CLR 0X20
    MOV A,@0X1F
    MOV 0X20,A                          ; SET CLR COUNTER
    MOV A,@0XC0
    AND A,RSR
    OR A,@0X20
    MOV RSR,A                            ; SET RSR INDEX

    INC RSR
    CLR R0
    DJZ 0X20
    JMP $-3
    CLR RSR
    RET

;=====
;START
;=====
ORG 0X100
START:
    DISI
    CALL INITIAL
    CALL SET_INITIAL_VALUE
    BS R13,SSE
    ENI
    JMP MAIN

SET_INITIAL_VALUE:
    CLRA
    MOV R1C,A
    CLR RSR
    CALL CLR_RAM                        ; CLR BANK0 0X20~0X3F
    MOV A,@0X40
    MOV RSR,A
    CALL CLR_RAM                        ; CLR BANK1 0X20~0X3F
    MOV A,@0X08
    MOV 0X11,A                          ; SET SPI BYTE NUMBER REISTER
    RET

MAIN:
    WDTC
    BC PORT5,2
ROUTINE:
    WDTC
    JBC R13,SSE
    JMP $-2

                                ; DATA TRANSMISSION COMPLETE

    DISI
    BC PORT5,1
    BC PORT5,0

READLOOP:
    JBC R13,5
    JMP SLAVE_READ_OVERFLOW
    BS PORT5,0
    MOV A,0X19
```

```
XOR A,@0XAA
JBS STATUS,2
JMP ERROR
JMP NEXTTURN

ERROR:
BC R13,SSE
BC R13,6
DISI
BC PORT5,0
BS PORT5,1
JMP $

SLAVE_READ_OVERFLOW:
BC R13,6
DISI
BS PORT5,1
BC PORT5,1
JMP $-2

NEXTTURN:
NOP
BS RA,7 ; SET EXTRA RAM1
MOV A,@0B00001000 ;SET SPI BYTE NUMBER
MOV R11,A
CLR R1C

SLAVE_SEND_DATA:
MOV A,@0X07 ; SET SPI OUT FIFO DATA
MOV RC,A
MOV A,@0X5A
MOV RD,A
RET
BS R13,SSE
ENI
JMP MAIN
```

5.12.7 SPI Timer 1 Mode

5.12.7.1 Overview

Timer 1 (TMR1) is an 8-bit clock counter with a programmable prescaler. It is designed for the SPI module as a baud rate clock generator. TMR1 can be read and written to and cleared on any reset conditions. If employed, it can be turned-down for power conservation by setting TMR1EN Bit [T1CON<2>] to 0.

5.12.7.2 Function Description

Figure 5-11 shows Timer 1 block diagram. Each signal and block is described as follows:

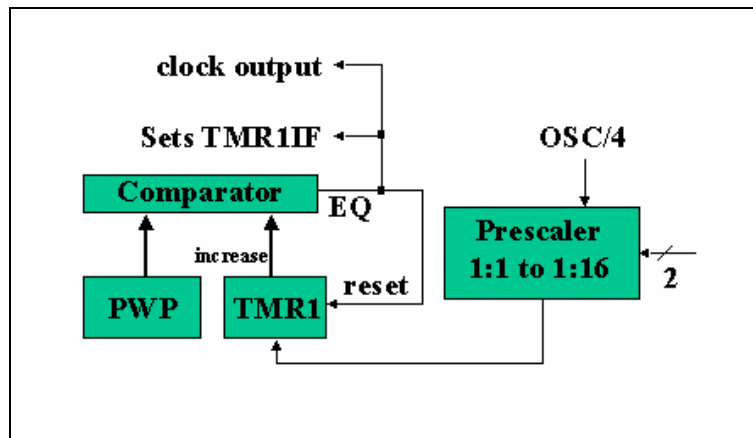


Figure 5-11 Timer 1 Block Diagram

OSC/4: Input clock

Prescaler: Option of 1:4, 1:16, 1:32, and 1:64 defined by T1P1 and T1P02 (T1CON<1, 0>). It is cleared when a value is written to TMR1 or T1CON, and during any kind of reset as well.

PWP: Pulse width preset register. The desired width of baud clock is written in advance.

TMR1: Timer 1 register. TMR1 increases until it matches with PWP, and then resets to 0. If it is chosen optionally in the SPI mode, its output is fed as a shifting clock.

Comparator: To change the output status while a match occurs. The TMR1IF flag will be set at the same time.

5.12.7.3 Programmed the Related Registers

The related registers of the defining TMR1 operation are shown in Table 5 and Table 6.

Table 5 TMR1Related Control Registers

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------|----------|----------|-------------|-------|----------|---------|----------|---------|
| 0x0F | IOCF | | | TMR1E/SPIIE | | | | | |
| 0x12 | SPIS | Lstatus1 | Lstatus0 | M/LSB | - | OD3 | OD4 | - | RBF |
| 0x0E | ISR | P77_IF | P76_IF | TM1IF | SPIIF | RF_2High | RF_2Low | RF_1High | RF_1Low |

Table 6 TMR1Related Status/Data Registers

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0x14 | TMR1 | TMR17 | TMR16 | TMR15 | TMR14 | TMR13 | TMR12 | TMR11 | TMR10 |
| 0x10 | PWP | PWP7 | PWP6 | PWP5 | PWP4 | PWP3 | PWP2 | PWP1 | PWP0 |
| 0x0C | T1CON | 0 | 0 | 0 | 0 | 0 | TM1E | TM1P1 | TM1P0 |

TMR1: Timer 1 Register

TMR17~TMR10 bits are set of Timer 1 registers and it increases until the value matches PWP and then it reset to 0.



PWP: Pulse Width Preset Register

PWP7~PWP0 bits are set of pulse width preset in advance for the desired width of baud clock.

T1CON: Timer 1 Control Register

TM1E (Bit 2): Timer 1 enable bit

TM1P1 and TM1P0 (Bits 1~0): Timer 1 prescaler for FSCO

| TM1P1 | TM1P0 | Prescaler Rate |
|-------|-------|----------------|
| 0 | 0 | 1:4 |
| 0 | 1 | 1:16 |
| 1 | 0 | 1:32 |
| 1 | 1 | 1:64 |

6 Absolute Maximum Ratings

| Items | Min | Max | Unit |
|------------------------|------|-----|------|
| Temperature under bias | 0 | 70 | °C |
| Storage temperature | -65 | 150 | °C |
| Input voltage | -0.5 | 6.0 | V |
| Output voltage | -0.5 | 6.0 | V |

7 DC Electrical Characteristic

Ta=25°C, VDD=5V, VSS=0V

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|--|--|------|-----|------|------|
| VDD | Operating voltage | Operation condition Fosc= 8,16MHz | 4.0 | 5.0 | 5.25 | V |
| | | Fosc=24MHz | 5.0 | 5.0 | 5.25 | V |
| IIL | Input Leakage Current | VIN = VDD, VSS | - | - | ±1 | μA |
| VIH | Input High Voltage | - | 2.0 | - | - | V |
| VIL | Input Low Voltage | - | - | - | 0.8 | V |
| VIHX | Clock Input High Voltage | OSCI | 2.5 | - | - | V |
| VILX | Clock Input Low Voltage | OSCI | - | - | 1.0 | V |
| VOH1 | Output High Voltage (P70~P72, P76~P77) | IOH = 10.0mA VDD = 5 V | 2.4 | - | - | V |
| VOH2 | Output High Voltage (Ports 5, 6, 8, 9) | IOH = 1.0mA Vreg = 3.3 V | 2.4 | - | - | V |
| VOL1 | Output Low Voltage (P70~P72, P76~77) | IOL = -10.0mA VDD = 5 V | - | - | 0.4 | V |
| VOL2 | Output Low Voltage (P70~P72 : LED drive mode) | IOL = -10.0mA VDD = 5 V | - | - | 3.0 | V |
| VOL3 | Output Low Voltage (Ports 5, 6, 8, 9) | IOL = -10.0mA Vreg = 3.3 V | - | - | 0.4 | V |
| IPH1 | Pull-high current (Ports 5, 6, 7, 8, 9) | Pull-high active, Input pin at VSS Vreg=3.3V | -20% | 132 | +20% | μA |
| IPH2 | Pull-high current (P70~P72, P76~77) | Pull-high active, Input pin at VSS VDD = 5 V | -20% | 132 | +20% | μA |
| IPH3 | Pull-high current (USB D+) | Pull-high active, Input pin at VSS Vreg=3.3V (PH rsister =1.5K) | - | 2.2 | - | mA |
| ICC1 | Operating supply current Normal operation | Fosc= 8MHz , no GPIO loading | - | - | 10 | mA |
| ICC2 | Operating supply current Sleep mode | All input and I/O pin at VDD Output pin floating, WDT disabled | - | - | 300 | μA |
| ICC3 | Operating supply current Dual clock mode – 256kHz | All input and I/O pin at VDD Output pin floating, WDT disabled | - | - | 250 | μA |
| Vreg | Output voltage of 3.3V regulator | VDD = 4.0V ~ 5.25V | 3.0 | 3.3 | 3.6 | V |

APPENDIX

A Special Register Map

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------------|-------------------------|-------|-------|-------|-------|-------|--------|--------|--------|
| N/A | IOC5 | Bit Name | C57 | C56 | C55 | C54 | C53 | C52 | C51 | C50 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| N/A | IOC6 | Bit Name | C67 | C66 | C65 | C64 | C63 | C62 | C61 | C60 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| N/A | IOC7 | Bit Name | C77 | C76 | - | - | - | C72 | C71 | C70 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| N/A | IOC8 | Bit Name | C87 | C86 | C85 | C84 | C83 | C82 | C81 | C80 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| N/A | IOC9 | Bit Name | C97 | C96 | C95 | C94 | C93 | C92 | C91 | C90 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | IOCA (RFCNT) | Bit Name | - | - | RF2 | RF1 | RF0 | RF_DB2 | RF_DB1 | RF_DB0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0B | IOCB (PWM_CNT) | Bit Name | PW2_E | PW1_E | - | -- | - | PWM_2 | PWM_1 | PWM_0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |



| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------------|-------------------------|-------|-------|-------|--------|-------|-------|-------|-------|
| 0x0C | IOCC (T1CON) | Bit Name | GPB | GPB | GPB | GPB | GPB | T1E | T1P1 | T1P0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0D | IOCD (P9_PH) | Bit Name | - | /PH96 | /PH95 | - | /PH93 | /PH92 | /PH91 | /PH90 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0E | IOCE (MCU Cnt) | Bit Name | S7 | /WUE | WTE | SLPC | - | /PU8 | /PU6 | /PU5 |
| | | Power-on | 1 | 1 | 0 | 1 | U | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 0 | 1 | U | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | 1 | U | P | P | P |
| 0x0F | IOCF | Bit Name | OUTEP | P7IE | SPIIE | ResulE | RF2IE | RF1IE | USBIE | TCIE |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| N/A | CONT | Bit Name | - | INT | TSR2 | TSR1 | TSR0 | PSR2 | PSR1 | PSR0 |
| | | Power-on | U | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | U | P | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | U | P | P | P | P | P | P | P |
| 0x00 | R0(IAR) | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x01 | R1(TCC) | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x02 | R2(PC) | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | **P | **P | **P | **P | **P | **P | **P | **P |



| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|-------------------------|-------|--------|-------|-------|--------|--------|-------|-------|
| 0x03 | R3 (SR) | Bit Name | PS2 | PS1 | PS0 | T | P | Z | DC | C |
| | | Power-on | 0 | 0 | 0 | t | t | U | U | U |
| | | /RESET and WDT | 0 | 0 | 0 | t | t | P | P | P |
| | | Wake-up from Pin Change | P | P | P | t | t | P | P | P |
| 0x04 | R4 (RSR) | Bit Name | RSR.1 | RSR.0 | - | - | - | - | - | - |
| | | Power-on | 0 | 0 | U | U | U | U | U | U |
| | | /RESET and WDT | 0 | 0 | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x05 | R5 (P5) | Bit Name | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x06 | R6 (P6) | Bit Name | P67 | P66 | P65 | P64 | P63 | P62 | P61 | P60 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x07 | R7 (P7) | Bit Name | P77 | P76 | - | - | - | P72 | P71 | P70 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | R8 (P8) | Bit Name | P87 | P86 | P85 | P84 | P83 | P82 | P81 | P80 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x09 | R9 (P9) | Bit Name | P97 | P96 | P95 | P94 | P93 | P92 | P91 | P90 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | RA(USBES) | Bit Name | Ext_R | Remote | EPO_W | EPO_R | D_Resu | UDC_Su | UDC_w | STALL |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |



| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------------|-------------------------|---------|--------|--------|---------|---------|---------|--------|--------|
| 0x0B | GPR | Bit Name | GPB | GPB | GPB | GPB | GPB | GPB | GPB | GPB |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0C | RC (FIFO_Index) | Bit Name | Index7 | Index6 | Index5 | Index4 | Index3 | Index2 | Index1 | Index0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0D | RD (FIFO_Data) | Bit Name | FIFO7 | FIFO6 | FIFO5 | FIFO4 | FIFO3 | FIFO2 | FIFO1 | FIFO0 |
| | | Power-un | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0E | RE (ISR0) | Bit Name | P77_IF | P76_IF | TM1IF | SPIIF- | RF2_H | RF2_L | RF1_H | RF1_L |
| | | Power-un | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0F | RF (ISR0) | Bit Name | Out_EP | GPB | GPB | ResumIF | USBres | Suspend | EP0_IF | TCCIF |
| | | Power-un | 0 | U | U | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | P | P | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x10 | R10 (USB EP stat) | Bit Name | GPB | GPB | GPB | EP5_ST | EP4_ST | EP3_ST | EP2_ST | EP1_ST |
| | | Power-on | U | U | U | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | P | P | P | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x11 | R11 (AD/Control) | Bit Name | ADstart | AD_R1 | AD_R0 | AD4 | AD3 | AD2 | AD1 | AD0 |
| | | Power-on | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x12 | R12 (Dual) | Bit Name | -- | USB_To | Low_F1 | Low_F0 | /LowFre | - | - | - |
| | | Power-on | U | U | 0 | 0 | 1 | U | U | U |
| | | /RESET and WDT | P | U | 0 | 0 | 1 | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |



| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------------------|-------------------------|----------|----------|-------|-------|-------|-------|-------|-------|
| 0x13 | R13 (ADLoData) | Bit Name | ADD1 | ADD0 | - | - | - | - | - | - |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x14 | R14 (ADHiData) | Bit Name | ADD9 | ADD8 | ADD7 | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x15 | R15 (PWM1_T) | Bit Name | PWM17 | PWM16 | PWM15 | PWM14 | PWM13 | PWM12 | PWM11 | PWM10 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x16 | R16 (PWM2_T) | Bit Name | PWM27 | PWM26 | PWM25 | PWM24 | PWM23 | PWM22 | PWM21 | PWM20 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x17~0x3F | GPR | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x10 | R10 (PWP) | Bit Name | PWP7 | PWP6 | PWP5 | PWP4 | PWP3 | PWP2 | PWP1 | PWP0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x11 | R11 (SPIN) | Bit Name | GPB | SPI7 | SPI6 | SPI5 | SPI4 | GPB | GPB | GPB |
| | | Power-on | U | 0 | 0 | 0 | 0 | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x12 | R12 (SPIS) | Bit Name | Lstatus1 | Lstatus0 | M/LSB | GPB | OD3 | OD4 | GPB | RBF |
| | | Power-on | 0 | 0 | 0 | U | 0 | 0 | U | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | P | 0 | 0 | P | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |



| Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Name |
|-----------|-------------------|-------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0x13 | R13 (SPIC) | Bit Name | CES | SPIE | SRO | SPISE | GPB | SBRS2 | SBRS1 | SBRS0 |
| | | Power-on | 0 | 0 | 0 | 0 | U | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | P | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x14 | R14 (TMR1) | Bit Name | TMR17 | TRM16 | TRM15 | TRM14 | TRM13 | TRM12 | TRM11 | TRM10 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x15 | R15 (SE1_LOW) | Bit Name | SE1_L7 | SE1_L6 | SE1_L5 | SE1_L4 | SE1_L3 | SE1_L2 | SE1_L1 | SE1_L0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x16 | R16 (SE1_HIGH) | Bit Name | SE1_H7 | SE1_H6 | SE1_H5 | SE1_H4 | SE1_H3 | SE1_H2 | SE1_H1 | SE1_H0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x17 | R17 (SE2_LOW) | Bit Name | SE2_L7 | SE2_L6 | SE2_L5 | SE2_L4 | SE2_L3 | SE2_L2 | SE2_L1 | SE2_L0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x18 | R18 (SE2_HIGH) | Bit Name | SE2_H7 | SE2_H6 | SE2_H5 | SE2_H4 | SE2_H3 | SE2_H2 | SE2_H1 | SE2_H0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x19-0x3F | GPR | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

** Execute the next instruction after the "SLPC" bit status of IOCE register has been on high-to-low transition.

X: Not for use. **U:** Unknown or don't care. **P:** Previous value before reset.



B Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consisting of 2 oscillator periods), unless the program counter is changed by-

- (a) Executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any other instructions that write to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ...).
- (b) Execute CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) which were tested to be true.

Under these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

- (1). Every bit of any register can be set, cleared, or tested directly.
- (2). The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

Legend:

R = Register designator that specifies which one of the 64 registers (including operation and general purpose registers) is to be utilized by the instruction.

Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

| Binary Instruction | Hex | Mnemonic | Operation | Status Affected |
|--------------------|------|----------|---------------------------------------|---------------------------|
| 0 0000 0000 0000 | 0000 | NOP | No Operation | None |
| 0 0000 0000 0001 | 0001 | DAA | Decimal Adjust A | C |
| 0 0000 0000 0010 | 0002 | CONTW | A → CONT | None |
| 0 0000 0000 0011 | 0003 | SLEP | 0 → WDT, Stop oscillator | T, P |
| 0 0000 0000 0100 | 0004 | WDTC | 0 → WDT | T, P |
| 0 0000 0000 rrrr | 000r | IOW R | A → IOCR | None <Note ¹ > |
| 0 0000 0001 0000 | 0010 | ENI | Enable Interrupt | None |
| 0 0000 0001 0001 | 0011 | DISI | Disable Interrupt | None |
| 0 0000 0001 0010 | 0012 | RET | [Top of Stack] → PC | None |
| 0 0000 0001 0011 | 0013 | RETI | [Top of Stack] → PC, Enable Interrupt | None |
| 0 0000 0001 0100 | 0014 | CONTR | CONT → A | None |
| 0 0000 0001 rrrr | 001r | IOR R | IOCR → A | None <Note ¹ > |
| 0 0000 0010 0000 | 0020 | TBL | R2+A → R2, Bits 8~9 of R2 unchanged | Z, C, DC |



| Binary Instruction | Hex | Mnemonic | Operation | Status Affected |
|--------------------|------|----------|--|-----------------|
| 0 0000 01rr rrrr | 00rr | MOV R,A | $A \rightarrow R$ | None |
| 0 0000 1000 0000 | 0080 | CLRA | $0 \rightarrow A$ | Z |
| 0 0000 11rr rrrr | 00rr | CLR R | $0 \rightarrow R$ | Z |
| 0 0001 00rr rrrr | 01rr | SUB A,R | $R-A \rightarrow A$ | Z, C, DC |
| 0 0001 01rr rrrr | 01rr | SUB R,A | $R-A \rightarrow R$ | Z, C, DC |
| 0 0001 10rr rrrr | 01rr | DECA R | $R-1 \rightarrow A$ | Z |
| 0 0001 11rr rrrr | 01rr | DEC R | $R-1 \rightarrow R$ | Z |
| 0 0010 00rr rrrr | 02rr | OR A,R | $A \vee VR \rightarrow A$ | Z |
| 0 0010 01rr rrrr | 02rr | OR R,A | $A \vee VR \rightarrow R$ | Z |
| 0 0010 10rr rrrr | 02rr | AND A,R | $A \& R \rightarrow A$ | Z |
| 0 0010 11rr rrrr | 02rr | AND R,A | $A \& R \rightarrow R$ | Z |
| 0 0011 00rr rrrr | 03rr | XOR A,R | $A \oplus R \rightarrow A$ | Z |
| 0 0011 01rr rrrr | 03rr | XOR R,A | $A \oplus R \rightarrow R$ | Z |
| 0 0011 10rr rrrr | 03rr | ADD A,R | $A + R \rightarrow A$ | Z, C, DC |
| 0 0011 11rr rrrr | 03rr | ADD R,A | $A + R \rightarrow R$ | Z, C, DC |
| 0 0100 00rr rrrr | 04rr | MOV A,R | $R \rightarrow A$ | Z |
| 0 0100 01rr rrrr | 04rr | MOV R,R | $R \rightarrow R$ | Z |
| 0 0100 10rr rrrr | 04rr | COMA R | $/R \rightarrow A$ | Z |
| 0 0100 11rr rrrr | 04rr | COM R | $/R \rightarrow R$ | Z |
| 0 0101 00rr rrrr | 05rr | INCA R | $R+1 \rightarrow A$ | Z |
| 0 0101 01rr rrrr | 05rr | INC R | $R+1 \rightarrow R$ | Z |
| 0 0101 10rr rrrr | 05rr | DJZA R | $R-1 \rightarrow A$, skip if zero | None |
| 0 0101 11rr rrrr | 05rr | DJZ R | $R-1 \rightarrow R$, skip if zero | None |
| 0 0110 00rr rrrr | 06rr | RRCA R | $R(n) \rightarrow A(n-1)$, $R(0) \rightarrow C$, $C \rightarrow A(7)$ | C |
| 0 0110 01rr rrrr | 06rr | RRC R | $R(n) \rightarrow R(n-1)$, $R(0) \rightarrow C$, $C \rightarrow R(7)$ | C |
| 0 0110 10rr rrrr | 06rr | RLCA R | $R(n) \rightarrow A(n+1)$, $R(7) \rightarrow C$, $C \rightarrow A(0)$ | C |
| 0 0110 11rr rrrr | 06rr | RLC R | $R(n) \rightarrow R(n+1)$, $R(7) \rightarrow C$, $C \rightarrow R(0)$ | C |
| 0 0111 00rr rrrr | 07rr | SWAPA R | $R(0-3) \rightarrow A(4-7)$, $R(4-7) \rightarrow A(0-3)$ | None |
| 0 0111 01rr rrrr | 07rr | SWAP R | $R(0-3) \leftrightarrow R(4-7)$ | None |
| 0 0111 10rr rrrr | 07rr | JZA R | $R+1 \rightarrow A$, skip if zero | None |
| 0 0111 11rr rrrr | 07rr | JZ R | $R+1 \rightarrow R$, skip if zero | None |



| Binary Instruction | Hex | Mnemonic | Operation | Status Affected |
|--------------------|------|----------|--|---------------------------|
| 0 100b brrr rrrr | 0xxx | BC R,b | $0 \rightarrow R(b)$ | None <Note ² > |
| 0 101b brrr rrrr | 0xxx | BS R,b | $1 \rightarrow R(b)$ | None |
| 0 110b brrr rrrr | 0xxx | JBC R,b | if $R(b)=0$, skip | None |
| 0 111b brrr rrrr | 0xxx | JBS R,b | if $R(b)=1$, skip | None |
| 1 00kk kkkk kkkk | 1kkk | CALL k | PC+1 \rightarrow [SP], (Page, k) \rightarrow PC | None |
| 1 01kk kkkk kkkk | 1kkk | JMP k | (Page, k) \rightarrow PC | None |
| 1 1000 kkkk kkkk | 18kk | MOV A,k | $k \rightarrow A$ | None |
| 1 1001 kkkk kkkk | 19kk | OR A,k | $A \vee k \rightarrow A$ | Z |
| 1 1010 kkkk kkkk | 1Akk | AND A,k | $A \& k \rightarrow A$ | Z |
| 1 1011 kkkk kkkk | 1Bkk | XOR A,k | $A \oplus k \rightarrow A$ | Z |
| 1 1100 kkkk kkkk | 1Ckk | RETL k | $k \rightarrow A$, [Top of Stack] \rightarrow PC | None |
| 1 1101 kkkk kkkk | 1Dkk | SUB A,k | $k-A \rightarrow A$ | Z, C, DC |
| 1 1110 0000 0kkk | 1E0k | | | None |
| 1 1111 kkkk kkkk | 1Fkk | ADD A,k | $k+A \rightarrow A$ | Z, C, DC |

Note: ¹ This instruction is applicable to IOCx only.

² This instruction is not recommended for RE, RF operation.

C Code Option

■ Address 000:

| Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|----------|-------|-------|-------|-------|-------|-------|-------|--------------|-------|----------|
| DEL1 | DEL0 | /AD_hold | - | PKG_1 | PKG_0 | FRQ_1 | FRQ_0 | OST_1 | OST_0 | /D+ resistor | USB | /Protect |

■ Address 001:

| Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 |
|---------------|---------------|---------------|-----------|-----------|---------------|---------------|---------------|-----------|-----------|----------|----------|----------|
| EP2_Max_Size1 | EP2_Max_Size0 | EP2_Direction | EP2_Type1 | EP2_Type0 | EP1_Max_Size1 | EP1_Max_Size0 | EP1_Direction | EP1_Type1 | EP1_Type0 | EPX_SEL2 | EPX_SEL1 | EPX_SEL0 |

■ Address 002:

| Bit 38 | Bit 37 | Bit 36 | Bit 35 | Bit 34 | Bit 33 | Bit 32 | Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 |
|---------------|-----------|-----------|---------------|---------------|---------------|-----------|-----------|---------------|---------------|---------------|-----------|-----------|
| EP5_Direction | EP5_Type1 | EP5_Type0 | EP4_Max_Size1 | EP4_Max_Size0 | EP4_Direction | EP4_Type1 | EP4_Type0 | EP3_Max_Size1 | EP3_Max_Size0 | EP3_Direction | EP3_Type1 | EP3_Type0 |

■ Address 003:

| Bit 51 | Bit 50 | Bit 49 | Bit 48 | Bit 47 | Bit 46 | Bit 45 | Bit 44 | Bit 43 | Bit 42 | Bit 41 | Bit 40 | Bit 39 |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|--------|--------|---------------|---------------|
| USER_ID8 | USER_ID7 | USER_ID6 | USER_ID5 | USER_ID4 | USER_ID3 | USER_ID2 | USER_ID1 | USER_ID0 | -- | -- | EP5_Max_Size1 | EP5_Max_Size0 |

■ **Address 004:**

| Bit 64 | Bit 63 | Bit 62 | Bit 61 | Bit 60 | Bit 59 | Bit 58 | Bit 57 | Bit 56 | Bit 55 | Bit 54 | Bit 53 | Bit 52 |
|--------|-------------------|-------------------|-------------------|-------------------|----------------|----------------|----------------|----------------|---------------|---------------|-----------|----------|
| -- | QTP_ Code 3 | QTP_ Code 2 | QTP_ Code 1 | QTP_ Code 0 | USER_ _ID16 | USER_ _ID15 | USER_ _ID14 | USER_ _ID13 | USER_I D12 | USER_I D11 | USER_ID10 | USER_ID9 |

■ **Address 005:**

| Bit 66~75 | Bit 65 |
|-----------|----------|
| -- | /Ver_Sel |

Bit 0 (/Protect): Protect bit.

0: Enable

1: Disable

Bit 1 (USB): Operation mode.

0: Non-USB mode. Close UDC and Transceiver function.

1: USB mode

Bit 2 (/D+ resistor): D+ Resistor pull-high switch.

0: Enable internal USB D+ pull-high resistor.

1: Disable internal USB D+ pull-high resistor.

Bits 4~3 (OST1~OST0): Oscillator start time. WDT time-out time.

00: 500 μ s

01: 2 ms

10: 4 ms

11: 8 ms

Bits 6~5 (FRQ1~FRQ0): System clock frequency switch.

00: 8 MHz, External Crystal \times 2

01: 16 MHz, External Crystal \times 4

10: 24 MHz, External Crystal \times 6

11: Not Defined

Bits 8~7 (PKG1~PKG0): Package switch.

00: 20 pins

01: 24 pins

10: 40 pins

11: 44 pins



Bit 9 (Reverse): set to "0" as default value

Bit 10 (/ADHold): Setting for the MCU during AD conversion

0: Set the MCU on hold during AD conversion

1: Keep the MCU running during AD conversion

Bit 11 ~ Bit 12 : DEL 0~DEL1: Set as 0, 0.

Bits 15 ~ 13 (EPX_SEL2 ~ EPX_SEL0): Endpoint function selection

| EPX_SEL[2 : 0] (USB Mode) | EPX Status / EPX FIFO Max Size | | | | |
|------------------------------|--------------------------------|-------------------|-------------------|-------------------|-------------------|
| | EP1 | EP2 | EP3 | EP4 | EP5 |
| 000 | Enable / 64-byte | Disable / NA | Disable / NA | Disable / NA | Disable / NA |
| 001 | Enable / 64- byte | Enable / 64- byte | Disable / NA | Disable / NA | Disable / NA |
| 010 | Enable / 64- byte | Enable / 32- byte | Enable / 32- byte | Disable / NA | Disable / NA |
| 011 | Enable / 64- byte | Enable / 32- byte | Enable / 16- byte | Enable / 16- byte | Disable / NA |
| 100 | Enable / 64- byte | Enable / 32- byte | Enable / 16- byte | Enable / 8- byte | Enable / 8- byte |
| 101 | Enable / 64- byte | Enable / 16- byte | Enable / 16- byte | Enable / 16- byte | Enable / 16- byte |
| 110 | Enable / 32- byte | Enable / 32- byte | Enable / 32- byte | Enable / 32- byte | Disable / NA |
| 111 | Enable / 32- byte | Enable / 32- byte | Enable / 32- byte | Enable / 16- byte | Enable / 16- byte |

Bits 16 ~ 40:

EPx Type:

00: Not defined

01: Isochronous mode transfer

10: Bulk mode transfer

11: Interrupt mode transfer

EPx Direction:

0: Output way

1: Input way

EPx Max Size:

00: 8 bytes

01: 16 bytes

10: 32 bytes

11: 64 bytes

If EPx Max Size selection is larger than Endpoint function selection, EPX FIFO size will depend on the size of Endpoint function selector (EPX_Sel0~2]).

Bits 41 ~ 42 (Reserved): reserved bit

Default: 1

Bits 43~ Bit 59 (USER ID): Defined by user.

Bits 60~64 (Reserved): Reserved bit

Bits 65 (Ver_Sel):

0: New Version (Additional SPI function)

1: Original Version

Bits 66~75 (Reserved)

D Application Circuit

