EM78871

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.5

ELAN MICROELECTRONICS CORP.

May 2006

Trademark Acknowledgments:
IBM is a registered trademark and PS/2 is a trademark of IBM.
Windows is a trademark of Microsoft Corporation.
ELAN and ELAN logo are trademarks of ELAN Microelectronics Corporation.

The contents of this specification are subject to change without further notice. ELAN Microelectronics assumes no responsibility concerning the accuracy, adequacy, or completeness of this specification. ELAN Microelectronics makes no commitment to update, or to keep current the information and material contained in this specification. Such information and material may change to conform to each confirmed order.

In no event shall ELAN Microelectronics be made responsible for any claims attributed to errors, omissions, or other inaccuracies in the information or material contained in this specification. ELAN Microelectronics shall not be liable for direct, indirect, special incidental, or consequential damages arising from the use of such information or material.

The software (if any) described in this specification is furnished under a license or nondisclosure agreement, and may be used or copied only in accordance with the terms of such agreement.

ELAN Microelectronics products are not intended for use in life support appliances, devices, or systems. Use of ELAN Microelectronics product in such applications is not supported and is prohibited.
NO PART OF THIS SPECIFICATION MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE EXPRESSED WRITTEN PERMISSION OF ELAN MICROELECTRONICS.

ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation Road 1
Hsinchu Science Park
Hsinchu, Taiwan 30077
Tel: +886 3 563-9977
Fax:+886 3 563-9966
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Rm. 1005B, 10/F Empire Centre
68 Mody Road, Tsimshatsui
Kowloon , HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780
elanhk@emc.com.hk

USA:
Elan Information Technology Group (U.S.A.)
1821 Saratoga Ave., Suite 250
Saratoga, CA 95070
USA
Tel: +1 408 366-8225
Fax: +1 408 366-8220

Europe:
Elan Microelectronics Corp. (Europe)
Siewerdtstrasse 105
8050 Zurich, SWITZERLAND
Tel: +41 43 299-4060
Fax: +41 43 299-4079
http://www.elan-europe.com

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
SSMEC Bldg., 3F, Gaoxin S. Ave.
Shenzhen Hi-Tech Industrial Park
Shenzhen, Guandong, CHINA
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500

Shanghai:
Elan Microelectronics Shanghai, Ltd.
23/Bldg. #115 Lane 572, Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA
Tel: +86 21 5080-3866
Fax: +86 21 5080-4600

Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.5	Removed the Idle Mode Function	2006/05/25

1 General Description

The EM78871 is an 8-bit CID (Caller Identification) RISC architecture microprocessor with low-power and high-speed CMOS technology. Integrated onto a single IC are on-chip watchdog timer (WDT), RAM, program ROM, programmable real-time clock/counter, external/internal interrupt, power-down mode, LCD driver, FSK decoder, Call-waiting decoder, DTMF receiver, Programming Tone generator, built-in Keytone clock generation, Comparator and tri-state I/O. The EM78871 provides a single-chip solution to design a CID for call message display.

2 Features

2.1 CPU

- Operating voltage range : 2.2V~5.5V (Normal mode), 2.0V~5.5V (Green mode)
- 32K×13 on-chip Program ROM
- 4K×8 on-chip data RAM
- 144-byte working register
- 51 bi-directional tri-state I/O ports (32 shared with LCD Segment pins)
- I/O with internal Pull high, wake-up and interrupt functions
- Stack: 32 stack levels for subroutine nesting
- TCC: 8-bit real time clock/counter (TCC) with 8-bit prescaler
- Counter 1: 8-bit counter with 8-bit prescaler which can also be an interrupt source
- Counter 2: 8-bit counter with 8-bit prescaler which can also be an interrupt source
- On-chip Watchdog Timer
- CPU modes:

Mode	CPU Status	Main Clock	32.768kHz Clock Status
Sleep mode	Off	Off	Off
Green mode	On	Off	On
Normal mode	On	On	On

- Thirteen interrupt sources (8 external , 5 internal)
- Key Scan : Port key scan function scans up to 64 (16x4) keys
- Sub-clock: 32.768kHz crystal
- Main-clock: 3.5862MHz multiplied by 0.25, 0.5, 1 or 3 generated by the internal PLL

- Keytone output: 4kHz, 2kHz and1kHz (shared with I/O)
- Comparator: 3-channel comparators: internal (16 level) or external reference voltage (shared with I/O)
- Serial Peripheral Interface (SPI): Interrupt flag (when the read buffer is full), programmable baud rates and three-wire synchronous communication (shared with I/O)

2.2 Current D/A

- Operating voltage range: 2.5V～5.5V
- 7-bit resolution and 3-bit output level control
- Current DA output controls the speaker using a transistor for sound playing (shared with I/O)

2.3 Programmable Tone Generators

- Operating voltage: 2.2V～5.5V
- Two programmable generators: Tone 1 and Tone 2
- Independent single tone generation for Tone 1 and Tone 2
- Mixed dual tone generation by Tone 1 and Tone 2 differs by 2dB
- Programmable DTMF tone generation
- Programmable FSK signal (Bell202 or V.23) generation

2.4 CID

- Operating voltage: 2.7V～5.5V (FSK)
- Operating voltage: 2.7V～5.5V (DTMF receiver)
- Compatible with Bellcore GR-30-CORE (formerly known as TR-NWT-000030)
- Compatible with British Telecom (BT) SIN227 and SIN242)
- FSK demodulator for Bell 202 and ITU-T V.23 (formerly known as CCITT V.23)

2.5 Call Waiting

- Operating voltage: 2.6V～5.5V
- Compatible with Bellcore special report SR-TSV-002476
- Call-Waiting (2130Hz plus 2750Hz) Alert Signal Detector
- Good talk-down and talk-off performance
- Sensitivity compensated by adjusting input OP gain

2.6 LCD (8x80, 9x80, 16x80, 24x72)

- Maximum common driver pins: 16/24
- Maximum segment driver pins: 80 (SEG0 ~ SEG79) / 72 (SEG8 ~ SEG79)
- Shared pins: COM16 ~ COM23 pin-shared with SEG0 ~ SEG7
- 1/4 bias for 8, 9 and 16 common modes and 1/5 bias for 24 common mode
- 1/8, 1/9, 1/16, 1/24 duty
- 16 levels of LCD contrast control (software)
- Internal resistor circuit for LCD bias
- Internal voltage follower for better display

2.7 Die Type

- 132-pin die: EM78871H
- 128-pin package: EM78871AQ with POVD disabled

  EM78871BQ with POVD enabled

3 Application

Adjunct units

Answering machines

Feature phones

4 Pin Assignment

EM78871H

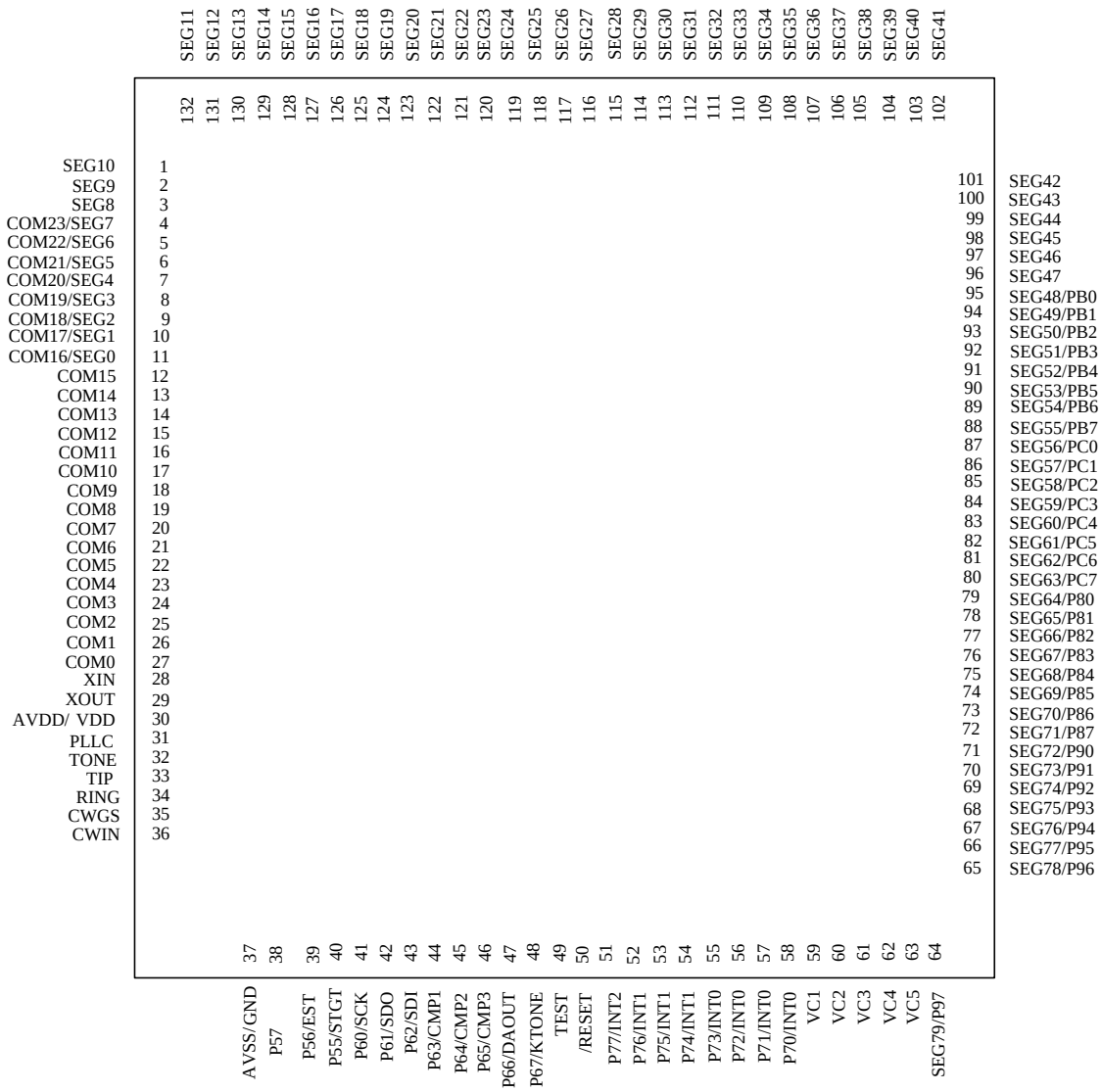


Fig.1.1 Pin Assignment (132-pin Die)

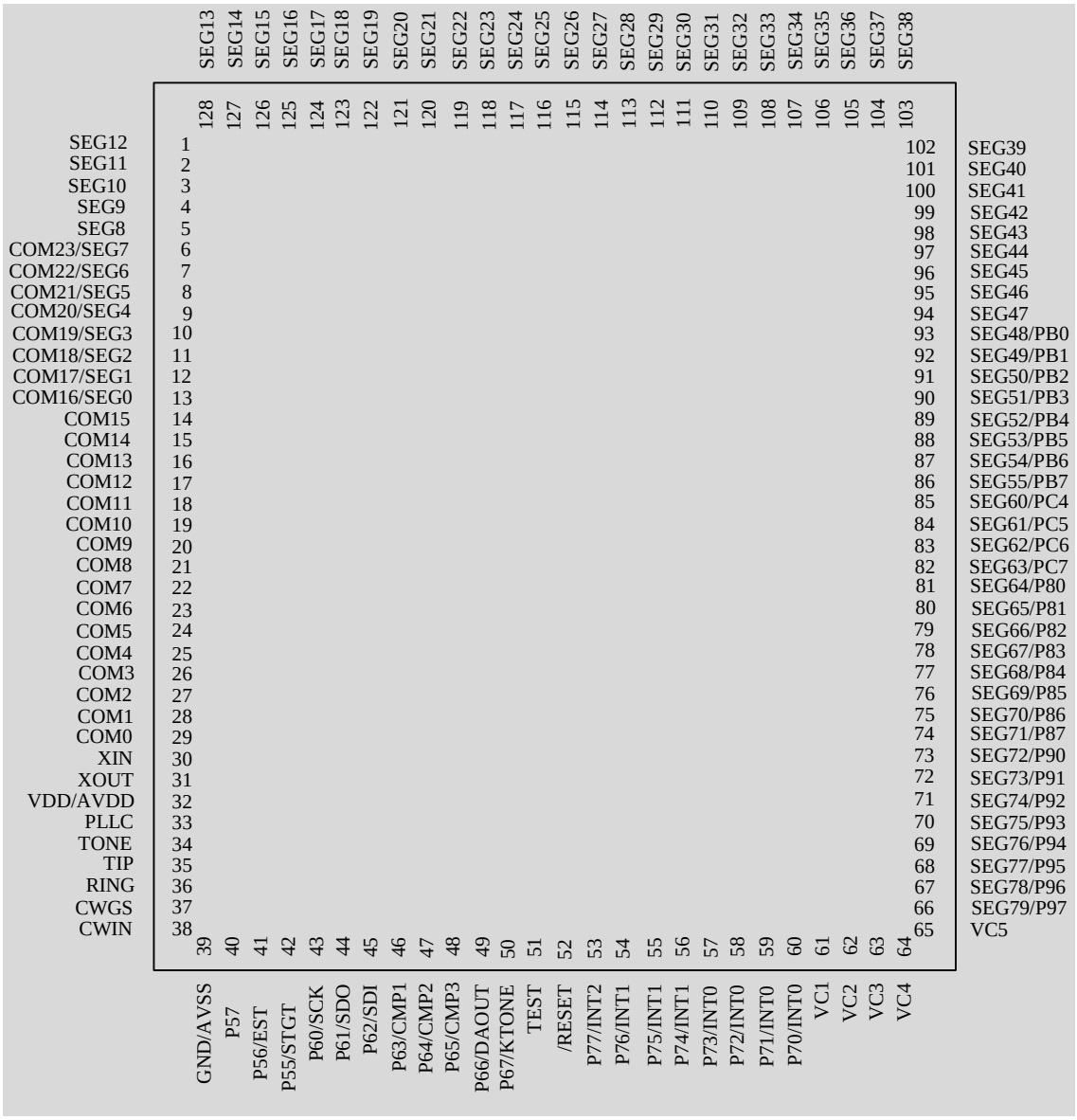


Fig.1.2 Pin Assignment (128-pin QFPA)

5 Block Diagram

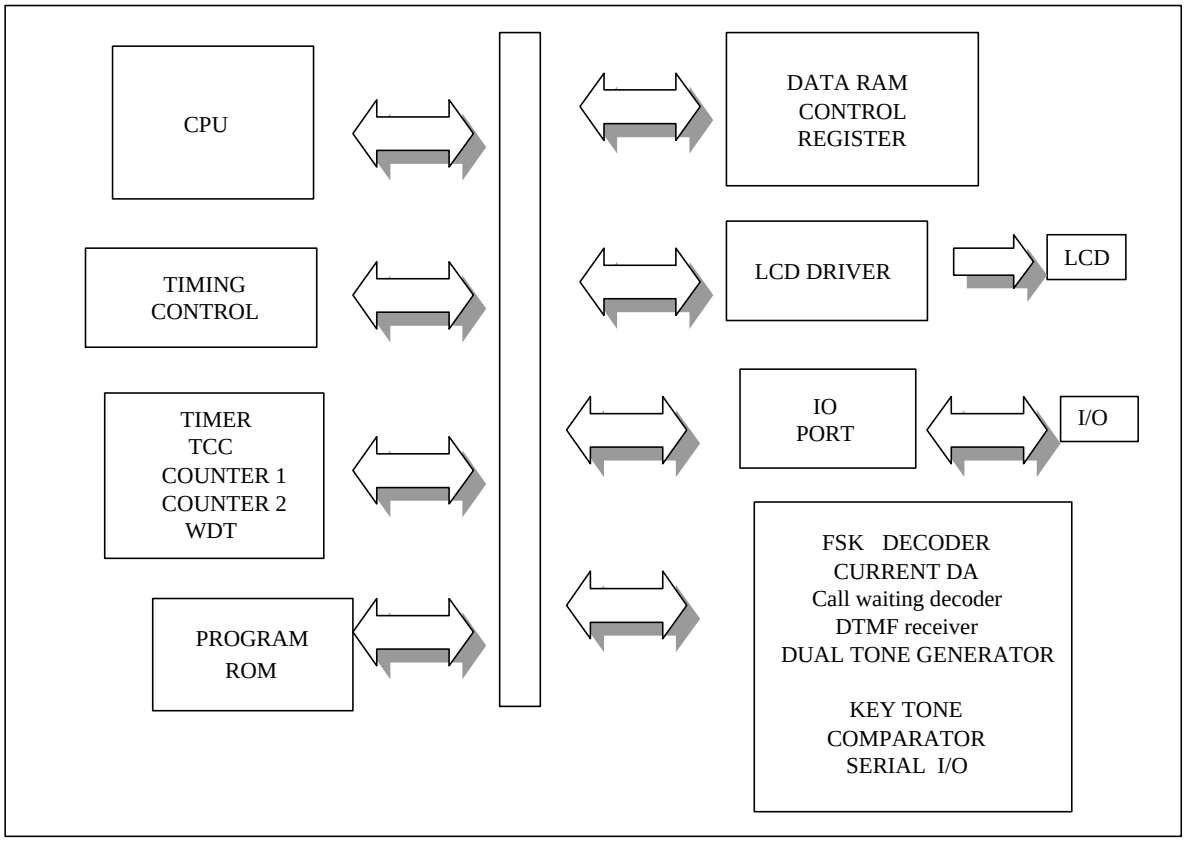


Fig. 2 Block Diagram 1

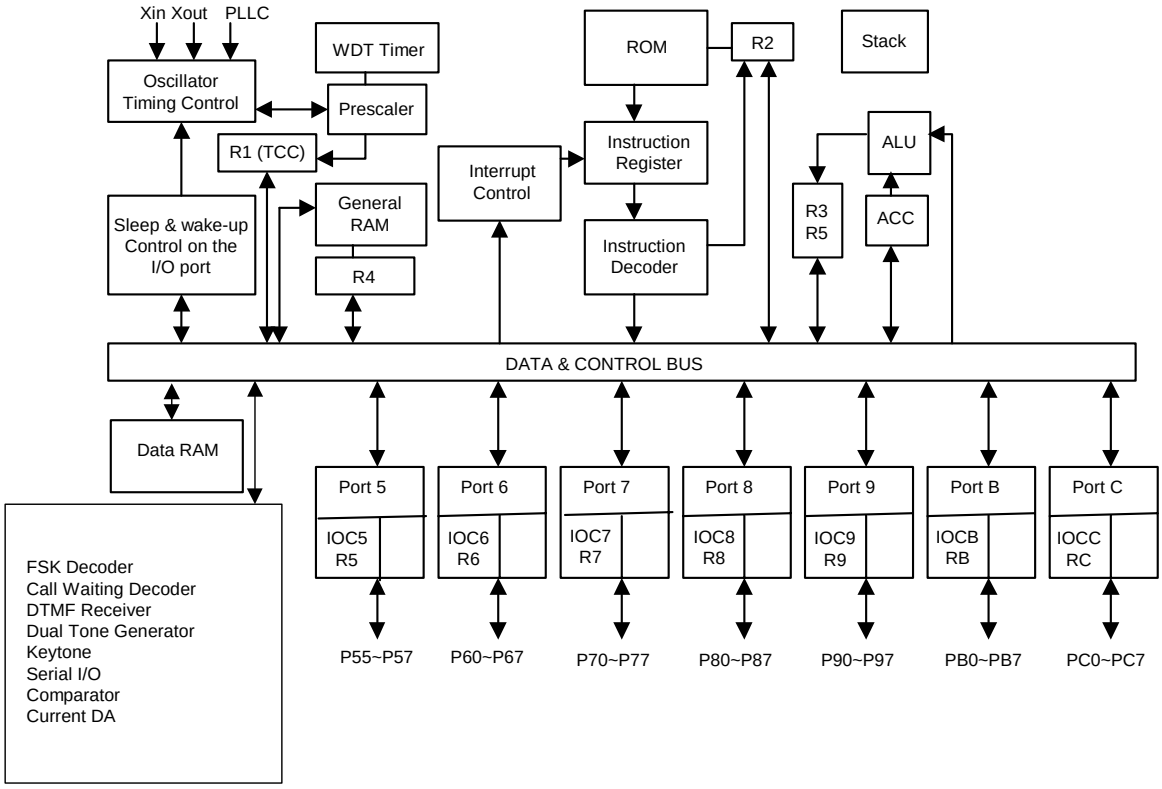


Fig.3 Block Diagram 2

6 Pin Description

Pin	I/O	Description
Power		
VDD AVDD	-	Digital power Analog power They are connected together when packaged as 128-pin QFP.
GND AVSS	-	Digital ground Analog ground They are connected together when packaged as 128-pin QFP.
Clock		
XIN	I	Input pin for the 32.768 kHz oscillator
XOUT	O	Output pin for the 32.768 kHz oscillator
PLLC	I	Phase loop clock capacitor. Connects to a capacitor (between 0.01µF and 0.1µF) to GND.
LCD		
COM0~COM15	O	Common driver pins of the LCD drivers
SEG0~SEG7 SEG8~SEG47 SEG48~SEG55 SEG56~SEG63 SEG64~SEG71 SEG72~SEG79	O (COM16~COM23) O O (I/O : Port B) O (I/O : Port C) O (I/O : Port 8) O (I/O : Port 9)	Segment driver pins for the LCD drivers SEG0 to SEG7 are pin-shared with COM16 to COM23 SEG48 to SEG79 are pin-shared with the I/O port.
VC1~VC5	I	Reference voltage input. Each is connects with a 0.1µ capacitor to GND.
FSK, TONE, KTONE		
TIP	I	Should be connected to the TIP side of the twisted pair lines for FSK.
RING	I	Should be connected to the RING side of the twisted pair lines for FSK.
TONE	O	Dual tone output pin
KTONE	O (Port 67)	Keytone output, pin-shared with Port 67.
CW		
CWGS	O	Gain adjustment for the single-ended input OP Amp
CWIN	I	Single-ended input OP Amp for the call waiting decoder
DTMF Receiver		
EST	O	Early steering output. Returns HI immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause EST to return to LO. This pin is shared with Port 56.
STGT	I/O	Steering input/guard time output (bi-directional). A voltage greater than Vtst detected at ST causes the device to register the detected tone-pair and update the output latch. A voltage less than Vtst frees the device to accept a new tone-pair. The GT output resets the external steering time-constant; its state is a function of EST and the voltage on ST. This pin is shared with Port 55.

Serial I/O		
SCK	IO (Port 60)	Master: output pin, Slave: input pin. This is pin-shared with Port 60.
SDO	O (Port 61)	Output pin for serial data transferring. This pin is shared with Port 61.
SDI	I (Port 62)	Input pin for receiving data. This pin is shared with Port 62.
Comparator		
CMP1 CMP2 CMP3	I (Port 63) I (Port 64) I (Port 65)	Comparator input pins. These are pin-shared with Port 63, Port 64 and Port 65.
Current DA		
DAOUT	O (Port 66)	Current DA output pin. Also acts as a control signal for sound generation. Shared with Port 66.
I/O		
P55 ~P57	I/O	Each bit in Port 5 can be an input or output port.
P60 ~P67	I/O	Each bit in Port 6 can be an input or output port. Internal pull high.
P70 ~ P77	I/O	Each bit in Port 7 can be an input or output port. Internal Pull-high function. Auto key scan function. Interrupt function.
P80 ~ P87	I/O	Each bit in Port 8 can be an input or output port. These are pin-shared with LCD Segment signal.
P90 ~ P97	I/O	Each bit in Port 9 can be an input or output port. These are pin-shared with LCD Segment signal.
PB0 ~ PB7	I/O	Each bit in Port B can be an input or output port. These are pin-shared with LCD Segment signal.
PC0 ~ PC7	I/O	Each bit in Port C can be an input or output port. These are pin-shared with LCD Segment signal.
INT0	Ports 70~73	Interrupt sources with the same interrupt flag. A falling-edge signal on any pin from Port 70 to Port 73 generates an interrupt.
INT1	Ports 74~76	Interrupt sources with the same interrupt flag. An edge signal on any pin from Port 74 to Port 76 generates an interrupt.
INT2	Port 77	Interrupt source. Once Port 77 has a falling-edge or rising-edge signal (controlled by the CONT register), it will generate an interrupt.
TEST	I	Sets the device to test mode for testing purposes only. Connect it to GND.
/RESET	I	Reset pin.

7 Function Description

7.1 Operational Registers

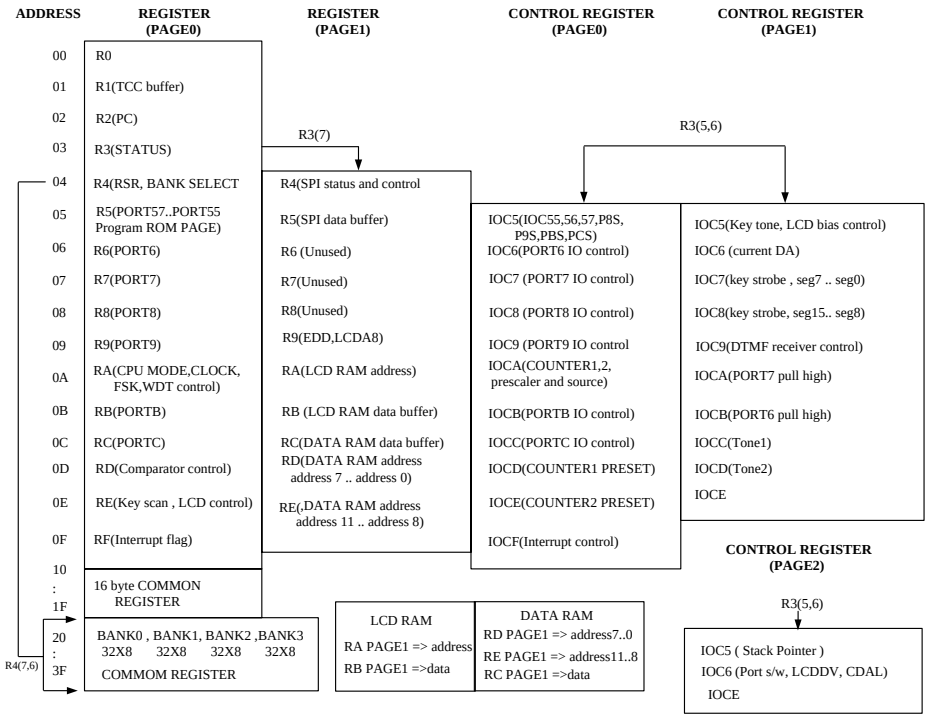


Fig.4 Control Register Configuration

7.2 Operational Register Detailed Description

7.2.1 R0 (Indirect Addressing Register)

R0 is not a physically-implemented register. It is useful as an indirect addressing pointer. Any instruction using R0 accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov    a,@0x20      ; stores an address at R4 for indirect addressing
Mov    0x04,A
Mov    a,@0xAA      ; writes data 0xAA to R20 at Bank 0 through R0
Mov    0x00,A
```

7.2.2 R1 (TCC)

TCC data buffer. Incremented by 16.38kHz or by the instruction clock cycle (controlled by the CONT register).

Written and read by the program as any other register.

7.2.3 R2 (Program Counter)

The structure is depicted in Fig. 5.

R2 generates 32K×13 on-chip program ROM addresses to the corresponding instruction codes.

"JMP" directly loads the low 10 program counter bits.

"CALL" loads the low 10 bits of the PC, PC+1, and then pushes the bits into the stack.

"RET" ("RETL k", "RETI") loads the program counter with the contents at the top of the stack.

"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address to be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address to be added to the current PC, with the contents of the ninth and tenth bits remaining unchanged. The most significant bit (A10~A14) will be loaded with the contents of the bits PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

If an interrupt is triggered, the program ROM jumps to Address 8 at Page 0. The CPU will store ACC, R3 status and R5 PAGE automatically. It will be restored after instruction RETI.

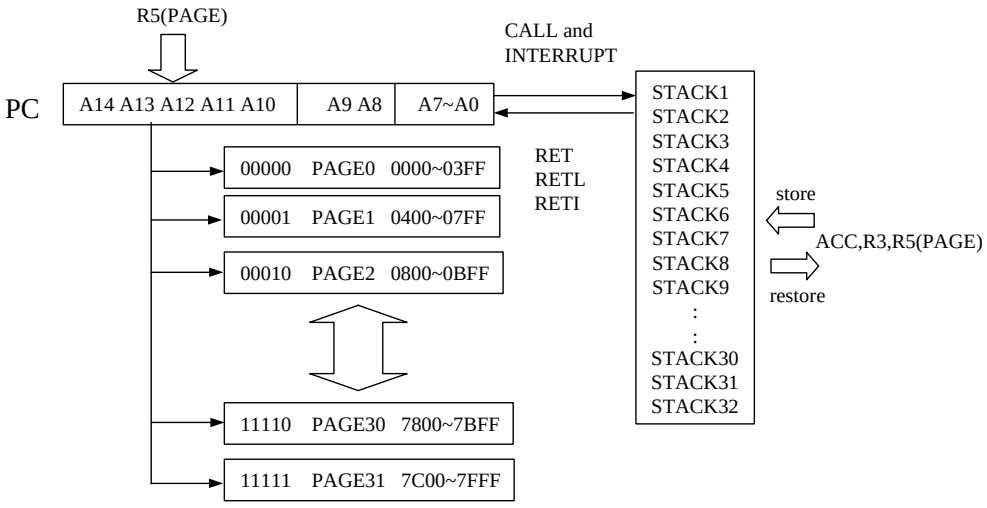


Fig.5 Program Counter Organization

7.2.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAGE	IOCP1S	IOCPAGE	T	P	Z	DC	C

Bit 0 (C): Carry flag

Bit 1 (DC): Auxiliary carry flag

Bit 2 (Z): Zero flag

Bit 3 (P): Power down bit.

Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T): Time-out bit.

Set to 1 by the "SLEP" and "WDTC" commands, or during power-up and reset to 0 when WDT times out.

Event	T	P	Remark
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	×	×	× : don't care

Bit 5 (IOCPAGE): changes IOC5 ~ IOCE to another page

Refer to Fig. 4 control register configuration for details.

"**0**" : Page 0

"**1**" : Page 1

Bit 6 (IOCP1S): changes IOC Page 1 and Page 2 to another register option

Refer to Fig. 4 control register configuration for details.

"**0**" : Page 1

"**1**" : Page 2

Bit 6 (IOCP1S)	Bit 5 (IOCPAGE)	Page Select
×	0	Page 0
0	1	Page 1
1	1	Page 2

Bit 7(PAGE): changes R4 ~ RE to another page

Refer to Fig. 4 control register configuration for details.

"**0**" : Page 0

"**1**" : Page 1

7.2.5 R4 (RAM Selection for Common Registers R20 ~ R3F, SPI)

- **Page 0 (RAM Selection Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the four banks for the 32 registers (R20 to R3F).

Refer to Fig.4 control register configuration for details.

- **Page 1 (SPI Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBF	SPIE	SRO	SE	SCES	SBR2	SBR1	SBR0

Fig. 6 shows how the SPI communicates with another device through the SPI module. If SPI is a master controller, it sends clock through the SCK pin. An 8-bit data is transmitted and received at the same time. If SPI, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted depending on the clock rate and the selected edge.

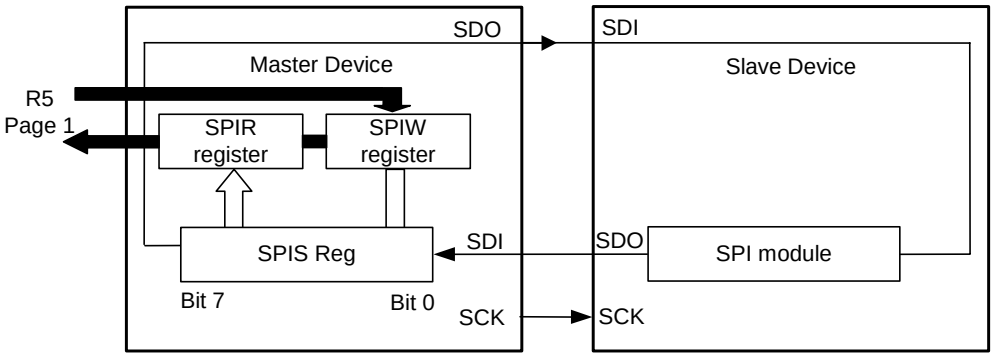


Fig.6 Single SPI Master / Slave Communication

Bit 0 ~ Bit 2 (SBR0 ~ SBR2) : SPI baud rate selection bits

SBR2	SBR1	SBR0	Mode	Baud Rate
0	0	0	Master	Fsco
0	0	1	Master	Fsco/2
0	1	0	Master	Fsco/4
0	1	1	Master	Fsco/8
1	0	0	Master	Fsco/16
1	0	1	Master	Fsco/32
1	1	0	Slave	
1	1	1	X	

Note: Fsco = CPU instruction clock

Example :

If PLL is enabled and RA PAGE 0 (Bit 5, Bit 4) = (1, 1), then the instruction clock is 3.58MHz/2 → Fsco=3.5862MHz/2

If PLL is enabled and RA PAGE 0 (Bit 5, Bit 4) = (0, 0), then the instruction clock is 0.895MHz/2 → Fsco=0.895MHz/2

If PLL is disabled, then the instruction clock is 32.768kHz/2 → Fsco=32.768kHz/2.

Bit 3 (SCES) : SPI clock edge selection bit

0 = Data shifts out on a rising edge, and shifts in on a falling edge. Data is held during a low level

1 = Data shifts out on a falling edge, and shifts in on a rising edge. Data is held during high level

Bit 4 (SE) : SPI shift enable bit

0 = Resets as soon as the data shift is completed, and the next byte is ready to shift

1 = Starts data shift, and remains on 1 while the current byte is still being transmitted

Note
This bit has to be reset by software.

Bit 5 (SRO) : SPI read overflow bit

0 = No overflow

1 = New data is received while there is still data in the SPIB register.

In this situation, data in the SPIS register will be discarded. To avoid setting this bit, data from the SPIB register must be read first before each data write action.

Note

This can only occur in slave mode.

Bit 6 (SPIE) : SPI enable bit

0 = Disable SPI mode

1 = Enable SPI mode

Bit 7 (RBF) : SPI read buffer full flag

0 = Data reception incomplete and SPIB is empty

1 = Finished receiving data and SPIB is full

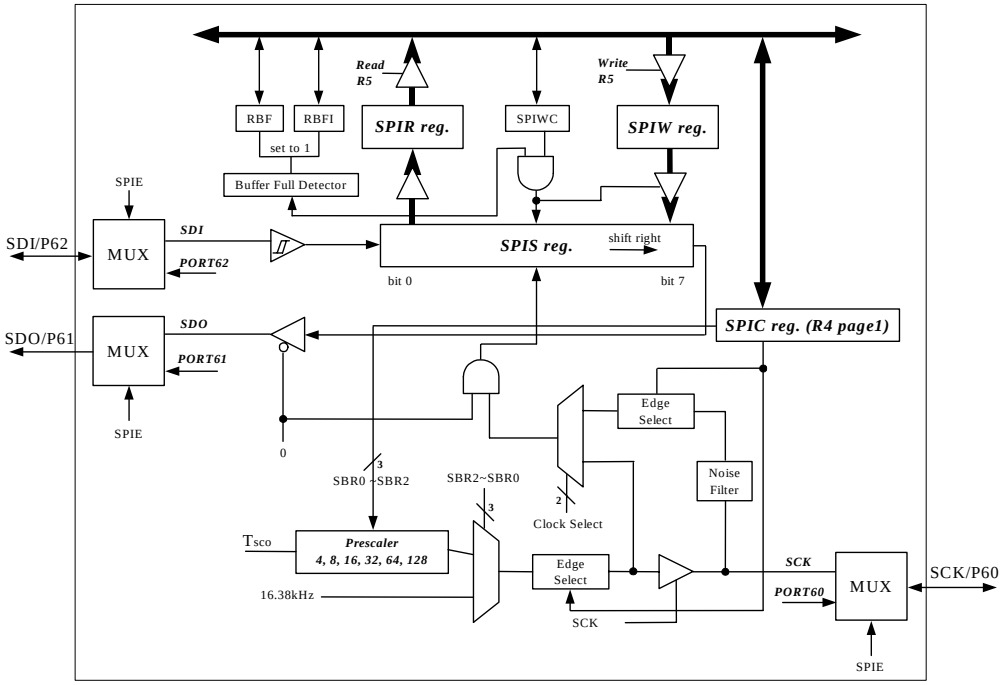


Fig.7 SPI Structure

SPIC reg. : SPI control register

SDO/P61 : Serial data out

SDI/P62 : Serial data in

SCK/P60 : Serial clock

RBF : Set by a buffer full signal, and reset in software.

RBFI : Interrupt flag. Set by a buffer full signal, and reset by software.

Buffer Full Detector : Sets to 1, when an 8-bit data shift is complete.

SE : Loads the data in the SPIW register, and starts data shift

SPIE : SPI control register

SPIS reg. : Shifting byte out and in. The MSB will be shifted first. Both the SPIS register and the SPIW register are loaded at the same time. Once data has been written, SPIS starts transmission / reception. The received data will be moved to the SPIR register, when the 8-bit data shift is completed. The RBF (Read Buffer Full) and the RBFI (Read Buffer Full Interrupt) flags are set.

SPIR reg. : Read buffer. The buffer will be updated as the 8-bit data shift is completed. The data must be read before the next reception is finished. The RBF flag is cleared as the SPIR register is read.

SPIW reg. : Write buffer. The buffer will block any write data operation until the 8-bit data shift is completed. The SE bit will be kept at 1 if the communication is still in progress. This flag must be cleared when the data shift is finished. Users can determine if the next write attempt is available.

SBR2 ~ SBR0: Program the clock frequency/rates and sources

Clock select : Selecting either the internal instruction clock or the external 16.338kHz clock as the shifting clock.

Edge Select : Selecting the appropriate clock edges by programming the SCES bit

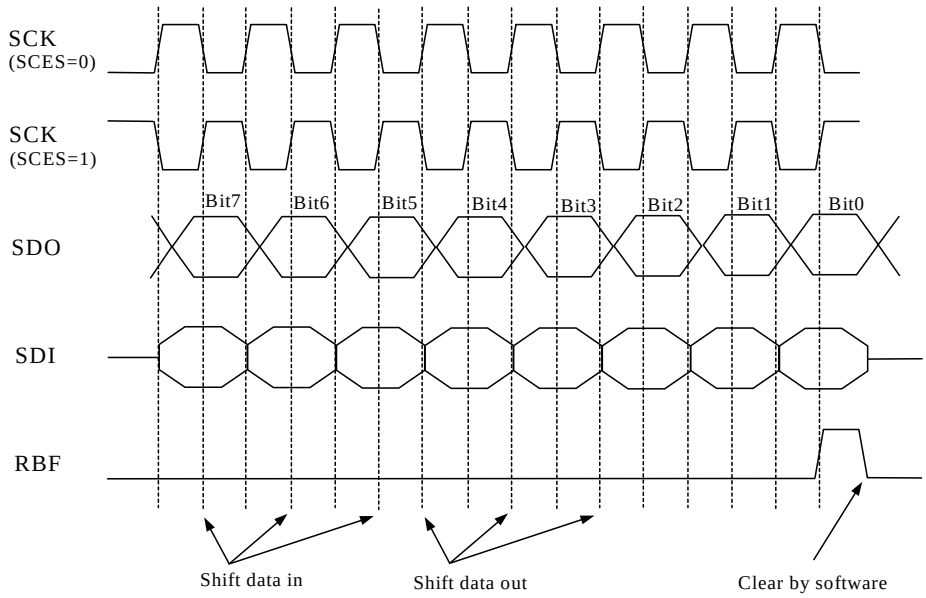


Fig.8 SPI Timing

7.2.6 R5 (Port 5 I/O Data, Program Page Selection, SPI Data)

- **Page 0 (Port 5 I/O Data Register, Program Page Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R57	R56	R55	PS4	PS3	PS2	PS1	PS0

Bit 0 ~ Bit 4 (PS0 ~ PS4) : Program page selection bits

PS4	PS3	PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	0	0	Page 0
0	0	0	0	1	Page 1
0	0	0	1	0	Page 2
0	0	0	1	1	Page 3
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	0	Page 30
1	1	1	1	1	Page 31

User can use the PAGE instruction to change page to maintain the program page. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. In this case, the program page is maintained by EMC's complier. It will change the user's program by inserting instructions within the program.

Bit 5 ~ Bit 6(P55 ~ P57) : 3-bit Port 5 (5~7) I/O data register

The IOC register can be used to set each bit either as input or output.

- **Page 1 (SPI Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0

Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7) : SPI data buffer

If you write data to this register, data will be written to the SPIW register. If you read this data, it will read the data from the SPIR register. Please refer to figure7

7.2.7 R6 (Port 6 I/O Data)

- **Page 0 (Port 6 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Bit 0 ~ Bit 7 (P60 ~ P67) : 8-bit Port 6 (0~7) I/O data register

The IOC register can be used to set each bit either as input or output.

- **Page 1 (Unused)**

  Bit 0 ~ Bit 7: unused

7.2.8 R7 (Port 7 I/O Data)

- **Page 0 (Port 7 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70

Bit 0 ~ Bit 7 (P70 ~ P77): 8-bit Port 7 (0~7) I/O data register

The IOC register can be used to set each bit either as input or output.

- **Page 1 (Unused)**

  Bit 0 ~ Bit 7: unused

7.2.9 R8 (Port 8 I/O Data)

- **Page 0 (Port 8 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80

Bit 0 ~ Bit 7 (P80 ~ P87): 8-bit Port 8 (0~7) I/O data register

The IOC register can be used to set each bit either as input or output.

- **Page 1 (Unused)**

Bit 0 ~ Bit 7: unused

7.2.10 R9 (Port 9 I/O Data, Extra LCD Address Bit)

- **Page 0 (Port 9 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90

Bit 0 ~ Bit 7 (P90 ~ P97): 8-bit Port 9 I/O data register

The IOC register can be used to set each bit either as input or output.

- **Page 1 (LCD Address MSB Bit)**

Bit 0 ~ Bit 6: unused

Bit 7 (LCDA8): MSB of the LCD address for reading or writing the LCD RAM.

Other LCD address bits (LCDA7 ~ LCDA0) are set from RA PAGE 1 Bit 7 ~ Bit 0.

For LCD address accessed over 0xFFH, set this bit to “1”; otherwise set this bit to “0”.

7.2.11 RA (CPU Power Saving, PLL, Main Clock Selection, FSK, Watchdog Timer, LCD Address)

- **Page 0 (CPU power saving bit, PLL, Main clock selection bits, FSK, watchdog timer enable bit)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLEEP_N	PLLEN	CLK1	CLK0	FSKPWR	FSKDATA	/CD	WDTEN

Bit 0 (WDTEN): Watchdog timer control register

User can use the WDTC instruction to clear the watchdog counter. The counter's clock source is 32768/2 Hz. If the prescaler is assigned to TCC, the watchdog counter will time out by(1/32768)×2× 256 = 15.616ms. If the prescaler is assigned to WDT, a longer timeout period is allowed depending on the ratio of the prescaler.

0 : Disable watchdog

1 : Enable watchdog

Bit 1 (/CD): FSK carrier detect indication

0 : Carrier Valid

1 : Carrier Invalid

It's a read-only signal. If the FSK decoder detects the energy mark or space signal, the Carrier signal will be LO. Otherwise it will be HI. **Note:** Should be at normal mode.

Bit 2 (FSKDATA): FSK decoding data output

It's a read-only signal. If the FSK decodes the mark or space signal, it sends a HI or LO signal at this register. It's a raw data type. That means the decoder just decodes the signal and does not process data. **Note:** Should be at normal mode.

User can use the FSK data's falling edge interrupt function to facilitate data decoding.

Ex:

```
MOV   A,@01000000
IOW   IOCF          ;enable FSK interrupt function
CLR   RF
ENI                 ;wait for FSK data's falling edge
:
```

0 : Space data (2200Hz)

1 : Mark data (1200Hz)

Bit 3 (FSKPWR) : FSK power control

0 : turn off the FSK decoder

1 : turn on the FSK decoder

This is the control register of the FSK block power. The FSK must be turned off before turning on the DTMF (IOC9 Page 1 Bit 7 set 1, this bit is set to 0)

The relation between Bit 1 to Bit 3 is shown in Fig.9. Turn on the FSK decoder first, then wait for the setup time (Tsup) to finish and check the carrier signal (/CD). If the carrier signal is low, it means the program can process the FSK data.

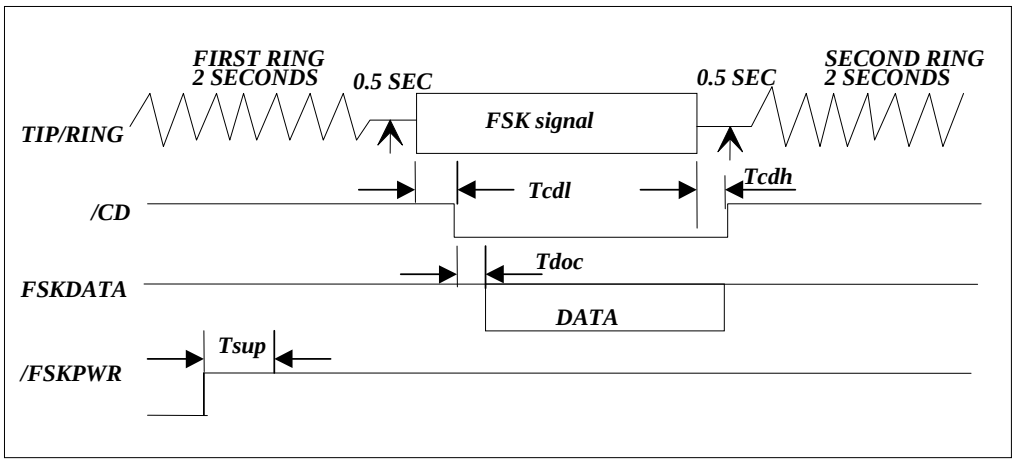


Fig.9 Correlation between Bit 1 ~ Bit 3

The controller is a CMOS device designed to support the Caller Number Deliver feature which is offered by the local telephone company. The FSK block contains one signal path. The signal path consists of an input differential buffer, a band pass filter, an FSK demodulator and a data validation and carrier detection circuit.

In a typical application, user can use his own external ring detection output to input to the IO port. User can use this signal to wake up the chip by an external ring detect signal.

Activate the FSK decoder, set Bit 3 (FSKPWR) of register RA to 1. Disable the FSK by setting Bit 3 (FSKPWR) of register RA to 0.

The input buffer accepts a differential AC coupled input signal through the TIP and RING input and feeds this signal to a band pass filter. Once the signal is filtered, the FSK demodulator decodes the information and sends it to a post filter. The output data is then made available at Bit 2 (FSKDATA) of register RA. This data, as sent by the central office, includes the header information (alternate "1" and "0") and 150 ms of marking which precedes the date, time and calling number. If no data is present, Bit 2 (Data) of register RA remains on “1”. This is accomplished by a carrier detection circuit which determines if the in-band energy is high enough. If the incoming signal is valid, Bit 1 (/CD) of register RA will be “0” otherwise it will be “1”. Thus the demodulated data is transferred to Bit 2 (Data) of register RA. If it is not, then the FSK demodulator is blocked.

Bit 4 ~ Bit 5 (CLK0 ~ CLK1): Main clock selection bits

User can choose a different frequency for the main clock by setting CLK1 and CLK2. The following lists the various clock frequencies.

PLLEN	CLK1	CLK0	Sub Clock	Main Clock	CPU Clock
1	0	0	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	32.768kHz	1.7913MHz	1.7913MHz (Normal mode)
1	1	0	32.768kHz	10.7479MHz	10.7479MHz (Normal mode)
1	1	1	32.768kHz	3.5826MHz	3.5826MHz (Normal mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)

Bit 6 (PLLEN): PLL enable control bit

This is the CPU mode control register. If PLL is enabled, the CPU will operate at normal mode (high frequency, main clock); otherwise, it will run at green mode (low frequency, 32768 Hz).

0 = disable

1 = enable

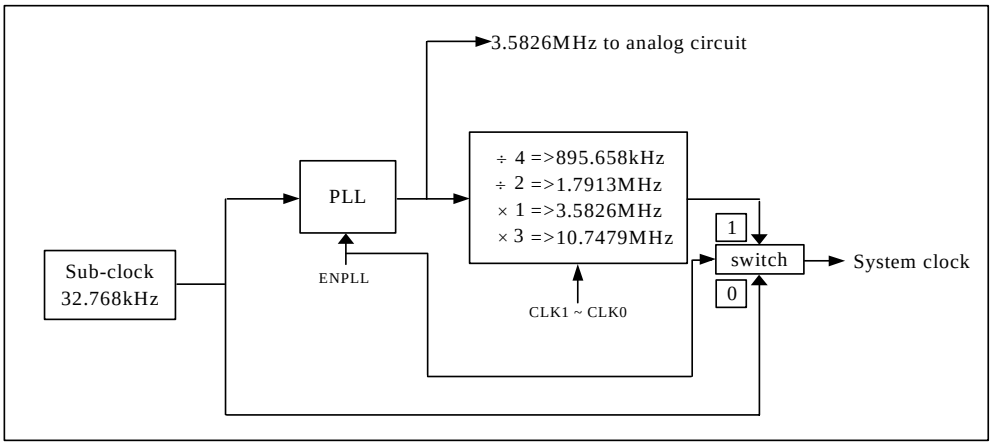


Fig.10 Correlation between 32.768kHz and PLL

Bit 7(SLEEP_N) : Power saving mode control register

When PLL is disabled, user can set this bit using the "SLEP" instruction for Sleep mode or Idle mode selection.

0 = Sleep mode

1 = *Not allowed*

This bit sets the SLEP mode.

The following table lists the relation between the wake-up signal and Sleep mode.

Wake-up Signal	Sleep Mode	Green Mode	Normal Mode
	RA (7, 6) = (0, 0) + SLEP	RA (7, 6) = (x, 0) no SLEP	RA (7, 6) = (x, 1) no SLEP
TCC time out IOCF Bit 0=1 And "ENI"	No function	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Counter 1 time out IOCF Bit 1=1 And "ENI"	No function	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Counter 2 time out IOCF Bit 2=1 And "ENI"	No function	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
WDT time out	Reset and Jump to Address 0	Reset and Jump to Address 0	Reset and Jump to Address 0
Port 7 IOCF Bit 3 or Bit 4 or Bit 5 = 1 And "ENI"	Reset and Jump to Address 0	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
IOCE Page 2 Bit 6 = 1 And RE Page 1 Bit 6 logic level variation (switch by EDGE bit) And “ENI”	No function	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)
Stack overflow IOC5 Page 2 Bit 7=1 & Bit 6: 0→1 And “ENI”	No function	Interrupt (Jump to Address 8 at Page 0)	Interrupt (Jump to Address 8 at Page 0)

Note

- *Stack overflow interrupt function is in the ROM less and OTP chip only.*
- *The wake-up function for Port 70 ~ Port 73 is controlled by IOCF Bit 3 and the ENI instruction. They are falling edge triggers.*

The wake-up function for Port 74 ~ Port 76 is controlled by IOCF bit4 and the ENI instruction. They are falling edge triggers.

The wake-up function for Port 77 is controlled by IOCF bit5 and the ENI instruction. It's a falling edge or rising edge trigger (controlled by the CONT register).

- **Page 1 (LCD Address)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDA7	LCDA6	LCDA5	LCDA 4	LCDA 3	LCDA 2	LCDA 1	LCDA 0

Bit 0 ~ Bit 7 (LCDA0 ~ LCDA7) : LCD address for LCD RAM reading or writing

The data in the LCD RAM corresponds to the COMMON and SEGMENT signals as listed in the following table.

COM23 ~ COM16 (Set R9 Page 1 Bit 7=1)	COM15 ~COM8 (Set R9 Page 1 Bit 7=0)	COM7 ~ COM0 (Set R9 Page 1 Bit 7=0)	
Address 100H	Address 80H	Address 00H	SEG0
Address 101H	Address 81H	Address 01H	SEG1
Address 102H	Address 82H	Address 02H	SEG1
:	:	:	:
:	:	:	:
:	:	:	:
Address 14EH	Address CEH	Address 4EH	SEG78
Address 14FH	Address CFH	Address 4FH	SEG79
Address 150H	Address D0H	Address 50H	Empty
:	:	:	:
Address 17FH	Address FFH	Address 7FH	Empty

7.2.12 RB (Port B I/O Data, LCD Data)

- **Page 0 (Port B I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

Bit 0 ~ Bit 7 (PB0 ~ PB7) : 8-bit PORTB(0~7) I/O data register

The IOC register can be used to set each bit either as input or output.

- **Page 1 (LCD Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 Bit	Bit 1	Bit 0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0

Bit 0 ~ Bit 7 (LCDD0 ~ LCDD7) : LCD data buffer for reading data from or writing data to the LCD RAM

Example.

```
MOV     A,@0
MOV     R9_PAGE1,A
MOV     RA_PAGE1,A          ;ADDRESS
MOV     A,@0XAA
MOV     RB_PAGE1,A          ; Write data 0XAA to the LCD RAM
MOV     A,RB_PAGE1          ; Read data from the LCD RAM
        :
```

7.2.13 RC (Port C I/O Data, Data RAM Data)

- **Page 0 (Port C I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Bit 0 ~ Bit 7 (PC0 ~ PC7) : 8-bit Port C I/O data register

The IOC register can be used to set each bit either as input or output.

- **Page 1 (Data RAM Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAMD7	RAMD6	RAMD5	RAMD4	RAMD3	RAMD2	RAMD1	RAMD0

Bit 0 ~ Bit 7 (RAMD0 ~ RAMD7) : Data RAM data buffer for reading data from or writing data to RAM.

Ex.

```
MOV         A , @1
MOV         RD_PAGE1 , A
MOV         A , @0
MOV         RE_PAGE1 , A
MOV         A , @0x55
MOV         RC_PAGE1 , A     ;write data 0x55 to DATA
                             ;RAM at address "0001"
MOV         A , RC_PAGE1     ;read data
:
```

7.2.14 RD (Comparator Control, Data RAM Address)

- **Page 0 (Comparator Control Bits)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPEN	CMPFLAG	CMPS1	CMPS0	CMP_B3	CMP_B2	CMP_B1	CMP_B0

When Port 63, Port 64 or Port 65 are defined (by CMPIN1, CMPIN2, CMPIN3 at IOCE Page 1) as comparator input or Port 6, user can use this register to control the function of the comparator.

Bit 0~Bit 3(CMP_B0~CMP_B3) : Reference voltage selection of internal bias circuit for the comparator.

Reference voltage for comparator = VDD × (n + 0.5)/ 16 , n = 0 to 15

Bit 4~Bit 5 (CMPS0~CMPS1) : Channel selection from CMP1 to CMP3 for the comparator

CMPS1	CMPS0	Input
0	0	CMP1
0	1	CMP2
1	0	CMP3
1	1	Reserved

Bit 6(CMPFALG) : Comparator output flag

0 = Input voltage is lesser than the reference voltage

1 = Input voltage is greater than the reference voltage

Bit 7(CMPEN) : Enable control bit of comparator.

0 = disable

1 = enable

When this bit is set to “0”, the 2.0V reference circuit is also powered off.

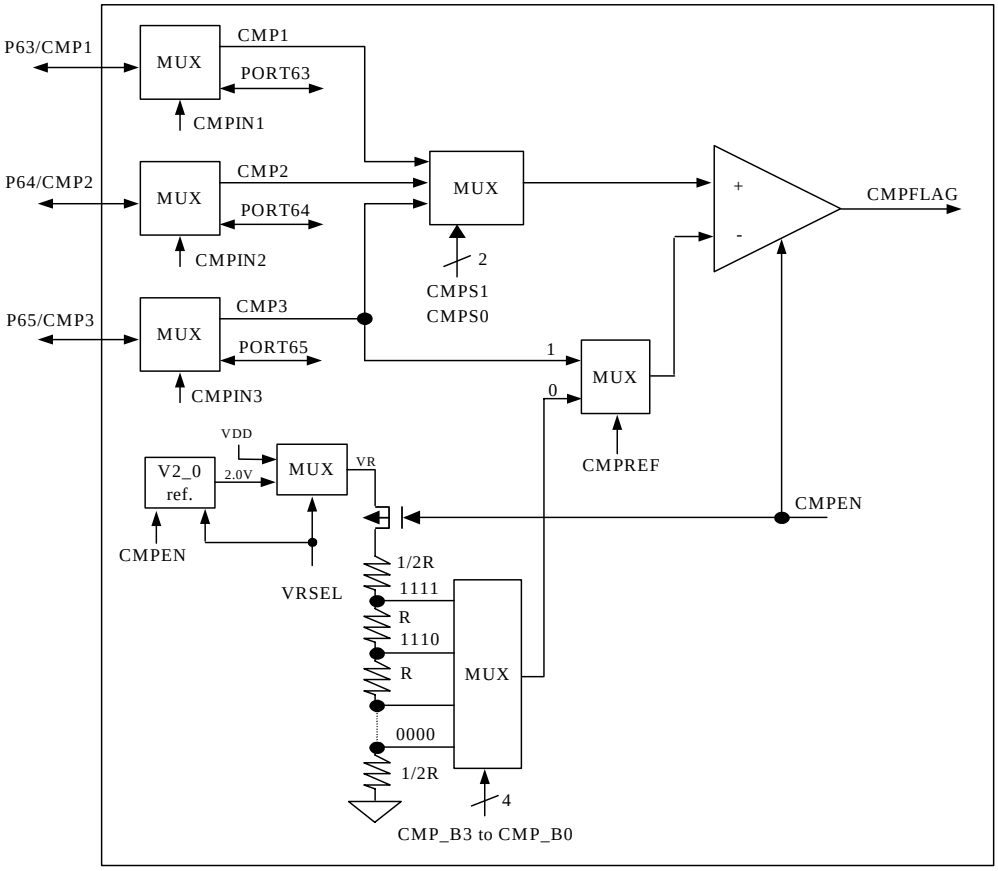


Fig.11 Comparator Circuit

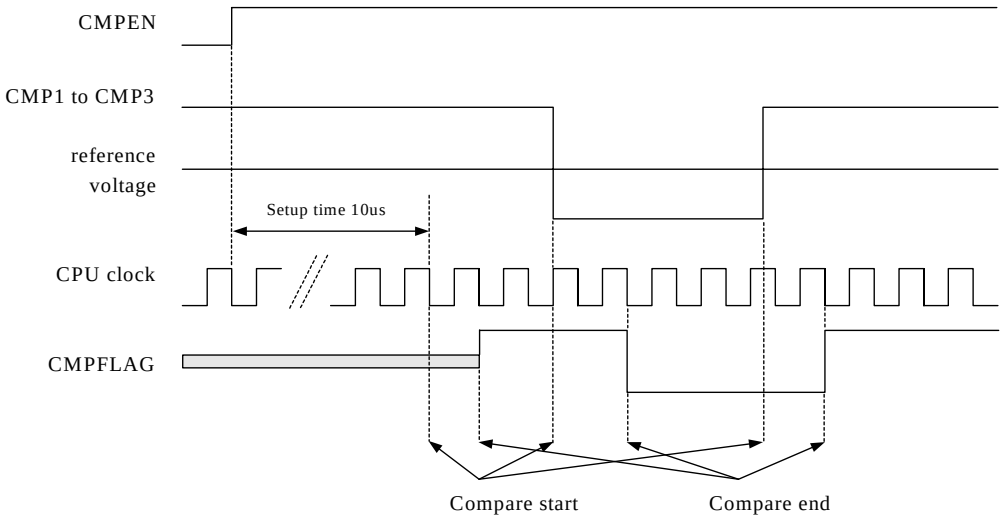


Fig.12 Comparator Timing

- **Page 1 (Data RAM Address 0 ~ Address 7)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAMA7	RAMA6	RAMA5	RAMA4	RAMA3	RAMA2	RAMA1	RAMA0

Bit 0~Bit 7(RAMA0~RAMA7) : Data RAM address (address0 to address7) for reading data from or writing data to RAM.

7.2.15 RE (CAS, Key Scan, LCD Control, Data RAM Address)

- **Page 0 (Key Scan Control, LCD Control)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CAS	KEYCHK	KEYSTRB	KEYSCAN	LCD1	LCD0	LCDM1	LCDM0

Bit 0~Bit 1(LCDM0~LCDM1) : LCD common mode, bias selection and COM/SEG switch control bits

LCDM1, LCDM0	COM Output Mode	LCD Bias	COM/SEG Switch
0, 0	16 common	1/4 bias	SEG0 ~ SEG7 select
0, 1	9 common	1/4 bias	SEG0 ~ SEG7 select
1, 0	8 common	1/4 bias	SEG0 ~ SEG7 select
1, 1	24 common	1/5 bias	COM16 ~ COM23 select

Note

When 8, 9 and 16 LCD common mode is set, COM16/SEG0 pin~COM23/SEG7 pin are also set to SEG0~SEG7 and LCD bias is 1/4 bias. When 24 LCD common mode is set, COM16/SEG0 pin~COM23/SEG7 pin are also set to COM16~COM23 and LCD bias is 1/5 bias.

Bit 2~Bit 3 (LCD0~LCD1) : LCD operation function definition

LCD1, LCD0	LCD Operation
0,0	Disable
0,1	Blanking
1,0	Reserved
1,1	LCD enable

Note

Key strobe and Key check functions should be enabled whenever LCD is enabled or disabled.

The controller can control the LCD directly. The LCD block is made up of an LCD driver, display RAM, segment output pins, common output pins and LCD operating bias pins.

Duty, the number of segments, the number of common and frame frequency are determined by LCD mode register RE Page 0 Bit 0~ Bit 1.

When 8, 9 or 16 LCD commons are used, the LCD operating bias pins VC1, VC2, VC4 and VC5 need to be set to 0 and the1µF capacitors connected to ground (VC3 is not necessary). When 24 LCD common is used, all LCD operating bias pins VC1 ~ VC5 need to be connected to the 0.1µF capacitors to the ground.

The LCD driver can be controlled as different driving ability (refer to IOC6 Page 1 Option-B register).

The basic structure contains a timer which uses the basic frequency of 32.768kHz to generate the proper timing for different duty and display access. RE Page 1 register is a command register for the LCD driver and display. The LCD display function (disable, enable, blanking) is controlled by RE Page 0 Bit 2 ~ Bit 3 and the driving duty is decided by RE PAGE Bit 0 ~ Bit 2. LCD display data is stored in data RAM which is addressed and data access controlled by registers R9, RA Page 1 and RB Page 1.

User can change the contrast of the LCD display by setting IOC5 Page 1 (BIAS3 ~ BIAS0). Up to 16 levels of contrast is allowed. In addition, the internal voltage follower allows greater driving source.

COM signal : The number of COM pins varies according to the duty cycle used, as follows:

In 1/8 duty mode COM8 ~ COM15 must be opened.

In 1/9 duty mode COM9~ COM15 must be opened.

In 1/16 duty mode COM0 ~ COM15 pins must be used.

In 1/24 duty mode COM0 ~ COM23 pins must be used.

Duty	COM0 ~ COM7	COM8	COM9	..	COM15	COM15 ~ COM23
1/8	O	×	×	..	×	×
1/9	O	O	×	..	×	×
1/16	O	O	O	..	O	×
1/24	O	O	O	..	O	O

Note: " × " means open **" O "** means select

SEG Signal : The segment signal pins are connected to the corresponding display RAM. The high byte to the low byte Bit 0 ~ Bit 7 correspond to COM0 ~ COM23 respectively. When a bit of display RAM is 1, a select signal is sent to the corresponding pin segment. When the bit is 0, a non-select signal is sent to the corresponding pin segment.

Bit 4 (KEYSCAN) : Key scan function enable control bit

0 = Disable

1 = Enable

If the key scan function is enabled, the LCD waveform will produce a small pulse for each time period as shown in Fig.13.

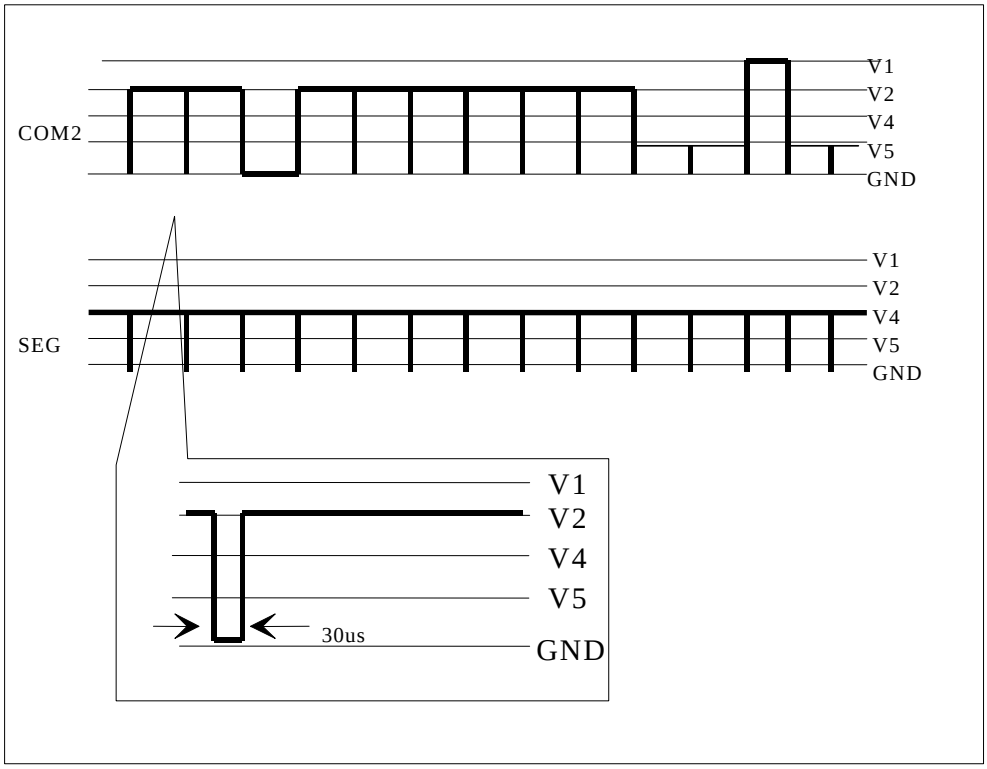


Fig.13 Key Scan Waveform for 1/8, 1/9, 1/16 Duty

Bit 5 (KEYSTRB) : Key strobe enable control bit

0 = Disable

1 = Enable

If this bit is set, the segment will switch to strobe signal temporally and output a zero signal (one instruction long) one by one from Segment 8 to Segment 23. During one segment strobe time, the CPU will check whether Port 7 (0:3) is equal to "1111" or not. If it is not, the CPU will latch a zero at IOC7 PAGE1 and IOC8 PAGE1 one by one depending on which segment strobes.

After a strobe, this bit will be cleared . Fig.14 shows a key strobe signal.

One instruction

REGISTER

STROBE	IOC7(0)	IOC7(1)	IOC7(2)	IOC7(3)	IOC7(4)	IOC7(5)	IOC7(6)	IOC7(7)	IOC8(0)	IOC8(1)	IOC8(2)	IOC8(3)	IOC8(4)	IOC8(5)	IOC8(6)	IOC8(7)
SEG8	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG9	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG10	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG11	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
SEG12	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
SEG13	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
SEG14	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
SEG15	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
SEG16	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
SEG17	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
SEG18	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
SEG19	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
SEG20	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
SEG21	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
SEG22	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
SEG23	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Fig.14 Key Strobe Signal

Bit 6 (KEYCHK): Key check enable control bit

0 = Disable key check function

1 = Enable key check function. SEG8 to SEG23 will stay at low level

Figure 15 shows the relationship between Key Scan, Key strobe, Key check and Segments.

Figure 16 shows key scan function flow triggered by an interrupt.

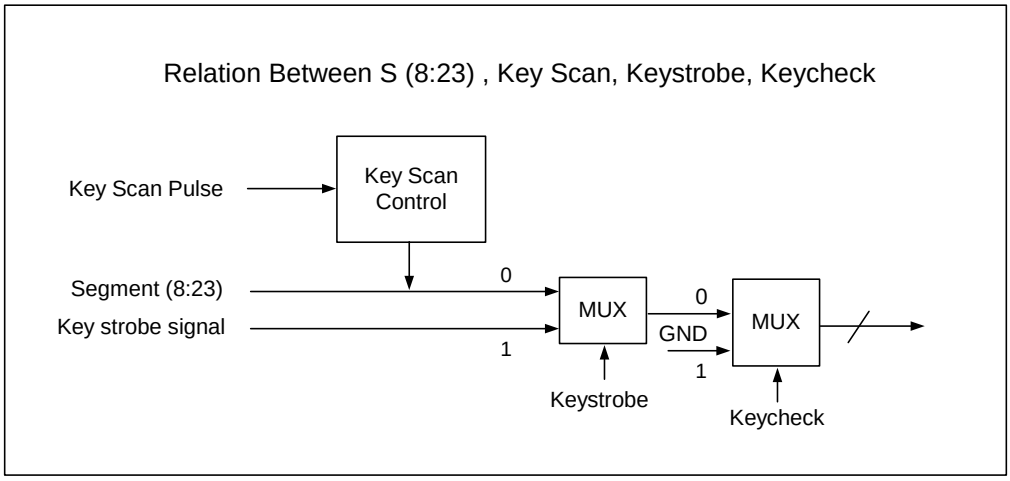


Fig.15 Key Scan, Keystrobe, Keycheck and Segments

Bit 7 (CAS) : Call Waiting decoding output

0 = CW data valid

1 = No data

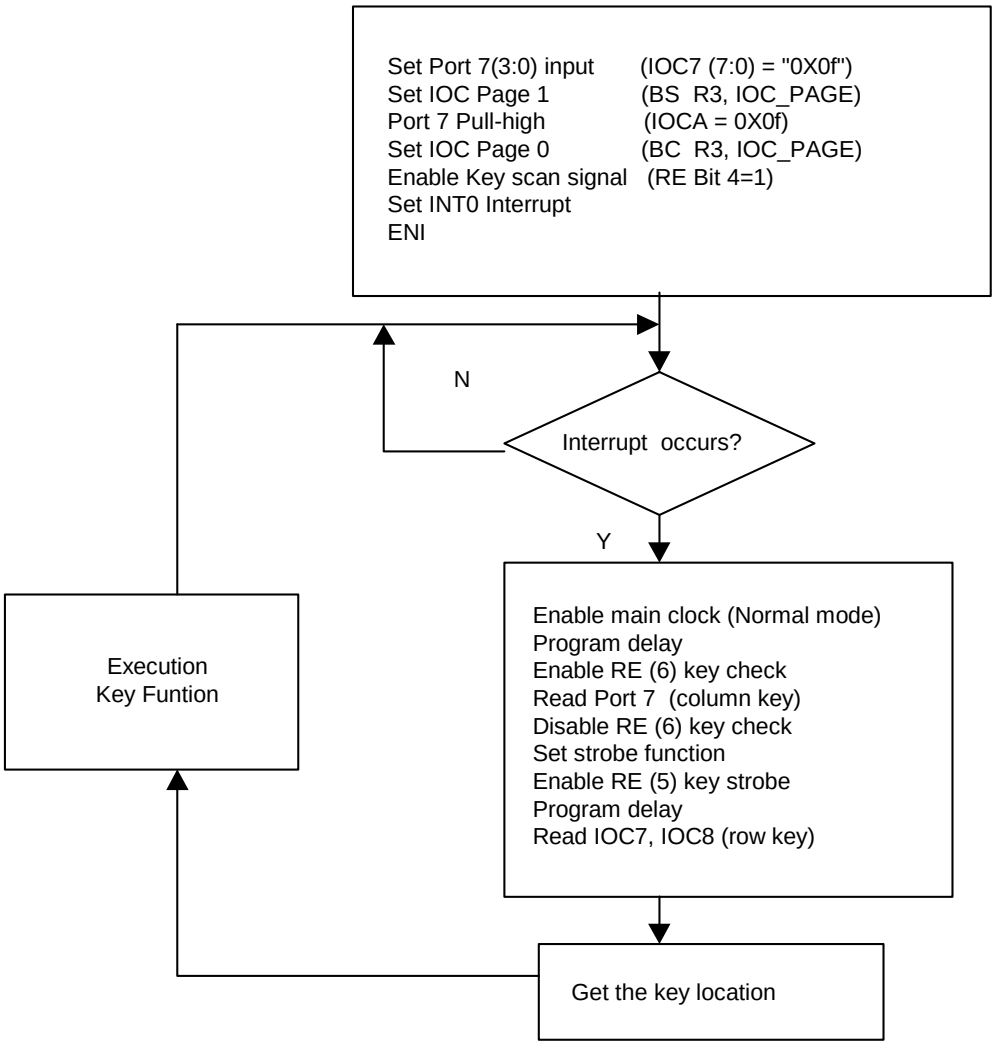


Fig.16 Key Scan Flow by Interrupt Trigger

- **Page 1 (Data RAM Address 8 ~ Address 11)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	RAMA11	RAMA10	RAMA9	RAMA8

Bit 0~Bit 3 (RAMA8~RAMA11): Data RAM address (Address 8 to Address 11) for RAM reading.

Bit 4~Bit 5: unused

Bit 6: unused

Bit 7: unused

7.2.16 RF (Interrupt Flags)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBF/SDT	FSK/CW	INT2	INT1	INT0	CNT2	CNT1	TCIF

Note: **" 1 "** means with interrupt request **" 0 "** means no interrupt occurs

Bit 0 (TCIF): TCC timer overflow interrupt flag

Set when TCC timer overflows.

Bit 1 (CNT1): Counter 1 timer overflow interrupt flag

Set when Counter 1 timer overflows.

Bit 2 (CNT2): Counter 2 timer overflow interrupt flag

Set when Counter 2 timer overflows.

Bit 3 (INT0): External INT0 pin interrupt flag

If Port 70, Port 71, Port 72 or Port 73 has a falling edge trigger signal, the CPU will set this bit.

Bit 4 (INT1): External INT1 pin interrupt flag

If Port 74, Port 75 or Port 76 has a falling edge trigger signal, the CPU will set this bit.

Bit 5 (INT2): External INT2 pin interrupt flag

If Port 77 has a falling edge or rising edge (controlled by CONT register) trigger signal, the CPU will set this bit.

Bit 6 (FSK/CW): FSK data or Call waiting data interrupt flag

If FSKDATA or CAS has a falling edge trigger signal, the CPU will set this bit.

Bit 7 (RBF/STD): SPI data transfer complete or DTMF receiver signal valid interrupt

If serial IO's RBF signal has a rising edge signal (RBF set to "1" after the data transfer is completed), the CPU will set this bit. This bit is also set when the DTMF receiver's STD signal has a rising edge signal (DTMF decode a DTMF signal).

IOCF is the interrupt mask register which the user can read and clear.

Trigger edge is shown in the following table:

Signal	Trigger	Remark
TCC	Time out	-
Counter 1	Time out	-
Counter 2	Time out	-
INT0	Falling edge	-
INT1	Falling edge	-
INT2	Falling/Falling & rising edge	Controlled by CONT register
FSK	Falling edge	-
RBF/STD	Rising edge	-

7.2.17 R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3): All of these are general purpose registers.

7.3 Special Function Registers

7.3.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

7.3.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS		PAB	PSR2	PSR1	PSR0

Bit 0~Bit 2(PSR0~PSR2): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB): Prescaler assignment bit

0 = TCC

1 = WDT

Bit 4: unused

Bit 5 (TS): TCC signal source

0 = Instruction clock

1 = 16.384kHz

Instruction clock = MCU clock/2, Refer to RA Bit 4 ~ Bit 6 for PLL and Main clock selection. See Fig.17.

Bit 6(INT) : INT enable flag

0 = interrupt masked by DISI or hardware interrupt

1 = interrupt enabled by the ENI/RETI instructions

Bit 7 (INT_EDGE): interrupt edge type for P77

0 = P77's interrupt source is a rising edge signal and falling edge signal

1 = P77's interrupt source is a falling edge signal

The CONT register is readable (CONTR) and writable (CONTW).

7.3.3 TCC and WDT :

There is an 8-bit counter available as the prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

An 8 bit counter is available for TCC or WDT and it is determined by the status of Bit 3 (PAB) of the CONT register.

See the prescaler ratio in the CONT register.

Fig.16 shows the circuit diagram of TCC/WDT.

Both TCC and the prescaler will be cleared by instructions which write to TCC each time.

The prescaler will be cleared by the WDTC and SLEP instructions, when set to WDT mode.

The prescaler will not be cleared by the SLEP instructions, when set to TCC mode.

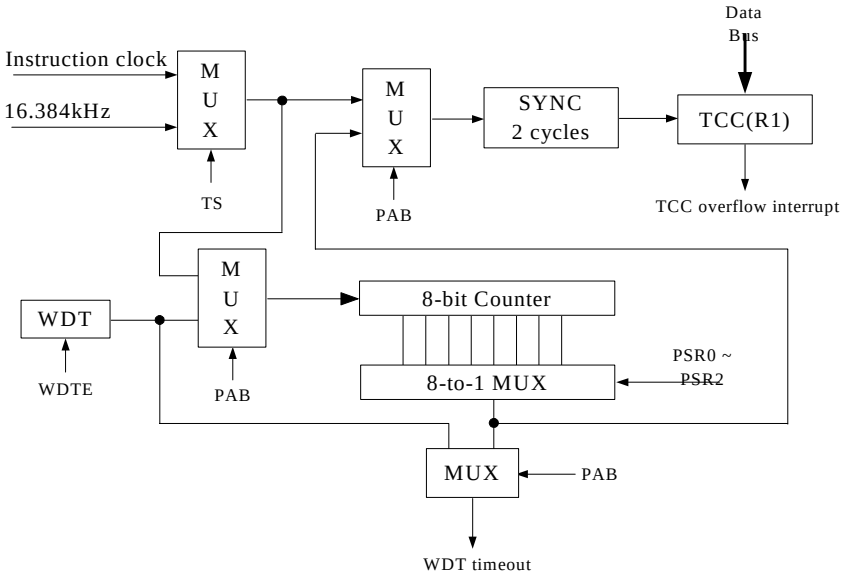


Fig.17 Block Diagram of TCC WDT

7.3.4 IOC5 (Port 5 I/O Control, Port Switch, Keytone, CDAS, LCD Bias)

- **Page 0 (Port 5 I/O Control Register, Port Switch)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	CASPWR	P9SH	P9SL	P8SH	P8SL

Bit 0 (P8SL) : Switch low nibble I/O Port 8 or LCD segment output for the shared SEGxx/P8x pins

0 = select normal P80 ~ P83 for low nibble Port 8

1 = select SEG64 ~ SEG67 output for LCD segment output

Bit 1 (P8SH) : Switch high nibble I/O Port 8 or LCD segment output for the shared SEGxx/P8x pins

0 = select normal P84 ~ P87 for high nibble Port 8

1 = select SEG68 ~ SEG71 output for LCD segment output

Bit 2 (P9SL): Switch low nibble I/O Port 9 or LCD segment output for share pins SEGxx/P9x pins

0 = select normal P90 ~ P93 for low nibble Port 9

1 = select SEG72 ~ SEG75 output for LCD segment output

Bit 3 (P9SH): Switch high nibble I/O Port 9 or LCD segment output for the shared SEGxx/P9x pins

0 = select normal P94 ~ P97 for high nibble Port 9

1 = select SEG76 ~ SEG79 output for LCD segment output

***Bit 4:** general register

Bit 4 (CWPWR): Power control for the Call Waiting circuit

0 = disable the circuit

1 = enable the circuit

Bit 5~Bit 6 (IOC55~IOC57): Port 5 I/O direction control registers

0 = set the relative I/O pin as output

1 = set the relative I/O pin to high impedance

- **Page 1 (Keytone Control, CDAS, LCD Bias Control)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KT1	KT0	KTS	CDAS	BIAS3	BIAS2	BIAS1	BIAS0

Bit 0~Bit 3 (BIAS0~BIAS3): LCD operation voltage selection

V1 = VDD * (5 - n/15)/5

(BIAS3 to BIAS0)	V1 Voltage	Example (VDD=5V)
0000	VDD * (5-0/15)/5	5V
0001	VDD * (5-1/15)/5	4.93V
0010	VDD * (5-2/15)/5	4.86V
0011	VDD * (5-3/15)/5	4.80V
0100	VDD * (5-4/15)/5	4.73V
:	:	:
1101	VDD * (5-13/15)/5	4.13V
1110	VDD * (5-14/15)/5	4.07V
1111	VDD * (5-15/15)/5	4.0V

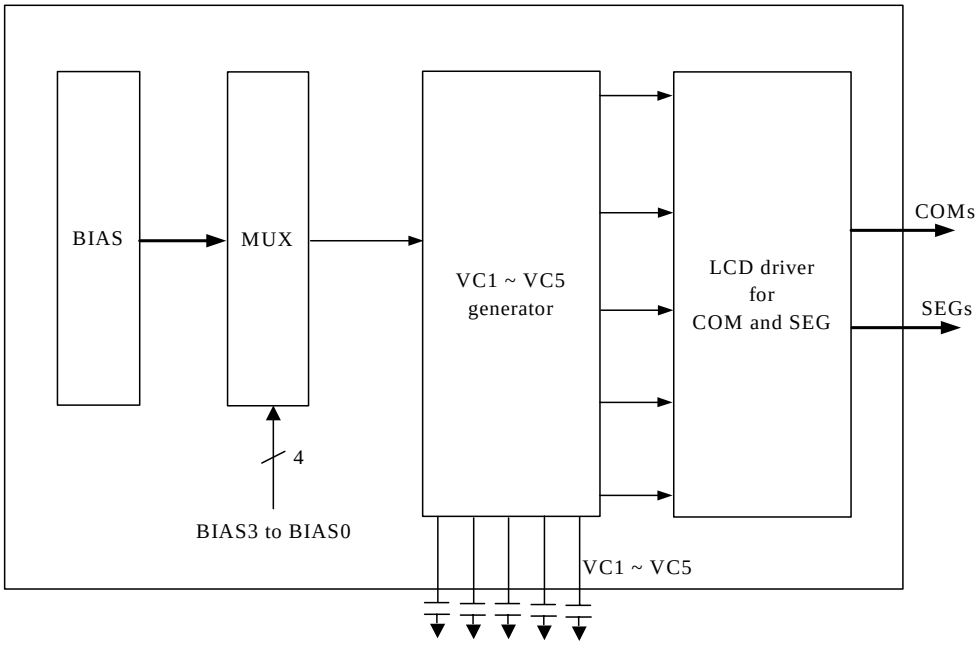


Fig.18 Correlation between Bias and V1 to V5

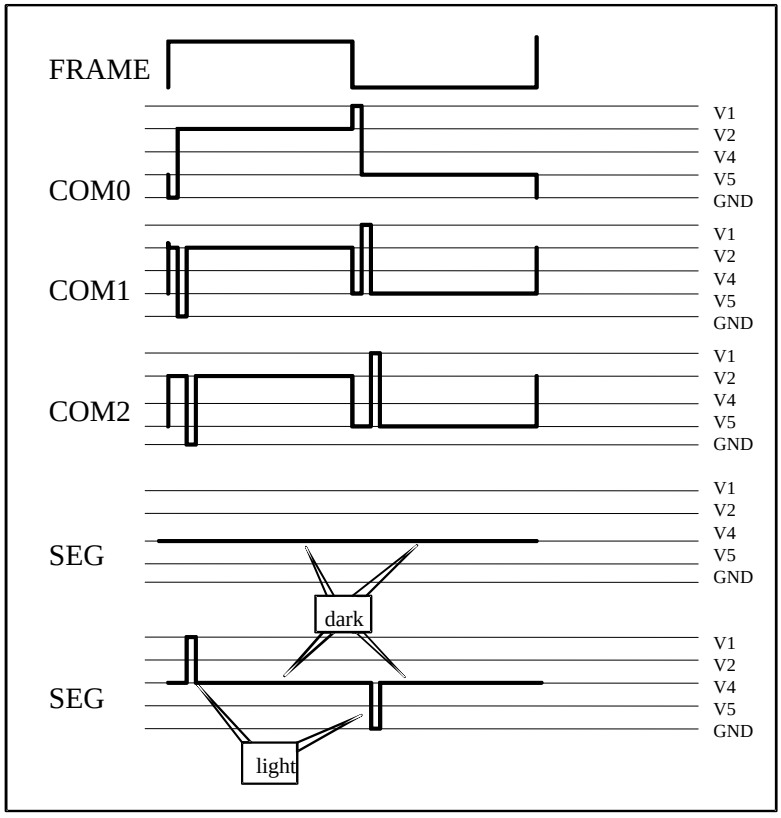


Fig.19a LCD waveform (1/4 bias) for 1/8 duty, 1/9 duty, 1/16 duty

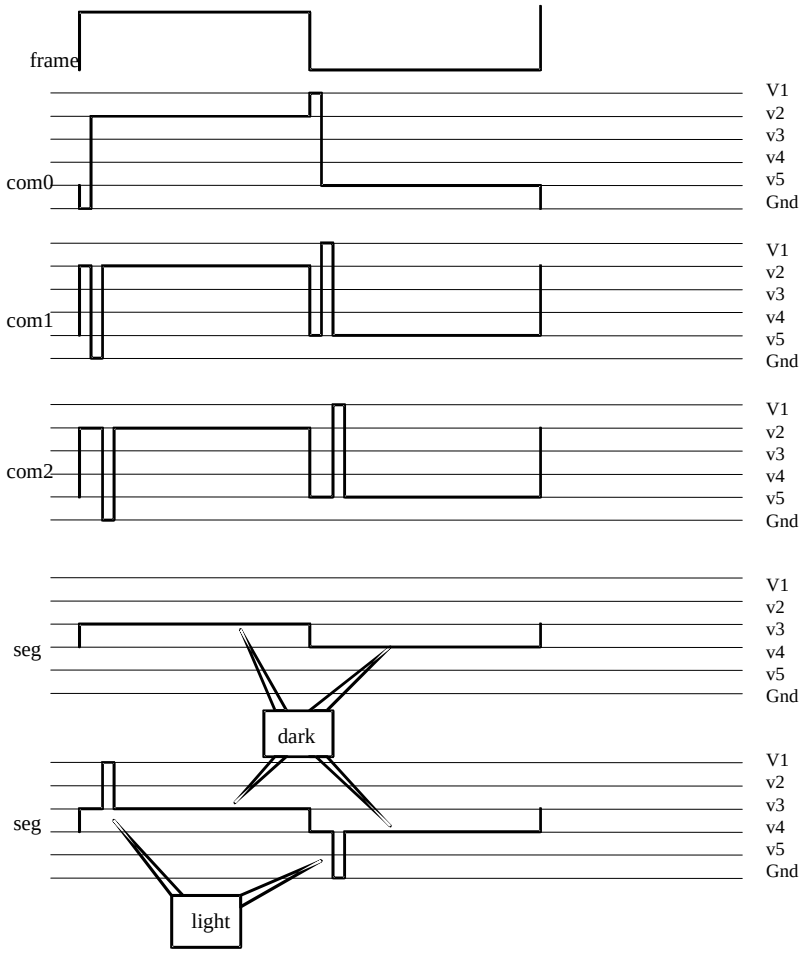


Fig.19b LCD Waveform (1/5 bias) for 1/24 duty

Bit 4 (CDAS): Current DA switch

0 = normal Port 66

1 = Current DA output

Bit 5 (KTS): Key tone output switch

0 = normal Port 67

1 = keytone output

Bit 6~Bit 7(KT0~KT1): Keytone output frequency and its power control

KT1	KT0	Keytone Frequency and Power
0	0	32.768kHz/32 = 1.024kHz clock and power enabled
0	1	32.768kHz/16 = 2.048kHz clock and enable
1	0	32.768kHz/8 = 4.096kHz clock and enable
1	1	Power off keytone

7.3.5 IOC6 (Port 6 I/O Control, CDA, Port Switch, LCD Driving Control)

- **Page 0 (Port 6 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60

Bit 0~Bit 7(IOC60~IOC67): Port 6 I/O direction control register

0 = set the relative I/O pin as output

1 = set the relative I/O pin to high impedance

- **Page 1 (Current DA Control)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAEN	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Bit 0~Bit 6(DA0~DA6): Current DA output buffer

User can use this buffer to control the output current of the current DA for driving the transistor of the speaker.

Bit 7 (DAEN): Current DA enable control

0 = disable

1 = enable

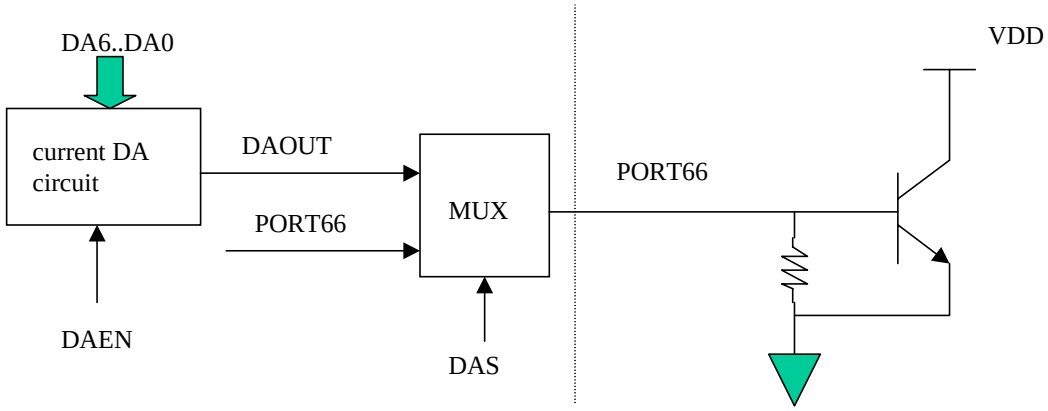


Fig.20 Current DA Structure

- **Page 2 (Port Switch, LCD Driving Ability Control)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCSH	PCSL	PBS	LCDDV1	LCDDV0	CDAL2	CDAL1	CDAL0

Bit 0~Bit 2 (DAL0~DAL1): change the output level of the current DA

CDAL2	CDAL1	CDAL0	Output Level
0	0	0	L0 (ratio = 1/8)
0	0	1	L1 (ratio = 2/8)
0	1	0	L2 (ratio = 3/8)
0	1	1	L3 (ratio = 4/8)

CDAL2	CDAL1	CDAL0	Output Level
1	0	0	L4 (ratio = 5/8)
1	0	1	L5 (ratio = 6/8)
1	1	0	L6 (ratio = 7/8)
1	1	1	L7 (ratio =1)

Bit 3~Bit 4 (LCDDV0~LCDDV1) : LCD driver's driving ability control

LCDDV1	LCDDV0	Driving mode
0	0	Normal mode (ratio = 1)
0	1	Weak mode (ratio = 1/2)
1	0	Strong mode (ratio = 2)
1	1	Maximum mode (ratio = 4)

LCDDV0 ~ LCDDV1 are used to select the driving ability of the LCD driver. The driving ability is Maximum mode > Strong mode > Normal mode > Weak mode by 1/2 ratio individually. The larger the driving ability selected, the larger the output loading of the LCD driver and the more power is allowed to be consumed. It depends on user's application.

Bit 5 (PBS): Switch I/O Port B or LCD segment output for the shared SEGxx/PBx pins

0 = select normal PB0 ~ PB7 for Port B

1 = select SEG48 ~ SEG55 output for LCD segment output

Bit 6(PCSL): Switch low nibble I/O Port C or LCD segment output for the shared SEGxx/PCx pins

0 = select normal PC0 ~ PC3 for low nibble Port C

1 = select SEG56 ~ SEG59 output for LCD SEGMENT output

Bit 7(PCSH): Switch high nibble I/O Port C or LCD segment output for the shared SEGxx/PCx pins

0 = select normal PC4 ~ PC7 for high nibble Port C

1 = elect SEG60 ~ SEG63 output for LCD SEGMENT output

7.3.6 IOC7 (Port 7 I/O Control, Key Strobe)

- **Page 0 (Port 7 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

Bit 0~Bit 7(IOC70~IOC77): Port 7 I/O direction control register

0 = set the relative I/O pin as output

1 = set the relative I/O pin to high impedance

- **Page 1 (Keystrobe Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STRB15	STRB14	STRB13	STRB12	STRB11	STRB10	STRB9	STRB8

Bit 0~Bit 7 (STRB8~STRB15): Key strobe control bits

These key strobe control registers correspond to SEGMENT8 to SEGMENT15. Refer to the Keystobe description (RE Page 0).

7.3.7 IOC8 (Port 8 I/O Control, Keystrobe)

- **Page 0 (Port 8 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80

Bit 0~Bit 7(IOC80~IOC87) : Port 8(0~7) I/O direction control register

0 = set the relative I/O pin as output

1 = set the relative I/O pin to high impedance

- **Page 1 (Key Strobe Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STRB23	STRB22	STRB21	STRB20	STRB19	STRB18	STRB17	STRB16

Bit 0~Bit 7(STRB16~STRB23): Keystrobe control bits

These key strobe control registers correspond to Segment 16 ~ Segment 23. Refer to the Keystobe description (RE Page 0).

7.3.8 IOC9 (Port 9 I/O Control, DTMF Receiver)

- **Page 0 (Port 9 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90

Bit 0~Bit 7 (IOC90~IOC97): Port 9 I/O direction control register

0 = set the relative I/O pin as output

1 = set the relative I/O pin to high impedance

- **Page 1 (DTMF Receiver)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DREN	STD	TDP2	TDP1	Q4	Q3	Q2	Q1

Bit 0~Bit 3 (Q1~Q4): DTMF receiver decoding data

This provides the code corresponding to the last valid tone-pair received (see the following code table). The STD signal, whose steering output is HI when a received tone-pair has been registered and the Q4 ~ Q1 output latch updated and generated an interrupt (IOCF has enabled), returns to LO when the voltage on ST/GT falls below Vtst.

F low	F high	Key	DREN	Q4~Q1
697	1209	1	1	0001
697	1336	2	1	0010
697	1477	3	1	0011
770	1209	4	1	0100
770	1336	5	1	0101
770	1477	6	1	0110
852	1209	7	1	0111
852	1336	8	1	1000
852	1477	9	1	1001
941	1209	0	1	1010
941	1336	*	1	1011
941	1477	#	1	1100
697	1633	A	1	1101
770	1633	B	1	1110
852	1633	C	1	1111
941	1633	D	1	0000
Any	Any	Any	0	xxxx (x:unknown)

Bit 4~Bit 5 (TDP1~TDP2): Set the current time for tone detection.

TDP2	TDP1	Tdp
0	0	20 ms
0	1	15 ms
1	0	10 ms
1	1	5 ms

Bit 6 (STD): Delayed steering output

At HI when a received tone-pair has been registered and the output latch updated; returns to LO when the voltage on St/GT falls below Vtst.

0 = invalid data

1 = valid data

Bit 7 (DREN): DTMF receiver power control

0 = power down

1 = power up

Be sure to enable the main clock before using the DTMF receiver circuit and shut down the FSK power (R9 Page 0 Bit 3 set to 0). When DREN is LO, this will shut down the device to minimize power consumption (standby mode). It stops the functions of the filters.

When independent selection of receive and pause is not required, simple steering of the circuit is applicable. Component values are chosen according to the following formula:

t REC = t DP + t GTP t ID = t DA + t GTA

The value of t DP is a parameter of the device and t REC is the minimum signal duration to be recognized by the receiver. A value of 0.1 µF for C is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t REC of 30mS would be 300k.

Different steering arrangements may be used to select independent guard-times for tone-present (tGTP) and tone-absent (t GTA). This may be necessary to meet system specifications which place the allowable limits on both the tone duration and inter digital pause.

Adjusting the guard-time also allows the designer to tailor the system parameters such as talk-off and noise immunity. Increasing tREC improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. On the other hand, a relatively short tREC with a long tDO would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs are required.

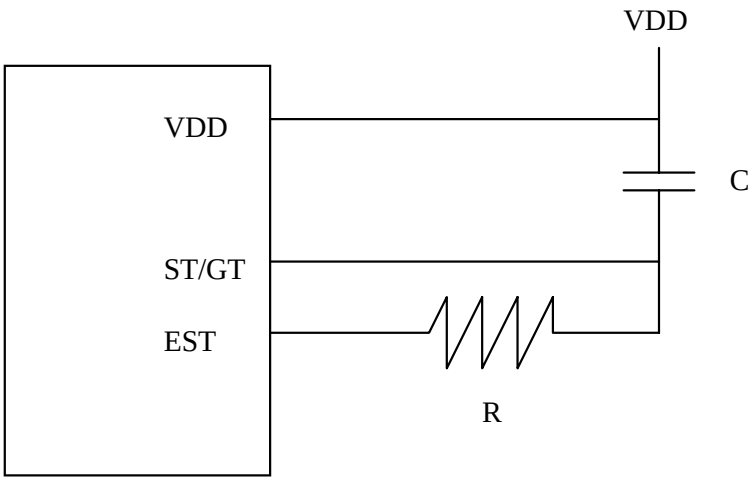


Fig.21 DTMF Receiver Delay Time Control

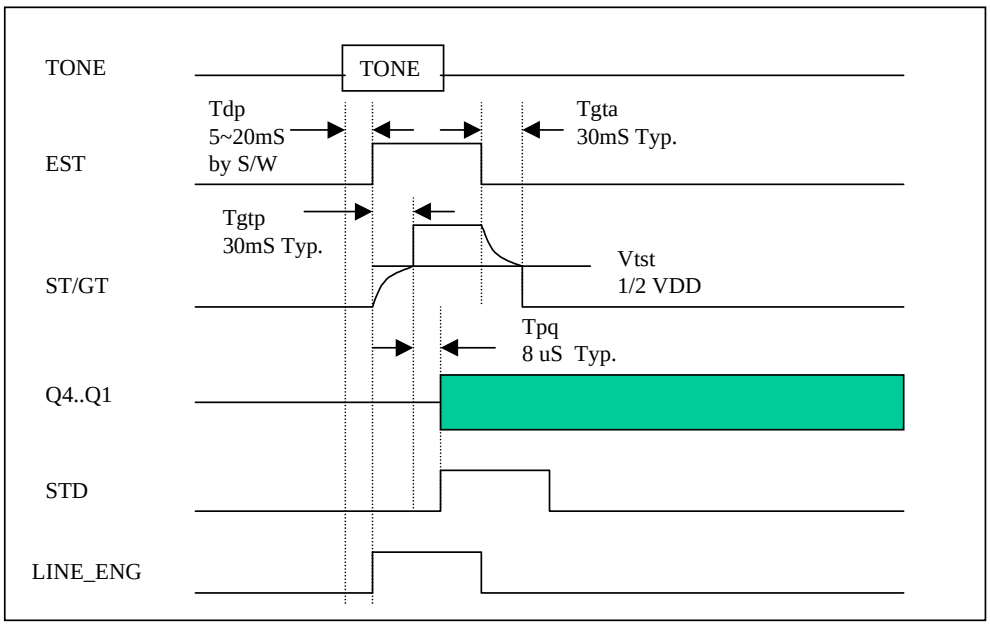


Fig.22 DTMF Receiver Timing

7.3.9 IOCA (CN1's and CN2's Clock and Scaling, Port 7 Pull-high Control)

- **Page 0 (Counter 1's and Counter 2's Clock and Scale Setting)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	C2P2	C2P1	C2P0	CNT1S	C1P2	C1P1	C1P0

Bit 0~Bit 2 (C1P0~C1P2): Counter 1 scaling

C1P2	C1P1	C1P0	Counter 1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S): Counter 1 clock source

0 = 16.384kHz

1 = instruction clock

Bit 4~Bit 6(C2P0~C2P2): Counter 2 scaling

C2P2	C2P1	C2P0	Counter 2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7 (CNT2S): Counter 2 clock source

0 = 16.384kHz

1 = instruction clock

- **Page 1 (Port 7 Pull-high Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70

Bit 0~Bit 7 (PH70~PH77): Port 7 pull high control register

0 = disable pull high function

1 = enable pull high function

7.3.10 IOCB (Port B I/O Control, Port 6 Pull-high Control)

- **Page 0 (Port B I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0

Bit 0~Bit 7(IOCB0~IOCB7): Port B I/O direction control register

0 = set the relative I/O pin as output

1 = set the relative I/O pin to high impedance

- **Page 1 (Port 6 Pull-high Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60

Bit 0~Bit 7 (PH60~PH67): Port 6 pull high control register

0 = disable pull-high function

1 = enable pull-high function

7.3.11 IOCC (Port C I/O Control, Tone 1 Control)

- **Page 0 (Port 9 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCC7	IOCC6	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0

Bit 0~Bit 7(IOCC0~IOCC7): Port C I/O direction control register

0 = set the relative I/O pin as output

1 = set the relative I/O pin to high impedance

- **Page 1 (Tone 1 Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T17	T16	T15	T14	T13	T12	T11	T10

Bit 0~Bit 7 (T10~T17): Tone Generator 1's frequency divider and power control

Must run in Normal mode.

Clock source = 111957Hz

T17~T10 = '11111111' → Tone Generator 1 will have 439 (111957/N, N=255) Hz SIN wave output.

:

:

T17~T10 = '00000010' → Tone Generator 1 will have 55978 (111957/N, N=2) Hz SIN wave output.

T17~T10 = '00000001' → DC bias voltage output

T17~T10 = '00000000' → Power off

The built-in tone generator can generate dialing tone signals for telephone dialing tone or just a single tone. In DTMF application, there are two kinds of tones. One is a group of row frequency (Tone 1), the other is a group of column frequency (Tone 2). Each group has four kinds of frequencies allowing up to 16 kinds of DTMF frequencies. The tone generator contains a row frequency sine wave generator to generate the DTMF signal and a column frequency sine wave generator to generate the DTMF signal both of which IOCD Page 1 selects. This block can generate single tone by filling one of these two registers.

If all the values are low, the tone generators will be turned off.

		Tone 2 (IOCD Page 1) High group freq.			
		1203.8Hz (0X5D)	1332.8Hz (0X54)	1473.1Hz (0X4C)	1646.4Hz (0X44)
Tone 1 (IOCC Page 1)	699.7Hz (0x0A0)	1	2	3	A
	772.1Hz (0x091)	4	5	6	B
Low group freq.	854.6Hz (0x083)	7	8	9	C
	940.8Hz (0x077)	*	0	#	D

In addition, Tone 1 and Tone 2 are asynchronous tone generators that generate Caller ID FSK signal. In FSK generator applications, Tone 1 or Tone 2 can generate 1200Hz Mark bit and 2200Hz Space bit for Bell202 or 1300Hz Mark bit and 2100Hz Space bit for V.23. See the following table.

Tone 1 (IOCC Page 1) or Tone 2 (IOCD Page 1)	Freq. (Hz)	Meaning
0x5D	1203.8	Bell202 FSK Mark bit
0x33	2195.2	Bell202 FSK Space bit
0x56	1301.8	V.23 FSK Mark bit
0x35	2112.4	V.23 FSK Space bit

7.3.12 IOCD (Counter 1 Data, Tone 2 Control)

- **Page 0 (Counter 1 Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10

Bit 0~Bit 7(CN10~CN17): Counter1's data buffer

Data can be read from and write to this buffer. Counter 1 is an 8-bit up-counter with 8-bit prescaler that can be preset or data written to, using IOCD to read data from the counter. After an interrupt, it will reload the preset value.

Example: write: IOW 0x0D ; write the data from the accumulator to Counter 1 (preset)

Example: read: IOR 0x0D ; read IOCD data and write to the accumulator

- **Page 1 (Tone 2 Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T27	T26	T25	T24	T23	T22	T21	T20

Bit 0~Bit 7 (T20~T27): Tone Generator 1's frequency divider and power control.

Refer to IOCC Page 1 Tone 1 control register for details.

7.3.13 IOCE (Counter 2 Data, Comparator and OP Control, Energy Detector)

- **Page 0 (Counter 2 Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20

Bit 0~Bit 7(CN20~CN27) : Counter 2's data buffer

Data can be read from and written to this buffer. Counter 2 is an 8-bit up-counter with 8-bit prescaler that can be preset or written to, using IOCD and read data from the counter. (write = preset) After an interrupt, it will reload the preset value.

Example: write: IOW 0x0E ; write the data from the accumulator to counter2 (preset)

Example: read: IOR 0x0E ; read IOCE data and write data to the accumulator

- **Page 1 (Comparator Reference Voltage, Port Switch)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPREF	CMPIN3	CMPIN2	CMPIN1	P5S2	P5S1	-	-

Bit 0: unused

Bit 1: unused

Bit 2~Bit 3 (P5S1~P5S2): Port 5 switch

P5S2	P5S1	Port 55	Port 56	Status
0 or 1	0	Port 55	Port 56	Normal Port 5 I/O
0 or 1	1	STGT	EST	DTMF receiver I/O

External reference signal

The analog signal that is presented at Cin- compares to the signal at Cin+, and the digital output of the comparator is adjusted accordingly.

* The reference signal must be between Vss and Vdd.

* For threshold detector applications, the same reference may be used.

* The comparator can operate from the same or different reference source.

Bit 4 (CMPIN1): Switch for controlling Port 63 as I/O Port or a comparator input

0 = I/O Port 63

1 = comparator input

Bit 5 (CMPIN2): Switch for controlling Port 64 as I/O Port or a comparator input

0 = I/O Port 64

1 = comparator input

Bit 6 (CMPIN3): Switch for controlling Port 65 as I/O Port or a comparator input

0 = I/O Port 65

1 = comparator input

Bit 7 (CMPREF): Switch for comparator reference voltage

0 = internal reference voltage

1 = external reference voltage

- **Page 2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRSEL	-	-	-	CW_SMB	-	-	-

Bit 0: unused

Bit 1: unused

Bit 2: unused

Bit 3 (CW_SMB): Call Waiting / short message receiver switch

0 = enable Short message mode ±5.5% CAS tone acceptable frequency range (Protocol: ±5%)

1 = enable Call Waiting mode. The acceptable CAS tone frequency range is determined by Code Option Register Bit 5 (0: for Europe and USA / 1: for China)

Bit 4: unused

Bit 5: unused

Bit 6: unused

Bit 7 (VRSEL): Reference voltage VR selection bit for the comparator

0/1 → VR = VDD/VR = 2.0V, When this bit is set to "0", V2_0 ref. circuit will be powered off.

The 2.0V reference circuit is only powered on when this bit and RD Page 0 Bit 7 (CMPEN) are all set to "1".

7.3.14 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBF/STD	FSK/CW	INT2	INT1	INT0	CNT2	CNT1	TCIF

Bit 0 ~ Bit 7: Interrupt enable bits

0 = disable interrupt

1 = enable interrupt

7.4 I/O Port

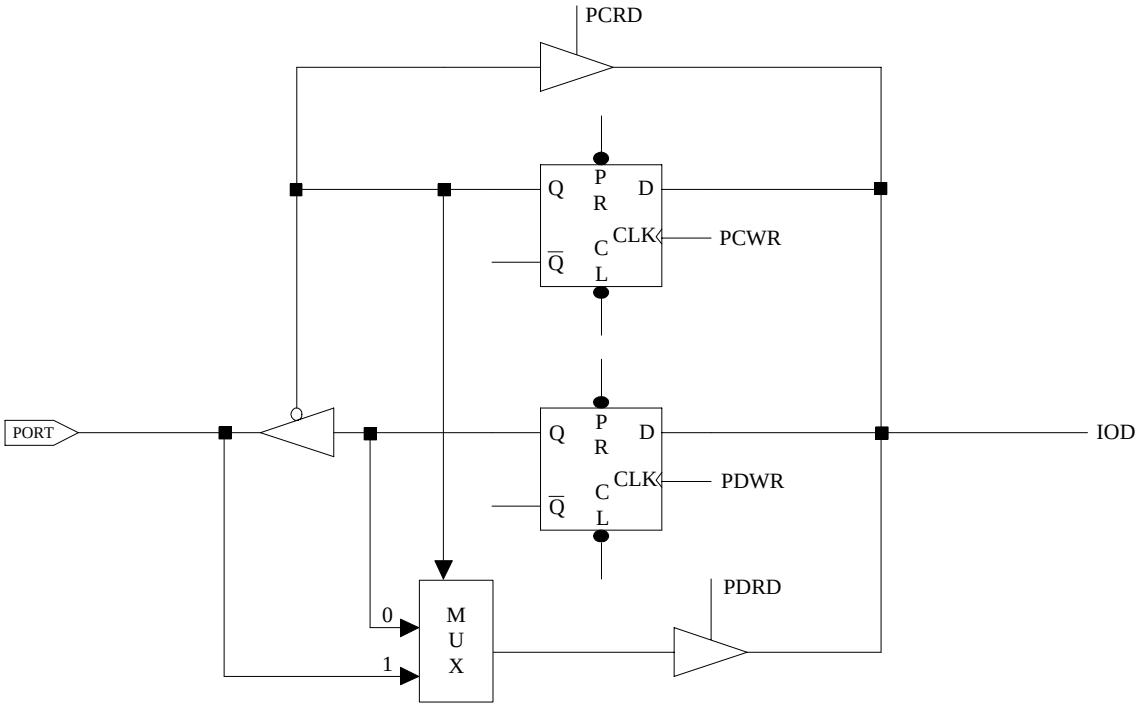


Fig.25 I/O Port and I/O Control Register Circuit

The I/O registers are bi-directional, tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.25

7.5 Reset

The following conditions trigger a Reset function:

(1) Power-on voltage detector reset (POVD) and power-on reset

(2) WDT timeout. (if enabled in Green or Normal mode)

(3) /RESET pin is set to low

Note

For Case (1), POVD is controlled by Code Option. If POVD is enabled, the CPU will reset at under 2V. The CPU will consume more current (about 3μA). This power-on reset is always enabled on the circuit. It will reset the CPU at 1.4V and power consumption at 0.5μA.

Once a Reset occurs, the following functions are performed:

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to "1"
- The values for the other registers (Bit 7~Bit 0) are set to the values as shown in the table below. (x = don't care)

Address	R Register Page 0	R Register Page 1	IOC Register Page 0	IOC Register Page 1	IOC Register Page 2
4	00xxxxxx	00000000			xxxxxxxx
5	xxx00000	xxxxxxxx	11100000	00000000	00000000
6	xxxxxxxx	xxxxxxxx	11111111	00000000	00000000
7	xxxxxxxx	xxxxxxxx	11111111	11111111	xxxxxxxx
8	xxxxxxxx	xxxxxxxx	11111111	11111111	xxxxxxxx
9	xxxxxxxx	xxxxxxxx	11111111	00000000	xxxxxxxx
A	00000xx0	xxxxxxxx	00000000	00000000	xxxxxxxx
B	xxxxxxxx	xxxxxxxx	11111111	00000000	xxxxxxxx
C	xxxxxxxx	xxxxxxxx	11111111	00000000	xxxxxxxx
D	00000000	xxxxxxxx	00000000	00000000	xxxxxxxx
E	00000000	00xxxxxx	00000000	00000000	00000000
F	00000000	-	00000000	-	

7.6 Wake-up

The controller has two types of sleep mode for power saving.

(1) Sleep mode, RA(7)=0 + "SLEP" instruction

The controller will turn off all the CPU and crystal. Turn off the other circuits with power control like keytone control or PLL control (which enables the register), by software.

The following triggers Wake-up from Sleep mode"

(1) WDT time out

(2) External interrupt

(3) /RESET pin is set to low

All the above cases will reset the controller, and run the program at address zero. The result is similar to a power-on reset. Be sure to enable the WDT timer and the external register cases (1) and (2) respectively.

7.7 Interrupt

RF is the interrupt status register which records the interrupt request using a flag. IOCF is the interrupt mask register. TCC timer, Counter 1 and Counter 2 are the internal interrupt sources. P70 ~ P77 (INT0 ~ INT1) are external interrupt input where interrupt sources come from. If the interrupts are caused by these interrupt sources, then RF will generate a '1' flag to the corresponding register if the IOCF register is enabled. Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) is generated, this will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

7.8 Instruction Set

The instruction set has the following features:

1) Every bit of any register can be set, cleared, or tested directly.
2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The following symbols are used in the Instruction Set table**:**

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z, C, DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1

Binary Instruction	Hex	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z	1
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z	1
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None	1
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None	1
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None	1
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z	1
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC	1
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1 1110 100k kkkk	1E8k	PAGE k	K->R5(4:0)	None	1
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC	1

7.9 Code Option Register

The controller has one Code option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

7.9.1 Code Option Register1 (Program ROM)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	/POVD	CWMODE	PACKSEL1	PACKSEL0	-

Bits 1~2 (PACKSEL0~PACKSEL1): package select

PACKSEL1	PACKSEL0	Package	PS
X	1	132 pin die	-
1	0	128 pin QFPA	PC0~PC3 floating

Bit 3 (CWMODE): Select acceptable CAS tone frequency range (2130 Hz plus 2750 Hz)

0 = set the acceptable Call Waiting frequency range to ±2% .(Recommended in China where the acceptable range = ±1.5%)

1 = set the acceptable Call Waiting frequency range to ±1.2% (Recommended for Europe and USA where the acceptable range=: ±0.5%)

Bit 4 (/POVD): Power-on voltage detector

0 = enable

1 = disable

/POVD	2.2V /POVD Reset Voltage	2.2V Power-on Reset Voltage	Sleep Mode Current (VDD=5V)
1	No	Yes (2.2V)	1μA
0	Yes (2.2V)	No	15μA

7.10 Call Waiting Function Description

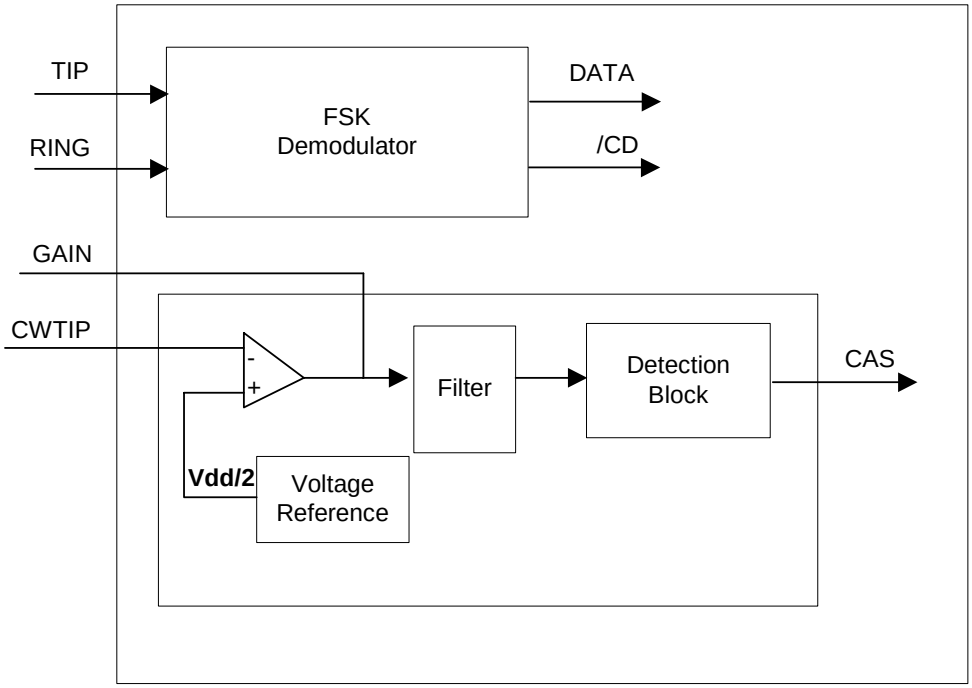


Fig.26 Call Waiting Block Diagram

The Call Waiting service works by alerting a customer engaged in a telephone call to a new incoming call. This allows the customer to receive important calls while engaged in the current call. The Call Waiting Decoder can detect CAS (Call-Waiting Alerting Signal 2130Hz plus 2750Hz) and generate a valid signal on the data pins.

The call waiting decoder is designed to support the Caller Number Deliver feature, which is offered by the local phone companies.

In a typical application, after enabling the CW circuit (by IOC5 Page 0 Bit 4 CWPWR), this IC receives Tip and Ring signals from the telephone wire. The signals as inputs for the pre-amplifier, and the amplifier sends input signal to a band pass filter. Once the signal is filtered, the Detection block decodes the information and sends it to R3 register Bit 7. The output data is then made available at R3 CAS bit.

Data is from the CAS signals. During normal operation, CAS is set to high. When this IC detects 2130Hz and 2750Hz frequencies, then CAS is set to low.

8 Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.3 To 6	V
Input Voltage	Vin	-0.5 to VDD +0.5	V
Operating Temperature Range	Ta	0 to 70	℃

9 DC Electrical Characteristic

Operation Current Consumption for Analog Circuit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operation current for FSK	I_FSK	VDD=5V, CID power on	-	2.0	-	mA
		VDD=3V, CID power on	-	1.8	-	
Operation current for CW	I_CW	VDD=5V, CID power on	-	1.8	-	mA
		VDD=5V, CID power on	-	1.5	-	
Operation current for DTMF receiver	I_DR	VDD=3V, DTMFr power on	-	1.8	-	mA
		VDD=3V, DTMFr power on	-	1.5	-	
Operation current for Tone generator	I_DTMF	VDD=5V, DTMF power on	-	0.35	-	mA
		VDD=3V, DTMF power on	-	0.15	-	
Operation current for Current DA	I_DA	VDD=5V, CDA power on	-	-	-	mA
		VDD=3V, CDA power on	-	-	-	
Operation current for OP	I_OP	VDD=5V, PT power on	-	0.17	-	mA
		VDD=3V, PT power on	-	0.1	-	
Operation current for Comparator	I_CMP	VDD=5V, PT power on	-	0.17	-	mA
		VDD=3V, PT power on	-	0.1	-	

Current DA Output Current

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current DA output current	I_DAO	VDD=5V, CDA power on	-	-	-	mA
		VDD=3V, CDA power on	-	-	-	

Ta=0°C ~ 70°C, VDD=5V±5%, VSS=0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Leakage Current for input pins	IIL1	VIN = VDD, VSS	-	-	±1	μA
Input Leakage Current for bi-directional pins	IIL2	VIN = VDD, VSS	-	-	±1	μA
Input High Voltage	VIH	-	2.0	-	-	V
Input Low Voltage	VIL	-	-	-	0.8	V
Input High Threshold Voltage	VIHT	/RESET, TCC, RDET1	2.0	-		V
Input Low Threshold Voltage	VILT	/RESET, TCC, RDET1	-	-	0.8	V
Clock Input High Voltage	VIHX	OSCI	1.8	-		V
Clock Input Low Voltage	VILX	OSCI		-	1.2	V
Output High Voltage (Ports 5, 8, 9, B, C)	VOH1	IOH = -5mA	2.0	-	-	V
(Ports 6, 7)	-	IOH = -8mA	2.0	-	-	V
Output Low Voltage (Port 5, 8, 9, B, C)	VOL1	IOL = 5mA	-	-	0.4	V
(Ports 6,7)	-	IOL = 8mA	-	-	0.4	V
Pull-high current	IPH	Pull-high active input pin at VSS	-	-10	-15	μA
Power down current (Sleep mode)	ISB1	All input and I/O pin at VDD, Output pin floating, WDT disabled	-	1	4	μA
Low clock current (Green mode)	ISB2	CLK=32.768kHz, All analog circuit disabled, All input and I/O pin at VDD, Output pin floating, WDT disabled, LCD enabled	-	50	80	μA
Operating supply current (Normal mode)	ICC	/RESET=High, PLL enabled CLK=3.579MHz, LCD enabled, Output pin floating All analog circuit disable	-	1.0	1.3	mA
Tone generator reference voltage	Vref2	-	0.5	-	0.7	VDD

10 AC Electrical Characteristic

10.1 CPU Instruction Timing (Ta=0°C ~ 70°C, VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.579MHz		60 550		us ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		16		ms

Note: N = selected prescaler ratio

10.2 FSK AC Characteristic (Vdd=5V,Ta=+25°C)

Characteristic	Min.	Typ.	Max.	Unit
FSK Sensitivity				
Low Level Sensitivity Tip & Ring @SNR 20dB	-40	-48	-	dBm
High Level Sensitivity Tip & Ring @SNR 20dB	-	0	-	dBm
Signal Reject	-	-51	-	dBm
FSK Twist				
Positive Twist (High Level)	+10	-	-	dB
Positive Twist (Low Level)	+10	-	-	dB
Negative Twist (High Level)	-6	-	-	dB
Negative Twist (Low Level)	-6	-	-	dB

10.3 CW AC Characteristic (Vdd=5V, Ta=+25°C)

Characteristic	Min.	Typ.	Max.	Unit
CW Sensitivity				
Sensitivity @SNR 20dB	-	-38	-	dBm
Low Tone Frequency 2130Hz	-	±1.2	-	%
High Tone Frequency 2750Hz	-	±1.2	-	%
CW Twist				
Twist	±7	-	-	dB

10.4 DTMFr (DTMF Receiver) AC Characteristic

Vdd=5V, Ta=+25°C

Characteristic	Min.	Typ.	Max.	Unit
DTMFr				
Low Level Signal Sensitivity	-	-36	-	dBm
High Level Signal Sensitivity	-	0	-	dBm
Low Tone Frequency	-	±2	-	%
High Tone Frequency	-	±2	-	%
DTMFr Noise Endurance				
Signal to noise ratio	15	-	-	dB

10.5 Tone Generators for AC Characteristic

Vdd=5V, Ta=+25°C

CHARACTERISTIC	Min.	Typ.	Max.	Unit
Tone 1/Tone 2 signal strength (root mean square voltage)				
Tone1 signal strength V1rms (ps1)	130	155	180	mV
Tone2 signal strength V2rms (ps1)	1.259V1rms			mV
Tone Twist				
(Tone 1 – Tone 2) twist		-2		dB
Tone Frequency Deviation				
Frequency deviation			±1	%

(ps1) : V1rms and V2rms has 2 dB difference. It means 20log(V2rms/V1rms) = 20log1.259 = 2 (dB)

10.6 Timing Characteristic (Vdd=5V, Ta=+25°C)

Description		Symbol	Min.	Typ.	Max.	Unit
Oscillator Timing Characteristic						
OSC start up	32.768kHz	Tosc	-	-	400	ms
	3.579MHz PLL		-	-	10	
FSK Timing Characteristic						
Carrier detect low		Tcdl	-	10	14	ms
Data out to Carrier det low		Tdoc	-	10	20	ns
Power up to FSK(setup time)		Tsup	-	15	20	ms
End of FSK to Carrier Detect high		Tcdh	-	-	4	ms
CW Timing Characteristic						
CAS input signal length (2130, 2750 Hz @ -20dBm)		Tcasi	-	80	-	ms
Call waiting data detect delay time		Tcwd	-	42	-	ms
Call waiting data release time		Tcwr	-	26	-	ms

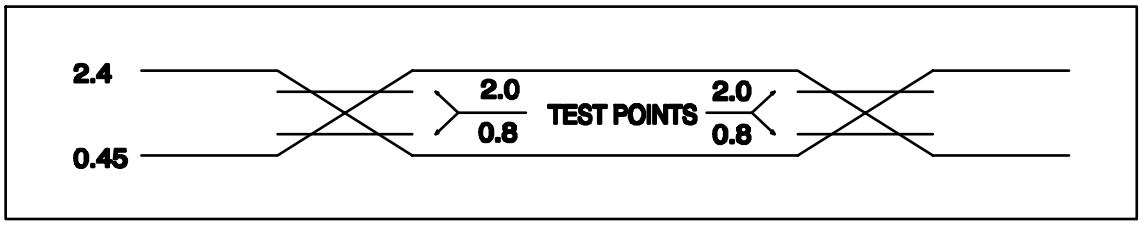
Description	Symbol	Min.	Typ.	Max.	Unit
DTMF Receiver Timing Characteristic					
Tone Present Detection Time	Tdp		(ps1)		
the guard-times for tone-present (C=0.1uF, R=300K)	Tgtp		30		ms
the guard-times for tone-absent (C=0.1uF, R=300K)	Tgta		30		mS
Propagation Delay (St to Q)	Tpq		8		us
Tone Absent Detection Time	Tda		(ps2)		ms
SPI Timing Characteristic (CPU Clock 3.58MHz and Fsco = 3.58Mhz /2)					
/SS set-up time	Tcss	560	-	-	ns
/SS hold time	Tcsh	250	-	-	ns
SCLK high time	Thi	250	-	-	ns
SCLK low time	Tlo	250	-	-	ns
SCLK rising time	Tr	-	15	30	ns
SCLK falling time	Tf	-	15	30	ns
SDI set-up time to the reading edge of SCLK	Tisu	25	-	-	ns
SDI hold time to the reading edge of SCLK	Tihd	25	-	-	ns
SDO disable time	Tdis	-	-	560	ns

(ps1) : Controlled by software

(ps2) : Controlled by RC circuit.

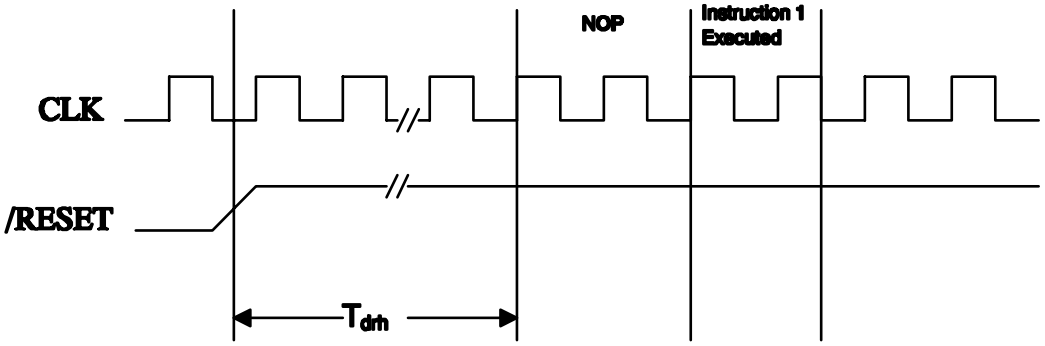
11 Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

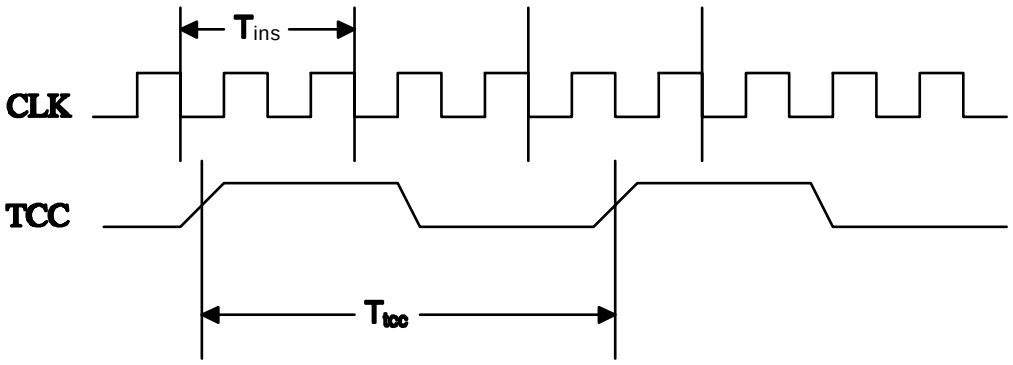


Fig.28 AC timing

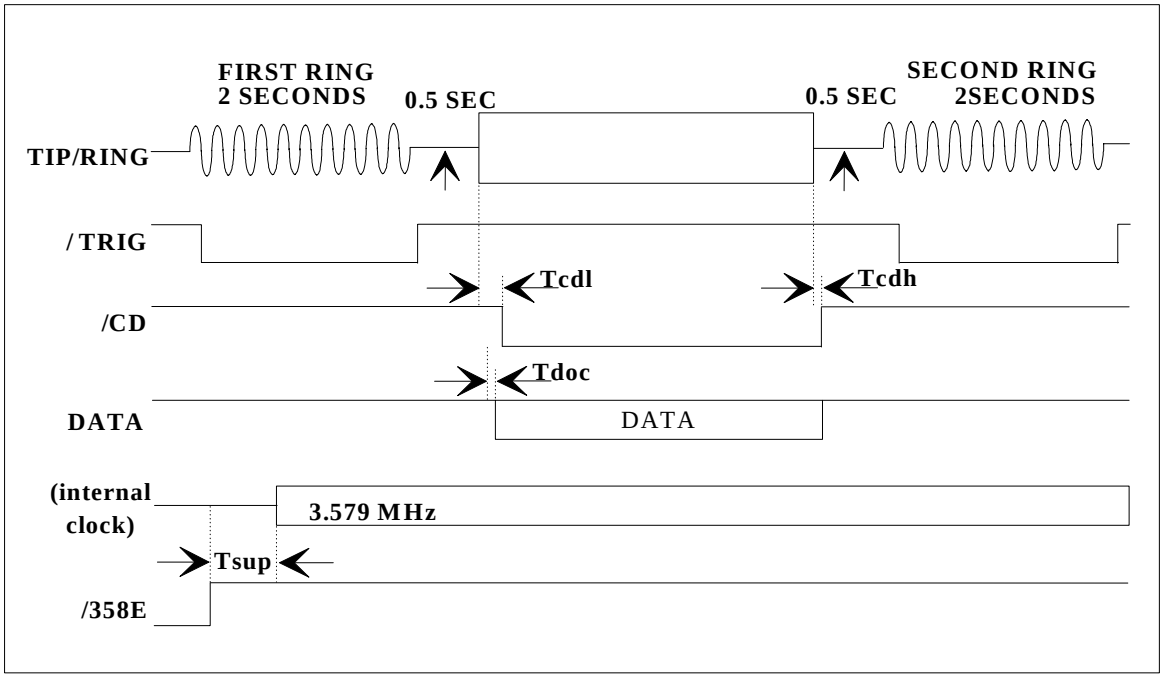


Fig. 29 FSK Timing Diagram

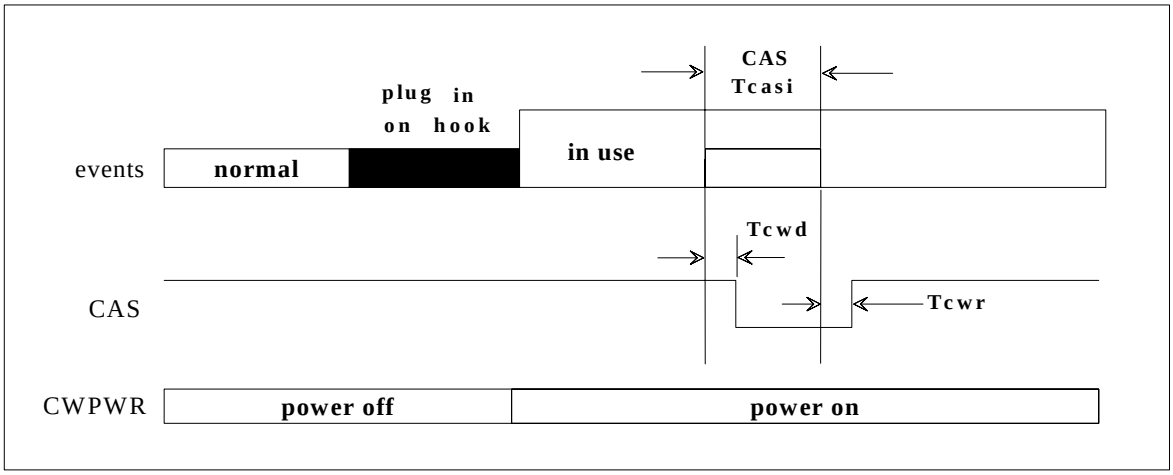


Fig. 30 Call Waiting Timing Diagram

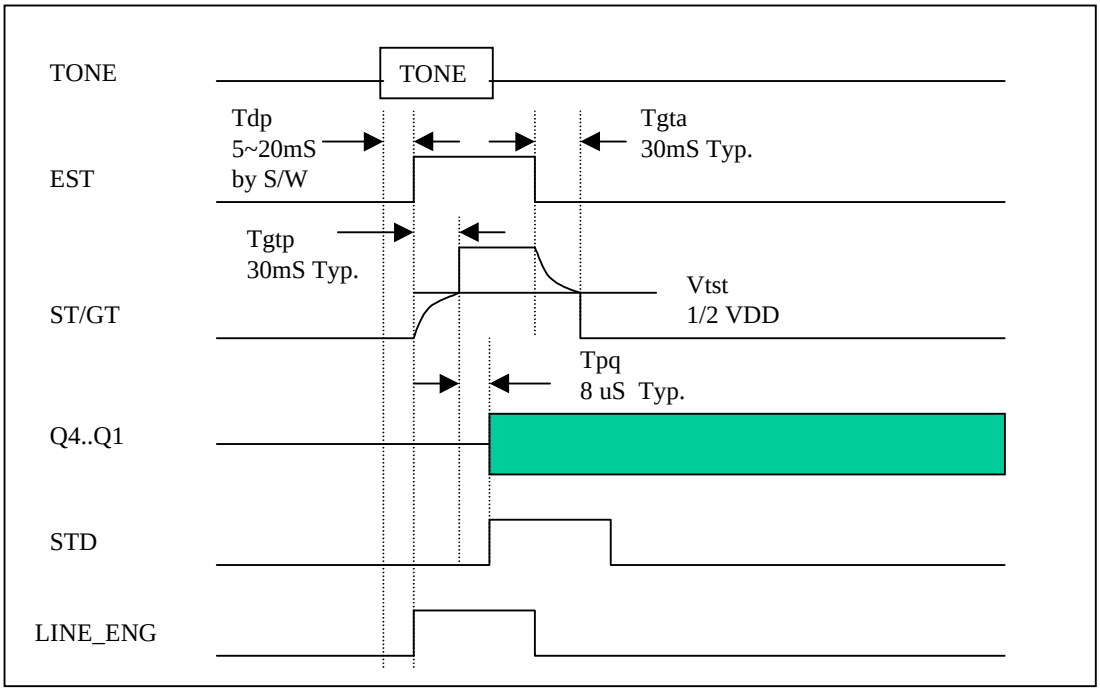


Fig. 31 DTMF Receiver Timing Diagram