
EM78470N

**8-Bit Microprocessor
with OTP ROM**

**Product
Specification**

DOC. VERSION 1.1

ELAN MICROELECTRONICS CORP.


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Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2012/08/10
1.1	1. Added LVR specifications 2. Added Device Characteristics Curve	2013/05/06



1 General Description

The EM78470N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It is integrated with Watchdog Timer (WDT), Data RAM, ROM, programmable real time clock counter, internal/external interrupt, power-down mode, LCD driver, infrared transmitter function, and tri-state I/O. The microprocessor is equipped with an on-chip 4K×13-bit Electrical Mask Read Only Memory (Mask-ROM) and provides multi-protection bits to prevent intrusion of user's Mask memory code. Seven Code option bits are available for user's requirements. Special 13 bits customer ID options are also provided.

2 Features

- CPU Configuration:
 - 4K×13 bits on-chip Mask-ROM
 - 144 bytes general purpose register
 - 128 bytes on-chip data RAM
 - 272 bytes SRAM
 - 8-level stacks for subroutine nesting
- I/O Port Configuration:
 - Typically, 12 bidirectional tri-state I/O ports
 - 13 bidirectional tri-state I/O ports shared with LCD segment output pin
 - Up to 25 bidirectional tri-state I/O ports
- Operating Voltage and Temperature Range:
 - Commercial: 1.9V ~ 3.6 V (at 0°C~+70°C)
 - Industrial: 2.1V ~ 3.6 V (at -40°C ~+85°C)
- Operating Mode:
 - Normal Mode: the CPU operates on main oscillator frequency (Fm)
 - Green Mode: the CPU operates on sub-oscillator frequency (Fs) and the main oscillator (Fm) is stopped
 - Idle Mode: CPU is idle, LCD display remains working
 - Sleep Mode: the whole chip stops working
 - Operation speed: DC ~ 10 MHz clock input
 - Dual clock operation
- Oscillation Mode:
 - High frequency oscillator can be selected from among the Crystal, RC, or PLL (phase lock loop)
 - Low frequency oscillator can select between Crystal and RC modes
- Peripheral Configuration:
 - 8-bit real Time Clock/Counter (TCC)
 - One infrared transmitter / PWM generator
 - Four sets of 8-bit auto reload count-down timers which can be used as interrupt sources:
 - ◇ Counter 1: Independent count- down timer
 - ◇ Counter 2: High Pulse Width Timer (HPWT) and Low Pulse Width Timer (LPWT) shared with IR function.
 - ◇ Programmable free running on-chip watchdog timer (WDT). This function operates under Normal, Green, and Idle modes.
 - Input port wake-up function (Port 6, Port 8). Works under Idle and Sleep modes.
 - Power-on reset and 3 programmable Level Voltage Reset
POR: 1.8V (Default), LVR :2.7V, 2.4V, 2.1V
- Eight Interrupt Sources: 3 External and 5 Internal:
 - Internal interrupt source: TCC; Counters 1, 2; and High/Low pulse width timer.
 - External interrupt source: INT0, INT1, and Pin change wake-up (Port 6 and Port 8)
- LCD Circuit:
 - Common driver pins: 4
 - Segment driver pins: 17
 - LCD Bias: 1/3, 1/2 bias
 - LCD Duty: 1/4, 1/3, 1/2 duty
- Package Type:
 - Dice 44-pin EM78470NH
 - LQFP 44-pin EM78470NL44 (10mm × 10mm)

3 Pin Configuration (Package)

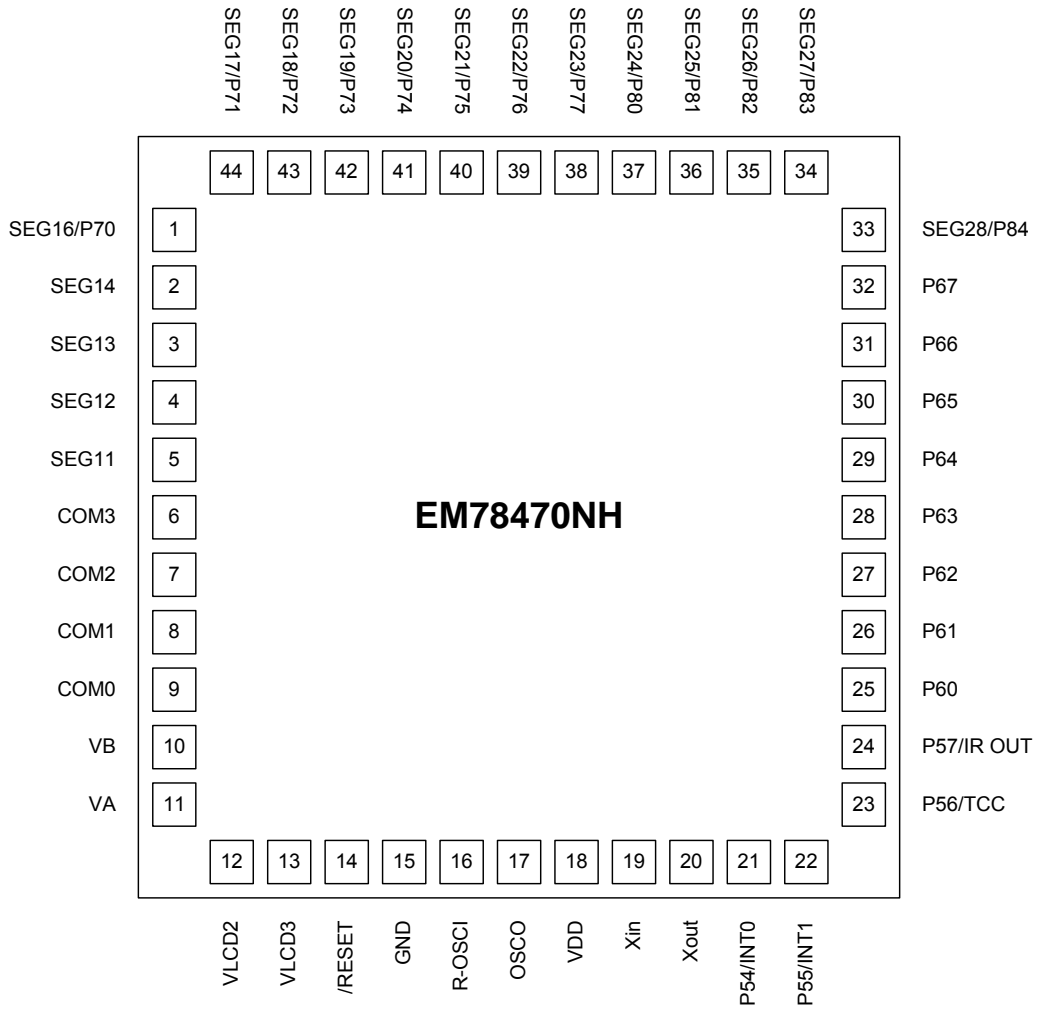


Figure 3-1 EM78470NH Pin Configuration

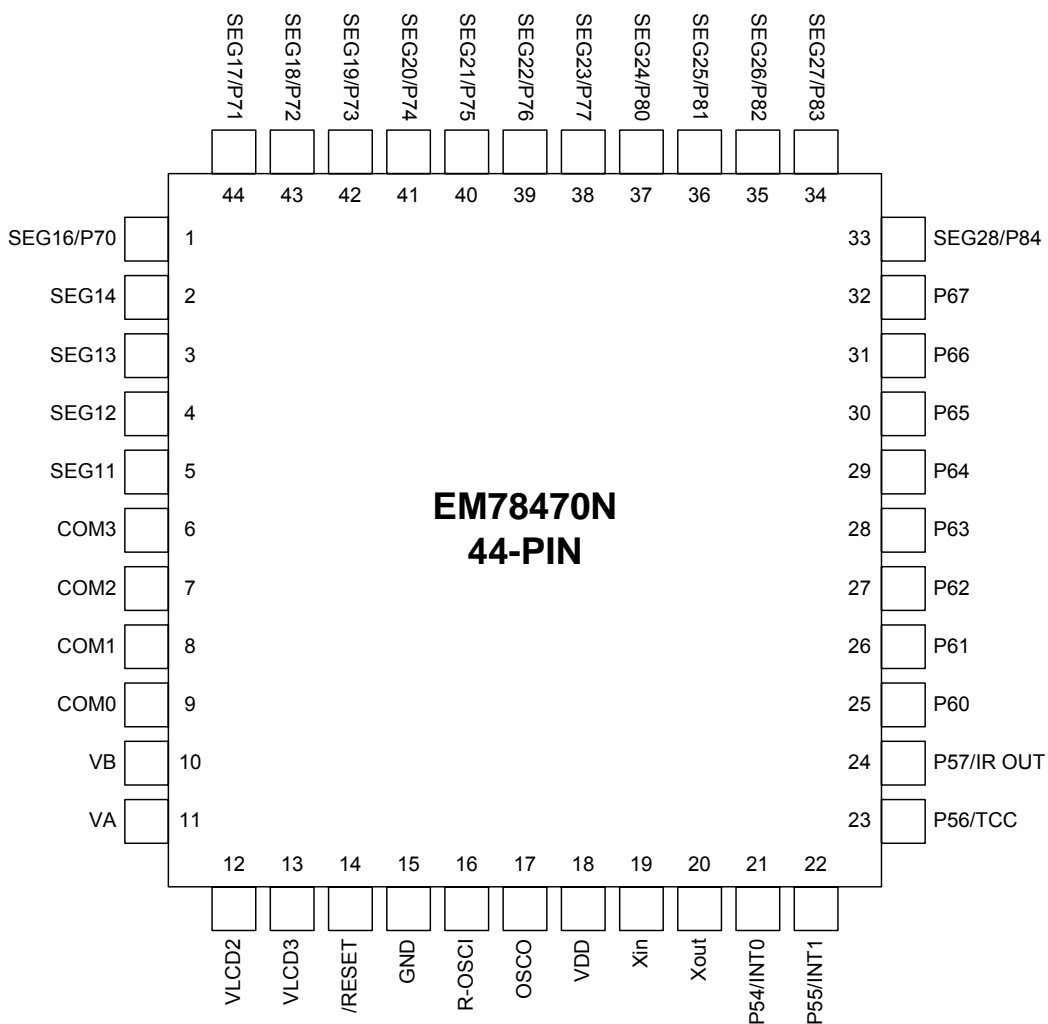


Figure 3-2 EM78470NL44

4 Pin Description

Name	Function	Input Type	Output Type	Description
P54/INT0	P54	ST	CMOS	Bidirectional I/O pin
	INT0	ST	-	External interrupt pin. INT0 interrupt source can be set to falling or rising edge by IOC71 register Bit 7 (INT_EDGE). Wakes up from Sleep mode and Idle mode when the pin status changes.
P55/INT1	P55	ST	CMOS	Bidirectional I/O pin
	INT1	ST	-	External interrupt pin Interrupt source is a falling edge signal. Wakes up from Sleep mode and Idle mode when the pin status changes.
P56/TCC	P56	ST	CMOS	Bidirectional I/O pin .. This pin works in Normal/Green/Idle mode.
	TCC	ST	-	External input pin of TCC
P57/IROUT	P57	ST	CMOS	Bidirectional I/O pin. This pin is capable of sinking 20mA/3V.
	IROUT	ST	-	IR/PWM mode output pin
P60	P60	ST	CMOS	Programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P61	P61	ST	CMOS	Programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P62	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P63	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P64	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P65	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P66	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P67	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.



(Continuation)

Name	Function	Input Type	Output Type	Description
COM0~3	COM0~3		AN	LCD common output pin
SEG11~15	SEG11~15		AN	LCD segment output pin
SEG16/P70	SEG16		AN	LCD segment output pin
	P70	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG17/P71	SEG17		AN	LCD segment output pin
	P71	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG18/P72	SEG18		AN	LCD segment output pin
	P73	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG19/P73	SEG19		AN	LCD segment output pin
	P73	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG20/P74	SEG20		AN	LCD segment output pin
	P74	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG21/P75	SEG21		AN	LCD segment output pin
	P75	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG22/P76	SEG22		AN	LCD segment output pin
	P76	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG23/P77	SEG23		AN	LCD segment output pin
	P77	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG24/P80	SEG24		AN	LCD segment output pin
	P80	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG25/P81	SEG25		AN	LCD segment output pin
	P81	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.

(Continuation)

Name	Function	Input Type	Output Type	Description
SEG26/P82	SEG26		AN	LCD segment output pin
	P82	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG27/P83	SEG27		AN	LCD segment output pin
	P83	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG28/P84	SEG28		AN	LCD segment output pin
	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
VB	VB		AN	Connects capacitors for LCD bias voltage
VA	VA		AN	Connects capacitors for LCD bias voltage
VLCD2	VLCD2		AN	One of LCD bias voltage
VLCD3	VLCD3		AN	One of LCD bias voltage
/RESET	/RESET	ST		General-purpose Input only Low active. If it remains at logic low, the device will reset. /RESET pin for writer programming
R-OSCI	R-OSCI	AN		In Crystal mode: crystal input In RC mode: pull-high resistor In PLL mode: connect 0.01 μ F capacitor to GND Connect 0.01 μ F capacitor to GND and code option selects PLL mode when high oscillator is not used.
OSCO	OSCO		XTAL	In Crystal mode: crystal input
Xin	Xin	XTAL		In Crystal mode: Input pin for sub-oscillator. Connect to a 32.768kHz crystal.
Xout	Xout		XTAL	In Crystal mode: Connect to a 32.768kHz crystal. In RC mode: instruction clock output
VDD	VDD	Power		Power
GND	GND	Power		Ground

Legend: ST : Schmitt Trigger input

AN : Analog pin

XTAL : Oscillation pin for crystal/resonator

CMOS : CMOS output

Pin control condition repeat function starting capability

Pin Function	I/O Status		Pin Control		
	I/O Direction	Pin Change WK/Int.	Pull High	Pull Low	O.D.
General Input	Input	S/W	S/W	S/W	S/W
General Output	Output	Disable	S/W	S/W	S/W
TCC	Input	Disable	S/W	S/W	S/W
EX_INT	Input	Disable	S/W	S/W	S/W
LCD Driver	Input	Disable	Disable	Disable	S/W

Disable → forced to shutoff

Enable → forced to open

S/W → The initial value in the control register is set as “Disable”.

1. For non-I/O function, the Pin Change Wake-up/Interrupt function should be disabled
2. Priority: Analog function > Output Digital Function > Input Digital Function > General I/O Function

5 Functional Block Diagram

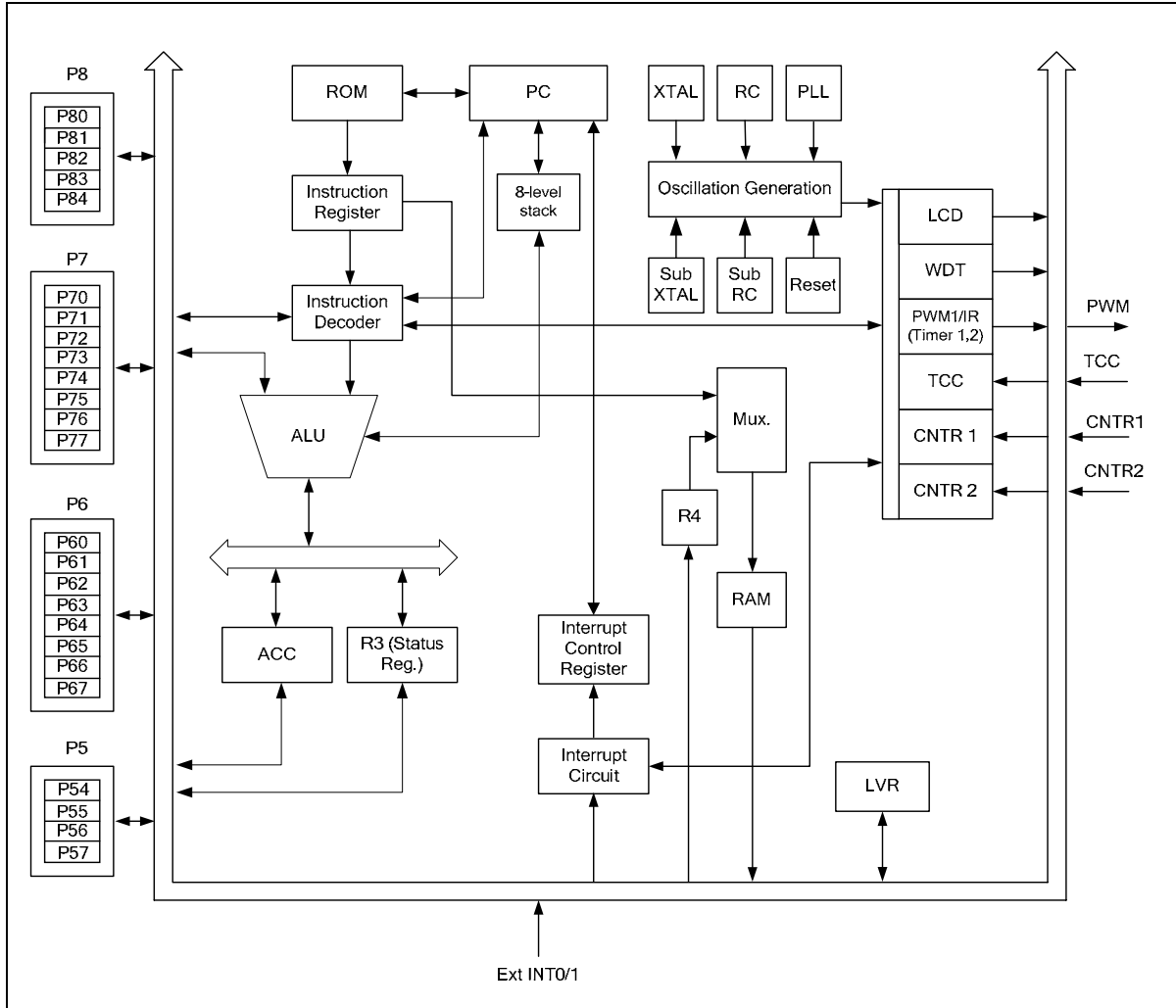


Figure 5-1 EM78470N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 BSR (Bank Selection Control Register)

The Timer Clock Counter is increased by an external signal edge applied to TCC, or by the instruction cycle clock. Written and read by the program as any other register.

6.1.3 R2/PC (Program Counter)

- The R2 structure is depicted in Figure 6-1 shown below.

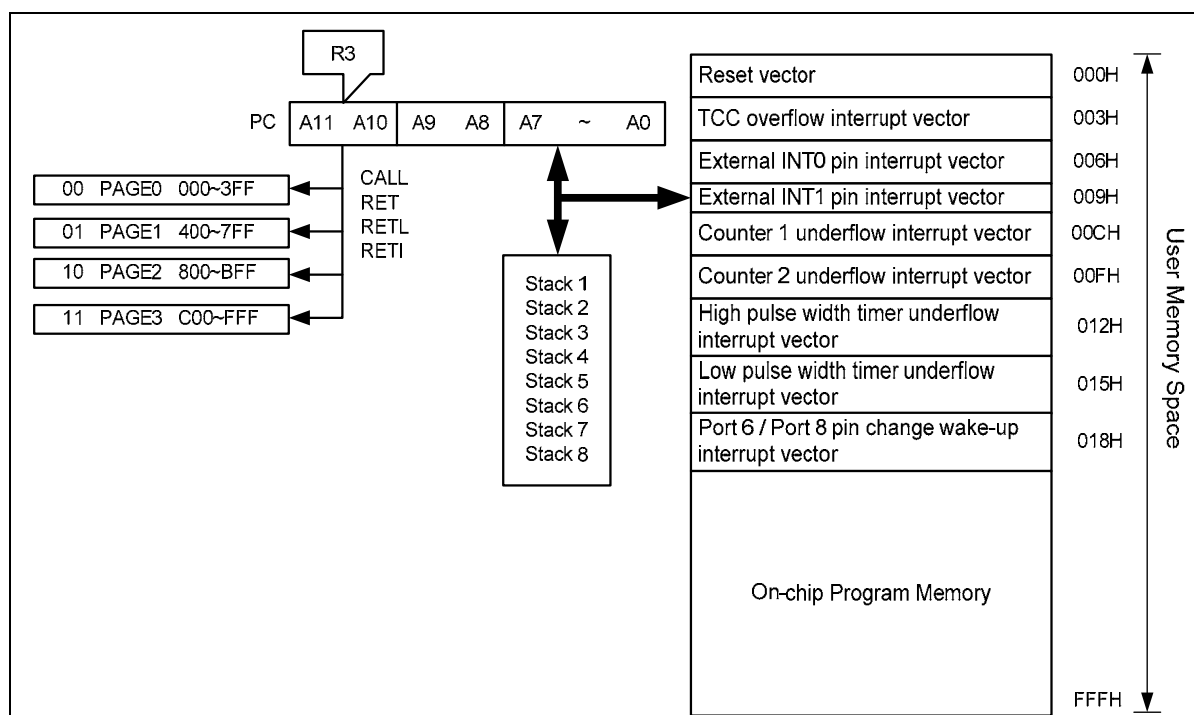


Figure 6-1 Program Counter Organization

- The configuration structure generates 4K×13 bits on-chip ROM addresses to the relative programming instruction codes.
- The contents of R2 are all set to "0"s when a Reset condition occurs.



- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC remain unchanged.
- The most significant bits (A10~A11) are loaded with the contents of PS0~PS1 into the Status Register (R3) upon execution of a "JMP" or "CALL" instruction.

ADDRESS	SBANK0	SBANK1	IOCPAGE0	IOCPAGE1
00	R0			
01	R1 (TCC)			
02	R2 (PC)			
03	R3 (Status & ROM page)			
04	R4 (RAM select)			
05	R5 (Port 5 and IOC page)	R5 (TBRDH)	IOC50 (Port 5 I/O control)	IOC51 (unused)
06	R6 (Port 6)	R6 (TBRDL)	IOC60 (Port 6 I/O control)	IOC61 (wake-up register)
07	R7 (Port 7)		IOC70 (Port 7 I/O control)	IOC71 (TCC control)
08	R8 (Port 8)		IOC80 (Port 8 I/O control)	IOC81 (WDT control)
09	R9 (LCD control)		IOC90 (RAM Address)	IOC91 (CNT1/2 control)
0A	RA (LCD contrast and addr.)		IOCA0 (RAM Data)	IOCA1 (H/L pulse time control)
0B	RB (LCD data)		IOCB0 (CNT1 preset)	IOCB1 (Port 6 pull high)
0C	RC (Counter enable reg.)		IOCC0 (CNT2 preset)	IOCC1 (Port 6 open drain)
0D	RD (system clock control)		IOCD0 (high pulse timer preset)	IOCD1 (Port 8 pull high)
0E	RE (IR control)		IOCE0 (low pulse timer preset)	IOCE1 (Port 6 pull down)
0F	RF (Interrupt status)		IOCF0 (interrupt mask)	IOCF1 (unused)
10 1F	16 byte common register			
20 3F	Bank 0 32 byte common register	Bank 1 32 byte common register	Bank 2 32 byte common register	Bank 3 32 byte common register

Figure 6-2 Data Memory Configuration

6.1.4 R3, SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PS1	PS0	T	P	Z	DC	C
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Unused bit

Bit 6~Bit 5 (PS1~PS0): Page select bits

PS1	PS0	Program Memory Page (Address)
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

PS0~PS1 are used to select a ROM page. User can use the "PAGE" instruction (e.g., "PAGE 1") or set PS0~PS1 bits to change the ROM page. When executing a "JMP", "CALL", or other instructions which causes the program counter to be changed (e.g., "MOV R2, A"), the PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that "RET" ("RETL", "RETI") instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power up and reset to 0 by WDT timeout.

Event	T	P	Remark
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	x	x: don't care

Bit 3 (P): Power down bit. Set to "1" during power-on or by a "WDTC" command and reset to "0" by a "SLEP" command.

Bit 2 (Z): Zero flag

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4, RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6 (RBS1 ~ RBS0): Determine which bank among the four banks, is activated (see the data memory configuration in Figure 6-2. Use the “BANK” instruction (e.g., “Bank 1”) to change banks.

Bits 5~0 (RSR5 ~ RSR0): Used to select up to 64 registers (Address: 00~3F) under indirect addressing mode. If no indirect addressing is used, the RSR is used as an 8-bit general purpose read/write register.

6.1.6 SBANK 0 R5, Port 5 (Port 5 I/O Data and Page of Register Selection)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	-	-	-	IOCPAGE
R/W	R/W	R/W	R/W				R/W

Bits 7~4 (P57~P54): 4-bit I/O registers of Port 5. Use the IOC50 register to define each bit either as input or output.

Bits 3~1: Unused bits

Bit 0 (IOCPAGE): Switch Registers IOC5 ~ IOCF to another page

IOCPAGE = “0”: Page 0 (Registers IOC 50 to IOC F0) selected

IOCPAGE = “1”: Page 1 (Registers IOC 51 to IOC F1) selected

6.1.7 SBANK 0 R6, Port 6 (Port 6 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (P67~P60): 8-bit I/O registers of Port 6. Use the IOC60 register to define each bit either as input or output.

6.1.8 SBANK 0 R7, Port 7 (Port 7 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (P77~P70): 8-bit I/O registers of Port 7. Use the IOC70 register to define each bit either as input or output.

6.1.9 SBANK 0 R8, Port 8 (Port 8 I/O Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	P84	P83	P82	P81	P80
			R/W	R/W	R/W	R/W	R/W

Bits 7~5: Unused bits

Bits 4~0 (P84~P80): 8-bit I/O registers of Port 8. Use IOC80 register to define each bit either as input or output.

6.1.10 SBANK 0 R9, LCDCR (LCD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BS	DS1	DS0	LCDEN	-	LCDTYPE	LCDF1	LCDF0
R/W	R/W	R/W	R/W		R/W	R/W	R/W

Bit 7 (BS): LCD bias select bit

- 0: 1/2 bias
- 1: 1/3 bias

Bits 6~5 (DS1 ~ DS0): LCD duty select

DS1	DS0	LCD Duty
0	0	1/2 duty
0	1	1/3 duty
1	×	1/4 duty

Bit 4 (LCDEN): LCD enable bit

- 0: LCD circuit disabled. All common/segment outputs are set to ground (GND) level.
- 1: LCD circuit enabled

Bit 3: Unused bit

Bit 2 (LCDTYPE): LCD drive waveform type select bit

- 0: "A" type waveform
- 1: "B" type waveform

Bits 1~0 (LCDF1 ~ LCDF0): LCD frame frequency control bits

LCDF1	LCDF0	LCD Frame Frequency (e.g., $F_s=32.768\text{kHz}$)		
		1/2 Duty	1/3 Duty	1/4 Duty
0	0	$F_s/(256 \times 2)=64.0$	$F_s/(172 \times 3)=63.5$	$F_s/(128 \times 4)=64.0$
0	1	$F_s/(280 \times 2)=58.5$	$F_s/(188 \times 3)=58.0$	$F_s/(140 \times 4)=58.5$
1	0	$F_s/(304 \times 2)=53.9$	$F_s/(204 \times 3)=53.5$	$F_s/(152 \times 4)=53.9$
1	1	$F_s/(232 \times 2)=70.6$	$F_s/(156 \times 3)=70.0$	$F_s/(116 \times 4)=70.6$

F_s : sub-oscillator frequency

6.1.11 SBANK 0 RA, LCD_ADDR (LCD Address control register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
			R/W	R/W	R/W	R/W	R/W

Bits 7~5: Unused bits

Bits 4~0 (LCDA4 ~ LCDA0): LCD RAM addresses

RA (LCD Address)	RB (LCD Data Buffer)					Segment
	Bits 7 ~4	Bit 3 (LCD_D3)	Bit 2 (LCD_D2)	Bit 1 (LCD_D1)	Bit 0 (LCD_D0)	
00H	-	-	-	-	-	SEG0
01H	-	-	-	-	-	SEG1
02H	-	-	-	-	-	SEG2
1DH	-	-	-	-	-	SEG29
1EH	-	-	-	-	-	SEG30
1FH	-	-	-	-	-	SEG31
Common	x	COM3	COM2	COM1	COM0	

6.1.12 SBANK 0 RB, LCD_DB (LCD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	LCD_D3	LCD_D2	LCD_D1	LCD_D0
				R/W	R/W	R/W	R/W

Bits 7~4: Unused bits

Bits 3~0 (LCD_D3~LCD_D0): LCD RAM data transfer register

6.1.13 SBANK 0 RC, COUNTER (Counter Enable Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	LPWTEN	HPWTEN	CNT2EN	CNT1EN
				R/W	R/W	R/W	R/W

Bits 7~4: Unused bits

Bit 3 (LPWTEN): Low pulse width timer enable bit

0: Disable LPWT. Stop counting operation.

1: Enable LPWT. Start counting operation.

Bit 2 (HPWTEN): High pulse width timer enable bit

0: Disable HPWT. Stop counting operation.

1: Enable HPWT. Start counting operation.

Bit 1 (CNT2EN): Counter 2 enable bit

0: Disable Counter 2. Stop counting operation.

1: Enable Counter 2. Start counting operation.

Bit 0 (CNT1EN): Counter 1 enable bit

0: Disable Counter 1. Stop counting operation.

1: Enable Counter 1. Start counting operation.

6.1.14 SBANK 0 RD, SBPCR (System, Booster and PLL Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBANK	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (SBANK): Special Register 0x05 ~ 0x0F bank select bit

0: SBANK 0

1: SBANK 1

Bits 6~4 (CLK2 ~ CLK0): Main clock selection bits for PLL mode (code option select)

CLK2	CLK1	CLK0	Main clock	Example Fs=32.768K
0	0	0	Fs×130	4.26 MHz
0	0	1	Fs×65	2.13 MHz
0	1	0	Fs×65/2	1.065 MHz
0	1	1	Fs×65/4	532kHz
1	×	×	Fs×244	8 MHz

Bit 3 (IDLE): Idle mode enable bit. This bit determines the intended mode of the SLEP instruction.

0: "IDLE = 0"+SLEP instruction → Sleep mode

1: "IDLE = 1"+SLEP instruction → Idle mode

NOTE

NOP instruction must be added after SLEP instruction.

Example: Idle mode: Idle bit = "1" +SLEP instruction + NOP instruction
Sleep mode: Idle bit = "0" +SLEP instruction + NOP instruction

Bits 2~1 (BF1~BF0):LCD booster frequency select bit to adjust VLCD 2, 3 driving.

BF1	BF0	Booster Frequency
0	0	Fs
0	1	Fs/4
1	0	Fs/8
1	1	Fs/16

Bit 0 (CPUS): CPU oscillator source select. When CPUS=0, the CPU oscillator selects the Sub-oscillator and the Main oscillator is stopped.

0: Sub-oscillator (Fs) selected

1: Main oscillator (Fm) selected

■ CPU Operation Mode

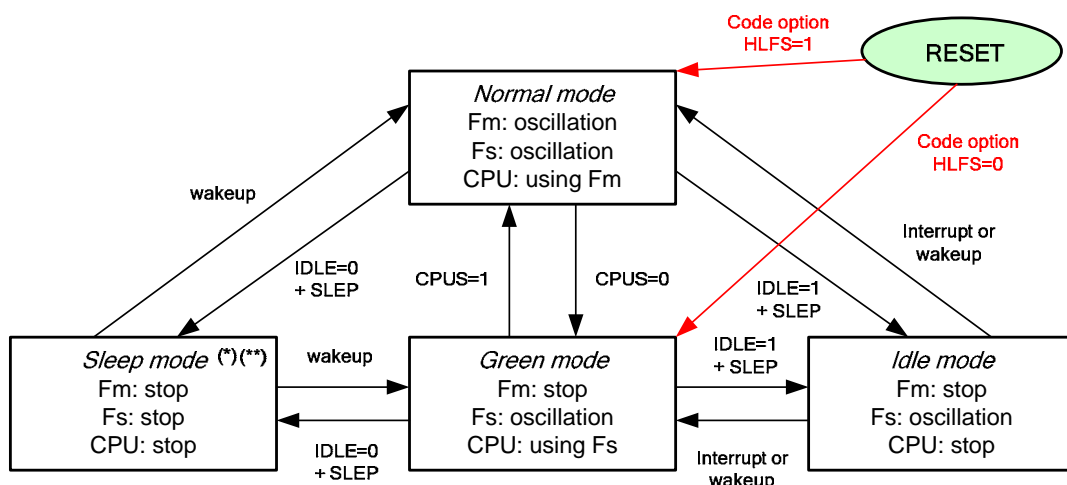


Figure 6-3 CPU Operation Mode

Note

(*)

If the watchdog function is enabled before going into sleep mode, some circuits like the timer (its clock source is F_s) must stop counting.

If the watchdog function is enabled before going into sleep mode, some circuits like the timer (its clock source is an external pin) can still count and its interrupt flag can be active at matching condition as corresponding interrupt is enabled. But the CPU cannot be awakened by this event.

(**)

Switching Operation Mode at Sleep → Normal, Green → Normal

If the timer clock source is F_m , the timer/counter must stop counting at sleep or green mode. Then, the timer can continue to count until the clock source is stable at normal mode. That clock source is stable means that the CPU starts to work at normal mode.

Switching Operation Mode at Sleep → Green:

If the timer clock source is F_s , timer must stop counting at sleep mode. Then, timer can continue to count until clock source is stable at green mode. That clock source is stable means that the CPU starts to work at green mode.

Switching Operation Mode at Sleep → Normal:

If the clock source of timer is F_s , timer must stop counting at sleep mode. Then, timer can continue to count until clock source is stable at normal mode. That clock source is stable means that the CPU starts to work at normal mode.

HLFS=1

Fmain	Fsub	Power-on LVR	Pin-Reset / WDT	
			N / G / I	S
RC	RC	16ms + WSTO + 64*1/Fmain	WSTO + 64*1/Fmain	WSTO + 64*1/Fmain
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 64*1/Fmain	WSTO + 510*1/Fsub
XT	RC	16ms + WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 510*1/Fmain	WSTO + 510*1/Fsub
PLL	RC	16ms + WSTO + 510*1/Fsub	WSTO + 510*1/Fsub	WSTO + 510*1/Fsub
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 510*1/Fsub	WSTO + 510*1/Fsub

HLFS=0

Fmain	Fsub	Power-on LVR	Pin-Reset / WDT	
			N / G / I	S
RC	RC	16ms + WSTO + 8*1/Fsub	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub
XT	RC	16ms + WSTO + 8*1/Fsub	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub
PLL	RC	16ms + WSTO + 8*1/Fsub	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub

Fmain	Fsub	G → N	I → N	S → N
RC	RC	WSTO + 64*1/Fmain	WSTO + 64*1/Fmain	WSTO + 64*1/Fmain
	XT	WSTO + 64*1/Fmain	WSTO + 64*1/Fmain	WSTO + 510*1/Fsub
XT	RC	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain
	XT	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fsub
PLL	RC	WSTO + 126*1/Fsub	WSTO + 510*1/Fsub	WSTO + 510*1/Fsub
	XT	WSTO + 126*1/Fsub	WSTO + 510*1/Fsub	WSTO + 510*1/Fsub

Fmain	Fsub	I → G	S → G
RC	RC	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
XT			
PLL	XT	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub

WSTO: Waiting Time from Start-to-Oscillation **N:** Normal mode
G: Green mode **I:** Idle mode **S:** Sleep mode

6.1.15 SBANK 0 RE, IRCR (IR Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRE	HF	LGP	-	IROUTE	TCCE	EINT1	EINT0
R/W	R/W	R/W		R/W	R/W	R/W	R/W

Bit 7 (IRE): Infrared Remote Enable bit

0: Disable the IR/PWM function. The state of P5.7/IROUT pin is determined by Bit 7 of IOC 50 if it is used as IROUT.

1: Enable IR or PWM function.

Bit 6 (HF): High carry frequency

0: For PWM application, disable the H/W modulator function. The IROUT waveform is generated according to high-pulse and low-pulse time as determined by the respective high pulse and low pulse width timers. Counter 2 is an independent auto reload timer.

1: For IR application mode, enable the H/W modulator function. The low time section of the generated pulse is modulated with the Fcarrier frequency. The Fcarrier frequency is provided by Counter 2.

Bit 5 (LGP): IROUT for low pulse width timer

0: Both high-pulse width timer register and low-pulse width timer are valid.

1: The high-pulse width timer register is ignored. So the IROUT waveform is dependent on the low-pulse width timer register only.

Bit 4: Unused bit**Bit 3 (IROUTE):** Defines the function of the P57/IROUT pin

0: Define as bi-directional general I/O pin

1: Define as IR or PWM output pin.

The P57 control bit (Bit 7 of IOC50) must be set to “0”

Bit 2 (TCCE): Defines the function of the P56/TCC pin.

0: Define as bi-directional general I/O pin

1: Define as external input pin of TCC.

The P56 control bit (Bit 6 of IOC50) must be set to “1”

Bit 1 (EINT1): Define the function of the P55/INT1 pin.

0: Define as bi-directional general I/O pin.

1: Define as external interrupt pin of INT1.

The P55 control bit (Bit 5 of IOC50) must be set to “1”

Bit 0 (EINT0): Defines the function of the P54/INT0 pin.

0: Define as bi-directional general I/O pin.

1: Define as external interrupt pin of INT0.

The P54 control bit (Bit 4 of IOC50) must be set to “1”

6.1.16 SBANK 0 RF, ISR (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These bits are set to “1” when interrupt occurs respectively.

Bit 7 (ICIF): Port 6 and Port 8 input status change interrupt flag. Set when Port 6 and Port 8 input status changes.

Bit 6 (LPWTF): Interrupt flag when the internal low-pulse width timer underflows.

Bit 5 (HPWTF): Interrupt flag when the internal high-pulse width timer underflows.

Bit 4 (CNT2F): Interrupt flag when the internal Counter 2 underflows.

Bit 3 (CNT1F): Interrupt flag when the internal Counter 1 underflows.

Bit 2 (INT1F): External INT1 pin interrupt flag

Bit 1 (INT0F): External INT0 pin interrupt flag

Bit 0 (TCIF): TCC timer overflow interrupt flag. Set when TCC timer overflows.

6.1.17 SBANK 1 R5, TBRDH (TBRD High Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	-	-	-	RBit11	RBit10	RBit9	RBit8
R/W				R/W	R/W	R/W	R/W

Bit 7 (HLB): Take MLB or LSB at machine code

0: Low 8 bits machine code.

1: Low 5 bits machine code.

Bits 6~4: Unused bits

Bits 3~0 (RBit11 ~ RBit8): program ROM high address.

6.1.18 SBANK 1 R6, TBRDL (TBRD Low Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (RBit7 ~ RBit0): program ROM low address.

6.1.19 R10~R3F (General Purpose Register)

R10~R1F and R20~R3F (Banks 0~3) are general purpose registers.

6.2 Special Purpose Registers – Accumulator

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.3 Special Purpose Registers - IOC Page 0 (IOC50 ~ IOCF0, Bit 0 of R5 = “0”)

6.3.1 IOC50, P5CR (Port 5 I/O and Ports 7, 8 for LCD Segment Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~4 (IOC57~ IOC54): Port 5 I/O direction control register

0: Set the relative P5x I/O pins as output

1: Set the relative P5x I/O pin into high impedance (input pin)

Bit 3 (P8HS): Switch to high nibble I/O of Port 8 or to LCD segment output while sharing pins with SEG28/P84 pins.

0: Select Port 8 as normal P84

1: Select LCD segment output as SEG 28 output

Bit 2 (P8LS): Switch to low nibble I/O of Port 8 or to LCD segment output while sharing pins with SEGxx/P8x pins.

0: Select low nibble of Port 8 as normal P80~P83

1: Select LCD Segment output as SEG 24~SEG 27 output

Bit 1 (P7HS): Switch to high nibble I/O of Port 7 or to LCD segment output while sharing pins with SEGxx/P7x pins.

0: Select high nibble of Port 7 as normal P74~P77

1: Select LCD Segment output as SEG 20~SEG 23 output

Bit 0 (P7LS): Switch to low nibble I/O of Port 7 or to LCD segment output while sharing pins with SEGxx/P7x pins.

0: Select low nibble of Port 7 as normal P70~P73

1: Select LCD segment output as SEG 16~SEG 19 output



6.3.2 IOC60, P6CR (Port 6 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (IOC67~ IOC60): Port 6 I/O direction control register

0: Set the relative Port 6x I/O pins as output

1: Set the relative Port 6x I/O pin into high impedance (input pin)

6.3.3 IOC70, P7CR (Port 7 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (IOC77~ IOC70): Port 7 I/O direction control register

0: Set the relative Port 7x I/O pins as output

1: Set the relative Port 7x I/O pin into high impedance (input pin)

6.3.4 IOC80, P8CR (Port 8 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	IOC84	IOC83	IOC82	IOC81	IOC80
			R/W	R/W	R/W	R/W	R/W

Bits 7~5: Unused bits

Bits 4~0 (IOC84~ IOC80): Port 8 I/O direction control register

0: Set the relative Port 8x I/O pins as output

1: Set the relative Port 8x I/O pin into high impedance (input pin)

6.3.5 IOC90, RAM_ADDR (128 Bytes RAM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Unused bit

Bits 6~0 (RAM_A6 ~ RAM_A 0): 128 bytes RAM address

6.3.6 IOCA0, RAM_DB (128 Bytes RAM Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (RAM_D7 ~ RAM_D0): 128 bytes RAM data transfer register

6.3.7 IOCB0, CNT1PR (Counter 1 Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (Bit 7~Bit 0): These are Counter 1 buffers which user can read and write.

Counter 1 is an 8-bit down-count timer with 8-bit prescaler used to preset the counter and read the preset value. The prescaler is set by the IOC91 register. After an interrupt, the preset value will be auto-reloaded.

6.3.8 IOCC0, CNT2PR (Counter 2 Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (Bit 7~Bit 0): These are Counter 2 buffers which you can read and write.

Counter 2 is an 8-bit down-count timer with 8-bit prescaler used to preset the counter and read the preset value. The prescaler is set by IOC91 register. After an interrupt, the preset value will be auto-reloaded.

When IR output is enabled, this control register can obtain carrier frequency output. If the Counter 2 clock source is equal to F_T , then-

$$\text{Carrier frequency (F}_{\text{carrier}}) = \frac{F_T}{2 * (\text{preset_value} + 1) * \text{prescaler}}$$

6.3.9 IOCD0, HPWTPR (High-Pulse Width Timer Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (Bit 7~Bit 0): These are high-pulse width timer buffers which user can read and write. The High-pulse width timer preset register is an 8-bit down-counter with 8-bit prescaler used as IOCD0 to preset the counter and read the preset value. The prescaler is set by the IOCA1 register. After an interrupt, the preset value will be auto-reloaded.

For PWM or IR application, this control register is set as high pulse width. If the high-pulse width timer clock source is F_T , then-

$$\text{High pulse time} = \frac{\text{prescaler} * (\text{preset_value} + 1)}{F_T}$$

6.3.10 IOCE0, LPWTPR (Low-Pulse Width Timer Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (Bit 7~Bit 0): All are low-pulse width timer buffer that user can read and write. Low-pulse width timer preset is an eight-bit down-counter with 8-bit prescaler that is used as IOCE0 to preset the counter and read preset value. The prescaler is set by IOCA1 register. After an interrupt, the preset value will be auto-reloaded.

For PWM or IR application, this control register is set as low pulse width. If the low-pulse width timer clock source is F_T , then -

$$\text{Low pulse time} = \frac{\text{prescaler} * (\text{preset_value} + 1)}{F_T}$$

6.3.11 IOCF0, IMR (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0: interrupt enable bit. Enable the respective interrupt source.

0: Disable interrupt

1: Enable interrupt

The IOCF0 register is readable and writable.

6.4 Special Purpose Registers – IOC Page 1 (IOC61 ~ IOCE1, Bit 0 of R5 = “1”)

6.4.1 IOC61, WUCR (Wake-up and Sink Current of P57, IROUT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IROCS	-	-	-	/WUE8H	/WUE8L	/WUE6H	/WUE6L
R/W				R/W	R/W	R/W	R/W

Bit 7 (IROCS): IROUT/Port 57 output sink current setting

IROCS	P57/IROUT Sink Current Setting	
	VDD=3V	
“0”	6 mA	
“1”	12 mA	

Bits 6~4: Unused bits.

Bit 3 (/WUE8H): “0”/“1” → Enable/disable Pin P84 to change wake-up function

Bit 2 (/WUE8L): “0”/“1” → Enable/disable Pins P80~P83 to change wake-up function

Bit 1 (/WUE6H): “0”/“1” → Enable/disable Pins P64~P67 to change wake-up function

Bit 0 (/WUE6L): “0”/“1” → Enable/disable Pins P60~P63 to change wake-up function

NOTE

*Do not set Port 6 and Port 8 as input floating when wake-up function is enabled.
“Enable” is the default status of wake-up function.*

6.4.2 IOC71, TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0
R/W	F	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT_EDGE): Interrupt edge select bit

0: Interrupt on the rising edge of P54/INT0 pin

1: Interrupt on the falling edge of P54/INT0 pin

Bit 6 (INT): INT enable flag. This bit is read only.

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock

1: Transition on TCC pin, TCC period > internal instruction clock period

Bit 4 (TE): TCC signal edge

0: Incremented by TCC pin rising edge

1: Incremented by TCC pin falling edge

Bits 3~0 (PSRE, TCCP2~ TCCP0): TCC prescaler bits

PSRE	TCCP2	TCCP1	TCCP0	TCC Rate
0	×	×	×	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

6.4.3 IOC81, WDTCR (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	WDTE	WDTP2	WDTP1	WDTP0
				R/W	R/W	R/W	R/W

Bits 7~4: Unused bits

Bit 3 (WDTE): Watchdog timer enable. This control bit is used to enable the Watchdog timer

0: Disable WDT function

1: enable WDT function

Bits 2~0 (WDTP2~ WDTP0): Watchdog Timer prescaler bits. The WDT clock source is sub-oscillation frequency.

WDTP2	WDTP1	WDTP0	WDT Rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

6.4.4 IOC91, CNT12CR (Counters 1, 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (CNT2S): Counter 2 clock source select

0: Fs (Fs: sub-oscillator clock)

1: Fm (Fm: main-oscillator clock)

Bits 6~4 (CNT2P2 ~ CNT2P0): Counter 2 prescaler select bits

CNT2P2	CNT2P1	CNT1P0	Counter 2 Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S): Counter 1 clock source select bit

0: Fs (Fs: sub-oscillator clock)

1: Fm (Fm: main-oscillator clock)

Bits 2~0 (CNT1P2~ CNT1P0): Counter 1 prescaler select bits

CNT1P2	CNT1P1	CNT1P0	Counter 1 Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256



6.4.5 IOCA1, HLPWTCR (High/Low Pulse Width Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (LPWTS): Low-pulse width timer clock source select bit

0: Fs (Fs: sub-oscillator clock)

1: Fm (Fm: main-oscillator clock)

Bits 6~4 (LPWTP2~ LPWTP0): Low-pulse width timer prescaler select bits

LPWTP2	LPWTP1	LPWTP0	Low-pulse Width Timer Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (HPWTS): High-pulse width timer clock source select bit

0: Fs (Fs: sub-oscillator clock)

1: Fm (Fm: main-oscillator clock)

Bits 2~0 (HPWTP2 ~ HPWTP0): High-pulse width timer prescaler select bits

HPWTP2	HPWTP1	HPWTP0	High-pulse width timer scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.4.6 IOCB1, P6PH (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PH67~PH60): Port 6 Pull high function Enable bits

0: Disable P6x pin internal pull-high resistor function

1: Enable P6x pin internal pull-high resistor function

6.4.7 IOCC1, P6OD (Port 6 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD67~OD60): Port 6 Open Drain function Enable bits

0: Disable P6x pin open drain function

1: Enable P6x pin open drain function

6.4.8 IOCD1, P8PH (Port 8 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	PH84	PH83	PH82	PH81	PH80
			R/W	R/W	R/W	R/W	R/W

Bits 7~5: Unused bits

Bits 4~0 (PH84~PH80): Port 8 Pull-high function Enable bits

0: Disable P8x pin internal pull-high resistor function

1: Enable P8x pin pull-high resistor function

6.4.9 IOCE1, P6PL (Port 6 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PL67~PL60): Port 6 Pull low function Enable bits

0: Disable P6x pin internal pull-low resistor function

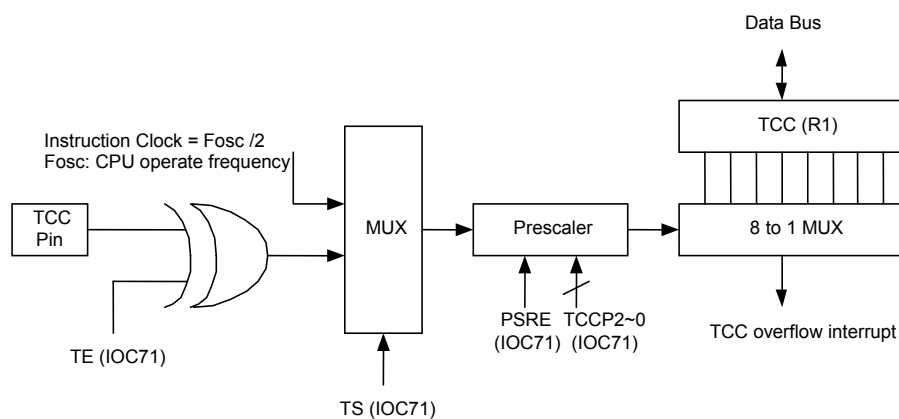
1: Enable P6x pin internal pull-low resistor function

6.5 TCC and WDT Prescaler

Two 8-bit counters are available as prescalers for the TCC (Time Clock Counter) and WDT (Watchdog Timer). The TCCP2~TCCP0 bits of the IOC71 register are used to determine the ratio of the TCC prescaler. Likewise, the WDTP2~WDTP0 bits of the IOC81 register are used to determine the WDT prescaler. The TCC prescaler (TCCP2~TCCP0) is cleared by the instructions each time they are written into TCC, while the WDT prescaler is cleared by the “WDTC” and “SLEP” instructions. Figure 6-3 depicts the circuit diagram of TCC and WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be selected by internal instruction clock or external signal input (edge selectable from the TCC control register). If the TCC signal source is from the internal instruction clock, the TCC will be incremented by 1 at every instruction cycle (without prescaler). If the TCC signal source is from an external clock input, the TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin.

The Watchdog Timer is a free running on sub-oscillator. The WDT will keep on running even after the oscillator driver has been turned off. During Normal mode, Green mode, or Idle mode operation, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during Normal mode and Green mode by software programming. Refer to WDTE bit of IOC81 register. The WDT time-out period is equal to $(\text{prescaler} \times 256 / (F_s/2))$.



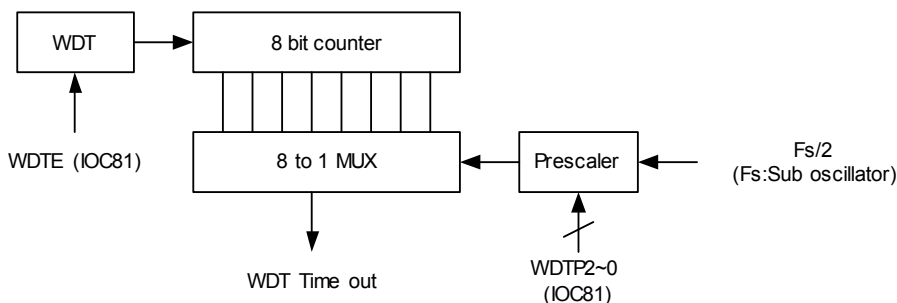


Figure 6-3 Block diagram of TCC WDT

6.6 I/O Ports

The I/O registers, (Port 5, Port 6, Port 7 and Port 8), are bidirectional tri-state I/O ports. Port 6 and Port 8 are pulled-high internally by software. Port 6 is pulled-down internally by software. Likewise, Port 6 has its open-drain output also through software. Port 5, Port 6 and Port 8 features an input status changed interrupt (or wake-up) function and is pulled-high by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits are shown in Figure 6-4

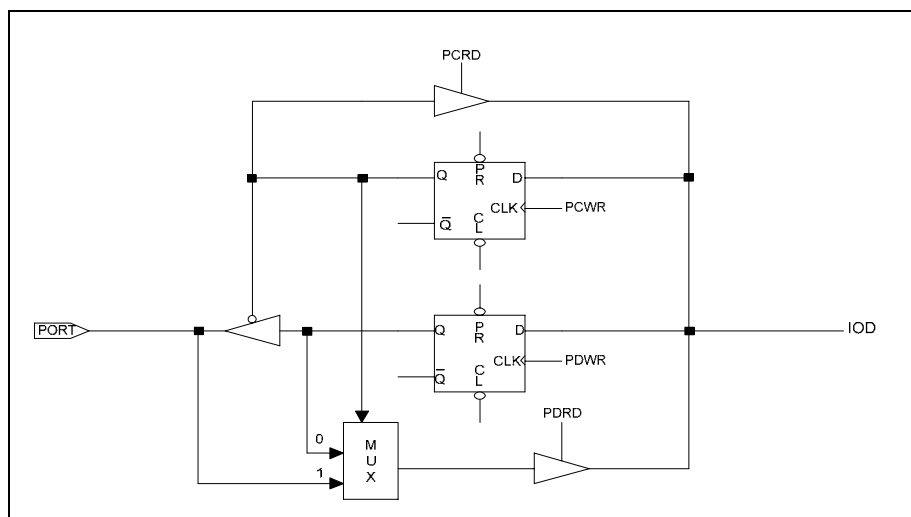
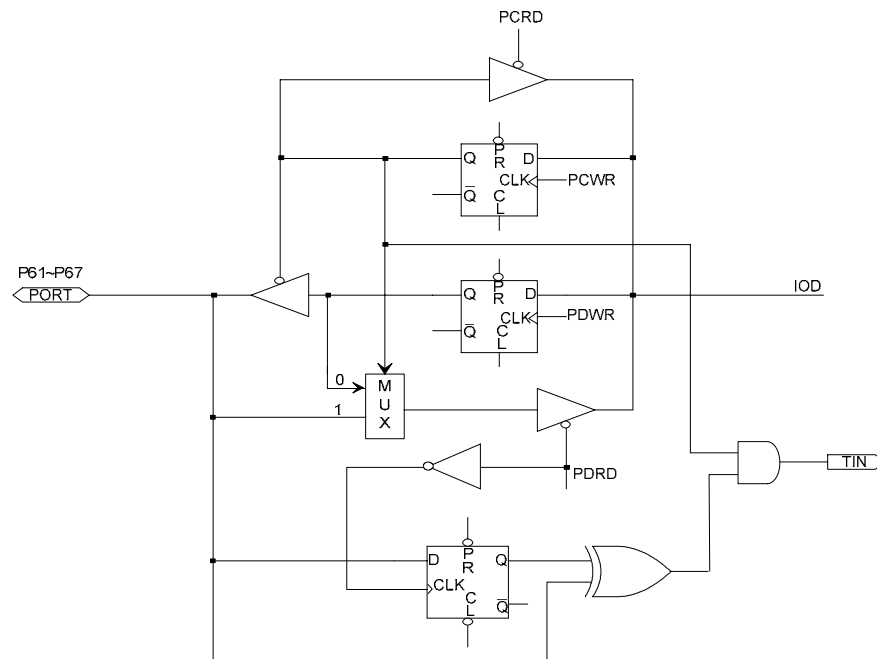


Figure 6-4 Circuit of I/O port and I/O control register for Port 5 and Port 7



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-5 Circuit of I/O Port and I/O Control Register for Port 6 and Port 8

6.7 Reset and Wake-up

A reset can be activated by

- POR (Power-on Reset)
- WDT timeout (if enabled)
- LVR (if enabled)
- /RESET pin goes to low

Note that the reset circuit is always enabled. It will reset the CPU at 1.9V. Once a reset occurs, the following functions are performed:

- The oscillator is running, or will be started
- The program counter (R2/PC) is set to all "0"
- All I/O port pins are configured as input mode (high-impedance state)
- The TCC/Watchdog timer and prescaler are cleared
- When power is on, Bits 5 and 6 of R3 and the upper two bits of R4 are cleared.
- Bits of the IOC71 register are set to all "1," except for Bit 6 (INT flag)
- For other registers, see the following table.

6.7.1 Summary of Registers Initialized Values

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	IOC50 P5CR	Bit Name	IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS
		Power-on	1	1	1	1	0	0	0	0
		/RESET and WDT	1	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	IOC60 P6CR	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	IOC70 P7CR	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	IOC80 P8CR	Bit Name	×	×	×	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-on	0	0	0	1	1	1	1	1
		/RESET and WDT	0	0	0	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	IOC90 RAM_ADDR	Bit Name	×	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	IOCA0 RAM_DB	Bit Name	RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x0B	IOCB0 CNT1PR	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
		Power-on	0	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P	P
0x0C	IOCC0 CNT2PR	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
		Power-on	0	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P	P
0x0D	IOCD0 HPWTPR	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
		Power-on	0	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P	P
0x0E	IOCE0 LPWTPR	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
		Power-on	0	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P	P
0x0F	IOCF0 IMR	Bit Name	ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE	
		Power-on	0	0	0	0	0	0	0	0	
		/RESET and WDT	0	0	0	0	0	0	0	0	
		Wake-up from Pin Change	P	P	P	P	P	P	P	P	
0x06	IOC61 WUCR	Bit Name	IROCS	X	X	X	/WUE8H	/WUE8L	/WUE6H	/WUE6L	
		Power-on	0	U	U	U	0	0	0	0	
		/RESET and WDT	0	U	U	U	0	0	0	0	
		Wake-up from Pin Change	P	U	U	U	P	P	P	P	

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	IOC71 TCCCR	Bit Name	INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	IOC81 WDTCR	Bit Name	×	×	×	×	WDTE	WDTP2	WDTP1	WDTP0
		Power-on	0	0	0	0	0	1	1	1
		/RESET and WDT	0	0	0	0	0	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	IOC91 CNT12CR	Bit Name	CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	IOCA1 HLPWTCR	Bit Name	LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB1 P6PH	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC1 P6OD	Bit Name	OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	IOCD1 P8PH	Bit Name	X	X	X	PH84	PH83	PH82	PH81	PH80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE1 P6PL	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	SBANK0/1 R0 IAR	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	SBANK0/1 R1 TCC	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	SBANK0/1 R2 PC	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to address 0x0018 or continue to execute next instruction							
0x03	SBANK0/1 R3 SR	Bit Name	X	PS1	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P



(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	SBANK0/1 R4 RSR	Bit Name	RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	SBANK0 R5 Port 5	Bit Name	P57	P56	P55	P54	×	×	×	IOCPAGE
		Power-on	1	1	1	1	U	U	0	0
		/RESET and WDT	1	1	1	1	U	U	0	0
		Wake-up from Pin Change	P	P	P	P	U	U	P	P
0x06	SBANK0 R6 Port 6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	SBANK0 R7 Port 7	Bit Name	P77	P76	P75	P74	P73	P62	P71	P70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	SBANK0 R8 Port 8	Bit Name	×	×	×	P84	P83	P82	P81	P80
		Power-on	0	0	0	1	1	1	1	1
		/RESET and WDT	0	0	0	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	SBANK0 R9 LCDCR	Bit Name	BS	DS1	DS0	LCDEN	×	LCDTYPE	LCDF1	LCDF0
		Power-on	1	1	0	0	0	0	0	0
		/RESET and WDT	1	1	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P