
EM78P374N

8-Bit Microcontroller

**Product
Specification**

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ELAN MICROELECTRONICS CORP.


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Contents

1	General Description	1
2	Features	1
3	Pin Configuration (Package)	2
4	Pin Description	3
5	Functional Block Diagram	6
6	Functional Description	7
6.1	Operational Registers.....	7
6.1.1	R0: IAR (Indirect Addressing Register).....	7
6.1.2	R1: BSR (Bank Select Control Register)	7
6.1.3	R2: PCL (Program Counter Low).....	7
6.1.4	R3: SR (Status Register).....	12
6.1.5	R4: RSR (RAM Select Register).....	13
6.1.6	Bank 0 R5 ~ R7: (Port 5 ~ Port 7).....	13
6.1.7	Bank 0 R8~RA	13
6.1.8	Bank 0 RB~RD: (IOCR5 ~ IOCR7).....	13
6.1.9	Bank 0 RE: OMCR (Operating Mode Control Register)	13
6.1.10	Bank 0 RF: IESCR (External Interrupt Edge Select Control Register)	15
6.1.11	Bank 0 R10: WUCR1 (Wake-up Control Register 1).....	15
6.1.12	Bank 0 R11: WUCR2 (Wake-up Control Register 2)	15
6.1.13	Bank 0 R12: WUCR3 (Wake-up Control Register 3).....	16
6.1.14	Bank 0 R13	16
6.1.15	Bank 0 R14: SFR1 (Status Flag Register 1).....	17
6.1.16	Bank 0 R15: SFR2 (Status Flag Register 2).....	18
6.1.17	Bank 0 R16: SFR3 (Status Flag Register 3).....	18
6.1.18	Bank 0 R17: SFR4 (Status Flag Register 4).....	19
6.1.19	Bank 0 R18: SFR5 (Status Flag Register 5).....	19
6.1.20	Bank 0 R1B: IMR1 (Interrupt Mask Register 1)	20
6.1.21	Bank 0 R1C: IMR2 (Interrupt Mask Register 2).....	20
6.1.22	Bank 0 R1D: IMR3 (Interrupt Mask Register 3).....	21
6.1.23	Bank 0 R1E: IMR4 (Interrupt Mask Register 4)	22
6.1.24	Bank 0 R1F: IMR5 (Interrupt Mask Register 5)	22
6.1.25	Bank 0 R21: WDTCR (Watchdog Timer Control Register).....	23
6.1.26	Bank 0 R22: TCCCR (TCC Control Register).....	23
6.1.27	Bank 0 R23: TCCD (TCC Data Register)	24
6.1.28	Bank 0 R24: TC1CR1 (Timer/Counter 1 Control Register 1).....	24
6.1.29	Bank 0 R25: TC1CR2 (Timer/Counter 1 Control Register 2).....	25
6.1.30	Bank 0 R26: TC1DA (Timer/Counter 1 Data Buffer A).....	26
6.1.31	Bank 0 R27: TC1DB (Timer/Counter 1 Data Buffer B)	26
6.1.32	Bank 0 R28~R2F	27
6.1.33	Bank 0 R30: I2CCR1 (I2C Status and Control Register 1).....	27

6.1.34	Bank 0 R31: I2CCR2 (I2C Status and Control Register 2)	28
6.1.35	Bank 0 R32: I2CSA (I2C Slave Address Register)	29
6.1.36	Bank 0 R33: I2CDB (I2C Data Buffer Register)	29
6.1.37	Bank 0 R34: I2CDAL (I2C Device Address Register)	29
6.1.38	Bank 0 R35: I2CDAH (I2C Device Address Register)	29
6.1.39	Bank 0 R36~R3A	30
6.1.40	Bank 0 R3B: CMP2CR (Comparator 2 Control Register)	30
6.1.41	Bank 0 R3C: CMP3CR (Comparator 3 Control Register)	30
6.1.42	Bank 0 R3D	31
6.1.43	Bank 0 R3E: ADCR1 (ADC Control Register 1)	31
6.1.44	Bank 0 R3F: ADCR2 (ADC Control Register 2)	32
6.1.45	Bank 0 R40: ADISR (Analog to Digital Converter Input Channel Select Register)	33
6.1.46	Bank 0 R41: ADER1 (Analog to Digital Converter Input Control Register 1)	34
6.1.47	Bank 0 R42: ADER2 (Analog to Digital Converter Input Control Register 2)	35
6.1.48	Bank 0 R43: ADDL (Low Byte of Analog to Digital Converter Data)	35
6.1.49	Bank 0 R44: ADDH (High Byte of Analog to Digital Converter Data)	36
6.1.50	Bank 0 R45 ADCVL (Low Byte of Analog to Digital Converter Comparison)	36
6.1.51	Bank 0 R46 ADCVH (High Byte of Analog to Digital Converter Comparison)	36
6.1.52	Bank 1 R5 ~ R7	36
6.1.53	Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)	37
6.1.54	Bank 1 R9: P6PHCR (Port 6 Pull-high Control Register)	37
6.1.55	Bank 1 RA: P7PHCR (Port 7 Pull-high Control Register)	38
6.1.56	Bank 1 RB: P5PLCR (Port 5 Pull-low Control Register)	38
6.1.57	Bank 1 RC: P6PLCR (Port 6 Pull-low Control Register)	38
6.1.58	Bank 1 RD: P7PLCR (Port 7 Pull-low Control Register)	39
6.1.59	Bank 1 RE: P5HDSCR (Port 5 High Drive/Sink Control Register)	39
6.1.60	Bank 1 RF: P6HDSCR (Port 6 High Drive/Sink Control Register)	39
6.1.61	Bank 1 R10: P7HDSCR (Port 7 High Drive/Sink Control Register)	40
6.1.62	Bank 1 R11: P5ODCR (Port 5 Open-drain Control Register)	40
6.1.63	Bank 1 R12: P6ODCR (Port 6 Open-drain Control Register)	40
6.1.64	Bank 1 R13: P7ODSCR (Port 7 Open-drain Control Register)	40
6.1.65	Bank 1 R14~R15	41
6.1.66	Bank 1 R16: PWMSCR (PWM Source Clock Control Register)	41
6.1.67	Bank 1 R17: PWMACR (PWMA Control Register)	41
6.1.68	Bank 1 R18: PRDAL (Low Byte of PWMA Period)	42
6.1.69	Bank 1 R19: PRDAH (High Byte of PWMA Period)	42
6.1.70	Bank 1 R1A: DTAL (Low Byte of PMWA Duty)	42
6.1.71	Bank 1 R1B: DTAH (High Byte of PMWA Duty)	43
6.1.72	Bank 1 R1C: TMRAL (Low Byte of Timer A)	43
6.1.73	Bank 1 R1D: TMRAH (High Byte of Timer A)	43
6.1.74	Bank 1 R1E: PWMB CR (PWMB Control Register)	43
6.1.75	Bank 1 R1F: PRDBL (Low Byte of PWMB Period)	44
6.1.76	Bank 1 R20: PRDBH (High Byte of PWMB Period)	44

6.1.77	Bank 1 R21: DTBL (Low Byte of PMWB Duty)	44
6.1.78	Bank 1 R22: DTBH (High Byte of PMWB Duty).....	44
6.1.79	Bank 1 R23: TMRBL (Low Byte of Timer B)	45
6.1.80	Bank 1 R24: TMRBH (High Byte of Timer B).....	45
6.1.81	Bank 1 R25: PWMCCR (PWMC Control Register).....	45
6.1.82	Bank 1 R26: PRDCL (Low Byte of PWMC Period).....	46
6.1.83	Bank 1 R27: PRDCH (High Byte of PWMC Period)	46
6.1.84	Bank 1 R28: DTCL (Low Byte of PMWC Duty).....	46
6.1.85	Bank 1 R29: DTCH (High Byte of PMWC Duty)	46
6.1.86	Bank 1 R2A: TMRCL (Low Byte of Timer C).....	46
6.1.87	Bank 1 R2B: TMRCH (High Byte of Timer C)	47
6.1.88	Bank 1 R41 (Reserved)	47
6.1.89	Bank 1 R42 (Reserved)	47
6.1.90	Bank 1 R43 (Reserved)	47
6.1.91	Bank 1 R44 (Reserved)	47
6.1.92	Bank 1 R45: TBPTL (Table Pointer Low Register).....	47
6.1.93	Bank 1 R46: TBPTH (Table Pointer High Register)	47
6.1.94	Bank 1 R48: PCH (Program Counter High).....	47
6.1.95	Bank 1 R49: LVDCCR (Low Voltage Detector Control Register)	48
6.1.96	Bank 1 R4A~R4C (Reserved).....	48
6.1.97	Bank 1 R4D (Reserved).....	48
6.1.98	Bank 1 R4E (Reserved).....	48
6.1.99	Bank 1 R4F (Reserved)	48
6.2	TCC/WDT and Prescaler.....	49
6.3	I/O Ports	50
6.3.1	Usage of Ports 5~6 Input Change Wake-up/Interrupt Function.....	52
6.4	Reset and Wake-up Operation	53
6.4.1	Summary of Wake-up and Interrupt Modes.....	55
6.4.2	Status of RST, T, and P of Status Register.....	57
6.4.3	Summary of Register Initial Values after Reset	58
6.5	Interrupt.....	71
6.6	Analog-to-Digital Converter (ADC)	73
6.6.1	ADC Data Register.....	74
6.6.2	A/D Sampling Time	74
6.6.3	A/D Conversion Time	75
6.6.4	ADC Operation during Sleep Mode	75
6.6.5	Programming Process/Considerations	76
6.7	Timer	77
6.7.1	Timer/Counter Mode	78
6.7.2	Window Mode	79
6.7.3	Capture Mode	80



6.7.4	Programmable Divider Output (PDO) Mode and Pulse Width Modulation (PWM) Mode	81
6.7.5	Buzzer Mode	82
6.8	PWM Module	83
6.8.1	Overview	83
6.8.2	Control Register	84
6.8.3	Increment Timer Counter (TMRX: TMRAH/TMRAL, TMRBH/TMRBL, TMRCH/TMRCL, or TMRDH/TMRDL).....	85
6.8.4	PWM Time Period (PRDX: PRDAL/H, PRDBL/H, PRDCL/H, or PRDDL/H)	85
6.8.5	PWM Duty Cycle (DTX: DTAH/DTAL, DTBH/DTBL, DTCH/DTCL, or DTDH/DTDL)	86
6.8.6	Comparator X.....	87
6.8.7	PWM Programming Process/Steps.....	87
6.9	Comparator	88
6.9.1	External Reference Signal	89
6.9.2	Comparator Outputs.....	89
6.9.3	Programming the Related Registers.....	90
6.9.4	Comparator Interrupt.....	90
6.9.5	Wake-up from Sleep Mode	90
6.10	I2C Function	90
6.10.1	7-Bit Slave Address.....	92
6.10.2	10-Bit Slave Address.....	93
6.10.3	Master Mode I2C Transmit.....	96
6.10.4	Slave Mode I2C Transmit.....	96
6.11	LVD (Low Voltage Detector)	97
6.11.1	Low Voltage Reset (LVR).....	97
6.11.2	Low Voltage Detect	97
6.12	Oscillator	99
6.12.1	Oscillator Modes	99
6.12.2	Crystal Oscillator/Ceramic Resonators (XTAL).....	99
6.12.3	Internal RC Oscillator Mode.....	100
6.13	Power-on Considerations	101
6.14	External Power-on Reset Circuit	101
6.15	Residue-Voltage Protection	101
6.16	Code Option	102
6.16.1	Code Option Register (Word 0)	102
6.16.2	Code Option 1 (Word 1).....	103
6.16.3	Code Option 2 (Word 2).....	104
6.16.4	Code Option 3 (Word 3).....	104
6.16.5	Code Option F (Word F).....	105
6.17	Instruction Set	105



7	Absolute Maximum Ratings	108
8	DC Electrical Characteristics	109
8.1	AD Converter Characteristics	111
8.2	Comparator Characteristics	112
8.3	OP Characteristics	112
8.4	VREF 2V/3V/4V Characteristics	113
9	AC Electrical Characteristics	113

APPENDIX

A	Package Type.....	114
B	Packaging Configuration.....	115
B.1	EM78P374NSS24 150 mil.....	115
B.2	EM78P374NSO24 300 mil	116
B.3	EM78P374NK24 300 mil	117
B.4	EM78P374NSS20 209 mil.....	118
B.5	EM78P374NSO20 300 mil	119
B.6	EM78P374ND20 300 mil.....	120
B.7	EM78P374NSO18 300 mil	121
B.8	EM78P374ND18	122
C	Quality Assurance and Reliability	123
C.1	Address Trap Detect.....	123

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2011/04/26
1.1	<ol style="list-style-type: none">1. Modified the Features2. Modified the AD description3. Modified the DC and AC Electrical Characteristics4. Deleted VREFN	2011/08/17
1.2	<ol style="list-style-type: none">1. Modified the Code Option Word 0 and Word 2	2012/08/30
1.3	<ol style="list-style-type: none">1. Added LVR specification in the DC Electrical Characteristics section	2013/01/22
1.4	<ol style="list-style-type: none">1. Removed the dead time register from Section 6.8.22. Removed dead time from Figure 6-13a3. Modified VIH/VIL in Section 8	2014/01/06



1 General Description

The EM78P374N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It is used for 15 bits kernel simulation and it simulates the 4K×15-bit programmable ROM and 304×8-bit In-system programmable SRAM. Using the ICE370N, users can develop their program for ELAN's several OTP types of IC.

2 Features

■ CPU Configuration

- Support 4K×15 bits program ROM
- 304×8 bits on-chip registers (SRAM)
- More than 10 years data retention
- 8 level stacks for subroutine nesting
- Dual clock operation mode
- Four programmable Level Voltage Detector (LVD) : 4.5V, 4V, 3.3V, 2.2V
- Four programmable Level Voltage Reset (LVR) : 4.0V, 3.5V, 2.7V, 1.8V (POR)
- Power on reset level Voltage: 1.8V~1.9V
- Less than 1.0 mA at 5V/4MHz
- Typically 15 μ A, at 3V/16kHz
- Typically 2 μ A, during sleep mode
- Four operation mode

Mode	CPU	Main clock	Sub clock
Sleep mode	Turn off	Turn off	Turn off
Idle Mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

■ I/O Port Configuration

- 6 bi-directional I/O ports : P5, P6 and P7
- 22 I/O pins
- 22 Programmable open-drain I/O pins
- 21 programmable pull-high I/O pins
- 21 programmable pull-down I/O pins
- 21 programmable high sink/drive I/O pins
- External interrupt : INTO

■ Operating voltage range:

- 2.1V~5.5V at 0~70°C (commercial)
- 2.3V~5.5V at -40~85°C (industrial)

■ Operating frequency range:

- Crystal/IRC/ERC oscillation circuit selected by code option for system clock
- IRC oscillation circuit selected by code option for sub clock

Main Clock

- Crystal mode:
DC ~ 16 MHz at 5~5.5V
DC ~ 8 MHz at 3~5.5V
DC ~ 4 MHz at 2.1V~5.5V
- IRC mode:
DC ~ 16 MHz at 5~5.5V
DC ~ 8 MHz/2clks at 3V~5.5V
DC ~ 4 MHz/2clks at 2.1V~5.5V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.5V~5.5V)	Process	Total
1 MHz	± 2%	± 1%	± 1%	± 4%
4 MHz	± 2%	± 1%	± 1%	± 4%
8 MHz	± 2%	± 1%	± 1%	± 4%
16 MHz	± 2%	± 1%	± 1%	± 4%

Sub Clock

- IRC mode: 16kHz/32kHz

■ Peripheral Configuration

- 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges
- 14+2-channels Analog-to-Digital Converter with 12-bit resolution+ 1 internal reference for Vref+.
- One 8-bit Timer/Counter

TC1:

Timer/Counter/capture//window/buzzer/PWM/PDO (programmable divider output) Mode selection

- External interrupt wake-up. Function: rising or falling edge interrupt
- I2C-bus available. Function; 7/10-bit address, 8-bit data transmit/receive mode
- Port 56 input status change wake-up
- Three 16 bits PWM
- One Comparator/OP

■ 16 available interrupts

■ Special Features

- Programmable free running watchdog timer
- High ESD immunity
- Power saving Sleep mode
- Selectable Oscillation mode

■ Package types:

- 18 pin DIP 300mil : EM78P374ND18J/S
- 18 pin SOP 300mil : EM78P374NSO18J/S
- 20 pin DIP 300mil : EM78P374ND20J/S
- 20 pin SOP 300mil : EM78P374NSO20J/S
- 20 pin SSOP 209mil : EM78P374NSS20J/S
- 24 pin skinny DIP 300mil : EM78P374NK24J/S
- 24 pin SOP 300mil : EM78P374NSO24J/S
- 24 pin SSOP 150mil : EM78P374NSS24J/S

Note: These are Green product which do not contain hazardous substances

3 Pin Configuration (Package)

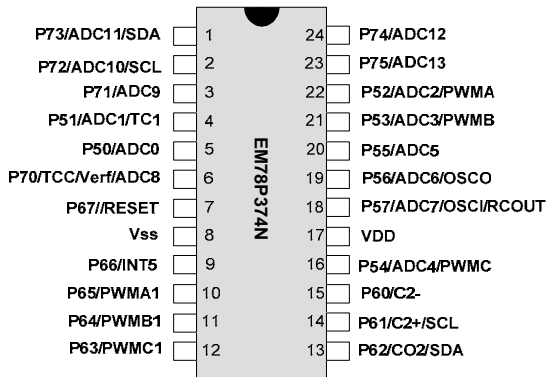


Figure 3-1a 24-Pin DIP/SOP/SSOP Pin Assignment

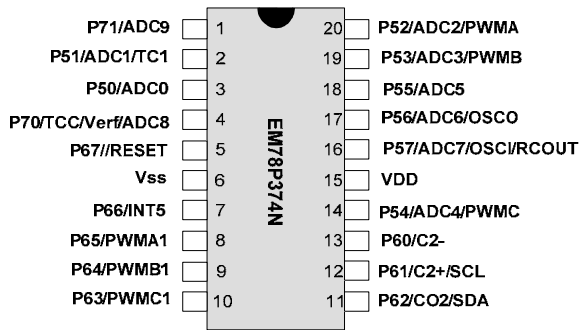


Figure 3-1b 20-Pin DIP/SOP/SSOP Pin Assignment

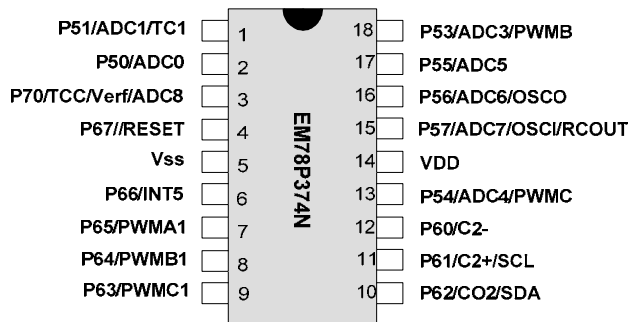


Figure 3-1c 18-Pin DIP/SOP Pin Assignment

4 Pin Description

Pin Name	Function	Input Type	Output Type	Description
P50/ADC0	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC0	AN	-	ADC Input 0
P51/ADC1/ TC1	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC1	AN	-	ADC Input 1
	TC1	ST	CMOS	Timer 1 clock input, capture input (TC1CAP), window input (TC1W), programmable divider output (PDO), pulse-width-modulation (PWM1), and buzzer output (BUZ)
P52/ADC2/ PWMA	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC2	AN	-	ADC Input 2
	PWMA	-	CMOS	PWMA output
P53/ADC3/ PWMB	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC3	AN	-	ADC Input 3
	PWMB	-	CMOS	PWMB output
P54/ADC4/ PWMC	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC4	AN	-	ADC Input 4
	PWMC	-	CMOS	PWMC output
P55/ADC5	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC5	AN	-	ADC Input 5
P56/ADC6/ OSCO	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC6	AN	-	ADC Input 6
	OSCO	-	XTAL	Clock output of crystal/resonator oscillator

(Continuation)

Pin Name	Function	Input Type	Output Type	Description
P57/ADC7/ OSCI/ RCOUT	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC7	AN	-	ADC Input 7
	OSCI	XTAL	-	Clock input of crystal/ resonator oscillator
	RCOUT	-	CMOS	Clock output of internal RC oscillator
P60/C2-	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	C2-	AN	-	Inverting end of Comparator 2 / OP2
P61/C2+/ SCL	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	C2+	AN	-	Non-inverting end of Comparator 2/OP2
	SCL	ST	CMOS	I ² C serial clock input/output (SCL)
P62/CO2/ SDA	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	CO2	-	CMOS	Output of Comparator 2
	SDA	ST	CMOS	I ² C serial data input/output (SDA)
P63/ PWMC1	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	PWMC1	-	CMOS	PWMC1 ouput (complementary PWM)
P64/ PWMB1	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up
	PWMB1	-	CMOS	PWMB1 ouput (complementary PWM)
P65/ PWMA1	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	PWMA1	-	CMOS	PWMA1 ouput (complementary PWM)
P66/INT	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	INT	ST		External interrupt pin
P67/ /RESET	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, high sink, and pin change wake-up. It is always open-drain
	/RESET	ST	-	Reset pin



(Continuation)

Pin Name	Function	Input Type	Output Type	Description
P70/TCC/ Verf/ADC8	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	TCC	ST	-	Real Time Clock/Counter clock input
	VREF	AN	-	ADC external voltage reference
	ADC8	AN	-	ADC Input 8
P71/ADC9	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC9	AN	-	ADC Input 9
P72/ADC10/ SCL	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC10	AN	-	ADC Input 10
	SCL	ST	CMOS	I ² C serial clock input/output (SCL)
P73/ADC11/ SDA	P73	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC11	AN	-	ADC Input 11
	SDA	ST	CMOS	I ² C serial data input/output (SDA)
P74/ADC12	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC12	AN	-	ADC Input 12
P75/ADC13	P75	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC13	AN	-	ADC Input 13
VDD	VDD	Power	-	Power supply pin
VSS	VSS	Power	-	Ground

5 Functional Block Diagram

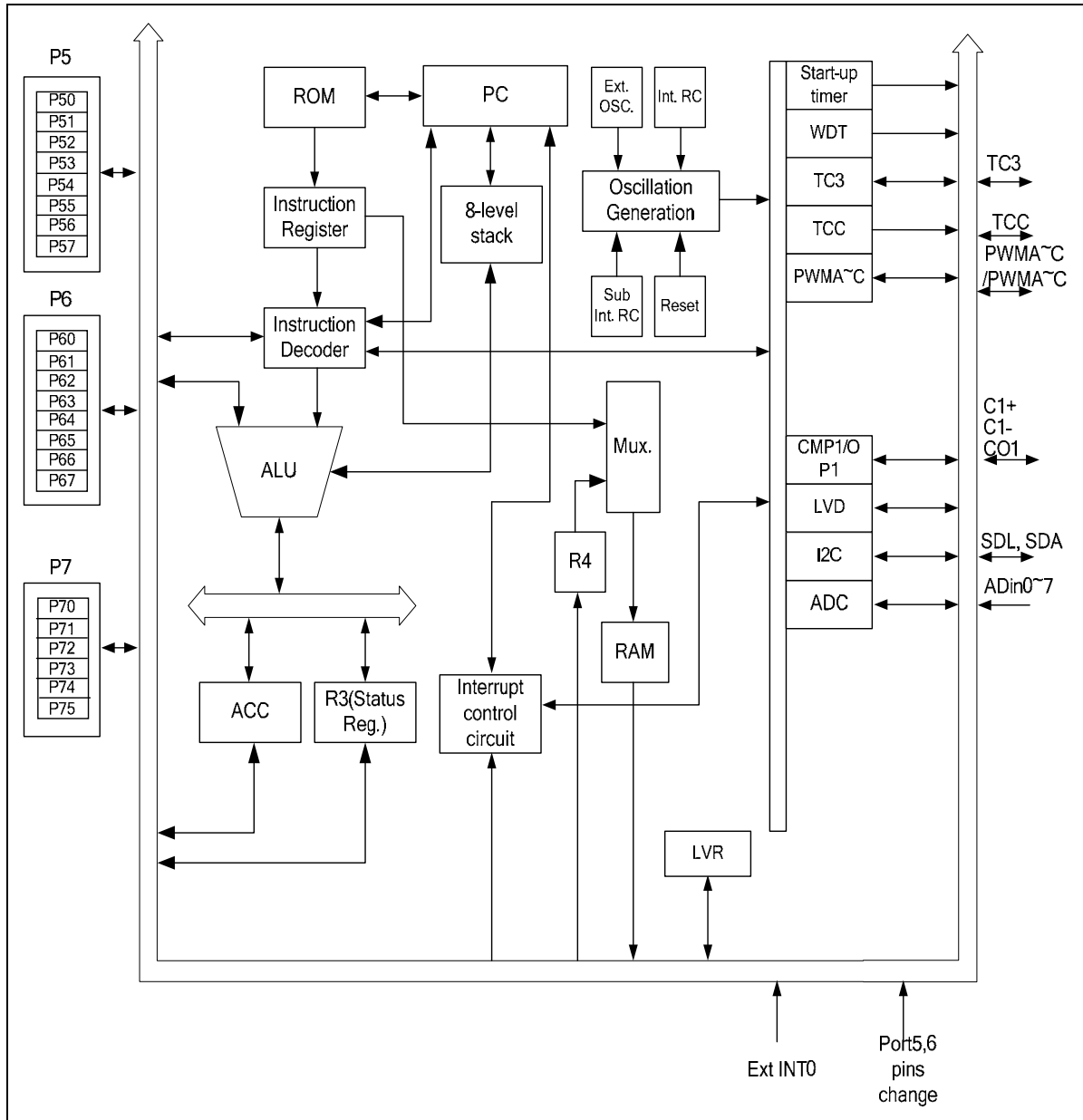


Figure 5-1 EM78P374N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	SBS0	-	GBS2	GBS1	GBS0
-	-	-	R/W	-	R/W	R/W	R/W

Bits 7 ~ 5: Not used, set to "0" all the time.

Bit 4 (SBS0): Special register bank select bit. It is used to select Bank 0/1 of Special Registers R5~R4F.

0: Bank 0

1: Bank 1

Bit 3: Not used, fixed to "0" all the time.

Bits 2 ~ 0 (GBS2 ~ GBS0): General register bank select bit. It is used to select Banks 0~7 of General Registers R80~RFF.

GBS2	GBS1	GBS0	RAM Bank
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

6.1.3 R2: PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (PC7~PC0): Low byte of the program counter.

- Depending on the device type, R2 and hardware stack are 14-bit wide. The structure is depicted in Figure 6-1.



- Generates 4K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "0"s when under reset condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the current PC value will be incremented by 1 and is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 15 program counter bits. Therefore, "LJMP" allows the PC to jump to any location within 4K (2^{12}).
- "LCALL" instruction loads the lower 15 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will remain unchanged.
- Any instruction, except "ADD R2,A" that is written to R2 (e.g., "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the above bits (A8~A12) of the PC to remain unchanged.
- All instructions are single instruction cycle ($F_{sys}/2$), except "LCALL" and "LJMP" instructions. The "LCALL" and "LJMP" instructions need two instruction cycles.

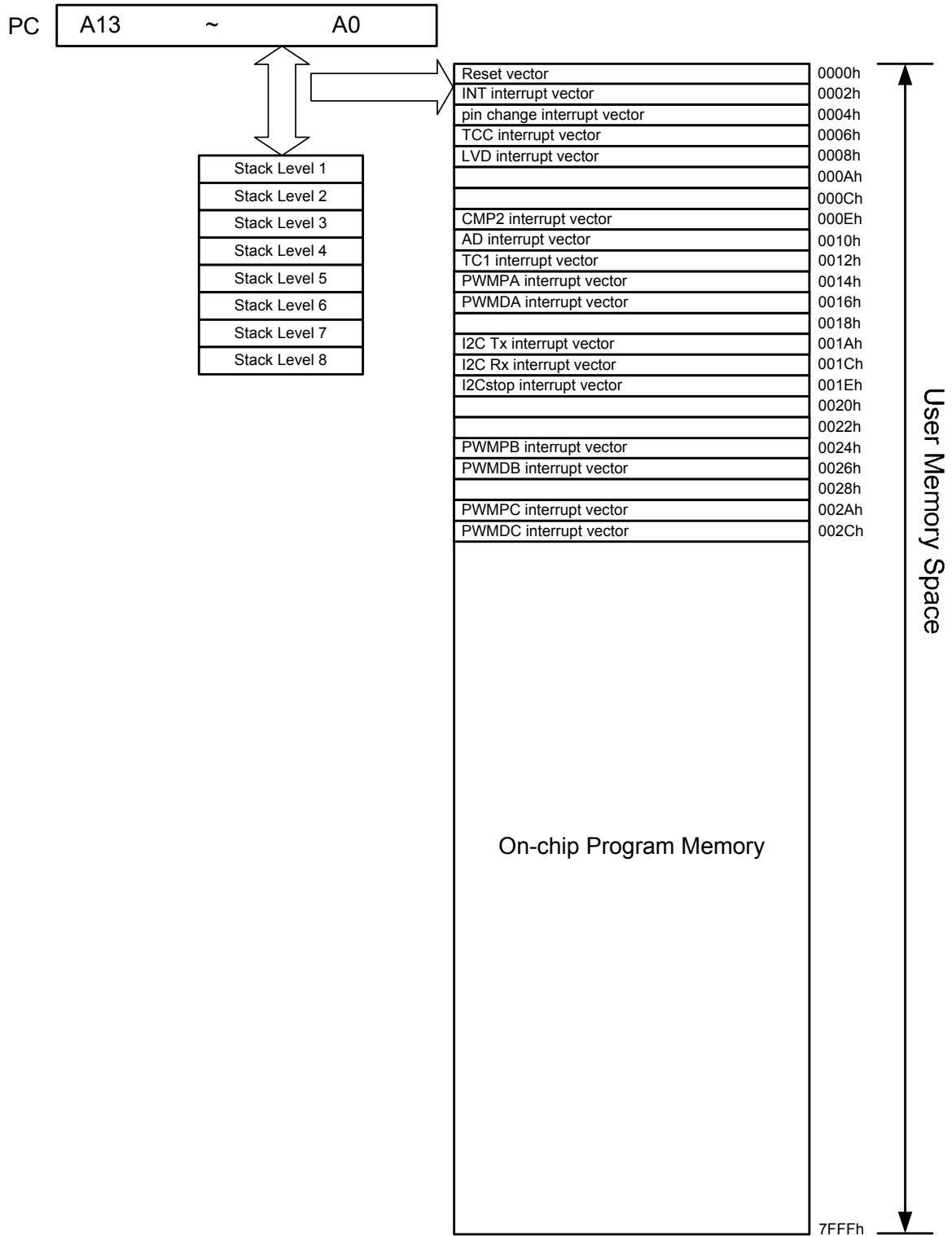


Figure 6-1 EM78P374N Program Counter Organization

■ **Data Memory Configuration**

Address	Bank 0	Bank 1
0X00	IAR (Indirect Addressing Register)	
0X01	BSR (Bank Select Control Register)	
0X02	PC (Program Counter)	-
0X03	SR (Status Register)	
0X04	RSR (RAM Select Register)	
0X05	Port 5	-
0X06	Port 6	-
0X07	Port 7	-
0X08	-	P5PHCR
0X09	-	P6PHCR
0X0A	-	P7PHCR
0x0B	IOC5	P5PLCR
0X0C	IOC6	P6PLCR
0X0D	IOC7	P7PLCR
0X0E	OMCR (Operating Mode Control Reg.)	P5HDSCR
0X0F	IESCR	P6HDSCR
0X10	WUCR1	P7HDSCR
0X11	WUCR2	P5ODCR
0X12	WUCR3	P6ODCR
0X13	-	P7ODCR
0X14	SFR1 (Status Flag Register 1)	-
0X15	SFR2 (Status Flag Register 2)	-
0X16	SFR3 (Status Flag Register 3)	PWMSCR
0X17	SFR4 (Status Flag Register 4)	PWMACR
0X18	SFR5 (Status Flag Register 5)	PRDAL
0X19	-	PRDAH
0X1A	-	DTAL
0X1B	IMR1 (Interrupt Mask Register 1)	DTAH
0X1C	IMR2 (Interrupt Mask Register 2)	TMRAL
0X1D	IMR3 (Interrupt Mask Register 3)	TMR AH
0X1E	IMR4 (Interrupt Mask Register 4)	PWMBCR
0X1F	IMR5 (Interrupt Mask Register 5)	PRDBL
0X20	-	PRDBH
0X21	WDTCR	DTBL
0X22	TCCCR	DTBH
0X23	TCCD	TMRBL
0X24	TC1CR1	TMRBH
0X25	TC1CR2	PWMCCR
0X26	TC1DA	PRDCL
0X27	TC1DB	PRDCH
0X28	-	DTCL
0X29	-	DTCH
0X2A	-	TMRCL
0x2B	-	TMRCH



(Continuation)

Address	Bank 0	Bank 1
0X2C	-	-
0X2D	-	-
0X2E	-	-
0X2F	-	-
0X30	I2CCR1	-
0X31	I2CCR2	-
0X32	I2CSA	-
0X33	I2CDB	-
0X34	I2CDAL	-
0X35	I2CDAH	-
0X36	-	-
0X37	-	-
0X38	-	-
0X39	-	-
0X3A	-	-
0x3B	CMP2CR	-
0X3C	CMP3CR	-
0X3D	-	-
0X3E	ADCR1	-
0X3F	ADCR2	-
0X40	ADISR	-
0X41	ADER1	-
0X42	ADER2	-
0X43	ADDL	-
0X44	ADDH	-
0X45	ADCVL	TBPTL
0X46	ADCVH	TBPTH
0X47	Unused	STKMON
0X48	-	PCH
0X49	-	LVDCR
0X4A	-	-
0x4B	-	-
0X4C	-	-
0X4D	-	-
0X4E	-	-
0X4F	-	-
0X50	General Purpose Register	
0X51		
:		
:		
0X7F		

(Continuation)

Address	Bank 0	Bank 1
0X80	Bank 0	Bank 1
0X81		
:		
:		
:		
0XFE		
0XFF		

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	-	-	T	P	Z	DC	C
F	-	-	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/DISI instructions

Bits 6 ~ 5: Not used, set to "0" all the time.

Bit 4 (T): Time-out bit

Set to "1" with the "SLEP" and "WDTC" commands, or during power up.

Reset to "0" by WDT time-out.

Bit 3 (P): Power down bit

Set to "1" during power on or by a "WDTC" command

Reset to "0" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (RSR7 ~ RSR0): These bits are used to select registers (Address: 00~FF) in the indirect address mode. For more details, refer to the table on Data Memory Configuration in Section 6.1.3, R2: PCL (Program Counter Low).

6.1.6 Bank 0 R5 ~ R7: (Port 5 ~ Port 7)

R5, R6 and R7 are I/O data registers.

6.1.7 Bank 0 R8~RA:

(Not used. Set to "0" all the time)

6.1.8 Bank 0 RB~RD: (IOCR5 ~ IOCR7)

These registers are used to control I/O port direction. They are both readable and writable.

0: Put the relative I/O pin as output

1: Put the relative I/O pin into high impedance

6.1.9 Bank 0 RE: OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	-	-	-	-	RCM1	RCM0
R/W	R/W	-	-	-	-	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select

0: Fs: sub-oscillator

1: Fm: main-oscillator

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit determines which mode (see figure below) is to be activated after SLEP instruction.

0: "IDLE=0"+SLEP instruction → Sleep mode

1: "IDLE=1"+SLEP instruction → Idle mode

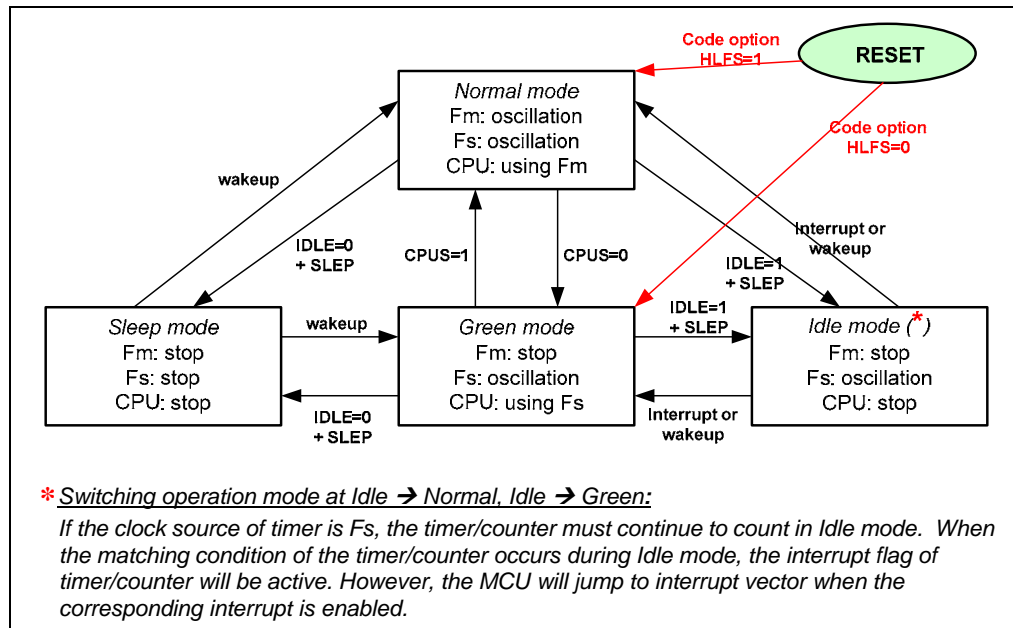


Figure 6-2 CPU Operation Mode

■ Oscillation Characteristics

Oscillation Mode	CPU Mode Switch	Waiting Time before CPU Starts to Work
Crystal Mode	Sleep → Normal	WSTO + 510 clocks (main frequency)
	Idle → Normal	WSTO + 510 clocks (main frequency)
	Green → Normal	WSTO + 510 clocks (main frequency)
	Sleep → Green	WSTO + 8 clocks (sub frequency)
	Idle → Green	WSTO + 8 clocks (sub frequency)
IRC Mode	Sleep → Normal	WSTO + 8 clocks (main frequency)
	Idle → Normal	WSTO + 8 clocks (main frequency)
	Green → Normal	WSTO + 8 clocks (main frequency)
	Sleep → Green	WSTO + 8 clocks (sub frequency)
	Idle → Green	WSTO + 8 clocks (sub frequency)

WSTO: Waiting time of Start-to-Oscillation

Bits 5 ~ 3: Not used. Set to "0" all the time

Bits 2 ~ 1 (RCM1 ~ RCM0): Internal RC mode selection bits

RCM1	RCM0	Frequency (MHz)
0	0	1
0	1	8
1	0	16
1	1	4

6.1.10 Bank 0 RF: IESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	EIES54	-	-	-	-	-
-	-	R/W	-	-	-	-	-

Bits 5 (EIES54): External interrupt edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

6.1.11 Bank 0 R10: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2WK	-	LVDWK	ADWK	-	-	-	-
R/W	-	R/W	R/W	-	-	-	-

Bit 7 (CMP2WK): Comparator 2 Wake-up Enable bit

0: Disable Comparator 2 wake-up.

1: Enable Comparator 2 wake-up.

Bit 6: Not used. Set to “0” all the time.

Bit 5 (LVDWK): Low Voltage Detect Wake-up Enable bit

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

Bit 4 (ADWK): A/D Converter Wake-up Function Enable bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When the AD Complete status is used to enter an interrupt vector or to wake-up IC from Sleep/Idle mode with AD conversion running, the ADWK bit must be set to “Enable”.

Bits 3 ~ 0: Not used. Set to “0” all the time

6.1.12 Bank 0 R11: WUCR2 (Wake-up Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	I2CWK	-	-
-	-	-	-	-	R/W	-	-

Bits 7 ~ 3: Not used. Set to “0” all the time.

Bit 2 (I2CWK): I2C wake-up enable bit. It is available when I2C works in Slave mode.

0: Disable

1: Enable

Bits 1 ~ 0: Not used. Set to “0” all the time.



6.1.13 Bank 0 R12: WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ICWKP6	ICWKP5	-	-	INTWK5	-
-	-	R/W	R/W	-	-	R/W	-

Bits 5 ~ 4 (ICWKP6 ~ 5): (Ports 6 ~ 5) Pin-change Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status change is used to enter an interrupt vector or to wake-up the IC from Sleep/Idle, the INTWK bits must be set to "Enable".

Pin Change Wake-up Function Enable*				
CPU Mode	Normal / Green		Sleep / Idle	
Global interrupt	DISI	ENI	DISI	ENI
ICIE = 0 Next instruction	(ICSF=1 or 0)** Next instruction	(ICSF=1 or 0) Wake up (ICSF=1)	+	Next instruction Wake up (ICSF=1)
ICIE = 1 Next instruction	(ICSF=1 or 0) Interrupt vector	(ICSF=1) Wake up (ICSF=1)	+	Next instruction Wake up (ICSF=1)

* If the Pin Change Wake-up function is disabled, the ICSF is always equals to "0".

** When the ICSF is equal to "1", the MCU will wake-up from Sleep or Idle mode. If ICSF is equal to "0", pin change condition does NOT occur. Hence, the MCU will NOT be awakened by pin change.

Bits 7 ~ 6, 3 ~ 2, 0: Not used. Set to "0" all the time.

Bit 1 (INTWK5): External Interrupt (INT pin) Wake-up Function Enable bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status change is used to enter an interrupt vector or to wake-up the MCU from Sleep/Idle mode, the EXWE bits must be set to "Enable".

6.1.14 Bank 0 R13:

(Not used. Set to "0" all the time)

6.1.15 Bank 0 R14: SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2SF	-	LVDSF	ADSF	-	-	-	TCSF
F	-	F	F	-	-	-	F

Each corresponding status flag is set to “1” when interrupt condition is triggered.

Bit 7 (CMP2SF): Comparator 2 status flag. Set when a change occurs in the output of Comparator 2. Reset by software.

Bit 6: Not used. Set to “0” all the time.

Bit 5 (LVDSF): Low Voltage Detector status flag:

LVDEN	LVDS2, LVDS1, LVDS0	LVD Voltage Interrupt Level	LVDSF
1	011	2.2V	1*
1	010	3.3V	1*
1	001	4.0V	1*
1	000	4.5V	1*
0	XX	NA	0

* If Vdd crossovers at the LVD voltage interrupt level as Vdd varies, LVDSF=1.

Bit 4 (ADSF): Status flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.

Bits 3 ~ 1: Not used. Set to “0” all the time.

Bit 0 (TCSF): TCC overflow status flag. Set when TCC overflows. Reset by software.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.



6.1.16 Bank 0 R15: SFR2 (Status Flag Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	TC1DSF
-	-	-	-	-	-	-	F

Each corresponding status flag is set to “1” when interrupt condition is triggered.

Bits 7 ~ 1: Not used. Set to “0” all the time.

Bit 0 (TC1DSF): 8-bit Timer/Counter 1 status flag. Clear by software.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.17 Bank 0 R16: SFR3 (Status Flag Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMCPSF	PWMCDSF	PWMBPSF	PWMBDSF	PWMA PSF	PWMA DSF
-	-	F	F	F	F	F	F

Bits 7 ~ 6: Not used. Set to “0” all the time.

Bit 5 (PWMCPSF): Status flag of period-matching for PWMC (Pulse Width Modulation).
Set when a selected period is reached. Reset by software.

Bit 4 (PWMCDSF): Status flag of duty-matching for PWMC (Pulse Width Modulation).
Set when a selected duty is reached. Reset by software.

Bit 3 (PWMBPSF): Status flag of period-matching for PWMB (Pulse Width Modulation).
Set when a selected period is reached. Reset by software.

Bit 2 (PWMBDSF): Status flag of duty-matching for PWMB (Pulse Width Modulation).
Set when a selected duty is reached. Reset by software.

Bit 1 (PWMA PSF): Status flag of period-matching for PWMA (Pulse Width Modulation).
Set when a selected period is reached. Reset by software.

Bit 0 (PWMA DSF): Status flag of duty-matching for PWMA (Pulse Width Modulation).
Set when a selected duty is reached. Reset by software.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.18 Bank 0 R17: SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6ICSF	P5ICSF	-	I2CSTPSF	I2CRSF	I2CTSF
-	-	F	F	-	F	F	F

Bits 7 ~ 6: Not used. Set to "0" all the time.

Bit 5 (P6ICSF): Port 6 status flag. Flag is cleared by software.

Bit 4 (P5ICSF): Port 5 status flag. Flag is cleared by software.

Bit 3: Not used. Set to "0" all the time.

Bit 2 (I2CSTPSF): I2C stop status flag. Set when I2C stop signal occurs.

Bit 1 (I2CRSF): I2C receive status flag. Set when I2C receives 1 byte data and responds with an ACK signal. Reset by firmware or disable I2C.

Bit 0 (I2CTSF): I2C transmit status flag. Set when I2C transmits 1 byte data and receives a handshake signal (ACK or NACK). Reset by firmware or disable I2C.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.19 Bank 0 R18: SFR5 (Status Flag Register 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EXSF5	-	-	-
-	-	-	-	F	-	-	-

Each corresponding status flag is set to "1" when interrupt condition is triggered.

Bits 7 ~ 4, 2 ~ 0: Not used. Set to "0" all the time.

Bit 3 (EXSF5): External interrupt status flag

INT Pin	Enable Condition	Edge	Digital Noise Reject
INTX	(ENI+) EXIEX	Rising or Falling	8/Fc or 32/Fc

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.20 Bank 0 R1B: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	-	LVDIE	ADIE	-	-	-	TCIE
R/W	-	R/W	R/W		-	-	R/W

Bit 7 (CMP2IE): CMP2SF interrupt enable bit

0: Disable CMP2SF interrupt

1: Enable CMP2SF interrupt

When the Comparator output status change is used to enter interrupt vector, the CMP2IE bit must be set to "Enable".

Bit 6: Not used. Set to "0" all the time.

Bit 5 (LVDIE): LVDSF interrupt enable bit

0: Disable LVDSF interrupt

1: Enable LVDSF interrupt

Bit 4 (ADIE): ADSF interrupt enable bit

0: Disable ADSF interrupt

1: Enable ADSF interrupt.

Bits 3~1: Not used. Set to "0" all the time.

Bit 0 (TCIE): TCSF interrupt enable bit.

0: Disable TCSF interrupt

1: Enable TCSF interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.21 Bank 0 R1C: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	TC1DIE
-	-	-	-	-	-	-	R/W

Bits 7 ~ 1: Not used. Set to "0" all the time.

Bit 0 (TC1DIE): Interrupt enable bit

0: Disable TC1DSF interrupt

1: Enable TC1DSF interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.22 Bank 0 R1D IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMCPIE	PWMC DIE	PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 6: Not used. Set to “0” all the time.

Bit 5 (PWMCPIE): PWMCP SF interrupt enable bit

0: Disable period-matching of PWMC interrupt

1: Enable period-matching of PWMC interrupt

Bit 4 (PWMC DIE): PWMCD SF interrupt enable bit

0: Disable duty-matching of PWMC interrupt

1: Enable duty-matching of PWMC interrupt

Bit 3 (PWMBPIE): PWMBP SF interrupt enable bit

0: Disable period-matching of PWMB interrupt

1: Enable period-matching of PWMB interrupt

Bit 2 (PWMBDIE): PWMBD SF interrupt enable bit

0: Disable duty-matching of PWMB interrupt

1: Enable duty-matching of PWMB interrupt

Bit 1 (PWMAPIE): PWMAP SF interrupt enable bit

0: Disable period-matching of PWMA interrupt

1: Enable period-matching of PWMA interrupt

Bit 0 (PWMADIE): PWMAD SF interrupt enable bit.

0: Disable duty-matching of PWMA interrupt

1: Enable duty-matching of PWMA interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.



6.1.23 Bank 0 R1E: IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6ICIE	P5ICIE	-	I2CSTPIE	I2CRIE	I2CTIE
-	-	R/W	R/W	-	R/W	R/W	R/W

Bits 7 ~ 6: Not used. Set to "0" all the time.

Bit 5 (P6ICIE): Port 6 pin-change Interrupt Enable bit
0: Disable P6ICSF interrupt
1: Enable P6ICSF interrupt

Bit 4 (P5ICIE): Port 5 pin-change Interrupt Enable bit
0: Disable P5ICSF interrupt
1: Enable P5ICSF interrupt

Bit 3: Not used. Set to "0" all the time.

Bit 2 (I2CSTPIE): I2C stop interrupt enable bit
0: Disable interrupt
1: Enable interrupt

Bit 1 (I2CRIE): I2C Interface Rx Interrupt Enable bit
0: Disable interrupt
1: Enable interrupt

Bit 0 (I2CTIE): I2C Interface Tx Interrupt Enable bit
0: Disable interrupt
1: Enable interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.24 Bank 0 R1F: IMR5 (Interrupt Mask Register 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EXIE5	-	-	-
-	-	-	-	R/W	-	-	-

Bits 7~ 4, 2 ~ 0: Not used. Set to "0" all the time.

Bit 3 (EXIE5): EXSF5 interrupt enable bit
0: Disable EXSF5 interrupt
1: Enable EXSF5 interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.25 Bank 0 R21: WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer enable bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1.

1: Prescaler enable bit. WDT rate is set at Bits 2~0.

Bits 2 ~ 0 (WPSR2 ~ WPSR0): WDT Prescale bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.26 Bank 0 R22: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TCCS	TS	TE	PSTE	TPSR2	TPSR1	TPSR0
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used. Set to "0" all the time.

Bit 6 (TCCS): TCC Clock Source Select Bit

0: Fs (sub clock)

1: Fm (main clock)

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock

1: Transition on the TCC pin. The TCC period must be larger than internal instruction clock period.

Bit 4 (TE): TCC Signal Edge
0: Increment if the transition from low to high takes place on the TCC pin.
1: Increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC
0: Prescaler disable bit. TCC rate is 1:1.
1: Prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bits 2 ~ 0 (TPSR2 ~ TPSR0): TCC Prescaler bits

TPSR2	TPSR1	TPSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.27 Bank 0 R23: TCCD (TCC Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TCC7 ~ TCC0): TCC data

Increase by an external signal edge through the TCC pin, or by the instruction cycle clock. The External signal of TCC trigger pulse width must be greater than one instruction. The signals to increase the counter are determined by Bit 4 and Bit 5 of the TCCCR register. They are writable and readable as any other registers. If there is an overflow, the value previously written to TCCD will be auto-reloaded to the TCC circuit.

6.1.28 Bank 0 R24: TC1CR1 (Timer/Counter 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1S	TC1RC	TC1SS1	-	TC1FF	TC1OMS	TC1IS1	TC1IS0
R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

Bit 7 (TC1S): Timer/Counter 1 start control
0: Stop and clear the counter (default)
1: Start Timer/Counter 1

- Bit 6 (TC1RC):** Timer 1 Read Control bit
0: When this bit is set to “0”, data from TC1DB can’t be read (default).
1: When this bit is set to “1”, data is read from TC1DB. The read data is the enumerated counting number.
- Bit 5 (TC1SS1):** Timer/Counter 1 clock source select bit
0: Select internal clock as count source (Fc) - Fs/Fm (default)
1: Select external TC1 pin as count source (Fc). It is used only for timer/counter mode.
- Bit 4:** Not used. Set to “0” all the time.
- Bit 3 (TC1FF):** Inversion for Timer/Counter 1 as PWM
0: Duty is Logic 1 (default)
1: Duty is Logic 0
- Bit 2 (TC1OMS):** Timer Output Mode select bit
0: Repeat mode (default)
1: One-shot mode

NOTE

One-shot mode means the Timer only counts a cycle.

- Bits 1 ~ 0 (TC1IS1 ~ TC1IS0):** Timer 1 Interrupt Type select bits. These two bits are used when the Timer operates in PWM mode.

TC1IS1	TC1IS0	Timer 1 Interrupt Type Select
0	0	TC1DA (period) matching
0	1	TC1DB (duty) matching
1	×	TC1DA and TC1DB matching

6.1.29 Bank 0 R25: TC1CR2 (Timer/Counter 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 7 ~ 5 (TC1M2 ~ TC1M0):** Timer/Counter 1 operation mode select

TC1M2	TC1M1	TC1M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of clock source must be 50/50)

Bit 4 (TC1SS0): Timer/Counter 1 clock source selection bit

0: Fs is used as count source (Fc) (default)

1: Fm is used as count source (Fc)

Bits 3~0 (TC1CK3~TC1CK0): Timer/Counter 1 clock source prescaler select:

TC3CK3	TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
				Normal	F _C =8M	F _C =8M	F _C =16K	F _C =16K
0	0	0	0	F _C	125ns	32μs	62.5μs	16ms
0	0	0	1	F _C /2	250ns	64μs	125μs	32ms
0	0	1	0	F _C /2 ²	500ns	128μs	250μs	64ms
0	0	1	1	F _C /2 ³	1μs	256μs	500μs	128ms
0	1	0	0	F _C /2 ⁴	2μs	512μs	1ms	256ms
0	1	0	1	F _C /2 ⁵	4μs	1024μs	2ms	512ms
0	1	1	0	F _C /2 ⁶	8μs	2048μs	4ms	1024ms
0	1	1	1	F _C /2 ⁷	16μs	4096μs	8ms	2048ms
1	0	0	0	F _C /2 ⁸	32μs	8192μs	16ms	4096ms
1	0	0	1	F _C /2 ⁹	64μs	16384μs	32ms	8192ms
1	0	1	0	F _C /2 ¹⁰	128μs	32768μs	64ms	16384ms
1	0	1	1	F _C /2 ¹¹	256μs	65536μs	128ms	32768ms
1	1	0	0	F _C /2 ¹²	512μs	131072μs	256ms	65536ms
1	1	0	1	F _C /2 ¹³	1.024ms	262144μs	512ms	131072ms
1	1	1	0	F _C /2 ¹⁴	2.048ms	524.288ms	1.024s	262144ms
1	1	1	1	F _C /2 ¹⁵	4.096ms	1.048s	2.048s	524288ms

6.1.30 Bank 0 R26: TC1DA (Timer/Counter 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TC1DA7 ~ TC1DA0): Data Buffer A of 8 bit Timer/Counter 1

6.1.31 Bank 0 R27: TC1DB (Timer/Counter 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TC1DB7 ~ TC1DB0): Data Buffer B of 8 bit Timer/Counter 1