EM78P372N

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

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ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre 95
How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:
Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Korea:
Elan Korea Electronics Company, Ltd.
301 Dong-A Building
632 Kojan-Dong, Namdong-ku
Incheon City, KOREA
Tel: +82 32 814-7730
Fax: +82 32 813-7730

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
8A Floor, Microprofit Building
Gaoxin South Road 6
South Area, Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:
ELAN Microelectronics Shanghai, Ltd.
6F, Ke Yuan Building
No. 5 Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA 201203
Tel: +86 21 5080-3866
Fax: +86 21 5080-0273
elan-sh@elanic.com.cn

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2010/06/21
0.91	Preliminary version	2010/07/19
0.92	Modified the IOCC0 Control Register Modified the Bank 1-RF[3:0] Control Reigster Modified the Bank 0-RA[2:0] Control Reigster	2010/08/06
1.0	Initial Version Modified the Operating frequency range (DC ~ 16 MHz)	2010/12/10
1.1	1. Modified the Electrical Characteristics 2. Modified the Quality Assurance and Reliability section in the Appendix.	2011/05/24
1.2	1. Added the EM78P372NQN16S Package Type 2. Deleted the EM78P372NSS10J/S Package Type . 3. Fixed the number of I/O and their description in the Features section. 4. Added Ordering and Manufacturing Information. 5. Modified the Instruction table 6. Modified the Part Number 7. Modifed the description about POR and LVR in the Features section	2012/02/10

1 General Description

The EM78P372N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has an on-chip 2K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Three Code option bits are also available to meet user's requirements.

With enhanced OTP-ROM features, the EM78P372N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 2K×13 bits on-chip ROM
  - 80×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Less than 1.5 mA at 5V/4 MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - Three bidirectional I/O ports: P5, P6, P7
  - 18 I/O pins
  - Wake-up port : P5
  - Eight programmable pull-down I/O pins (P50 ~ P57)
  - 16 programmable pull-high I/O pins (P50 ~ P57) (P60 ~ P67)
  - Eight programmable open-drain I/O pins (P60~P67)
  - 14 programmable high-sink current I/O pins (P51 ~ P54, P56 ~ P57) (P60 ~ P67)
  - External interrupt : P60
- Operating voltage range:
  - 2.1V~5.5V at 0°C~70°C (commercial)
  - 2.3V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on two clocks):
  - Crystal mode: DC ~ 16 MHz, 4.5V; DC ~ 8 MHz, 3V; DC ~ 4 MHz, 2.1V
  - ERC mode: DC ~ 2 MHz, 2.1V;
  - IRC mode
    Oscillation mode: 16 MHz, 4 MHz, 1 MHz, 8 MHz

Internal RC Freq.	Drift Rate			
	Temp. (-40~85℃)	Voltage (2.1~5.5V)	Process	Total
4 MHz	±2%	±1% *(2.1~5.5V)	±2%	±5%
16 MHz	±2%	±1% *(4.5~5.5V)	±2%	±5%
8 MHz	±2%	±1% *(3.0~5.5V)	±2%	±5%
1 MHz	±2%	±1% *(2.1~5.5V)	±2%	±5%

*Operating voltage range

- All the four main frequencies can be trimmed by programming with six calibrated bits in the ICE300N Simulator. OTP is auto trimmed by ELAN Writer.
- Fast set-up time requires only 0.8ms (VDD: 5V Crystal: 4 MHz, C1/C2: 15pF) in XT mode and 10μs in IRC mode (VDD: 5V, IRC: 4 MHz)
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 4 programmable Level Voltage Detector (LVD) : 4.5V, 4.0V, 3.3V, 2.2V
  - Power on reset and programmable level voltage reset POR: 1.8V (Default), LVR: 4.0V, 3.5V, 2.7V
  - 8-bit multi-channel Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - One pair of comparator or OP(offset voltage: smaller than 10mV)
  - Two Pulse Width Modulation (PWM) with 8-bit resolution
- Ten available interrupts
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - Comparator status change interrupt
  - Low voltage detect (LVD) interrupt
  - PWM1~2 period match interrupt
  - PWM1~2 duty match interrupt
- Special Features:
  - Programmable free running Watchdog Timer (4.5 ms : 18 ms)
  - Power saving Sleep mode
  - Power-on voltage detector available
  - High EFT immunity (better performance at 4 MHz or below)
- Package Type:
  - 10-pin MSOP 118mil : EM78P372NMS10J/S
  - 14-pin DIP 300mil : EM78P372ND14J/S
  - 14-pin SOP 150mil : EM78P372NSO14J/S
  - 16-pin SOP 150mil : EM78P372NSO16AJ/S
  - 18-pin DIP 300mil : EM78P372ND18J/S
  - 18-pin SOP 300mil : EM78P372NSO18J/S
  - 20-pin DIP 300mil : EM78P372ND20J/S
  - 20-pin SOP 300mil : EM78P372NSO20J/S
  - 20-pin SSOP 209mil : EM78P372NSS20J/S
  - 16-pin QFN 3×3×0.8mm : EM78P372NQN16S

Note: *These are Green products that do not contain hazardous substances.*

3 Pin Assignment

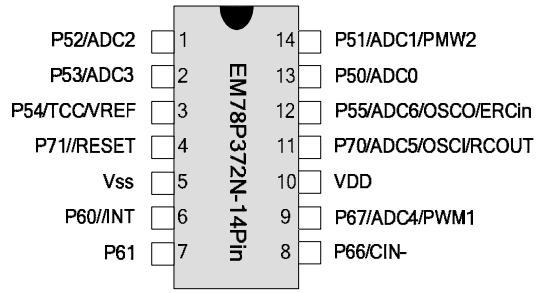

Figure 3-1 EM78P372ND14/SO14

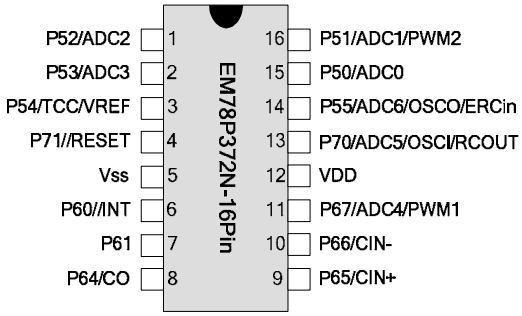

Figure 3-2 EM78P372NSO16A

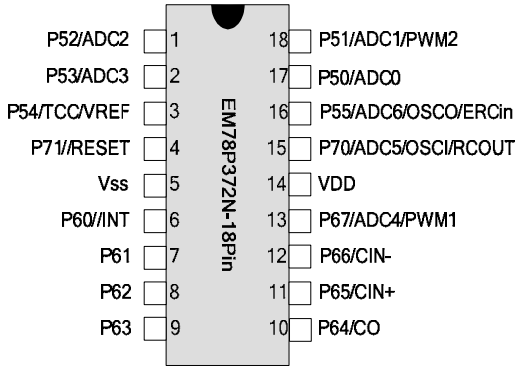

Figure 3-3 EM78P372ND18/SO18

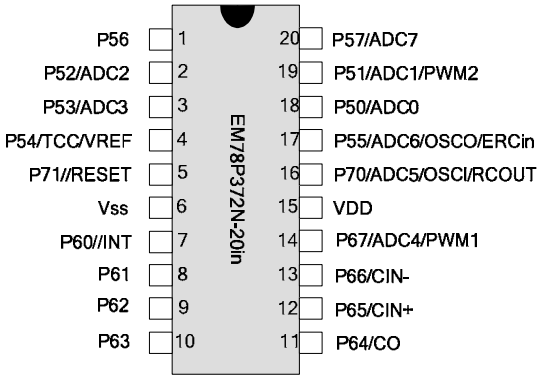

Figure 3-4 EM78P372ND20/SO20/SS20

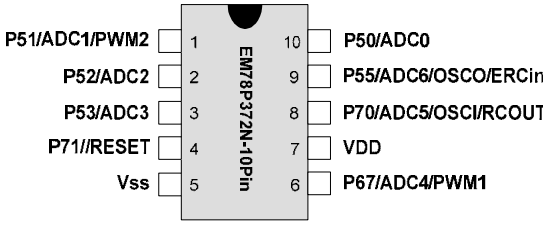

Figure 3-5 EM78P372NMS10

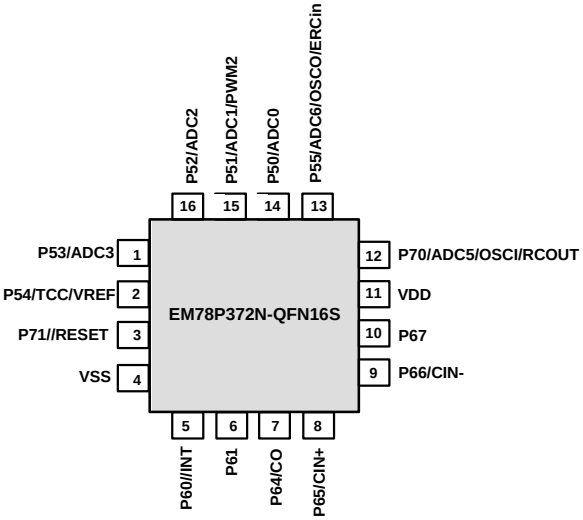

Figure 3-6 EM78P372NQN16S

4 Pin Description

Name	Function	Input Type	Output Type	Description
P50	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up.
	ADC0	AN	–	ADC Input 0
P51	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC1	AN	–	ADC Input 1
	PWM2	–	CMOS	PWM2 output
P52	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC2	AN	–	ADC Input 2
P53	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC3	AN	–	ADC Input 3
P54	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	TCC	ST	–	Real Time Clock/Counter clock input
	VREF	AN	–	ADC external voltage reference
P55	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up.
	ADC6	AN	–	ADC Input 6
	OSCO	–	XTAL	Clock output of crystal/ resonator oscillator
	ERCin	AN	–	External RC input pin
P56	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
P57	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC7	ST	–	ADC Input 7
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
	/INT	ST	–	External interrupt pin

Name	Function	Input Type	Output Type	Description
P61~P63	P61~P63	ST	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
P64/CO	P64	–	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
	CO	ST	–	Comparator output
P65/CIN+	P65	ST	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
	CIN+	ST	–	Non-inverting end of comparator
P66/CIN-	P66	ST	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
	CIN-	ST	–	Inverting end of comparator
P67/ADC4/PWM1	P67	ST	CMOS	Bidirectional I/O pins with programmable open-drain, pull-high, high-driver and high sink.
	ADC4	AN	–	ADC Input 4
	PWM1	–	CMOS	PWM1 output
P70/ADC5/OSCI/ RCOUT	P70	P70	–	Bidirectional I/O pin
	ADC5	AN	–	ADC Input 5
	OSCI	XTAL	–	Clock input of crystal/ resonator oscillator
	ROCUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P71	P71	ST	CMOS	Bidirectional I/O pin (open-drain)
	/RESET	ST	–	System reset pin (should be external pull-high)
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

Legend: *ST: Schmitt Trigger input* *AN: analog pin*

XTAL: oscillation pin for crystal/resonator *CMOS: CMOS output*

5 Block Diagram

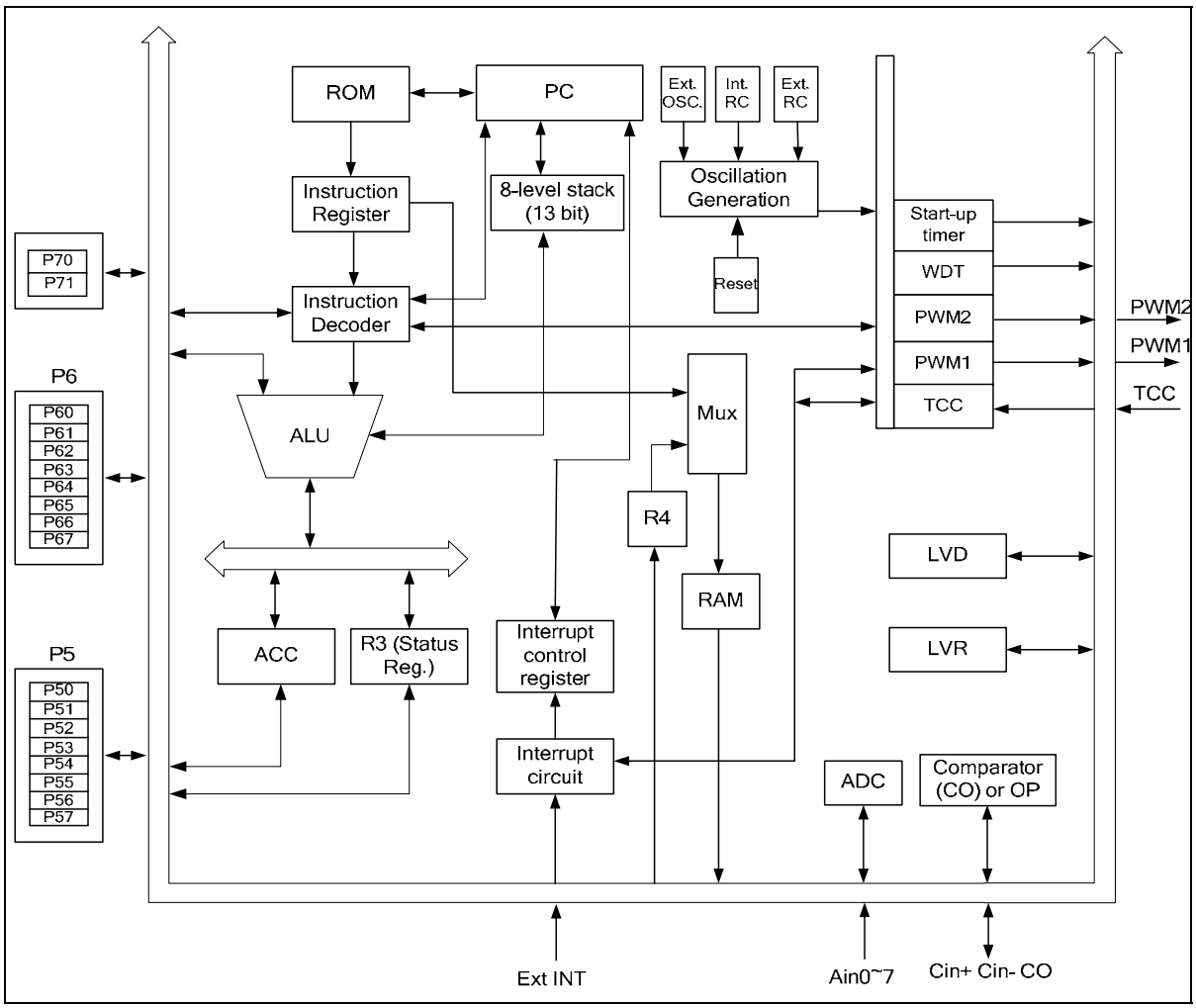

Figure 5-1 EM78P372N Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1 (Time Clock/Counter)

- Incremented by an external signal edge which is defined by the TE bit (CONT-5) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- The TCC prescaler counter is assigned to TCC
- The contents of the CONT register is cleared whenever –
  - a value is written to the TCC register
  - a value is written to the TCC prescaler bits (Bits 3, 2, 1, 0 of the CONT register)
  - there's power-on reset, /RESET, or WDT time out reset

6.1.3 R2 (Program Counter) and Stack

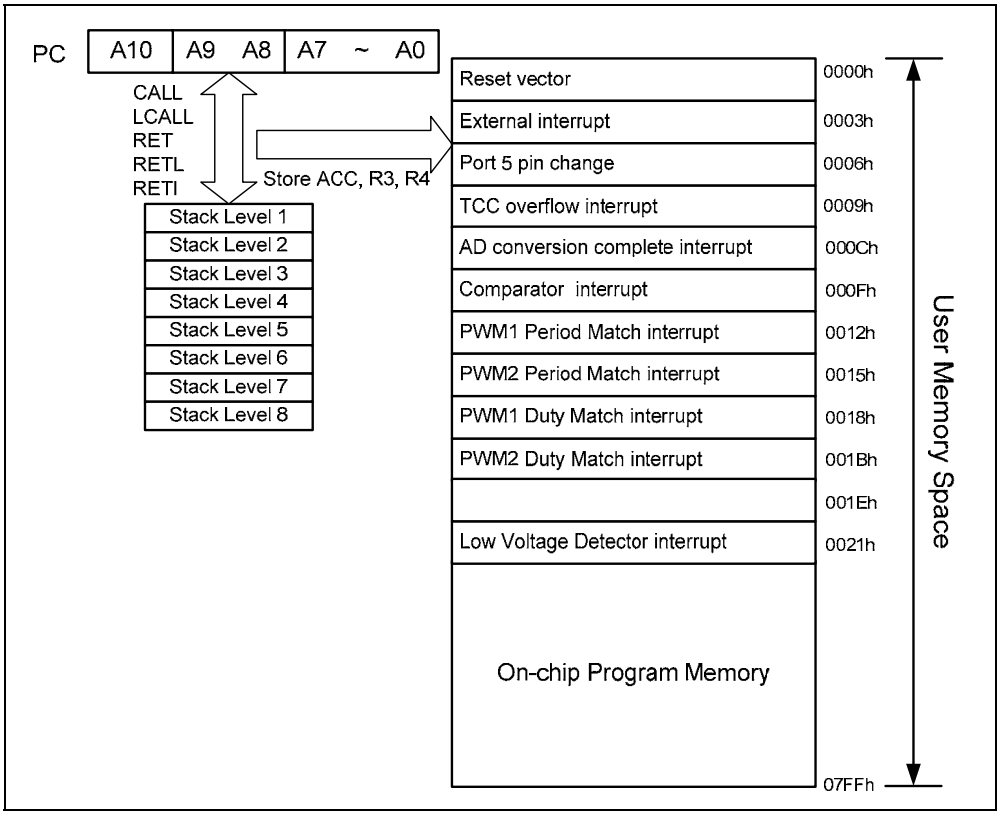

Figure 6-1 Program Counter Organization

- R2 and hardware stacks are 11-bit wide. The structure is depicted in the table under Section 6.1.3.1 *Data Memory Configuration*.
- The configuration structure generates 2K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "0"s when a reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the program counter bits (A0~A10). Therefore, "LJMP" allows the PC to jump to any location within 2K (2^{11}).
- "LCALL" instruction loads the program counter bits (A0 ~A10), and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 2K (2^{11})
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of the stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except “ADD R2, A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2) except “LCALL” and “LJMP” instructions. The “LCALL” and “LJMP” instructions need two instruction cycles.

6.1.3.1 Data Memory Configuration

Address	Register Bank 0	Register Bank 1	IOC Page 0	IOC Page 1
00	R0 (Indirect Addressing Register)			
01	R1 (Timer Clock Counter)			
02	R2 (Program Counter)			
03	R3 (Status Register)			
04	R4 (RSR, Bank select)			
05	R5 (Port 5 I/O data)	R5 (TBHP: Table Point Register)	IOC50 (Port 5 I/O control)	IOC51 (HSCR1: High Sink Control Register 1)
06	R6 (Port 6 I/O data)	R6 (TBLP: Table Point Register)	IOC60 (Port 6 I/O control)	IOC61 (HSCR2: High Sink Control Register 2)
07	R7 (Port 7 I/O data)	R7 (PWMCON: PWM Control Register)	IOC70 (Port 7 I/O control)	IOC71 (HDCR1: High Driver Control Register1)
08	R8 (ADC Input Select Register)	R8 (TMRCON: Timer Control Register)	IOC80 (Comparator Control Register)	IOC81 (HDCR2: High Driver Control Register2)
09	R9 (ADC Control Register)	R9 (PRD1: PWM1 Time Period)	IOC90 (TMR1: PWM1 Timer)	IOC91 (Reserved)
0A	RA (ADC Offset Calibration Register)	RA (PRD2: PWM2 Time Period)	IOCA0 ((TMR2: PWM2 Timer)	IOCA1 (Reserved)
0B	RB (Converted value AD11~AD4 of ADC)	RB (DT1: PMW1 Duty Cycle)	IOCB0 (Pull-down Control Register)	IOCB1 (Reserved))
0C	RC (Converted value AD11~AD8 of ADC)	RC (DT2: PMW2 Duty Cycle)	IOCC0 (Open-drain Control Register)	IOCC1 (Reserved))
0D	RD (Converted value AD7~AD0 of ADC)	RD (Reserved)	IOCD0 (Pull-high Control Register)	IOCD1 (Reserved)
0E	RE (Interrupt Status 2 and Wake-up Control Register 1)	RE (LVD Control and Wake-up Control Register 2)	IOCE0 (WDT Control Register and Interrupt Mask Register 2)	IOCE1 (Reserved)
0F	RF (Interrupt Status Register 1)	RF (Mode Select and IRC Switch Register)	IOCF0 (Interrupt Mask Register 1)	IOCF1 (Pull-high Control Register)
10 : 1F	16-Byte Common Register			
20 : 3F	Bank 0 32x8	Bank 1 32x8		

Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	IOCS	–	T	P	Z	DC	C

Bit 7 (RST): Bit of reset type

Set to “1” if wake-up from sleep on pin change, comparator status change, or AD conversion completed. Set to “0” if wake-up from other reset types.

Bit 6 (IOCS): Select the Segment of IO control register

0: Segment 0 (IOC50 ~ IOCF0) selected

1: Segment 1 (IOC51 ~ IOCC1) selected

Bit 5: Not used, set “0” at all the time.

Bit 4 (T): Time-out bit. Set to “1” by the "SLEP" and "WDTC" commands or during power on**,** and reset to “0” by WDT time-out (for more details, see Section 6.5.2, *The T and P Status under Status Register*).

Bit 3 (P): Power-down bit. Set to “1” during power-on or by a "WDTC" command and reset to “0” by a "SLEP" command (see Section 6.5.2, *The T and P Status under Status Register* for more details).

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7 (SBANK): Special Register 0x05~0x0F bank selection bit.

Bit 6 (BANK): Used to select Bank 0 or Bank 1 of the register

Bits 5 ~ 0: Used to select a register (Address: 00~0F, 10~3F) in indirect addressing mode.

See the table under Section 6.1.3.1 *Data Memory Configuration*.

6.1.6 Bank 0 R5 ~ R7 (Port 5 ~ Port 7)

R5 and R6, P70 and P71 are I/O registers.

6.1.7 Bank 0 R8 (AISR: ADC Input Select Register)

The AISR register individually defines the I/O Port as analog input or as digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P57 pin

0: Disable ADC7, P57 functions as I/O pin

1: Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P55 pin

0: Disable ADC6, P55 functions as I/O pin

1: Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P70 pin

0: Disable ADC5, P70 functions as I/O pin

1: Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P67 pin

0: Disable ADC4, P67 functions as I/O pin

1: Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0: Disable ADC3, P53 functions as I/O pin

1: Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0: Disable ADC2, P52 functions as I/O pin

1: Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0: Disable ADC1, P51 functions as I/O pin

1: Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0: Disable ADC0, P50 functions as I/O pin

1: Enable ADC0 to function as analog input pin

NOTE

The P55/ADC6/OSCO/ERCin pin cannot be applied to OSCO and ADC6 at the same time. If P55/ADC6/OSCO/ERCin functions as OSCO oscillator input pin, then ADE6 bit for R8 must be "0" and ADIS2~0 do not select "110". The P55/ADC6/OSCO/ERCin pin priority is as follows

:

P55/ADC6/OSCO/ERCin Pin Priority		
High	Medium	Low
OSCO/ERCin	ADC6	P55

The P70/ADC5/OSCI/RCOUT pin cannot be applied to OSCI and ADC5 at the same time. If P70/ADC5/OSCI/RCOUT acts as OSCI oscillator input pin, then ADE5 bit for R8 must be "0" and ADIS2~0 do not select "101". The P70/ADC5/OSCI/RCOUT pin priority is as follows:

P70/ADC5/OSCI/RCOUT Pin Priority		
High	Medium	Low
OSCI/RCOUT	ADC5	P70

The P67/ADC4/PWM1 pin cannot be applied to PWM1 and ADC4 at the same time. If P67/ADC4/PWM1 functions as ADC4 analog input pin, then the P67/ADC4/PWM1 pin priority is as follows:

P67/ADC4/PWM1 Pin Priority		
High	Medium	Low
ADC4	PWM1	P67

The P51/ADC1/PWM2 pin cannot be applied to PWM2 and ADC1 at the same time. If P51/ADC1/PWM2 functions as ADC1 analog input pin, then the P51/ADC1/PWM2 pin priority is as follows:

P51/ADC1/PWM2 Pin Priority		
High	Medium	Low
ADC1	PWM2	P51

The P50/ADC0 pin cannot be applied to ADC0 at the same time. If P50/ADC0 functions as ADC0 analog input pin, then the P50/ADC0 pin priority is as follows:

P50/ADC0 Pin Priority	
High	Low
ADC0	P50

6.1.8 Bank 0 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of Vref of the ADC

0: The Vref of the ADC is connected to Vdd (default value), and the VREF/TCC/P54 pin carries out the function of P54 (default)

1: The Vref of the ADC is connected to VREF/TCC/P54

NOTE

- *The P54/TCC/VREF pin cannot be applied to TCC and VREF at the same time. If P54/TCC/VREF functions as VREF analog input pin, then CONT Bit 5 "TS" must be "0."*
- *The VREF/TCC/P54 Pin Priority is as follows:*

P54/TCC/VREF Pin Priority		
High	Medium	Low
VREF	TCC	P54

Bit 6 and Bit 5 (CKR1 and CKR0): ADC Clock Rate Select

00 = 1 **:** 16 (default value)

01 = 1 **:** 4

10 = 1 **:** 64

11 = 1 **:** 1

Bit 4 (ADRUN): ADC starts to RUN

0: on completion of the conversion Reset by hardware. This bit cannot be reset through software (default)

1: an A/D conversion is started. This bit can be set by software

Bit 3 (ADPD): ADC Power

0: ADC is in power down mode (default)

1: ADC is operating normally

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

ADICS	ADIS2	ADIS1	ADIS0	Analog Input Select
0	0	0	0	ADIN0/P50
0	0	0	1	ADIN1/P51
0	0	1	0	ADIN2/P52
0	0	1	1	ADIN3/P53
0	1	0	0	ADIN4/P67
0	1	0	1	ADIN5/P70
0	1	1	0	ADIN6/P55
0	1	1	1	ADIN7/P57
1	0	X	X	OPOUT
1	1	X	X	Internal 1/4 VDD

These bits can only be changed when the ADIF bit and the ADRUN bit are both low. See Section 6.1.13, *RE (Interrupt Status 2 and Wake-up Control Register)*.

6.1.9 Bank 0 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	VREF1	VREF0	ADICS

Bit 7 (CALI): Calibration enable bit for ADC offset

0: Disable Calibration (default)

1: Enable Calibration

Bit 6 (SIGN): Polarity bit of the offset voltage

0: Negative voltage (default)

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P372N
0	0	0	0LSB
0	0	1	2LSB
0	1	0	4LSB
0	1	1	6LSB
1	0	0	8LSB
1	0	1	10LSB
1	1	0	12LSB
1	1	1	14LSB