EM78P342N

8-Bit Microprocessor with OTP ROM

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

April 2013

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial released version	2006/12/01
1.1	1. Added EM78P340N 10-pin and EM78P3411N 16-pin package. 2. Modified the programmable Level Voltage Reset (LVR). 3. Modified the operating voltage range and frequency range. 4. Modified the IRC mode Wake-up time. 5. Modified some code option bits available. 6. Added Appendix D: How to use the ICE341N	2007/11/15
1.2	Renamed the Product as EM78P342N from EM78P341N, EM78P3411N, EM78P342N, EM78P343N	2008/01/24
1.3	Modified the TCCA, TCCB, and TCCC Timer formula.	2008/11/12
1.4	Added LVR specifications	2013/04/17

Item	EM78P342N
Level Voltage Reset	4.0V, 3.5V, 2.4V
Crystal mode Operating frequency range at 0°C~ 70°C	DC ~ 16 MHz, 4.5V DC ~ 8 MHz, 3.0V DC ~ 4 MHz, 2.1V
IRC mode wake-up time (Sleep → Normal) Condition: 5V, 4MHz	10 μs
Code Option	Added a Code Option NRM

1 General Description

The EM78P342N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has an on-chip 2K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Three Code option bits are also available to meet user's requirements.

With enhanced OTP-ROM features, the EM78P342N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 2K×13 bits on-chip ROM
  - 80×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Four programmable Level Voltage Detector (LVD) : 4.5V, 4.0V, 3.3V, 2.2V
  - Three programmable Level Voltage Reset (LVR) : 4.0V, 3.5V, 2.4V
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - Three bidirectional I/O ports: P5, P6, P7
  - 18 I/O pins
  - Wake-up port : P5
  - Four programmable high-sink current I/O pins
  - Eight programmable open-drain I/O pins
  - Eight programmable pull-down I/O pins
  - 16 programmable pull-high I/O pins
  - External interrupt : P60
- Operating voltage range:
  - 2.1V~5.5V at 0°C~70°C (commercial)
  - 2.3V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on 2 clocks):
  - Crystal mode: DC ~ 16 MHz, 4.5V;
    DC ~ 8 MHz, 3V; DC ~ 4 MHz, 2.1V
  - ERC mode: DC ~ 16 MHz, 4.5V;
    DC ~ 125ns inst. cycle, 4.5V
    DC ~ 8 MHz, 3V; DC ~ 250ns inst. cycle, 3V
  - I RC mode

  Oscillation mode: 16 MHz, 4 MHz, 1 MHz, 455kHz

Internal RC Frequency	Drift Rate			
	Temperature (-40℃ ~85℃)	Voltage (2.3V~5.5V)	Process	Total
4 MHz	±5%	±5%	±4%	±14%
16 MHz	±5%	±5%	±4%	±14%
1 MHz	±5%	±5%	±4%	±14%
455kHz	±5%	±5%	±4%	±14%

- All the four main frequencies can be trimmed by programming with four calibrated bits in the ICE341N Simulator. OTP is auto trimmed by ELAN Writer.
- Fast set-up time requires only 0.8ms (VDD: 5V Crystal: 4MHz, C1/C2: 30pF) in HXT2 mode and 10μs in IRC mode (VDD: 5V, IRC: 4MHz)
- Peripheral configuration
  - Easily implemented IR (infrared remote control)
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 8-bit real time clock/counter (TCCA, TCCC) and 16-bit real time clock/counter (TCCB) with selective signal sources, trigger edges, and overflow interrupt
  - 8-bit Multi-channel Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - One pair of Comparator or OP (Offset Voltage: smaller than 10mV)
- Seven available interrupts
  - TCC, TCCA, TCCB, TCCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - IR/PWM period match completion
  - Comparator status change interrupt
  - Low voltage detect (LVD) interrupt
- Special Features:
  - Programmable free running Watchdog Timer (4.5 ms : 18 ms)
  - Power saving Sleep mode
  - Selectable Oscillation mode
  - Power-on voltage detector available (1.7V ± 0.1V)
  - High EFT immunity (better performance at 4 MHz or below)
- Package Type:
  - 14-pin DIP 300mil : EM78P342ND14J/S
  - 14-pin SOP 150mil : EM78P342NSO14J/S
  - 16-pin SOP 150mil : EM78P342NSO16AJ/S
  - 18-pin DIP 300mil : EM78P342ND18J/S
  - 18-pin SOP 300mil : EM78P342NSO18J/S
  - 20-pin DIP 300mil : EM78P342ND20J/S
  - 20 pin SOP 300mil : EM78P342NSO20J/S
  - 20 pin SSOP 209mil : EM78P342NSS20J/S

NOTE: *These are all Green Products which do not contain hazardous substances.*

3 Pin Assignment

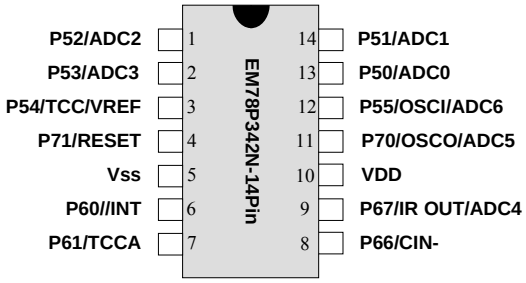


Figure 3-1 EM78P342ND14/SO14

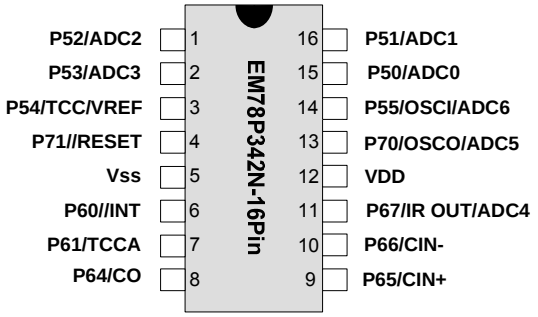


Figure 3-2 EM78P342NSO16A

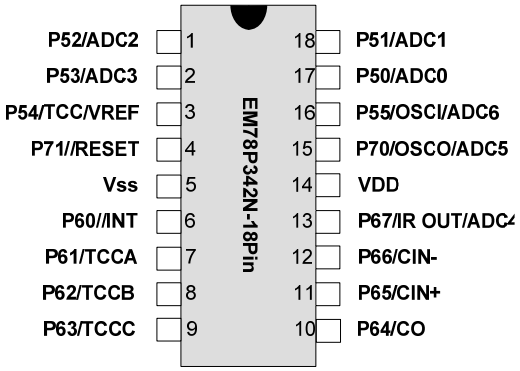


Figure 3-3 EM78P342ND18/SO18

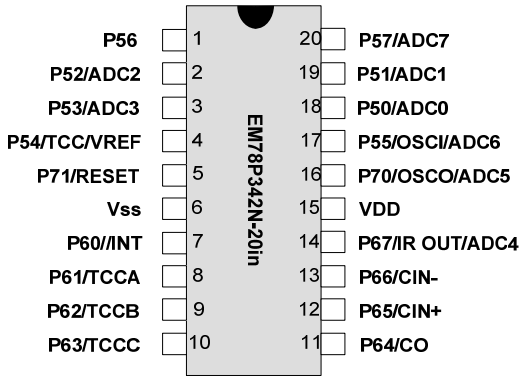


Figure 3-4 EM78P342ND20/SO20/SS20

4 Pin Description

4.1 EM78P342ND14/SO14

Symbol	Pin No.	Type	Function
P50~P55	1~3, 12~14	I/O	6-bit General purpose input/output pins Pull-high/Pull-down Function Wake up from sleep mode when the pin status changes Default value at power-on reset
P60, P61, P66, P67	6~9	I/O	4-bit General purpose input/output pins Pull-high/Open-drain Function Default value at power-on reset
P70~P71	11, 4	I/O	2-bit General purpose input/output pins Default value at power-on reset When P71 is used as output function, it is an open drain pin
/INT	6	I	External interrupt pin triggered by a falling or a rising edge. Defined by CONT <7>
ADC0~ADC6	1, 2, 9 11~14	I	7-bit channel Analog-to-Digital Converter with 12-bit resolution. Defined by ADCON (R9)<1:0>
VREF	3	I	External reference voltage for ADC Defined by ADCON (R9) <7>.
/RESET	4	I	If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
TCC, TCCA	3, 7	I	External Counter input TCC defined by CONT<5> TCCA defined by IOC80 <1>
OSCI	12	I	Crystal type: Crystal input terminal RC type: RC oscillator input pin
OSCO	11	O	Crystal type: Output terminal for crystal oscillator. RC type: Clock output with a duration of one instruction cycle time. External clock signal input.
VDD	10	–	Power supply
VSS	5	–	Ground

4.2 EM78P342NSO16A

Symbol	Pin No.	Type	Function
P50~P55	1~3, 14~16	I/O	6-bit General purpose input/output pins Pull-high/Pull-down Function Wake up from sleep mode when the pin status changes Default value at power-on reset
P60~P61, P64~P67	6~8, 9~11	I/O	6-bit General purpose input/output pins Pull-high/Open-drain Function Default value at power-on reset
P70~P71	13, 4	I/O	2-bit General purpose input/output pins Default value at power-on reset When P71 is used as output function, it is an open drain pin
/INT	6	I	External interrupt pin triggered by a falling or a rising edge. Defined by CONT <7>
ADC0~ADC6	1, 2, 11 13~16	I	7-bit channel Analog-to-Digital Converter with 12-bit resolution. Defined by ADCON (R9)<1:0>
VREF	3	I	External reference voltage for ADC Defined by ADCON (R9) <7>.
CIN- CIN+ CO	10 9 8	I I O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by IOC80 <4:3>
/RESET	4	I	If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
TCC, TCCA	3, 7	I	External Counter input TCC defined by CONT<5> TCCA defined by IOC80 <1>
OSCI	14	I	Crystal type: Crystal input terminal . RC type: RC oscillator input pin
OSCO	13	O	Crystal type: Output terminal for crystal oscillator. RC type: Clock output with a duration of one instruction cycle time. External clock signal input.
VDD	12	–	Power supply
VSS	5	–	Ground

4.3 EM78P342ND18/SO18

Symbol	Pin No.	Type	Function
P50~P55	1~3, 16~18	I/O	6-bit General purpose input/output pins Pull-high/Pull-down Function Wake up from sleep mode when the pin status changes Default value at power-on reset
P60~P67	6~13	I/O	8-bit General purpose input/output pins Pull-high/Open-drain Function Default value at power-on reset
P70~P71	15, 4	I/O	2-bit General purpose input/output pins Default value at power-on reset When P71 is used as output function, it is an open drain pin
/INT	6	I	External interrupt pin triggered by a falling or a rising edge. Defined by CONT <7>
ADC0~ADC6	1, 2, 13 15~18	I	7-bit channel Analog-to-Digital Converter with 12-bit resolution. Defined by ADCON (R9)<1:0>
VREF	3	I	External reference voltage for ADC Defined by ADCON (R9) <7>.
CIN- CIN+ CO	12 11 10	I I O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by IOC80 <4:3>
/RESET	4	I	If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
TCC, TCCA TCCB, TCCC	3, 7 8~9	I	External Counter input TCC defined by CONT<5> TCCA defined by IOC80 <1> TCCB defined by IOC90 <5> TCCC defined by IOC90 <1>
OSCI	16	I	Crystal type: Crystal input terminal . RC type: RC oscillator input pin
OSCO	15	O	Crystal type: Output terminal for crystal oscillator. RC type: Clock output with a duration of one instruction cycle time. External clock signal input.
VDD	14	–	Power supply
VSS	5	–	Ground

4.4 EM78P342ND20/SO20/SS20

Symbol	Pin No.	Type	Function
P50~P57	1~4, 17~20	I/O	8-bit General purpose input/output pins Pull-high/Pull-down Function Wake up from sleep mode when the pin status changes Default value at power-on reset
P60~P67	7~14	I/O	8-bit General purpose input/output pins Pull-high/Open-drain Function Default value at power-on reset
P70~P71	16, 5	I/O	2-bit General purpose input/output pins Default value at power-on reset When P71 is used as output function, it is an open drain pin
/INT	7	I	External interrupt pin triggered by a falling or a rising edge. Defined by CONT <7>
ADC0~ADC7	2, 3, 14 16~20	I	8-bit channel Analog-to-Digital Converter with 12-bit resolution. Defined by ADCON (R9) <2:0>
VREF	4	I	External reference voltage for ADC Defined by ADCON (R9) <7>.
CIN- CIN+ CO	13 12 11	I I O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by IOC80 <4:3>
/RESET	5	I	If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
TCC, TCCA TCCB, TCCC	4, 8 9~10	I	External Counter input TCC defined by CONT<5> TCCA defined by IOC80 <1> TCCB defined by IOC90 <5> TCCC defined by IOC90 <1>
OSCI	17	I	Crystal type: Crystal input terminal RC type: RC oscillator input pin
OSCO	16	O	Crystal type: Output terminal for crystal oscillator. RC type: Clock output with a duration of one instruction cycle time. External clock signal input.
VDD	15	–	Power supply
VSS	6	–	Ground

5 Block Diagram

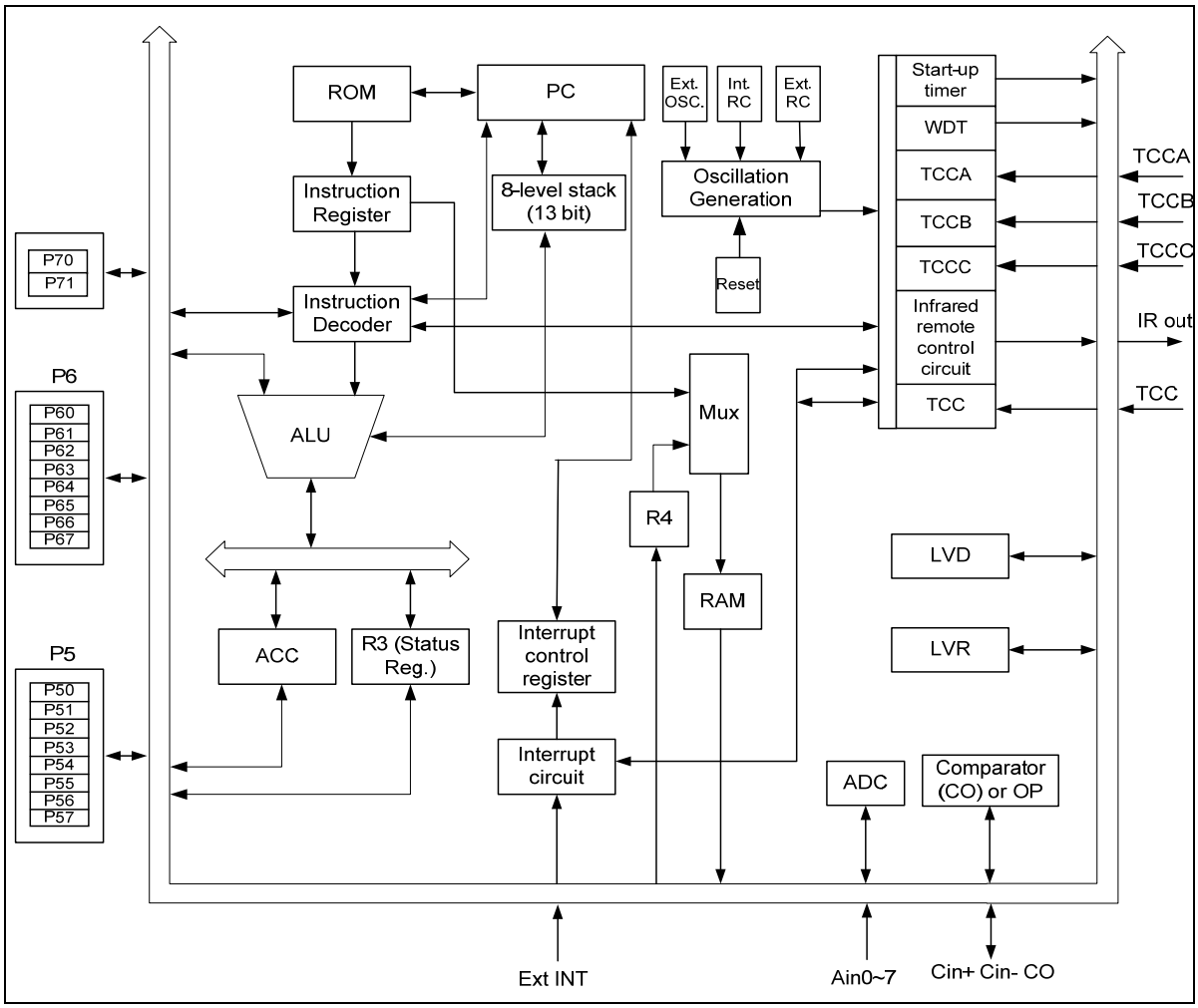


Figure 5 EM78P342N Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1 (Time Clock/Counter)

- Incremented by an external signal edge which is defined by the TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- The TCC prescaler counter (IOCC1) is assigned to TCC
- The contents of the IOCC1 register is cleared whenever –
  - a value is written to the TCC register.
  - a value is written to the TCC prescaler bits (Bits 3, 2, 1, 0 of the CONT register)
  - there is power-on reset, /RESET, or WDT time out reset.

6.1.3 R2 (Program Counter) and Stack

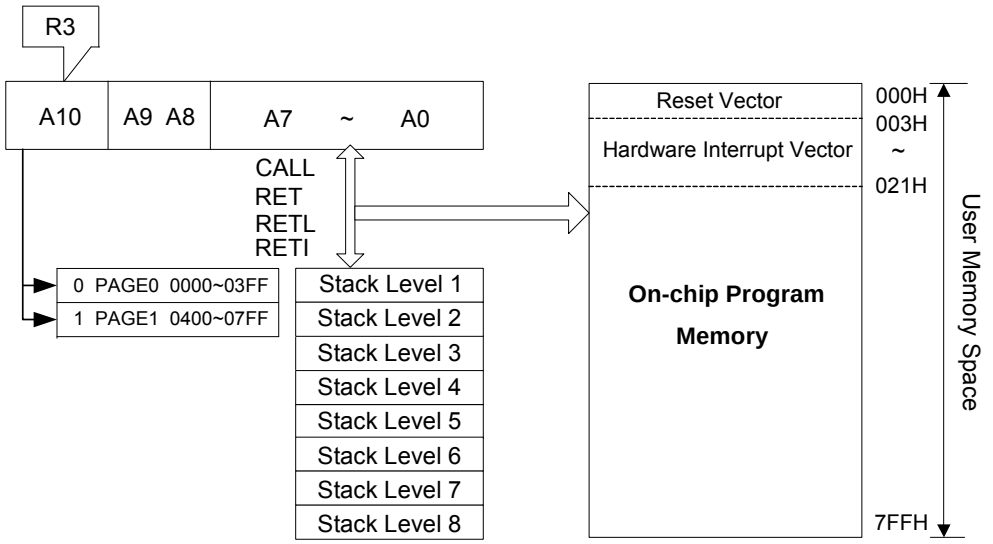


Figure 6-1 Program Counter Organization

- R2 and hardware stacks are 11-bit wide. The structure is depicted in the table under Section 6.1.3.1 *Data Memory Configuration*.
- The configuration structure generates 2K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "0"s when a reset condition occurs.

- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the program counter bits (A0~A10). Therefore, "LJMP" allows the PC to jump to any location within 2K (2^{11}).
- "LCALL" instruction loads the program counter bits (A0 ~A10), and PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 2K (2^{11})
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of the stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will be incremented progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except “ADD R2,A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2) except “LCALL” and “LJMP” instructions. The “LCALL” and “LJMP” instructions need two instruction cycles.

6.1.3.1 Data Memory Configuration

Address	R Page Registers	IOCX0 Page Registers	IOCX1 Page Registers
00	**R0** (Indirect Addressing Register)	Reserve	Reserve
01	**R1** (Timer Clock Counter)	Reserve	Reserve
02	**R2** (Program Counter)	Reserve	Reserve
03	**R3** (Status Register)	Reserve	Reserve
04	**R4** (RAM Select Register)	Reserve	Reserve
05	**R5** (Port 5)	**IOC50** (I/O Port Control Register)	**IOC51** (TCCA Counter)
06	**R6** (Port 6)	**IOC60** (I/O Port Control Register)	**IOC61** (TCCB LSB Counter)
07	**R7** (Port 7)	**IOC70** (I/O Port Control Register)	**IOC71** (TCCB HSB Counter)
08	**R8** (ADC Input Select Register	**IOC80** (Comparator and TCCA Control Register)	**IOC81** (TCCC Counter)
09	**R9** (ADC Control Register)	**IOC90** (TCCB and TCCC Control Register)	**IOC91** (Low-Time Register)
0A	**RA** (ADC Offset Calibration Register)	**IOCA0** (IR and TCCC Scale Control Register)	**IOCA1** (High-Time Register)
0B	**RB** (Converted value AD11~AD4 of ADC)	**IOCB0** (Pull-down Control Register)	**IOCB1** (High-Time and Low-Time Scale Control Register)
0C	**RC** (Converted value AD11~AD8 of ADC)	**IOCC0** (Open-drain Control Register)	**IOCC1** (TCC Prescaler Control)
0D	**RD** (Converted value AD7~AD0 of ADC)	**IOCD0** (Pull-high Control Register)	**IOCD1** (LVD Control Register)
0E	**RE** (Interrupt Status 2 and Wake-up Control Register	**IOCE0** (WDT Control Register and Interrupt Mask Register 2)	**IOCE1** (High Output Sink Current)
0F	**RF** (Interrupt Status Register 1)	**IOCF0** (Interrupt Mask Register 1)	**IOCF1** (Pull-high Control Register)
10 : 1F	General Registers		
20 : 3F	Bank 0	Bank 1	

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	IOCS	-	T	P	Z	DC	C

Bit 7 (RST): Bit of reset type

Set to “1” if wake-up from sleep on pin change, comparator status change, or AD conversion completed. Set to “0” if wake-up from other reset types.

Bit 6 (IOCS): Select the Segment of IO control register

0 = Segment 0 (IOC50 ~ IOCF0) selected

1 = Segment 1 (IOC51 ~ IOCC1) selected

Bit 5: **Not used (reserved)**

Bit 4 (T): Time-out bit. Set to “1” by the "SLEP" and "WDTC" commands or during power on**,** and reset to “0” by WDT time-out (for more details see Section 6.5.2, *The T and P Status under Status Register*).

Bit 3 (P): Power-down bit. Set to “1” during power-on or by a "WDTC" command and reset to “0” by a "SLEP" command (see Section 6.5.2, *The T and P Status under Status Register* for more details).

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7: Set to “0” all the time

Bit 6: Used to select Bank 0 or Bank 1 of the register

Bits 5~0: Used to select a register (Address: 00~0F, 10~3F) in indirect addressing mode.

See table under Section 6.1.3.1 *Data Memory Configuration*.

6.1.6 R5 ~ R6 (Port 5 ~ Port 6)

R5 and R6 are I/O registers.

6.1.7 R7 (Port 7)

Bit	7	6	5	4	3	2	1	0
EM78P342N	'0'	'0'	'0'	'0'	'0'	'0'	I/O	I/O
ICE341N	C3	C2	C1	C0	RCM1	RCM0	I/O	I/O

Note: *1. R7 is an I/O register.*

2. For the EM78P342N, only the lower two bits of R7 are available.

Bit 7 ~ Bit 2:

[With EM78P342N]: Unimplemented, read as '0'.

[With Simulator (C3~C0, RCM1, and **RCM0)]:** IRC calibration bits in IRC oscillator mode. In IRC oscillator mode of ICE341N simulator, these are the IRC mode selection bits and IRC calibration bits.

Bit 7 ~ Bit 4 (C3 ~ C0): Calibrator of internal RC mode

C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	(1-36%) × F
0	0	0	1	(1-31.5%) × F
0	0	1	0	(1-27%) × F
0	0	1	1	(1-22.5%) × F
0	1	0	0	(1-18%) × F
0	1	0	1	(1-13.5%) × F
0	1	1	0	(1-9%) × F
0	1	1	1	(1-4.5%) × F
1	1	1	1	F (default)
1	1	1	0	(1+4.5%) × F
1	1	0	1	(1+9%) × F
1	1	0	0	(1+135%) × F
1	0	1	1	(1+18%) × F
1	0	1	0	(1+22.5%) × F
1	0	0	1	(1+27%) × F
1	0	0	0	(1+31.5%) × F

Note: *1. Frequency values shown are theoretical and taken from an instance of a high frequency mode. Hence, they are shown for reference only. Definite values depend on the actual process.*

2. Similar way of calculation is also applicable for low frequency mode.

Bit 3 and Bit 2 (RCM1, RCM0): IRC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (default)
1	0	16
0	1	1
0	0	455kHz

6.1.8 R8 (AISR: ADC Input Select Register)

The AISR register individually defines the I/O Port as analog input or as digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P57 pin

0 = Disable ADC7, P57 functions as I/O pin

1 = Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P55 pin

0 = Disable ADC6, P55 functions as I/O pin

1 = Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P70 pin

0 = Disable ADC5, P70 functions as I/O pin

1 = Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P67 pin

0 = Disable ADC4, P67 functions as I/O pin

1 = Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0 = Disable ADC3, P53 functions as I/O pin

1 = Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0 = Disable ADC2, P52 functions as I/O pin

1 = Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0 = Disable ADC1, P51 functions as I/O pin

1 = Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0 = Disable ADC0, P50 functions as I/O pin

1 = Enable ADC0 to function as analog input pin

NOTE

The P55/OSCI/ADC6 pin cannot be applied to OSCI and ADC6 at the same time.

If P55/OSCI/ADC6 functions as OSCI oscillator input pin, then ADE6 bit for R8 must be "0" and ADIS2~0 do not select " 110". The P55/OSCI/ADC6 pin priority is as follows:

P55/OSCI/ADC6 Pin Priority		
High	Medium	Low
OSCI	ADC6	P55

The P70/OSCO/ADC5 pin cannot be applied to OSCO and ADC5 at the same time.

If P70/OSCO/ADC5 acts as OSCO oscillator input pin, then ADE5 bit for R8 must be "0" and ADIS2~0 do not select "101". The P70/OSCO/ADC5 pin priority is as follows:

P70/OSCO/ADC5 Pin Priority		
High	Medium	Low
OSCO	ADC5	P70

The P67/IR OUT/ADC4 pin cannot be applied to IR OUT and ADC4 at the same time.

If P67/IR OUT/ADC4 functions as ADC4 analog input pin, then IROUTE bit for IOCA0 must be "0"..

If P67/IR OUT/ADC4 functions as IR OUT analog input pin, then ADE4 bit for R8 must be "0" and ADIS2~0 do not select "100".

The P67/IR OUT/ADC4 pin priority is as follows:

P67/IR OUT/ADC4 Pin Priority		
High	Medium	Low
ADC4	IR OUT	P67

6.1.9 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of Vref of the ADC

0 : The Vref of the ADC is connected to Vdd (default value), and the VREF/TCC/P54 pin carries out the function of P54.

1 : The Vref of the ADC is connected to VREF/TCC/P54

NOTE

- *The P54/TCC/VREF pin cannot be applied to TCC and VREF at the same time. If P54/TCC/VREF functions as VREF analog input pin, then CONT Bit 5 "TS" must be "0."*
- *The VREF/TCC/P54 Pin Priority is as follows:*

P54/TCC/VREF Pin Priority		
High	**Medium**	**Low**
VREF	**TCC**	**P54**

Bit 6 and Bit 5 (CKR1 and CKR0): The prescaler of ADC oscillator clock rate

00 = 1 : 16 (default value)

01 = 1 : 4

10 = 1 : 64

11 = 1 : 8

CPUS	CKR1 : CKR0	Operation Mode	Max. Operation Frequency
1	00	Fosc/16	4 MHz
1	01	Fosc/4	1 MHz
1	10	Fosc/64	16 MHz
1	11	Fosc/8	2 MHz
0	××	Internal RC	–

Bit 4 (ADRUN): ADC starts to RUN.

0 : Reset upon completion of the conversion. This bit cannot be reset through software

1: an AD conversion is started. This bit can be set by software

Bit 3 (ADPD): ADC Power-down mode

0 : Switch off the resistor reference to save power even while the CPU is operating.

1 : ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ADIS0): Analog Input Select

000 = ADIN0/P50

001 = ADIN1/P51

010 = ADIN2/P52

011 = ADIN3/P53

100 = ADIN4/P67

101 = ADIN5/P70

110 = ADIN6/P55

111 = ADIN7/P57

These bits can only be changed when the ADIF bit and the ADRUN bit are both low. See Section 6.1.14, *RE (Interrupt Status 2 and Wake-up Control Register)*.

6.1.10 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	"0"	"0"	"0"

Bit 7 (CALI): Calibration enable bit for ADC offset

0 = disable Calibration

1 = enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0 = Negative voltage

1 = Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P342N	ICE341
0	0	0	0LSB	0LSB
0	0	1	2LSB	2LSB
0	1	0	4LSB	4LSB
0	1	1	6LSB	6LSB
1	0	0	8LSB	8LSB
1	0	1	10LSB	10LSB
1	1	0	12LSB	12LSB
1	1	1	14LSB	14LSB

Bit 2 ~ Bit 0: Unimplemented, read as '0'

6.1.11 RB (ADDATA: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When the AD conversion is completed, the result is loaded into the ADDATA. The ADRUN bit is cleared and the ADIF is set. See Section 6.1.14, *RE (Interrupt Status 2 and Wake-up Control Register)*.

RB is read only.

6.1.12 RC (ADDATA1H: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	AD11	AD10	AD9	AD8

When the AD conversion is completed, the result is loaded into the ADDATA1H. The ADRUN bit is cleared and the ADIF is set. See Section 6.1.14, *RE (Interrupt Status 2 and Wake-up Control Register*).

RC is read only.

6.1.13 RD (ADDATA1L: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

When the AD conversion is completed, the result is loaded into the ADDATA1L. The ADRUN bit is cleared and the ADIF is set. See Section 6.1.14, *RE (Interrupt Status 2 and Wake-up Control Register*).

RD is read only

6.1.14 RE (Interrupt Status 2 and Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/LVD	LVDIF	ADIF	CMPIF	ADWE	CMPWE	ICWE	LVDWE

Note: *1. RE <5, 4> can be cleared by instruction but cannot be set.*
2. IOCE0 is the interrupt mask register.
3. Reading RE will result to "logic AND" of the RE and IOCE0.

Bit 7 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0 : low voltage is detected

1 : low voltage is not detected or LVD function is disabled

Bit 6 (LVDIF): Low Voltage Detector Interrupt Flag

LVDIF is reset to "0" by software.

Bit 5 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.

0 : no interrupt occurs

1 : with interrupt request

Bit 4 (CMPIF): Comparator Interrupt Flag. Set when a change occurs in the Comparator output. Reset by software.

0 : no interrupt occurs

1 : with interrupt request

Bit 3 (ADWE): ADC wake-up enable bit

0 : Disable ADC wake-up

1 : Enable ADC wake-up

When AD Conversion enters sleep/idle mode, this bit must beset to "Enable".

Bit 2 (CMPWE): Comparator wake-up enable bit

0 : Disable Comparator wake-up

1 : Enable Comparator wake-up

When Comparator enters sleep/idle mode, this bit must be set to "Enable".

Bit 1 (ICWE): Port 5 input change to wake-up status enable bit

0 : Disable Port 5 input change to wake-up status

1 : Enable Port 5 input change to wake-up status

When Port 5 change enters sleep/idle mode, this bit must be set to "Enable".

Bit 0 (LVDWE): Low Voltage Detect wake-up enable bit

0 : Disable Low Voltage Detect wake-up

1 : Enable Low Voltage Detect wake-up

When the Low Voltage Detect is used to enter an interrupt vector or to wake-up the IC from sleep/idle with Low Voltage Detect running, the LVDWE bit must be set to "Enable".

6.1.15 RF (Interrupt Status 1 Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPWTIF	HPWTIF	TCCCIF	TCCBIF	TCCAIF	EXIF	ICIF	TCIF

Note: *1. "1" means there is interrupt request, "0"*
2. RF can be cleared by instruction but cannot be set.
3. IOCF0 is the interrupt mask register.
4. Reading RF will result to "logic AND" of the RF and IOCF0

Bit 7 (LPWTIF): Internal low-pulse width timer underflow interrupt flag for IR/PWM function. Reset by software.

Bit 6 (HPWTIF): Internal high-pulse width timer underflow interrupt flag for IR/PWM function. Reset by software.

Bit 5 (TCCCIF): TCCC overflow interrupt flag. Set when TCCC overflows. Reset by software.

Bit 4 (TCCBIF): TCCB overflow interrupt flag. Set when TCCB overflows. Reset by software.

Bit 3 (TCCAIF): TCCA overflow interrupt flag. Set when TCCA overflows. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by falling edge on /INT pin. Reset by software.

Bit 1 (ICIF): Port 5 input status change interrupt flag. Set when Port 5 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

6.1.16 R10 ~ R3F

All of these are 8-bit general-purpose registers.

6.2 Special Purpose Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Note: *The CONT register is both readable and writable.*
Bit 6 is read only.

Bit 7 (INTE): INT signal edge

0 : interrupt occurs at the rising edge of the INT pin

1 : interrupt occurs at the falling edge of the INT pin

Bit 6 (INT): Interrupt enable flag

0 : masked by DISI or hardware interrupt

1 : enabled by the ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC signal source

0 : internal instruction cycle clock. If P54 is used as I/O pin

1 : transition on the TCC pin

Bit 4 (TE): TCC signal edge

0 : increment if the transition from low to high takes place on the TCC pin

1 : increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

0 = prescaler disable bit. TCC rate is 1:1.

1 = prescaler enable bit. TCC rate is set as Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note: *Tcc time-out period [1/Fosc x prescaler x (256 – Tcc cnt) x 1*

6.2.3 IOC50 ~ IOC70 (I/O Port Control Register)

"**0**" defines the relative I/O pin as output

"**1**" sets the relative I/O pin into high impedance

- **Under 14 Pin :**

  IOC50<7, 6>, IOC60<5, 4, 3, 2 > : These bits must be set to “0” all the time,
  Other bits are readable and writable.

  IOC70 registers are all readable and writable.

- **Under 16 Pin :**

  IOC50<7, 6>, IOC60<3, 2 > : These bits must be set to “0” all the time.
  Other bits are readable and writable.

  IOC70 registers are all readable and writable.

- **Under 18 Pin :**

  IOC50<7, 6 > : These bits must be set to “0” all the time.
  Other bits are readable and writable.

  IOC60, IOC70 registers are all readable and writable.

- **Under 20 Pin :**

  IOC50, IOC60, IOC70 registers are all readable and writable.

6.2.4 IOC80 (Comparator and TCCA Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	CMPOUT	COS1	COS0	TCCAEN	TCCATS	TCCATE

Note: *Bits 4~0 of the IOC80 register are both readable and writable.*
Bit 5 of the IOC80 register is read only.

Bit 7 and Bit 6: Not used

Bit 5 (CMPOUT): Result of the comparator output. This bit is readable only.

Bit 4 and Bit 3 (COS1 and COS0): Comparator/OP Select bits

COS1	COS0	Functional Description
0	0	Comparator and OP are not used. P64, P65, and P66 are normal I/O pin
0	1	P65 and P66 are Comparator input pins and P64 is normal I/O pin
1	0	P65 and P66 are Comparator input pins and P64 is Comparator output pin (CO)
1	1	Used as OP and P64 is OP output pin (CO)

Bit 2 (TCCAEN): TCCA enable bit

0 = disable TCCA

1 = enable TCCA

Bit 1 (TCCATS): TCCA signal source

0 = internal clock (Fosc). P61 is a bidirectional I/O pin.

1 = transit through the TCCA pin

Bit 0 (TCCATE): TCCA signal edge

0 = increment if transition from low to high takes place on the TCCA pin

1 = increment if transition from high to low takes place on the TCCA pin

6.2.5 IOC90 (TCCB and TCCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCCBHE	TCCBEN	TCCBTS	TCCBTE	–	TCCCEN	TCCCTS	TCCCTE

Bit 7 (TCCBHE): Control bit is used to enable the most significant byte of the counter

0 : Disable the most significant byte of TCCBH (default value)
TCCB is an 8-bit counter.

1 : Enable the most significant byte of TCCBH
TCCB is a 16-bit counter.

Bit 6 (TCCBEN): TCCB enable bit

0 : disable TCCB

1 : enable TCCB

Bit 5 (TCCBTS) TCCB signal source

0 : internal clock (Fosc). P62 is a bi-directional I/O pin.

1 : transit through the TCCB/P62 pin

Bit 4 (TCCBTE): TCCB signal edge

0 : increment if the transition from low to high takes place on the TCCB pin

1 : increment if the transition from high to low takes place on the TCCB pin

Bit 3: Not used

Bit 2 (TCCCEN): TCCC enable bit

0 : disable TCCC

1 : enable TCCC

Bit 1 (TCCCTS) TCCC signal source

0 : internal clock (Fosc). P63 is a bidirectional I/O pin.

1 : transit through the TCCC/P63 pin

Bit 0 (TCCCTE): TCCC signal edge

0 : increment if the transition from low to high takes place on the TCCC pin

1 : increment if the transition from high to low takes place on the TCCC pin

6.2.6 IOCA0 (IR and TCCC Scale Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCCCSE	TCCCS2	TCCCS1	TCCCS0	IRE	HF	LGP	IROUTE

Bit 7 (TCCCSE): Scale enable bit for TCCC

An 8-bit counter is provided as scale for TCCC and IR-Mode. When in IR-Mode, TCCC counter scale uses the low-time segments of the pulse generated by Fcarrier frequency modulation (see Figure 6-11 in Section 6.8.2, *Functional Description*).

0 : scale disable bit, TCCC rate is 1:1

1 : scale enable bit, TCCC rate is set as Bit 6 ~ Bit 4

Bit 6 ~ Bit 4 (TCCCS2 ~ TCCCS0): TCCC scale bits

The TCCCS2 ~ TCCCS0 bits of the IOCA0 register are used to determine the scale ratio of TCCC as shown below:

TCCCS2	TCCCS1	TCCCS0	TCCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (IRE): Infrared Remote Enable bit

0 : Disable IRE, i.e., disable H/W Modulator Function. The IROUT pin is fixed at a high level and the TCCC is an Up Counter.

1 : Enable IRE, i.e., enable H/W Modulator Function. Pin 67 is defined as IROUT. If HF=1, the TCCC counter scale uses the low-time segments of the pulse generated by the Fcarrier frequency modulation (see Figure 6-11 in Section 6.8.2, *Functional Description*). When HF=0, the TCCC is an Up Counter

Bit 2 (HF): High Frequency bit

0 : PWM application. IROUT waveform is achieved base on the high-pulse width timer and low-pulse width timer which determine the high time width and low time width respectively.

1 : IR application mode. The low-time segments of the pulse generated by the Fcarrier frequency modulation (see Figure 6-11 in Section 6.8.2, *Functional Description*)

Bit 1 (LGP): Long Pulse

0 : The high-time and low-time registers are valid

1 : The high-time register is ignored. A single pulse is generated.

Bit 0 (IROUTE): Control bit used to define the P67 (IROUT) pin function

0 : P67 defined as bi-directional I/O pin

1 : P67 defined as IROUT. Under this condition, the I/O control bit of P67 (Bit 7 of IOC60) must be set to "0"

6.2.7 IOCB0 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50

The **IOCB0** register is both readable and writable.

Bit 7 (/PD57): Control bit used to enable internal pull-down of the P57 pin.

0: Enable internal pull-down

1 : Disable internal pull-down

Bit 6 (/PD56): Control bit used to enable internal pull-down of the P56 pin.

Bit 5 (/PD55): Control bit used to enable internal pull-down of the P55 pin.

Bit 4 (/PD54): Control bit used to enable internal pull-down of the P54 pin.

Bit 3 (/PD53): Control bit used to enable internal pull-down of the P53 pin.

Bit 2 (/PD52): Control bit used to enable internal pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable internal pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable internal pull-down of the P50 pin.

6.2.8 IOCC0 (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OD67	/OD66	/OD65	/OD64	/OD63	/OD62	/OD61	/OD60

The IOCC0 register is both readable and writable.

Bit 7 (/OD67): Control bit used to enable open-drain output of the P67 pin.

0 : Enable open-drain output

1 : Disable open-drain output

Bit 6 (/OD66): Control bit used to enable open-drain output of the P66 pin.

Bit 5 (/OD65): Control bit used to enable open-drain output of the P65 pin.

Bit 4 (/OD64): Control bit used to enable open-drain output of the P64 pin.

Bit 3 (/OD63): Control bit used to enable open-drain output of the P63 pin.

Bit 2 (/OD62): Control bit used to enable open-drain output of the P62 pin.

Bit 1 (/OD61): Control bit used to enable open-drain output of the P61 pin.

Bit 0 (/OD60): Control bit used to enable open-drain output of the P60 pin.

6.2.9 IOCD0 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

The **IOCD0** register is both readable and writable.

Bit 7 (/PH57): Control bit used to enable internal pull-high of the P57 pin.

0 = Enable internal pull-high

1 = Disable internal pull-high

Bit 6 (/PH56): Control bit used to enable internal pull-high of the P56 pin.

Bit 5 (/PH55): Control bit used to enable internal pull-high of the P55 pin.

Bit 4 (/PH54): Control bit used to enable internal pull-high of the P54 pin.

Bit 3 (/PH53): Control bit used to enable internal pull-high of the P53 pin.

Bit 2 (/PH52): Control bit used to enable internal pull-high of the P52 pin.

Bit 1 (/PH51): Control bit used to enable internal pull-high of the P51 pin.

Bit 0 (/PH50): Control bit used to enable internal pull-high of the P50 pin.

6.2.10 IOCE0 (WDT Control Register and Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable Watchdog Timer

0 : Disable WDT

1 : Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of the P60 (/INT) pin

0 : P60, bidirectional I/O pin

1 : /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC60) must be set to "1".

NOTE

- *When EIS is "0", the path of /INT is masked. When EIS is "1", the status of the /INT pin can also be read by way of reading Port 6 (R6). Refer to Figure 6-3 (I/O Port and I/O Control Register Circuit for P60 (/INT)) under Section 6.4 (I/O Ports).*
- *EIS is both readable and writable.*

Bit 5 (ADIE): ADIF interrupt enable bit

0 : disable ADIF interrupt

1 : enable ADIF interrupt

Bit 4 (CMPIE): CMPIF interrupt enable bit.

0 : disable CMPIF interrupt

1 : enable CMPIF interrupt

Bit 3 (PSWE): Prescaler enable bit for WDT

0 : prescaler disable bit, WDT rate is 1:1

1 : prescaler enable bit, WDT rate is set as Bit 2 ~ Bit 0

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.11 IOCF0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPWTIE	HPWTIE	TCCCIE	TCCBIE	TCCAIE	EXIE	ICIE	TCIE

Note: *The IOCF0 register is both readable and writable.*

Individual interrupt is enabled by setting to "1" its associated control bit in the IOCF0 and in IOCEO Bits 4 and 5.

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-7 Interrupt Input Circuit under Section 6 Interrupt.

Bit 7 (LPWTIE): LPWTIF interrupt enable bit

0 : Disable LPWTIF interrupt

1 : Enable LPWTIF interrupt

Bit 6 (HPWTIE): HPWTIF interrupt enable bit

0 : Disable HPWTIF interrupt

1 : Enable HPWTIF interrupt

Bit 5 (TCCCIE): TCCCIF interrupt enable bit

0 : Disable TCCCIF interrupt

1 : Enable TCCCIF interrupt

Bit 4 (TCCBIE): TCCBIF interrupt enable bit
0 : Disable TCCBIF interrupt
1 : Enable TCCBIF interrupt

Bit 3 (TCCAIE): TCCAIF interrupt enable bit
0 : Disable TCCAIF interrupt
1 : Enable TCCAIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit
0 : Disable EXIF interrupt
1 : Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit
0 : Disable ICIF interrupt
1 : Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit.
0 := Disable TCIF interrupt
1 : Enable TCIF interrupt

6.2.12 IOC51 (TCCA Counter)

The **IOC51 (TCCA)** is an 8-bit clock counter. It is also an Up Counter and it can be read, written to, and cleared on any reset condition.

$$TCCA\ Timeout\ \ period\ \ =\ \ \frac{1}{F_{OSC}}\ \times\ \left(256-TCCA\ \ cnt\right)\ \times\ 1$$

6.2.13 IOC61 (TCCB Counter)

The **IOC61 (TCCB)** is an 8-bit clock counter for the least significant byte of **TCCBX (TCCB)**. It is also an Up Counter, and it can be read, written to, and cleared on any reset condition.

6.2.14 IOC71 (TCCBH/MSB Counter)

The **IOC71 (TCCBH/MSB)** is an 8-bit clock counter for the most significant byte of **TCCBX (TCCBH)**. It can be read, written to, and cleared on any reset condition.

When TCCBHE (IOC90) is "**0**," then TCCBH is disabled. When TCCBHE is"**1**," then TCCB is a 16-bit counter.

When TCCBH is disabled:

$$TCCB\ Timeout\ \ period\ \ =\ \ \frac{1}{F_{OSC}}\ \times\ \left(256-TCCB\ \ cnt\right)\ \times\ 1$$

When TCCBH is enabled:

$$TCCB\ Timeout\ \ period\ \ =\frac{1}{F_{OSC}}\times\left[\ 65536\ -\ \left(TCCBH\ \times\ 256\ +\ TCCB\ cnt\right)\ \times\ 1\ \right]$$

6.2.15 IOC81 (TCCC Counter)

IOC81 (TCCC) is an 8-bit clock counter that can be extended to 16-bit counter. It can be read, written to and cleared on any reset condition.

If HF (Bit 2 of IOCA0) = 1 and IRE (Bit 3 of IOCA0) = 1, TCCC counter scale uses the low-time segments of the pulse generated by the Fcarrier frequency modulation (see Figure 6-11 in Section 6.8.2, *Function Description*). Then the TCCC value will be TCCC predicted value.

When HF = 0 or IRE = 0, the TCCC is an Up Counter.

In TCCC Up-counter mode:

$$TCCC\ \ Timeout\ \ period = \frac{1}{F_{OSC}} \times\ Scaler\ \ (IOCA0) \times\ \left(256 - TCCC\ \ cnt\right) \times\ 1$$

When HF = 1 and IRE = 1, TCCC counter scale uses the low-time segments of the pulse generated by the Fcarrier frequency modulation.

In IR mode:

$$F_{carrier} = \frac{FT}{2\left\{\left[\ 1 + Decimal\ \ TCCC\ \ Counter\ \ Value\ \ (IOC81)\ \right] \times\ TCCC\ \ Scale\ \ (IOCA0)\right\}}$$

$$\text{where}\quad FT = \frac{F_{OSC}}{1}$$

6.2.16 IOC91 (Low-Time Register)

The 8-bit Low-time register controls the active or Low segment of the pulse.

The decimal value of its contents determines the number of oscillator cycles and verifies that the IR OUT pin is active. The active period of IR OUT can be calculated as follows**:**

$$Low\ \ Time\ \ Width = \frac{\left\{\left[\ 1 + Decimal\ \ Low\ \ Time\ \ Value\ \ (IOC91)\right] \times Low\ \ Time\ \ Scale\ \ (IOCB1)\ \right\}}{FT}$$

$$\text{where}\quad FT = \frac{F_{OSC}}{1}$$

When an interrupt is generated by a Low time down counter underflow (when enabled), the next instruction will be fetched from Address 015H (Low time).

6.2.17 IOCA1 (High Time Register)

The 8-bit High-time register controls the inactive or High period of the pulse.

The decimal value of its contents determines the number of oscillator cycles and verifies that the IR OUT pin is inactive. The inactive period of IR OUT can be calculated as follows:

$$High\ Time\ Width = \frac{\left\{ \left[1 + Decimal\ \ High\ Time\ Value\ \ (IOCA1) \right] \times High\ Time\ \ Scale\ \ (IOCB1) \right\}}{FT}$$

$$\text{where} \quad FT = \frac{F_{OSC}}{1}$$

When an interrupt is generated by the High time down counter underflow (when enabled), the next instruction will be fetched from Address 012H (High time).

6.2.18 IOCB1 High/Low Time Scale Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HTSE	HTS2	HTS1	HTS0	LTSE	LTS2	LTS1	LTS0

Bit 7 (HTSE): High-time scale enable bit

0 : scale disable bit, High-time rate is 1:1

1 : scale enable bit, High-time rate is set at Bit 6~Bit 4.

Bit 6 ~ Bit 4 (HTS2 ~ HTS0): High-time scale bits:

HTS2	HTS1	HTS0	High-time Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (LTSE): Low-time scale enable bit.

0 : scale disable bit, Low-time rate is 1:1

1 : scale enable bit, Low-time rate is set at Bit 2~Bit 0.

Bit 2 ~ Bit 0 (LTS2 ~ LTS0): Low-time scale bits:

LTS2	LTS1	LTS0	Low-time Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.19 IOCC1 (TCC Prescaler Counter)

TCC prescaler counter can be read and written to:

PST2	PST1	PST0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TCC Rate
0	0	0	-	-	-	-	-	-	-	V	1:2
0	0	1	-	-	-	-	-	-	V	V	1:4
0	1	0	-	-	-	-	-	V	V	V	1:8
0	1	1	-	-	-	-	V	V	V	V	1:16
1	0	0	-	-	-	V	V	V	V	V	1:32
1	0	1	-	-	V	V	V	V	V	V	1:64
1	1	0	-	V	V	V	V	V	V	V	1:128
1	1	1	V	V	V	V	V	V	V	V	1:256

V = valid value

The TCC prescaler counter is assigned to TCC (R1).

The contents of the IOCC1 register are cleared when one of the following occurs:

- a value is written to the TCC register
- a value is written to the TCC prescaler bits (Bits 3, 2, 1, 0 of CONT)
- power-on reset, /RESET
- WDT time out reset

6.2.20 IOCD1 (LVD Control Register)

Bit	7	6	5	4	3	2	1	0
EM78P342N	–	–	–	–	LVDIE	LVDEN	LVD1	LVD0
ICE341N	TYPE1	TYPE0	LVR1	LVR0	LVDIE	LVDEN	LVD1	LVD0

Bits 7~6 (Type 1 ~ Type 0): Type selection for EM78P342N.

Type 1, Type 0	MCU Type
11	EM78P342N-20Pin (Default)
10	EM78P342N-18Pin or EM78P342N-16Pin
01	EM78P342N-14Pin
00	Not used

Bits 5~4 (LVR1 ~ LVR0): Low Voltage Reset enable bits.

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.4V	2.6V
01	3.5V	3.7V
00	4.0V	4.2V

Note: *The IOCD1 < 3 > register is both readable and writable.*
Individual interrupt is enabled by setting to "1" its associated control bit in the IOCD1 < 4 >.
Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.
Refer to *Figure* 6-8 *Interrupt Input Circuit* under Section 6.6 *Interrupt*.

Bit 3 (LVDIE): Low voltage Detector interrupt enable bit.

0 : Disable Low voltage Detector interrupt.

1 : Enable Low voltage Detector interrupt.

When the detect low level voltage is used to enter an interrupt vector or enter next instruction, the LVDIE bit must be set to "Enable".

Bit 2 (LVDEN): Low Voltage Detector enable bit

0 : Low voltage detector disable

1 : Low voltage detector enable

Bits 1~0 (LVD1:0): Low Voltage Detector level bits.

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	XX	NA	0

6.2.21 IOCE1 (Output Sink Select Control Register)

Bit	7	6	5	4	3	2	1	0
EM78P342N	-	TIMERSC	CPUS	IDLE	HS3	HS2	HS1	HS0
ICE341N	WDTPS	TIMERSC	CPUS	IDLE	HS3	HS2	HS1	HS0

Bit 7 (WDTPS): WDT time-out period selection bit.

0 : 4.5 ms

1 : 18 ms

Bit 6 (TIMERSC): TCC, TCCA, TCCB, TCCC clock sources select 0/1 → Fs/Fm*
Fs: sub frequency for WDT internal RC time base 15kHz ± 30%
Fm: main-oscillator clock

Bit 5 (CPUS): CPU Oscillator Source Select

0 : sub-oscillator (fs)

1 : main oscillator (fosc)

When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit. From SLEP instruction, this bit will determine as to which mode to go.

0 : Idle="0"+SLEP instruction → sleep mode

1 : Idle="1"+SLEP instruction → idle mode

CPU Operation Mode

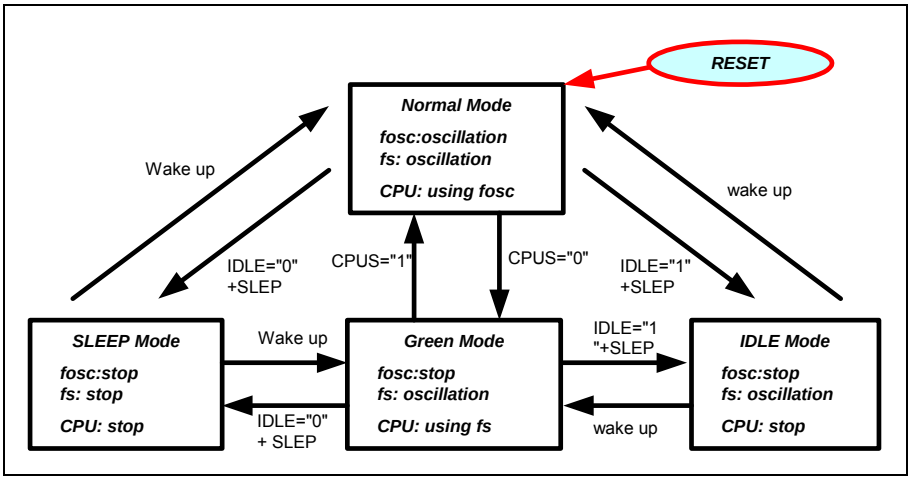


Figure 6-2 CPU Operation Mode

Bit 3 (HS3): Output Sink current Select for P63

Bit 2 (HS2): Output Sink current Select for P62.

Bit 1 (HS1): Output Sink current Select for P61.

Bit 0 (HS0): Output Sink current Select for P60.

HSx	VDD = 5V, Sink Current
0	20 mA (in 0.3VDD)
1	70 mA (in 0.3VDD)

6.2.22 IOCF1 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Note: *The IOCD0 register is both readable and writable.*

Bit 7 (/PH67): Control bit used to enable pull-high of the P67 pin.
0 = Enable internal pull-high
1 = Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable internal pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable internal pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable internal pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable internal pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable internal pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable internal pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable internal pull-high of the P60 pin.

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers that can be extended to 16-bit counter for the TCC and WDT respectively. The PST2 ~ PST0 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PSW2 ~ PSW0 bits of the IOCE0 register are used to determine the prescaler of WDT. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 depicts the block diagram of TCC/WDT.

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be internal clock (Fosc) or external signal input (edge selectable from the TCC pin). If TCC signal source is from an internal clock, the TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at High or Low level) must be greater than 1CLK. CLK=Fosc/2 or CLK=Fosc/4 is dependent on the Code Option bit <CLKS> = 0 or 1.

NOTE
The internal TCC will stop running when in sleep mode. However, during AD conversion, when TCC is set to "SLEP" instruction, if the ADWE bit of the RE register is enabled, the TCC will keep on running.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or in sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode through software programming. Refer to WDTE bit of IOCE0 register (Section 6.2.10 *IOCE0 (WDT Control and Interrupt Mask Registers 2)*. With no prescaler, the WDT time-out period is approximately 18ms[1] or 4.5ms[2].

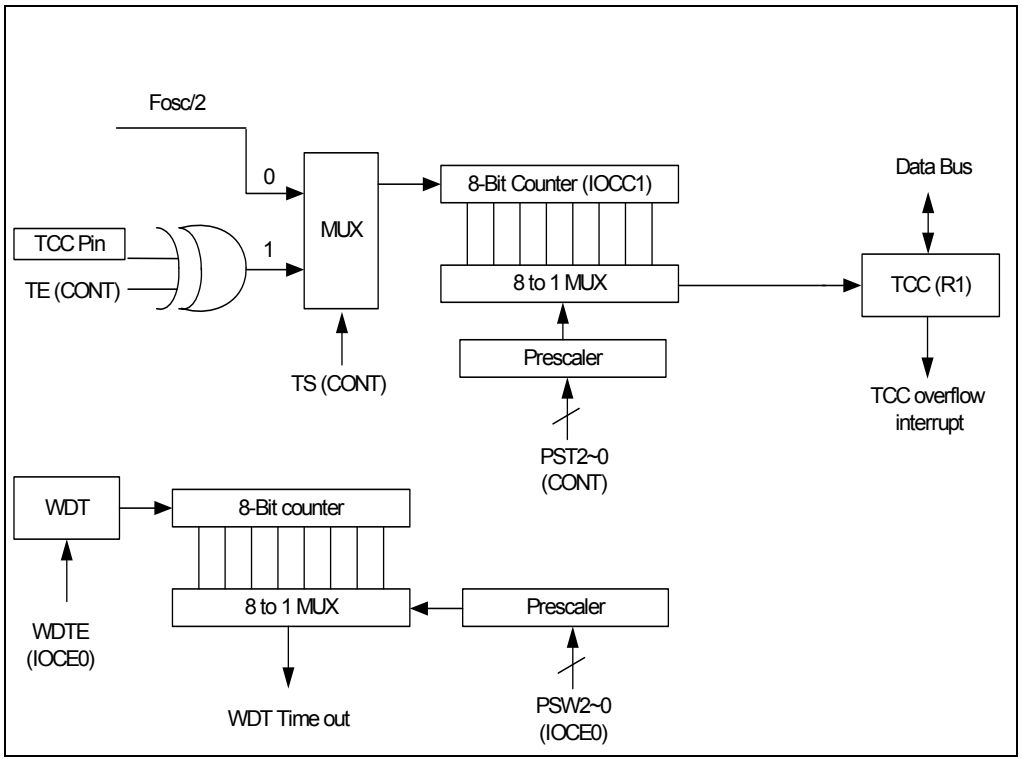


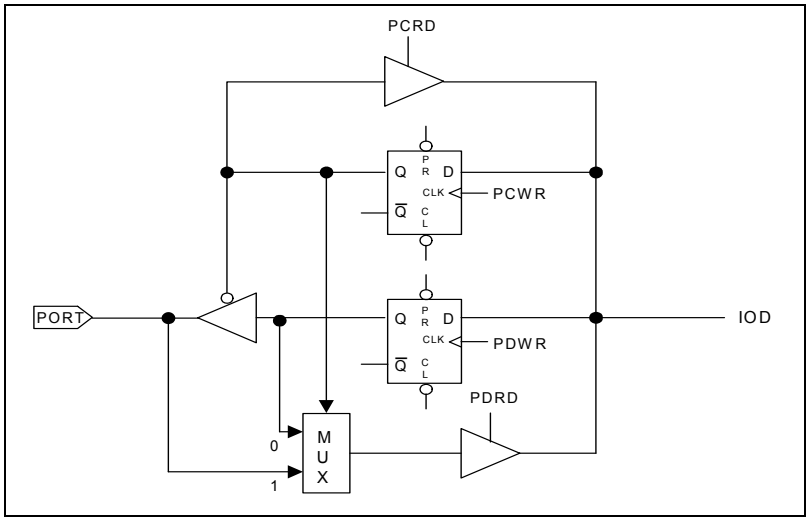
Figure 6-3 TCC and WDT Block Diagram

[1] *VDD=5V, WDT time-out period = 16.5ms ± 30%*
VDD=3V, WDT time-out period = 18ms ± 30%

[2] *VDD=5V, WDT time-out period = 4.2ms ± 30%*
VDD=3V, WDT time-out period = 4.5ms ± 30%

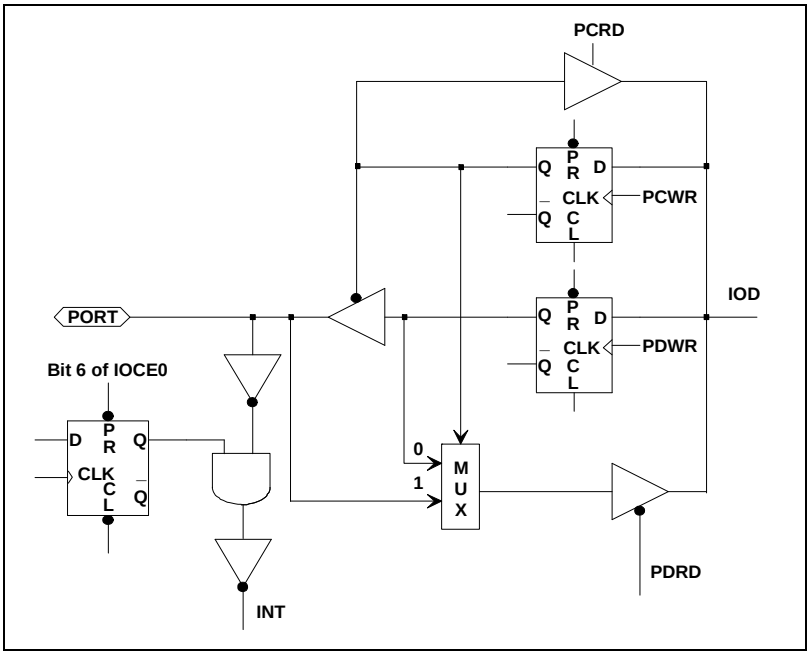
6.4 I/O Ports

The I/O registers (Port 5, Port 6, and Port 7) are bidirectional tri-state I/O ports. Port 5 is pulled-high and pulled-down internally by software. Likewise, P6 has its open-drain output set through software. Port 5 features an input status changed interrupt (or wake-up) function. Each I/O pin can be defined as an "input" or "output" pin by the I/O control register (IOC5 ~ IOC7). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, and Port 7 are illustrated in Figures 6-4, 6-5, 6-6, and 6-7.



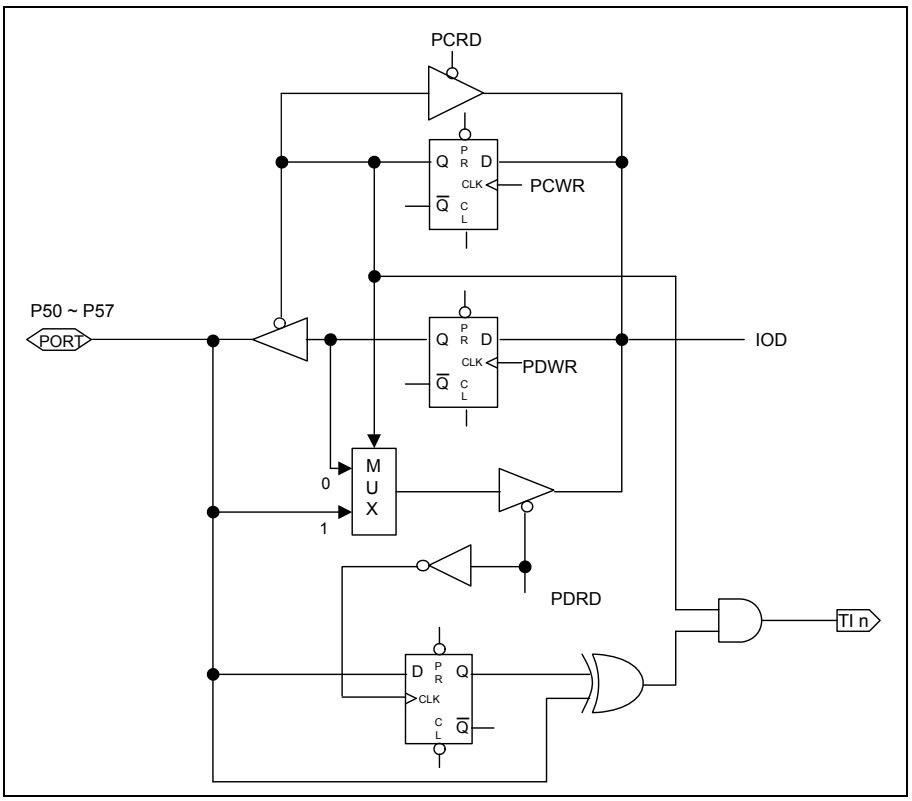
Note: *Pull-high and Open-drain are not shown in the figure.*

Figure 6-4 I/O Port and I/O Control Register Circuit for Port 6 and Port 7



Note: *Pull-high and Open-drain are not shown in the figure.*

Figure 6-5 I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-6 I/O Port and I/O Control Register Circuit for Ports 50~57

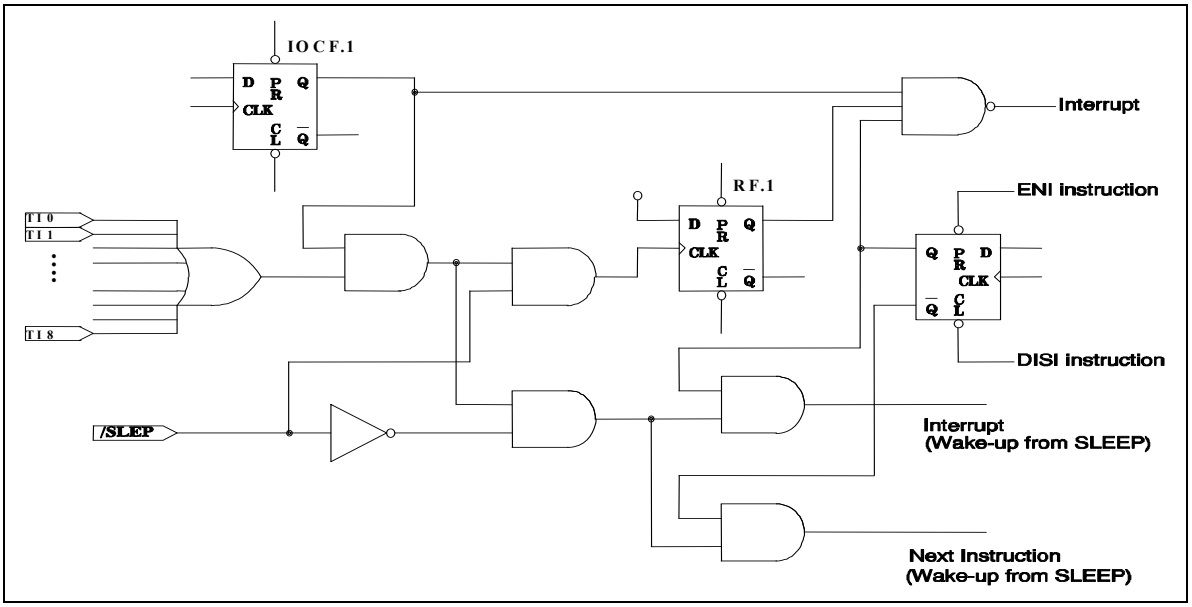


Figure 6-7 Port 5 Block Diagram with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 5 Input Change Wake-up/Interrupt Function

(1) Wake-up	(2) Wake-up and Interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port 5 (MOV R5,R5)	2. Read I/O Port 5 (MOV R5,R5)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set RE ICWE =1)	4. Enable wake-up bit (Set RE ICWE =1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set IOCF ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (008H)
	2. IF "DISI" → Next instruction
(3) Interrupt	
(a) Before Port 5 pin change	
1. Read I/O Port 5 (MOV R5,R5)	
2. Execute "ENI" or "DISI"	
3. Enable interrupt (Set IOCF ICIE =1)	
(b) After Port 5 pin changed (interrupt)	
1. IF "ENI" → Interrupt vector (006H)	
2. IF "DISI" → Next instruction	

6.5 Reset and Wake-up

6.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The device is kept in reset condition for a period of approximately 18ms[3] (except in LXT mode) after the reset is detected. When in LXT2 mode, the reset time is 500 ms. Two choices (18ms[3] or 4.5ms[4]) are available for WDT-time out period. Once a reset occurs, the following functions are performed (the initial Address is 000h):

- The oscillator continues running, or will be started (if in sleep mode).
- The Program Counter (R2) is set to all "0".

[3] *VDD=5V, Setup time period = 16.5ms ± 30%.*
VDD=3V, Setup time period = 18ms ± 30%.

[4] *VDD=5V, Setup time period = 4.2ms ± 30%.*
VDD=3V, Setup time period = 4.5ms ± 30%.

- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog Timer and prescaler are cleared
- When power is switched on, the upper three bits of R3 is cleared
- The IOCB0 register bits are set to all "1"
- The IOCC0 register bits are set to all "1"
- The IOCD0 register bits are set to all "1"
- Bits 7, 5, and 4 of the IOCE0 register are cleared
- Bits 5 and 4 of the RE register are cleared
- RF and IOCF0 registers are cleared

Executing the “SLEP” instruction will assert the sleep (power down) mode (When IDLE=”0”.). While entering into sleep mode, the Oscillator, TCC, TCCA, TCCB, and TCCC are stopped. The WDT (if enabled) is cleared but keeps on running.

During AD conversion, when “SLEP” instruction is set; the Oscillator, TCC, TCCA, TCCB, and TCCC keep on running. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

Case 1 External reset input on /RESET pin

Case 2 WDT time-out (if enabled)

Case 3 Port 5 input status changes (if ICWE is enabled)

Case 4 Comparator output status changes (if CMPWE is enabled)

Case 5 AD conversion completed (if ADWE is enabled)

Case 6 Low Voltage Detector (if LVDWE is enabled)

The first two cases (1 and 2) will cause the EM78P342N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, 5 and 6 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x06 (Case 3), 0×0F (Case 4), 0x0C (Case 5) and 0×21 (Case 6) after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP after wake-up.

Only one of Cases 2 to 6 can be enabled before entering into sleep mode. That is**:**

Case [a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78P342N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 6.6) for further details.

Case [b] If Port 5 Input Status Change is used to wake up the EM78P342N and the ICWE bit of the RE register is enabled before SLEP, and WDT must be disabled. Hence, the EM78P342N can be awakened only with Case 3. Wake-up time is dependent on the oscillator mode. In RC mode, Wake-up time is 10μs (for stable oscillators). In HXT2 (4 MHz) mode, Wake-up time is 800μs (for stable oscillators), and in LXT2 mode, Wake-up time is 2 ~ 3s.

Case [c] If the Comparator output status change is used to wake-up the EM78P342N and the CMPWE bit of the RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P342N can be awakened only with Case 4. Wake-up time is dependent on the oscillator mode. In RC mode, Wake-up time is 10μs (for stable oscillators). In HXT2 (4 MHz) mode, Wake-up time is 800μs (for stable oscillators), and in LXT2 mode, Wake-up time is 2s ~ 3s.

Case [d] If AD conversion completed is used to wake-up the EM78P342N and ADWE bit of RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P342N can be awakened only with Case 5. The wake-up time is 15 TAD (ADC clock period).

Case[e] If Low voltage detector is used to wake-up the EM78P342N and the LVDWE bit of Bank 0-RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P342N can be awakened only with Case 6. Wake-up time is dependent on oscillator mode.

If Port 5 Input Status Change Interrupt is used to wake up the EM78P342N (as in Case [b] above), the following instructions must be executed before SLEP:

```
BC              R3, 6              ; Select Segment 0
MOV             A, @00xx1110b      ; Select WDT prescaler and Disable WDT
IOW             IOCE0
WDTC                               ; Clear WDT and prescaler
MOV             R5, R5             ; Read Port 5
ENI (or DISI)                      ; Enable (or disable) global interrupt
MOV             A, @xxxxxx1xb      ; Enable Port 5 input change wake-up bit
MOV             RE
MOV             A, @xxxxxx1xb      ; Enable Port 5 input change interrupt
IOW             IOCF0
SLEP                               ; Sleep
```

Similarly, if the Comparator Interrupt is used to wake up the EM78P342N (as in Case [c] above), the following instructions must be executed before SLEP:

```
BC              R3, 6              ; Select Segment 0
MOV             A, @xxx10XXXb      ; Select a comparator and P64 functions as
                                   ; CO pin
IOW             IOC80
MOV             A, @00x11110b      ; Select WDT prescaler and Disable WDT,
                                   ; and enable comparator output status
                                   ; change interrupt
IOW             IOCE0
WDTC                               ; Clear WDT and prescaler
ENI (or DISI)                      ; Enable (or disable) global interrupt
MOV             A, @xxx0x1xxb      ; Enable comparator output status change
                                   ; wake-up bit
MOV             RE
SLEP                               ; Sleep
```

6.5.1.1 Wake-up and Interrupt Modes Operation Summary

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows.

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Port 5 pin change	If enable ICWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	If enable ICWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TCC overflow interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
AD conversion complete interrupt	If enable ADWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction **Fs and Fm don't stop**	If enable ADWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction **Fs and Fm don't stop**	× **Fs and Fm don't stop**	Interrupt (if interrupt is enabled) or next instruction
Comparator interrupt	If enable CMPWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	If enable CMPWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
High-pulse width timer underflow interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Low-pulse width timer underflow interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TCCA overflow interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TCCB overflow interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TCCC overflow interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Low Voltage Detector interrupt	If Enable LVDWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	If Enable LVDWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
WDT Time out			RESET	RESET
Low Voltage Reset			RESET	RESET

After wake up:

1. If interrupt is enabled → interrupt+ next instruction

2. If interrupt is disabled → next instruction

Signal	Sleep Mode	Idle Mode*	Normal Mode	Green Mode
INT Pin	NA	DISI+IOCF0(EXIE) Bit 2 =1	DISI + IOCF0 (EXIE) Bit 2=1	DISI + IOCF0 (EXIE) Bit 2=1
		Wake-up + next instruction Set RF (EXIF)=1	Next Instruction + Set RF (EXIF)=1	Next Instruction + Set RF (EXIF)=1
		ENI + IOCF0(EXIE) Bit 2 =1	ENI + IOCF0 (EXIE) Bit 2=1	ENI + IOCF0 (EXIE) Bit 2=1
		Wake-up + Interrupt Vector (003H) + Set RF (EXIF)=1	Interrupt Vector (003H) + Set RF (EXIF)=1	Interrupt Vector (003H) + Set RF (EXIF)=1
Port 5 Input Status Change	RE (ICWE) Bit 1=0, IOCF0 (ICIE) bit 1=0	RE (ICWE) Bit 1=0, IOCF0 (ICIE) Bit 1=0	IOCF0 (ICIE) Bit 1=0	IOCF0 (ICIE) Bit 1=0
	Oscillator, TCC, TCCX and IR/PWM are stopped. Port 5 input status changed wake-up is invalid.	TCC, TCCX and IR/PWM keep on running. Port 5 input status changed wake-up is invalid.	Port 5 input status change interrupted is invalid	Port 5 input status change interrupted is invalid
	RE (ICWE) Bit 1=0, IOCF0 (ICIE) Bit 1=1	RE (ICWE) Bit 1=0, IOCF0 (ICIE) Bit 1=1	N/A	N/A
	Set RF (ICIF)=1, Oscillator, TCC, TCCX and IR/PWM are stopped. Port 5 input status changed wake-up is invalid.	Set RF (ICIF)=1, TCC, TCCX and IR/PWM keep on running. Port 5 input status changed wake-up is invalid.	N/A	N/A
	RE (ICWE) Bit 1=1, IOCF0 (ICIE) Bit 1=0	RE (ICWE) Bit 1=1, IOCF0 (ICIE) Bit1=0	N/A	N/A
	Wake-up + Next Instruction Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Next Instruction TCC, TCCX and IR/PWM keep on running.	N/A	N/A
	RE (ICWE) Bit1=1, DISI + IOCF0 (ICIE) Bit 1=1	RE (ICWE) Bit 1=1, DISI + IOCF0 (ICE) Bit 1=1	DISI + IOCF0 (ICIE) Bit 1=1	DISI + IOCF0 (ICIE) Bit 1=1
	Wake-up + Next Instruction + Set RF (ICIF)=1 Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Next Instruction + Set RF (ICIF)=1 TCC, TCCX and IR/PWM keep on running.	Next Instruction + Set RF (ICIF)=1	Next Instruction + Set RF (ICIF)=1
	RE (ICWE) Bit 1=1, ENI + IOCF0 (ICIE) Bit 1=1	RE (ICWE) Bit 1=1, ENI + IOCF0 (ICIE) Bit 1=1	ENI + IOCF0 (ICIE) Bit 1=1	ENI + IOCF0 (ICIE) Bit 1=1
	Wake-up + Interrupt Vector (006H) + Set RF (ICIF)=1 Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Interrupt Vector (006H) + Set RF (ICIF)=1 TCC, TCCX and IR/PWM keep on running.	Interrupt Vector(006H) + Set RF (ICIF)=1	Interrupt Vector(006H) + Set RF (ICIF)=1
TCC Overflow	NA	DISI+IOCF0(TCIE) Bit 0 =1	DISI + IOCF0 (TCIE) Bit 0=1	DISI + IOCF0 (TCIE) Bit 0=1
		Wake-up + next instruction Set RF (TCIF)=1	Next Instruction + Set RF (TCIF)=1	Next Instruction + Set RF (TCIF)=1
		ENI + IOCF0(TCIE) Bit 0 =1	ENI + IOCF0 (TCIE) Bit 0=1	ENI + IOCF0 (TCIE) Bit 0=1
		Wake-up + Interrupt Vector (009H) + Set RF (TCIF)=1	Interrupt Vector (009H) + Set RF (TCIF)=1	Interrupt Vector (009H) + Set RF (TCIF)=1

Signal	Sleep Mode	Idle Mode*	Normal Mode	Green Mode
AD Conversion	RE (ADWE) Bit 3=0, IOCE0 (ADIE) Bit 5=0	RE (ADWE) Bit 3=0, IOCE0 (ADIE) Bit 5=0	IOCE0 (ADIE) Bit 5=0	IOCE0 (ADIE) Bit 5=0
	Clear R9 (ADRUN)=0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC, TCCX and IR/PWM are stopped.	Clear R9 (ADRUN)=0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC, TCCX and IR/PWM keep on running.	AD conversion interrupted is invalid	AD conversion interrupted is invalid
	RE (ADWE) Bit 3=0, IOCE0 (ADIE) Bit 5=1	RE (ADWE) Bit 3=0, IOCE0 (ADIE) Bit 5=1	N/A	N/A
	Set RF (ADIF)=1, R9 (ADRUN)=0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC, TCCX and IR/PWM are stopped.	Set RF (ADIF)=1, R9 (ADRUN)=0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC, TCCX and IR/PWM keep on running.	N/A	N/A
	RE (ADWE) Bit 3=1, IOCE0 (ADIE) Bit 5=0	RE (ADWE) Bit 3=1, IOCE0 (ADIE) Bit 5=0	N/A	N/A
	Wake-up + Next Instruction, Oscillator, TCC, TCCX and IR/PWM keep on running. Wake-up when ADC completed.	Wake-up + Next Instruction, Oscillator, TCC, TCCX and IR/PWM keep on running. Wake-up when ADC completed.	N/A	N/A
	RE (ADWE) Bit 3=1, DISI + IOCE0 (ADIE) Bit 5=1	RE (ADWE) Bit 3=1, DISI + IOCE0 (ADIE) Bit 5=1	DISI + IOCE0 (ADIE) Bit 5=1	DISI + IOCE0 (ADIE) Bit 5=1
	Wake-up + Next Instruction + RE (ADIF)=1, Oscillator, TCC, TCCX and IR/PWM keep on running. Wake-up when ADC completed.	Wake-up + Next Instruction + RE (ADIF)=1, Oscillator, TCC, TCCX and IR/PWM keep on running. Wake-up when ADC completed.	Next Instruction + RE (ADIF)=1	Next Instruction + RE (ADIF)=1
	RE (ADWE) Bit 3=1, ENI + IOCE0 (ADIE) Bit 5=1	RE (ADWE) Bit 3=1, ENI + IOCE0 (ADIE) Bit 5=	ENI + IOCE0 (ADI) Bit 5=1	ENI + IOCE0 (ADIE) Bit 5=1
	Wake-up + Interrupt Vector (00CH)+ RE (ADIF)=1, Oscillator, TCC, TCCX and IR/PWM keep on running. Wake-up when ADC completed.	Wake-up + Interrupt Vector (00CH)+ RE (ADIF)=1, Oscillator, TCC, TCCX and IR/PWM keep on running. Wake-up when ADC completed.	Interrupt Vector (00CH) + Set RE (ADIF)=1	Interrupt Vector (00CH) + Set RE (ADIF)=1

Signal	Sleep Mode	Idle Mode*	Normal Mode	Green Mode
Comparator (Comparator Output Status Change)	RE (CMPWE) Bit 2=0, IOCE0 (CMPIE) Bit 4=0	RE (CMPWE) Bit 2=0, IOCE0 (CMPIE) Bit 4=0	IOCE0 (CMPIE) Bit 4=0	IOCE0 (CMPIE) Bit 4=0
	Comparator output status changed wake-up is invalid. Oscillator, TCC, TCCX and IR/PWM are stopped.	Comparator output status changed wake-up is invalid. TCC, TCCX and IR/PWM keep on running.	Comparator output status change interrupt is invalid.	Comparator output status change interrupt is invalid.
	RE (CMPWE) Bit 2=0, IOCE0 (CMPIE) Bit 4=1	RE (CMPWE) Bit 2=0, IOCE0 (CMPIE) Bit 4=1	N/A	N/A
	Set RE (CMPIF)=1, Comparator output status changed wake-up is invalid. Oscillator, TCC, TCCX and IR/PWM are stopped.	Set RE (CMPIF)=1, Comparator output status changed wake-up is invalid. TCC, TCCX and IR/PWM keep on running.	N/A	N/A
	RE (CMPWE) Bit 2=1, IOCE0 (CMPIE) Bit 4=0	RE (CMPWE) Bit 2=1, IOCE0 (CMPIE) Bit 4=0	N/A	N/A
	Wake-up + Next Instruction, Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Next Instruction, TCC, TCCX and IR/PWM keep on running.	N/A	N/A
	RE (CMPWE) Bit 2=1, DISI + IOCE0 (CMPIE) Bit 4=1	RE (CMPWE) Bit 2=1, DISI + IOCE0 (CMPIE) Bit 4=1	DISI + IOCE0 (CMPIE) Bit 4=1	DISI + IOCE0 (CMPIE) Bit 4=1
	Wake-up + Next Instruction + Set RE (CMPIF)=1, Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Next Instruction + Set RE (CMPIF)1, TCC, TCCX and IR/PWM keep on running.	Next Instruction + Set RE (CMPIF)=1	Next Instruction + Set RE (CMPIF)=1
	RE (CMPWE) Bit 2=1, ENI + IOCE0 (CMPIE) Bit 4=1	RE (CMPWE) Bit 2=1, ENI + IOCE0 (CMPIE) Bit 4=1	ENI + IOCE0 (CMPIE) Bit 4=1	ENI + IOCE0 (CMPIE) Bit 4=1
	Wake-up + Interrupt Vector (00FH) + Set RE (CMPIF)=1,Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Interrupt Vector (00FH) + Set RE (CMPIF)=1 TCC, TCCX and IR/PWM keep on running.	Interrupt Vector (00FH) + Set RE (CMPIF)=1	Interrupt Vector (00FH) + Set RE (CMPIF)=1
IR/PWM underflow interrupt (High-pulse width timer underflow interrupt)	N/A	DISI + IOCF0 (HPWTIE) Bit 6=1	DISI + IOCF0 (HPWTIE) Bit 6=1	DISI + IOCF0 (HPWTIE) Bit 6=1
		Wake-up +Next Instruction + Set RF (HPWTIF)=1	Next Instruction + Set RF (HPWTIF)=1	Next Instruction + Set RF (HPWTIF)=1
		ENI + IOCF0 (HPWTIE) Bit 6 =1	ENI + IOCF0 (HPWTIE) Bit 6 =1	ENI + IOCF0 (HPWTIE) Bit 6 =1
		Wake-up + Interrupt Vector (012H) + Set RF (HPWTIF)=1	Interrupt Vector (012H) + Set RF (HPWTIF)=1	Interrupt Vector (012H) + Set RF (HPWTIF)=1

Signal	Sleep Mode	Idle Mode*	Normal Mode	Green Mode
IR/PWM underflow interrupt (Low-pulse width timer underflow interrupt)	N/A	DISI + IOCF0 (LPWTIE) Bit 7=1	DISI + IOCF0 (LPWTIE) Bit 7=1	DISI + IOCF0 (LPWTIE) Bit 7=1
		Wake-up +Next Instruction + Set RF (LPWTIF)=1	Next Instruction + Set RF (LPWTIF)=1	Next Instruction + Set RF (LPWTIF)=1
		ENI + IOCF0 (LPWTIE) Bit 7 =1	ENI + IOCF0 (LPWTIE) Bit 7 =1	ENI + IOCF0 (LPWTIE) Bit 7 =1
		Wake-up +Interrupt Vector (015H) + Set RF (LPWTIF)=1	Interrupt Vector (015H) + Set RF (LPWTIF)=1	Interrupt Vector (015H) + Set RF (LPWTIF)=1
TCCA Over Flow	N/A	DISI + IOCF0 (TCCAIE) Bit 3=1	DISI + IOCF0 (TCCAIE) Bit 3=1	DISI + IOCF0 (TCCAIE) Bit 3=1
		Wake-up +Next Instruction + Set RF (TCCAIF)=1	Next Instruction + Set RF (TCCAIF)=1	Next Instruction + Set RF (TCCAIF)=1
		ENI + IOCF0 (TCCAIE) Bit 3=1	ENI + IOCF0 (TCCAIE) Bit 3=1	ENI + IOCF0 (TCCAIE) Bit 3=1
		Wake-up +Interrupt Vector (018H) + Set RF (TCCAIF)=1	Interrupt Vector (018H) + Set RF (TCCAIF)=1	Interrupt Vector (018H) + Set RF (TCCAIF)=1
TCCB Over Flow	N/A	DISI + IOCF0 (TCCBIE) Bit 4=1	DISI + IOCF0 (TCCBIE) Bit 4=1	DISI + IOCF0 (TCCBIE) Bit 4=1
		Wake-up +Next Instruction + Set RF (TCCBIF)=1	Next Instruction + Set RF (TCCBIF)=1	Next Instruction + Set RF (TCCBIF)=1
		ENI + IOCF0 (TCCBIE) Bit 4=1	ENI + IOCF0 (TCCBIE) Bit 4=1	ENI + IOCF0 (TCCBIE) Bit 4=1
		Wake-up +Interrupt Vector (01BH) + Set RF(TCCBIF)=1	Interrupt Vector (01BH) + Set RF (TCCBIF)=1	Interrupt Vector (01BH) + Set RF (TCCBIF)=1
TCCC Over Flow	N/A	DISI + IOCF0 (TCCCIE) Bit 5=1	DISI + IOCF0 (TCCCIE) Bit 5=1	DISI + IOCF0 (TCCCIE) Bit 5=1
		Wake-up +Next Instruction + Set RF (TCCCIF)=1	Next Instruction + Set RF (TCCCIF)=1	Next Instruction + Set RF (TCCCIF)=1
		ENI + IOCF0 (TCCCIE) Bit 5=1	ENI + IOCF0 (TCCCIE) Bit 5=1	ENI + IOCF0 (TCCCIE) Bit 5=1
		Wake-up +Interrupt Vector (01EH) + Set RF (TCCCIF)=1	Interrupt Vector (01EH) + Set RF (TCCCIF)=1	Interrupt Vector (01EH) + Set RF (TCCCIF)=1

Signal	Sleep Mode	Idle Mode*	Normal Mode	Green Mode
Low Voltage Detector interrupt	RE (LVDWE) Bit 0=0, IOCD1 (LVDIE) Bit 3=0	RE (LVDWE) Bit 0=0, IOCD1 (LVDIE) Bit 3=0	IOCD1 (LVDIE) Bit 3=0	IOCD1 (LVDIE) Bit 3=0
	Low voltage detector wake-up is invalid. Oscillator, TCC, TCCX and IR/PWM are stopped.	Low voltage detector wake-up is invalid. TCC, TCCX and IR/PWM keep on running.	Low voltage detector interrupted is invalid.	Low voltage detector interrupted is invalid.
	RE (LVDWE) Bit 0=0, IOCD1 (LVDIE) Bit 3=1	RE (LVDWE) Bit 0=0, IOCD1 (LVDIE) Bit 3=1	N/A	N/A
	Set RE (LVDIF)=1, Low voltage detector wake-up is invalid. Oscillator, TCC, TCCX and IR/PWM are stopped.	Set RE (LVDIF)=1, Low voltage detector wake-up is invalid. TCC, TCCX and IR/PWM keep on running.	N/A	N/A
	RE (LVDWE) Bit 0=1, IOCD1 (LVDIE) Bit 3=0	RE (LVDWE) Bit 0=1, IOCD1 (LVDIE) Bit 3=0	N/A	N/A
	Wake-up + Next Instruction, Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Next Instruction, TCC, TCCX and IR/PWM keep on running.	N/A	N/A
	RE (LVDWE) Bit =1, DISI + IOCD1 (LVDIE) Bit 3=1	RE (LVDWE) Bit 0=1, DISI + IOCD1 (LVDIE) Bit 3 =1	DISI + IOCD1 (LVDIE) Bit 3=1	DISI + IOCD1 (LVDIE) Bit 3=1
	Wake-up + Next Instruction + Set RE (LVDIF)=1, Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Next Instruction + Set RE (LVDIF) =1, TCC, TCCX and IR/PWM keep on running.	Next Instruction + Set RE (LVDIF)=1	Next Instruction + Set RE (LVDIF) =1
	RE (LVDWE) Bit 2=1, ENI + IOCD1 (LVDIE) Bit 3=1	RE (LVDWE) Bit0=1, ENI + IOCD1 (LVDIE) Bit 3 =1	ENI + IOCD1 (LVDIE) Bit 3=1	ENI + IOCD1 (LVDIE) Bit 3=1
	Wake-up + Interrupt Vector (021H) + Set RE (LVDIF)=1,Oscillator, TCC, TCCX and IR/PWM are stopped.	Wake-up + Interrupt Vector (021H) + Set RE (LVDIF) =1, TCC, TCCX and IR/PWM keep on running.	Interrupt Vector (021H) + Set RE (LVDIF)=1	Interrupt Vector (021H) + Set RE (LVDIF) =1
WDT Timeout IOCE (WDTE) Bit 7=1	Wake-up + Reset (Address 0x00)	Wake-up + Reset (Address 0x00)	Reset (Address 0x00)	Reset (Address 0x00)
Low voltage reset	Wake-up + Reset (Address 0x00)	Wake-up + Reset (Address 0x00)	Reset (Address 0x00)	Reset (Address 0x00)

6.5.1.2 Register Initial Values after Reset

The following summarizes the initialized values for registers.

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Type	–	–	–	–	–	–	–	–
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Type	–	–	–	–	–	–	–	–
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC70	Bit Name	×	×	×	×	×	×	C71	C70
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC80	Bit Name	×	×	CMPOUT	COS1	COS0	TCCAEN	TCCATS	TCCATE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC90	Bit Name	TCCBHE	TCCBEN	TCCBTS	TCCBTE	×	TCCCEN	TCCCTS	TCCCTE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA0 (IRCR)	Bit Name	TCCCSE	TCCCS2	TCCCS1	TCCCS0	IRE	HF	LGP	IROUTE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB0 (PDCR)	Bit Name	/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCC0 (ODCR)	Bit Name	/OD67	/OD66	/OD65	/OD64	/OD63	/OD62	/OD61	/OD60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD0 (PHCR1)	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE0 (WDTCR)	Bit Name	WDTE	EIS	ADIE	CMPIE	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF0 (IMR)	Bit Name	LPWTIE	HPWTIE	TCCCIE	TCCBIE	TCCAIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC51 (TCCA)	Bit Name	TCCA7	TCCA6	TCCA5	TCCA4	TCCA3	TCCA2	TCCA1	TCCA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC61 (TCCB)	Bit Name	TCCB7	TCCB6	TCCB5	TCCB4	TCCB3	TCCB2	TCCB1	TCCB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC71 (TCCBH)	Bit Name	TCCBH7	TCCBH6	TCCBH5	TCCBH4	TCCBH3	TCCBH2	TCCBH1	TCCBH0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC81 (TCCC)	Bit Name	TCCC7	TCCC6	TCCC5	TCCC4	TCCC3	TCCC2	TCCC1	TCCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC91 (LTR)	Bit Name	LTR7	LTR6	LTR5	LTR4	LTR3	LTR2	LTR1	LTR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCA1 (HTR)	Bit Name	HTR7	HTR6	HTR5	HTR4	HTR3	HTR2	HTR1	HTR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB1 (HLTS)	Bit Name	HTSE	HTS2	HTS1	HTS0	LTSE	LTS2	LTS1	LTS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC1 (TCCPC)	Bit Name	TCCPC7	TCCPC6	TCCPC5	TCCPC4	TCCPC3	TCCPC2	TCCPC1	TCCPC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD1 (LVD CR) (ROMLESS)	Bit Name	TYPE1	TYPE0	LVR1	LVR0	LVDIE	LVDEN	LVD1	LVD0
		Power-on	1	1	1	1	0	0	1	1
		/RESET and WDT	P	P	P	P	0	P	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE1 (OSSCR) (ROMLESS)	Bit Name	WDPTS	TIMERSC	CPUS	IDLE	HS3	HS2	HS1	HS0
		Power-on	1	1	1	1	0	0	0	0
		/RESET and WDT	P	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF1 (PHCR2)	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	1	0	1	1	0	0	0	0
		/RESET and WDT	1	0	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	00	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×02	R2 (PC)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x06 or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	RST	IOCS	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	T	t	P	P	P
		Wake-up from Pin Change	P	P	P	T	t	P	P	P
0×04	R4 (RSR)	Bit Name	×	BS	–	–	–	–	–	–
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0×05	R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×7	R7	Bit Name	–	–	–	–	–	–	P71	P70
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×8	R8 (AISR)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0×9	R9 (ADCON)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	P	P
0×A	RA (ADOC)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×B	RB (ADDATA)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×C	RC (ADDATA1H)	Bit Name	"0"	"0"	"0"	"0"	AD11	AD10	AD9	AD8
		Power-on	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	U	U	U	U
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0×D	RD (ADDATA1L)	Bit Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×E	RE (ISR2)	Bit Name	/LVD	LVDIF	ADIF	CMPIF	ADWE	CMPWE	ICWE	LVDWE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×F	RF (ISR1)	Bit Name	LPWTIF	HPWTIF	TCCCIF	TCCBIF	TCCAIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x10~0x3F	R10~R3F	Bit Name	–	–	–	–	–	–	–	–
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: ***"x"*** *= not used* ***"P"*** *= previous value before reset*
"u" *= unknown or don't care* ***"t"*** *= check "Reset Type" Table in Section 6.5.2*

6.5.1.3 Controller Reset Block Diagram

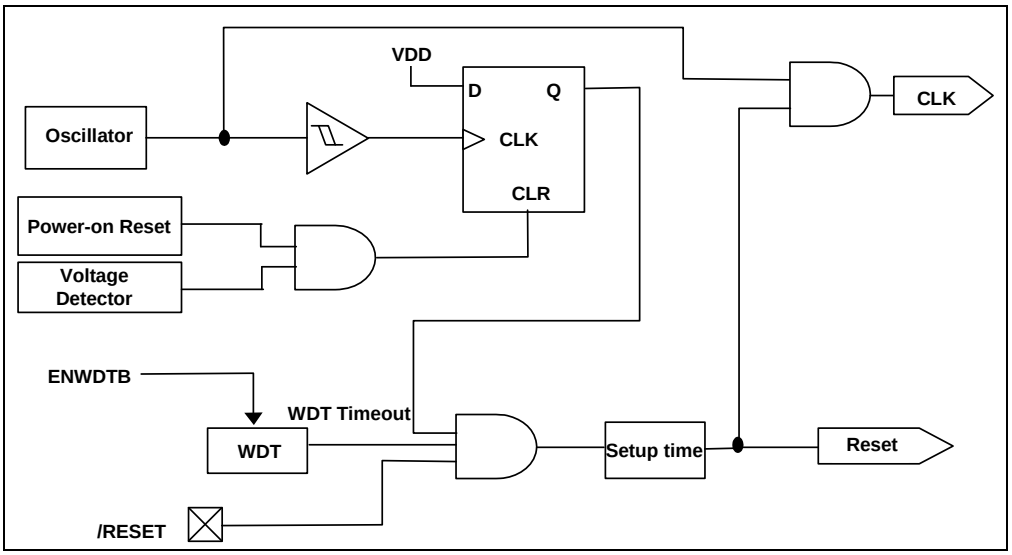


Figure 6-8 Controller Reset Block Diagram

6.5.2 The T and P Status under Status Register

A reset condition is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	RST	T	P
Power-on	0	1	1
/RESET during Operating mode,	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
LVR during Operating mode,	0	*P	*P
LVR wake-up during Sleep mode	0	1	0
WDT during Operating mode	0	0	1
WDT wake-up during Sleep mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0

*P: Previous status before reset

The following shows the events that may affect the status of T and P.

Event	RST	T	P
Power-on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin changed during Sleep mode	1	1	0

*P: Previous value before reset

6.6 Interrupt

The EM78P342N has seven interrupts enumerated below**:**

1. TCC, TCCA, TCCB, TCCC overflow interrupt
2. Port 5 Input Status Change Interrupt
3. External interrupt [(P60, /INT) pin]
4. Analog to Digital conversion completed
5. IR/PWM underflow interrupt
6. When the comparators status changes
7. Low voltage detector interrupt

Before the Port 5 Input Status Change Interrupt is enabled, reading Port 5 (e.g. "MOV R5,R5") is necessary. Each Port 5 pin will have this feature if its status changes. The Port 5 Input Status Change Interrupt will wake up the EM78P342N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP instruction. When wake up occurs, the controller will continue to execute program in-line if the global interrupt is disabled. If enabled, the global interrupt will branch out to the Interrupt Vector 006H.

External interrupt equipped with digital noise rejection circuit (input pulse less than system clock time) is eliminated as noise. However, under Low Crystal oscillator (LXT) mode the noise rejection circuit will be disabled. Edge selection is possible with INTE of CONT. When an interrupt is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H. Refer to Word 1 Bits 9 and 8, Section 6.14.2, *Code Option Register (Word 1)* for digital noise rejection definition.

RF and RE are the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 and IOCE0 are interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

When interrupt mask bits is “Enable”, the flag in the Interrupt Status Register (RF) is set regardless of the ENI execution. Note that the result of RF will be the logic AND of RF and IOCF0 (refer to figure below). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

When an interrupt is generated by the Timer clock/counter (when enabled), the next instruction will be fetched from Address 009, 018, 01B, and 01EH (TCC, TCCA, TCCB, and TCCC respectively).

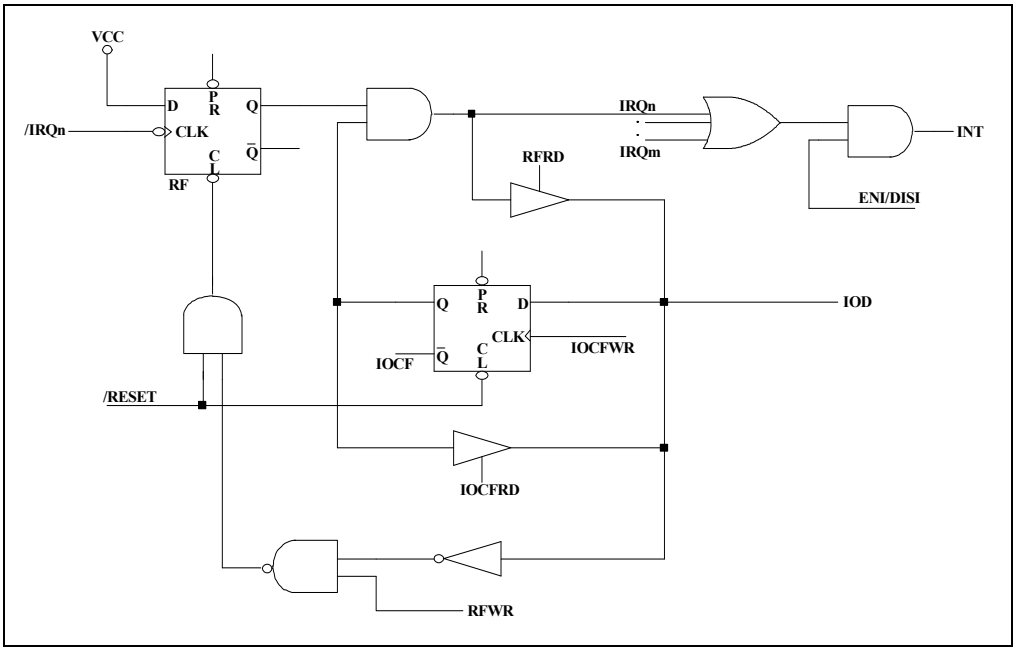
When an interrupt generated by the AD conversion is completed (when enabled), the next instruction will be fetched from Address 00CH.

When an interrupt is generated by the High time / Low time down counter underflow (when enabled), the next instruction will be fetched from Addresses 012 and 015H (High time and Low time respectively).

When an interrupt is generated by the Comparators (when enabled), the next instruction will be fetched from Address 00FH (Comparator interrupt).

When an interrupt is generated by the Low Voltage Detect (when enabled), the next instruction will be fetched from Address 021H (Low Voltage Detector interrupt).

Before an interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers are saved first by the hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After an interrupt service routine is completed, the ACC, R3, and R4 registers are restored.



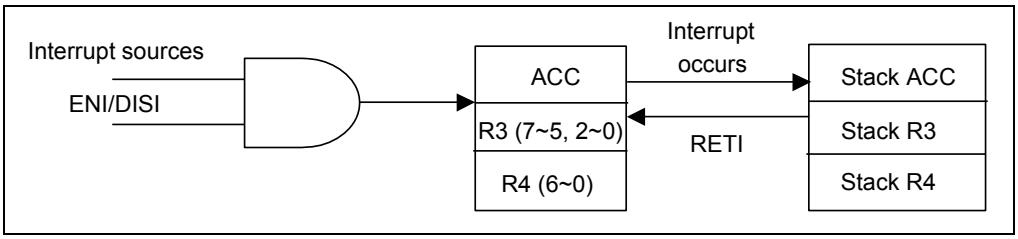


Figure 6-9 Interrupt Back-up Diagram

In EM78P342N, each individual interrupt source has its own interrupt vector as depicted in the table below.

Interrupt Vector	Interrupt Status	Priority *
003H	External interrupt	2
006H	Port 5 pin change	3
009H	TCC overflow interrupt	4
00CH	AD conversion complete interrupt	5
00FH	Comparator interrupt	6
012H	High-pulse width timer underflow interrupt	7
015H	Low-pulse width timer underflow interrupt	8
018H	TCCA overflow interrupt	9
01BH	TCCB overflow interrupt	10
01EH	TCCC overflow interrupt	11
021H	Low Voltage Detector interrupt	1

***Note:** *Priority: 1 = highest ; 11 = lowest priority*

6.7 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer; three control registers (AISR/R8, ADCON/R9, & ADOC/RA), three data registers (ADDATA1/RB, ADDATA1H/RC, and ADDATA1L/RD) and an ADC with 12-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins. Connecting to an external VREF is more accurate than connecting to an internal VDD.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA, ADDATA1H, and ADDATA1L. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS1 and ADIS0.

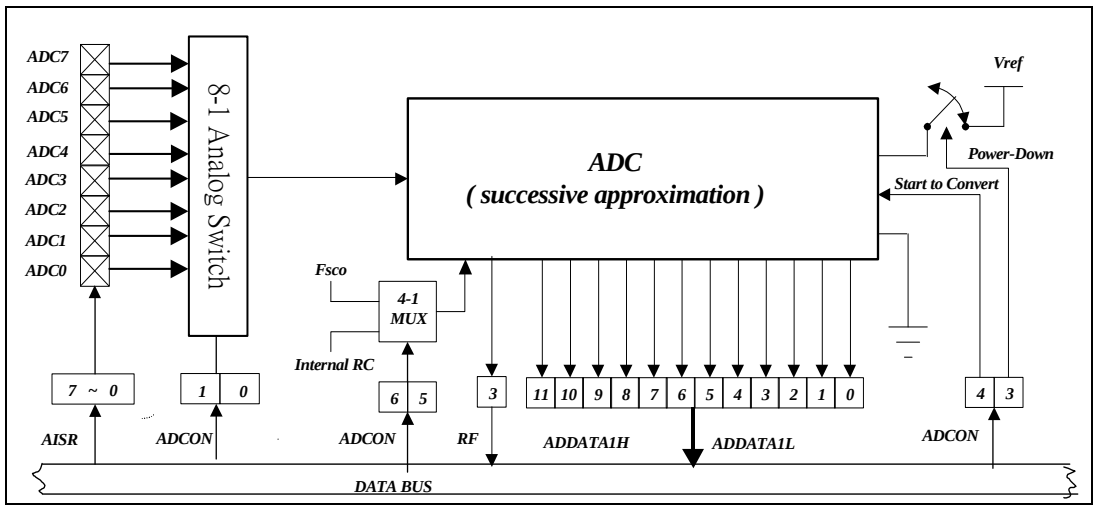


Figure 6-10 Analog-to-Digital Conversion Functional Block Diagram

6.7.1 ADC Control Register (AISR/R8, ADCON/R9, ADOC/RA)

6.7.1.1 R8 (AISR: ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

The **AISR** register individually defines the P5, P6 and P7 pins as analog inputs or as digital I/O.

Bit 7 (ADE7): AD converter enable bit of P57 pin

0 : Disable ADC7, P57 functions as I/O pin

1 : Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P55 pin

0 : Disable ADC6, P55 functions as I/O pin

1 : Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P70 pin

0 : Disable ADC5, P70 functions as I/O pin

1 : Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P67 pin

0 : Disable ADC4, P67 functions as I/O pin

1 : Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0 : Disable ADC3, P53 functions as I/O pin

1 : Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0 : Disable ADC2, P52 functions as I/O pin

1 : Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0 : Disable ADC1, P51 acts as I/O pin

1 : Enable ADC1 acts as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0 : Disable ADC0, P50 functions as I/O pin

1 : Enable ADC0 to function as analog input pin

6.7.1.2 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

The **ADCON** register controls the operation of the AD conversion and decides which pin should be currently active.

Bit 7(VREFS): The input source of the ADC Vref

0 : The ADC Vref is connected to Vdd (default value), and the VREF/TCC/P54 pin carries out the P54 function

1 : The ADC Vref is connected to VREF/TCC/P54

NOTE

The P54/TCC/VREF pin cannot be applied to TCC and VREF at the same time. If P54/TCC/VREF functions as VREF analog input pin, then CONT Bit 5 (TS) must be "0".

The P54/TCC/VREF pin priority is as follows:

P54/TCC/VREF Pin Priority		
High	**Medium**	**Low**
VREF	**TCC**	**P54**

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of ADC oscillator clock rate

00 = 1**:** 16 (default value)

01 = 1**:** 4

10 = 1**:** 64

11 = 1**:** 8

CPUS	CKR1: CKR0	Operation Mode	Max. Operation Frequency
1	00	Fosc/16	4 MHz
1	01	Fosc/4	1 MHz
1	10	Fosc/64	16 MHz
1	11	Fosc/8	2 MHz
0	××	Internal RC	–

Bit 4 (ADRUN): ADC starts to RUN

0 : Reset upon completion of the conversion. This bit **cannot** be reset though software.

1 : an AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0 : Switch off the resistor reference to conserve power even while the CPU is operating

1 : ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

000 = ADIN0/P50

001 = ADIN1/P51

010 = ADIN2/P52

011 = ADIN3/P53

100 = ADIN4/P67

101 = ADIN5/P70

110 = ADIN6/P55

111 = ADIN7/P57

These bits can only be changed when the ADIF bit and the ADRUN bit are both LOW

6.7.1.3 RA (ADOC: AD Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	"0"	"0"	"0"

Bit 7 (CALI): Calibration enable bit for ADC offset

0 = disable Calibration

1 = enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0 = Negative voltage

1 = Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits.

VOF[2]	VOF[1]	VOF[0]	EM78P342N	ICE341N
0	0	0	0LSB	0LSB
0	0	1	2LSB	2LSB
0	1	0	4LSB	4LSB
0	1	1	6LSB	6LSB
1	0	0	8LSB	8LSB
1	0	1	10LSB	10LSB
1	1	0	12LSB	12LSB
1	1	1	14LSB	14LSB

Bit 2 ~ Bit 0: Unimplemented**,** read as '0'.

6.7.2 ADC Data Register (ADDATA/RB, ADDATA1H/RC, ADDATA1L/RD)

When the AD conversion is completed, the result is loaded to the ADDATA, ADDATA1H and ADDATA1L registers. The ADRUN bit is cleared, and the ADIF is set.

6.7.3 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation of the AD converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2μs for each KΩ of the analog source impedance and at least 2μs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion is started.

6.7.4 AD Conversion Time

CKR1 and CKR0 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the AD conversion accuracy. For the EM78P342N, the conversion time per bit is about 4μs. The table below shows the relationship between Tct and the maximum operating frequencies.

CKR1:CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
00	Fosc/16	4 MHz	250kHz (4μs)	15×4μs=60μs (16.7kHz)
01	Fosc/4	1 MHz	250kHz (4μs)	15×4μs=60μs (16.7kHz)
10	Fosc/64	16 MHz	250kHz (4μs)	15×4μs=60μs (16.7kHz)
11	Fosc/8	2 MHz	250kHz (4μs)	15×4μs=60μs (16.7kHz)

NOTE

- *Pin not used as an analog input pin can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all of the pins.*

6.7.5 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, TCCA, TCCB, TCCC, and AD conversion.

The AD Conversion is considered completed as determined by**:**

1. The ADRUN bit of the R9 register is cleared to “0”.
2. The ADIF bit of the RE register is set to “1”.
3. The ADWE bit of the RE register is set to “1.” Wakes up from ADC conversion (where it remains in operation during sleep mode).
4. Wake up and execution of the next instruction if the ADIE bit of the IOCE0 is enabled and the “DISI” instruction is executed.

5. Wake up and enters into Interrupt vector (Address 0x00C) if the ADIE bit of the IOCE0 is enabled and the “ENI” instruction is executed.
6. Enters into an Interrupt vector (Address 0x00C) if the ADIE bit of the IOCE0 is enabled and the “ENI” instruction is executed.

The results are fed into the ADDATA, ADDATA1H, and ADDATA1L registers when the conversion is completed. If the ADIE is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADPD bit is.

6.7.6 Programming Process/Considerations

6.7.6.1 Programming Process

Follow these steps to obtain data from the ADC**:**

1. Write to the eight bits (ADE7: ADE0) on the R8 (AISR) register to define the characteristics of R5 (digital I/O, analog channels, or voltage reference pin)
2. Write to the R9/ADCON register to configure the AD module**:**
   a) Select the ADC input channel (ADIS2 : ADIS0)
   b) Define the AD conversion clock rate (CKR1 : CKR0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to 1 to begin sampling
3. Set the ADWE bit, if the wake-up function is employed
4. Set the ADIE bit, if the interrupt function is employed
5. Write “ENI” instruction, if the interrupt function is employed
6. Set the ADRUN bit to 1
7. Write “SLEP” instruction or Polling.
8. Wait for wake-up or for the ADRUN bit to be cleared to “0” , interrupt flag (ADIF) is set “1,” or ADC interrupt occurs.
9. Read the ADDATA or ADDATA1H and ADDATA1L conversion data registers. If the ADC input channel changes at this time, the ADDATA, ADDATA1H, and ADDATA1L values can be cleared to ‘0’.
10. Clear the interrupt flag bit (ADIF).
11. For the next conversion, go to Step 1 or Step 2 as required. At least two Tct is required before the next acquisition starts.

NOTE

In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

6.7.6.2 Sample Demo Programs

```
R_0 == 0          ; Indirect addressing register
PSW == 3          ; Status register
PORT5 == 5
PORT6 == 6
R_E== 0XE         ; Interrupt status register
```

B. Define a Control Register

```
IOC50 == 0X5      ; Control Register of Port 5
IOC60 == 0X6      ; Control Register of Port 6
IOCE0== 0XE       ; Interrupt Mask Register 2
C_INT== 0XF       ; Interrupt Mask Register
```

C. ADC Control Register

```
ADDATA == 0xB     ; The contents are the results of ADC
AISR == 0x08      ; ADC input select register
ADCON == 0x9      ;  7     6    5    4      3    2     1     0
                  ;VREFS CKR1 CKR0 ADRUN ADPD ADIS2 ADIS1 ADIS0
```

D. Define Bits in ADCON

```
ADRUN == 0x4      ; ADC is executed as the bit is set
ADPD == 0x3       ; Power Mode of ADC
```

E. Program Starts

```
ORG 0             ; Initial address
JMP INITIAL       ;

ORG 0x0C          ; Interrupt vector
JMP CLRRE
;
;(User program section)
;
CLRRE:
MOV A,RE
AND A, @0BXX0XXXXX  ; To clear the ADIF bit, "X" by application
MOV RE,A
BS ADCON, ADRUN     ; To start to execute the next AD conversion
                    ; if necessary
RETI
INITIAL:
MOV A,@0B00000001   ; To define P50 as an analog input
MOV AISR,A
MOV A,@0B00001000   ; To select P50 as an analog input channel, and
                    ;  AD power on
MOV ADCON,A         ; To define P50 as an input pin and set clock
                    ;  rate at fosc/16
En_ADC:
MOV A, @0BXXXXXXX1  ; To define P50 as an input pin, and the others
                    ; are dependent on applications
IOW PORT5
```

```
MOV A, @0BXXXX1XXX  ; Enable the ADWE wake-up function of ADC, "X"
                    ; by application
MOV RE,A
MOV A, @0BXX1XXXXX  ; Enable the ADIE interrupt function of ADC,
                    ; "X" by application
IOW IOCE0
ENI                 ; Enable the interrupt function

BS ADCON, ADRUN     ; Start to run the ADC

; If the interrupt function is employed, the following three lines
may be ignored

;If Sleep:
SLEP
;
;(User program section)
;

or
;If Polling:
POLLING:
JBC ADCON, ADRUN    ; To check the ADRUN bit continuously;
JMP POLLING         ; ADRUN bit will be reset as the AD conversion
                    ; is completed
;
;(User program section)
```

6.8 Infrared Remote Control Application/PWM Waveform Generation

6.8.1 Overview

This LSI can easily output infrared carrier or PWM standard waveform. As illustrated below, the IR and PWM waveform generation function include an 8-bit down count timer/counter, high-time, low-time, and IR control register. The IROUT pin waveform is determined by IOCA0 (IR and TCCC scale control register), IOCB1 (high-time rate, low-time rate control register), IOC81 (TCCC counter), IOCA1 (high-time register), and IOC91 (low-time register).

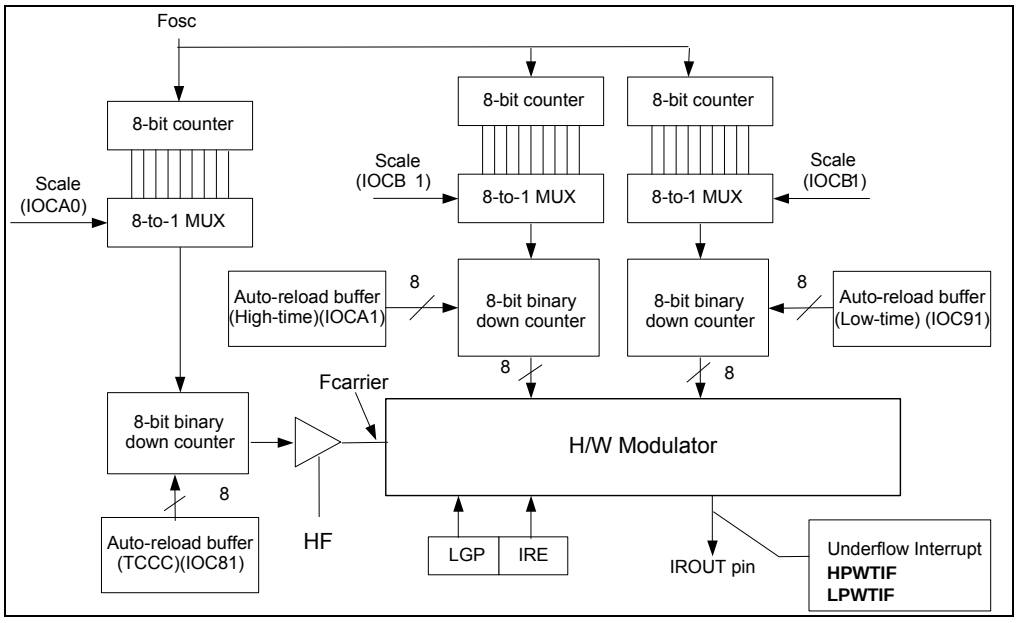


Figure 6-12 IR/PWM System Block Diagram

Details of the Fcarrier High Time Width and Low Time Width are shown below:

$$F_{carrier} = \frac{FT}{2\left\{\left[\ 1 + Decimal\ \ TCCC\ \ Counter\ \ Value\ \ (IOC81)\ \right] \times\ \ TCCC\ \ Scale\ \ (IOCA0)\right\}}$$

where $FT = \dfrac{F_{OSC}}{1}$

$$High\ \ Time\ \ Width = \frac{\left\{\left[\ 1 + Decimal\ \ High\ \ Time\ \ Value\ \ (IOCA1)\right] \times High\ \ Time\ \ Scale\ \ (IOCB1)\ \right\}}{FT}$$

$$Low\ \ Time\ \ Width = \frac{\left\{\left[\ 1 + Decimal\ \ Low\ \ Time\ \ Value\ \ (IOC91)\right] \times Low\ \ Time\ \ Scale\ \ (IOCB1)\ \right\}}{FT}$$

When an interrupt is generated by the High time down counter underflow (when enabled), the next instruction will be fetched from Address 018 and 01BH (High time and Low time respectively).

6.8.2 Function Description

The following figure shows **LGP=0** and **HF=1**. The IROUT waveform modulates the Fcarrier waveform at low-time segments of the pulse.

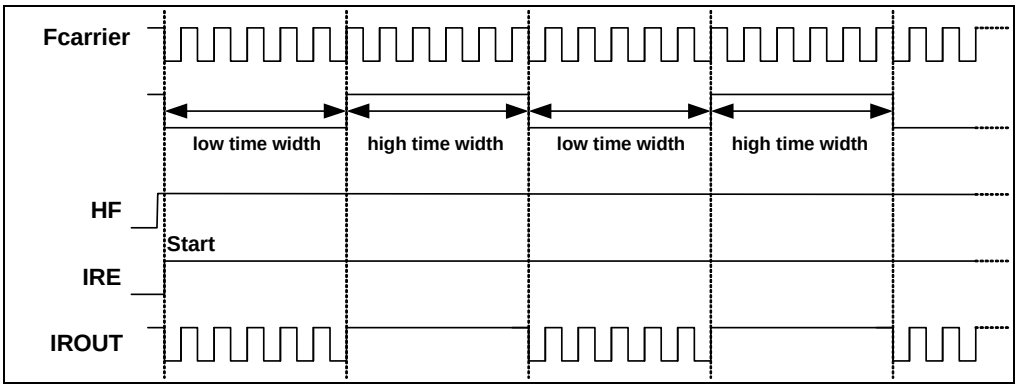


Figure 6-13a LGP=0, HF=1, IROUT Pin Output Waveform

The following figure shows **LGP=0** and **HF=0**. The IROUT waveform cannot modulate the Fcarrier waveform at low-time segments of the pulse. So IROUT waveform is determined by the high time width and low time width instead. This mode can produce standard PWM waveform.

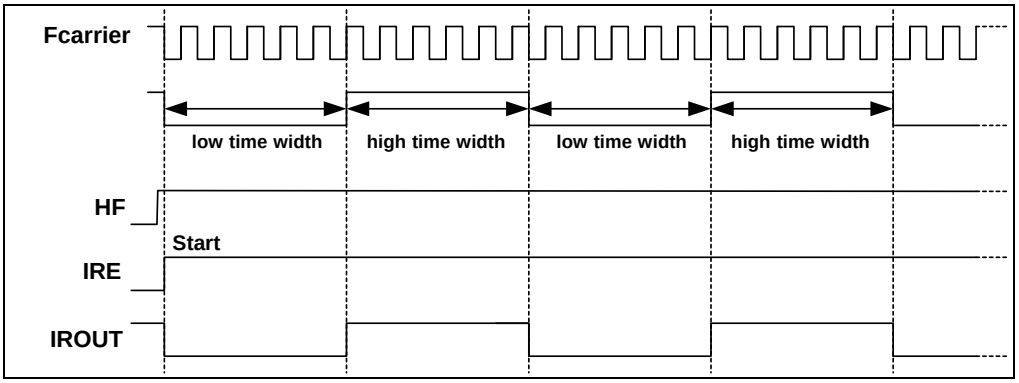


Figure 6-13b LGP=0, HF=0, IROUT Pin Output Waveform

The following figure shows LGP=0 and HF=1. The IROUT waveform modulates the Fcarrier waveform at low-time segments of the pulse. When IRE goes low from high, the output waveform of IROUT will keep transmitting until high-time interrupt occurs.

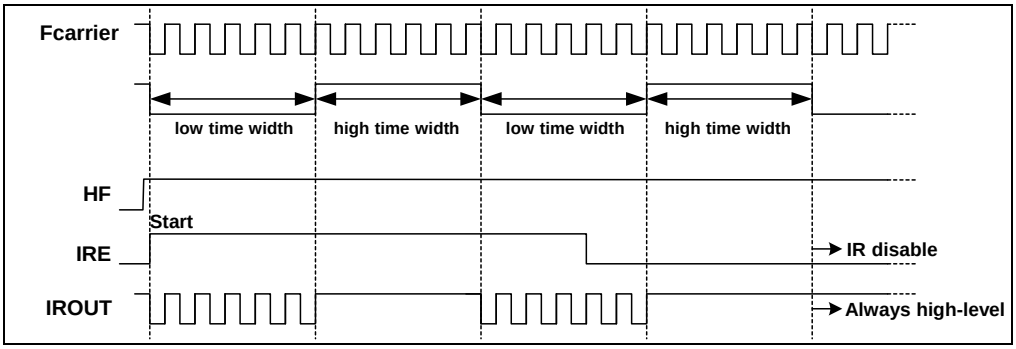


Figure 6-13c LGP=0, HF=1, When IRE goes Low from High, IROUT Pin Outputs Waveform

The following figure shows **LGP=0** and **HF=0**. The IROUT waveform cannot modulate the Fcarrier waveform at low-time segments of the pulse. So IROUT waveform is determined by high time width and low time width. This mode can produce standard PWM waveform when IRE goes low from high. The output waveform of IROUT will keep on transmitting until high-time interrupt occurs.

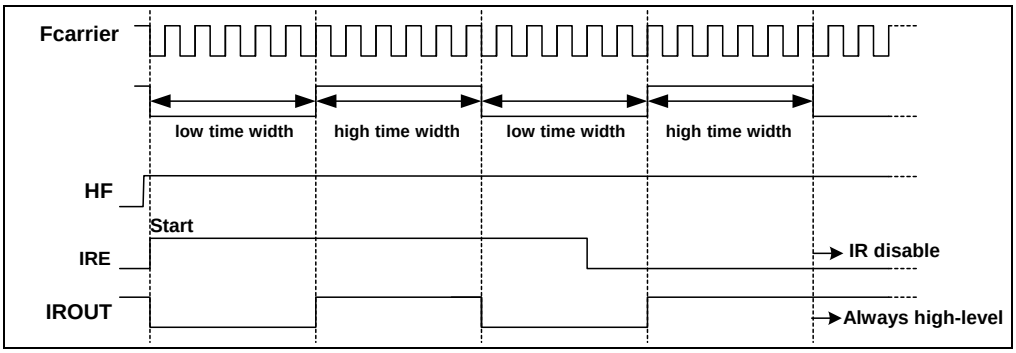


Figure 6-13d LGP=0, HF=0, When IRE goes Low from High, Irout Pin Output Waveform

The following figure shows **LGP=1** and **HF=1**. When this bit is set to high level, the high-time segment of the pulse is ignored. So, IROUT waveform output is determined by low-time width.

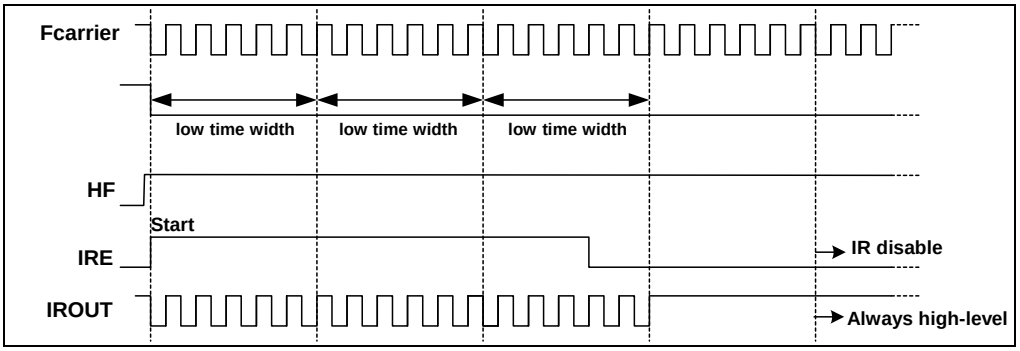


Figure 6-13e LGP=1 and HF=1, IROUT Pin Output Waveform

6.8.3 Programming the Related Registers

When defining IR/PWM, refer to the operation of the related registers as shown in the tables below.

IR/PWM Related Control Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×09	IOC90	TCCBHE/0	TCCBEN/0	TCCBTS/0	TCCBTE/0	0	TCCCEN/0	TCCCTS/0	TCCCTE/0
0×0A	IR CR /IOCA0	TCCCSE/0	TCCCS2/0	TCCCS1/0	TCCCS0/0	IRE/0	HF/0	LGP/0	IROUTE/0
0×0F	IMR /IOCF0	LPWTIE/0	HPWTIE/0	TCCCIE/0	TCCBIE/0	TCCAIE/0	EXIE/0	ICIE/0	TCIE/0
0×0B	HLTS /IOCB1	HTSE/0	HTS2/0	HTS1/0	HTS0/0	LTSE/0	LTS2/0	LTS1/0	LTS0/0

IR/PWM Related Status/Data Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0F	ISR/RF	LPWTIF/0	HPWTIF/0	TCCCIF/0	TCCBIF/0	TCCAIF/0	EXIF/0	ICIF/0	TCIF/0
0×06	TCCC /IOC81	TCCC7/0	TCCC6/0	TCCC5/0	TCCC4/0	TCCC3/0	TCCC2/0	TCCC1/0	TCCC0/0
0×09	LTR /IOC91	LTR7/0	LTR6/0	LTR5/0	LTR4/0	LTR3/0	LTR2/0	LTR1/0	LTR0/0
0×0A	HTR /IOCA1	HTR7/0	HTR6/0	HTR5/0	HTR4/0	HTR3/0	HTR2/0	HTR1/0	HTR0/0

6.9 Timer/Counter

6.9.1 Overview

Timer A (TCCA) is an 8-bit clock counter. Timer B (TCCB) is a 16-bit clock counter. Timer C (TCCC) is an 8-bit clock counter that can be extended to 16-bit clock counter with programmable scalers. TCCA, TCCB, and TCCC can be read and written to, and are cleared at every reset condition.

6.9.2 Functional Description

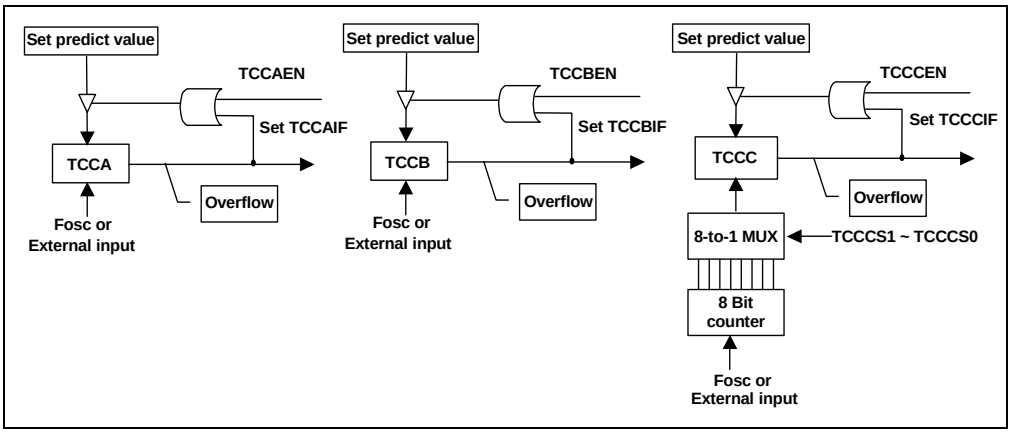


Figure 6-14 Timer Block Diagram

Each signal and block of the above Timer block diagram is described as follows:

TCCX: Timer A~C register. TCCX is incremented until it matches with zero, and then reloads the predicted value. When writing a value to TCCX, the predicted value and TCCX value become the set value. When reading from TCCX, the value will be the TCCX direct value. When TCCXEN is enabled, the reloading of the predicted value to TCCX, TCCXIE is also enabled. TCCXIF will be set at the same time. It is an up counter.

TCCA Counter (IOC51):

IOC51 (TCCA) is an 8-bit clock counter. It can be read, written to, and cleared on any reset condition and it is also an Up Counter.

$$TCCA\ Timeout\ \ period = \frac{1}{F_{OSC}} \times \left(256 - TCCA\ cnt\right) \times 1$$

TCCB Counter (IOC61):

IOC61 is an 8-bit clock counter for the least significant byte of TCCBX (TCCB). It can be read, written, and cleared on any reset condition and it is also an Up Counter.

TCCBH / MSB Counter (IOC71):

IOC71 is an 8-bit clock counter for the most significant byte of TCCBX (TCCBH). It can be read, written to, and cleared on any reset condition.

When TCCBHE (IOC90) is "0," then TCCBH is disabled. When TCCBHE is"1," then TCCB is a 16-bit length counter.

When TCCBH is disabled:

$$TCCB\ Timeout\ \ period = \frac{1}{F_{OSC}} \times \left(256 - TCCB\ cnt\right) \times 1$$

When TCCBH is enabled:

$$TCCB\ Timeout\ \ period = \frac{1}{F_{OSC}} \times \left[\ 65536\ -\ \left(TCCBH\ \times\ 256\ +\ TCCB\ cnt\right) \times 1\ \right]$$

TCCC Counter (IOC81):

IOC81 (TCCC) is an 8-bit clock counter. It can be read, written to, and cleared on any reset condition.

If HF (Bit 2 of IOCA0) = 1 and IRE (Bit 3 of IOCA0) = 1, TCCC counter scale uses the low-time segments of the pulse generated by Fcarrier frequency modulation (see Figure 6-11 in Section 6.8.2, *Function Description*). The TCCC value will then be the TCCC predicted value.

When HF = 0 or IRE = 0. The TCCC is an Up Counter.

In TCCC Up Counter mode:

$$TCCC\ Timeout\ \ period = \frac{1}{F_{OSC}} \times\ Scaler\ \left(IOCA0\right) \times \left(256 - TCCC\ cnt\right) \times 1$$

When HF = 1 and IRE = 1, TCCC counter scale uses the low-time segments of the pulse generated by the Fcarrier frequency modulation.

In IR mode:

$$F_{carrier} = \frac{FT}{2\left\{\left[\ 1 + Decimal\ TCCC\ Counter\ Value\ \left(IOC81\right)\ \right] \times\ TCCC\ Scale\ \left(IOCA0\right)\right\}}$$

$$\text{where}\ \ FT = \frac{F_{OSC}}{1}$$

6.9.3 Programming the Related Registers

When defining TCCX, refer to the operation of its related registers as shown in the tables below.

TCCX Related Control Registers:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	IOC80	0	0	CPOUT/0	COS1/0	COS0/0	TCCAEN/0	TCCATS/0	TCCATE/0
0x09	IOC90	TCCBHE/0	TCCBEN/0	TCCBTS/0	TCCBTE/0	0	TCCCEN/0	TCCCTS/0	TCCCTE/0
0x0A	IR CR /IOCA0	TCCCSE/0	TCCCS2/0	TCCCS1/0	TCCCS0/0	IRE/0	HF/0	LGP/0	IROUTE/0
0x0F	IMR /IOCF0	LPWTE/0	HPWTE/0	TCCCIE/0	TCCBIE/0	TCCAIE/0	EXIE/0	ICIE/0	TCIE/0

Related TCCX Status/Data Registers:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	ISR/RF	LPWTF/0	HPWTF/0	TCCCIF/0	TCCBIF/0	TCCAIF/0	EXIF/0	ICIF/0	TCIF/0
0x05	TCCA /IOC51	TCCA7/0	TCCA6/0	TCCA5/0	TCCA4/0	TCCA3/0	TCCA2/0	TCCA1/0	TCCA0/0
0x06	TCCB /IOC61	TCCB7/0	TCCB6/0	TCCB5/0	TCCB4/0	TCCB3/0	TCCB2/0	TCCB1/0	TCCB0/0
0x07	TCCBH /IOC71	TCCBH7/0	TCCBH6/0	TCCBH5/0	TCCBH4/0	TCCBH3/0	TCCBH2/0	TCCBH1/0	TCCBH0/0
0x08	TCCC /IOC81	TCCC7/0	TCCC6/0	TCCC5/0	TCCC4/0	TCCC3/0	TCCC2/0	TCCC1/0	TCCC0/0

6.10 Comparator

The EM78P342N has one comparator which has two analog inputs and one output. The comparator can be employed to wake up the system from sleep/idle mode. The Figure at right shows the comparator circuit.

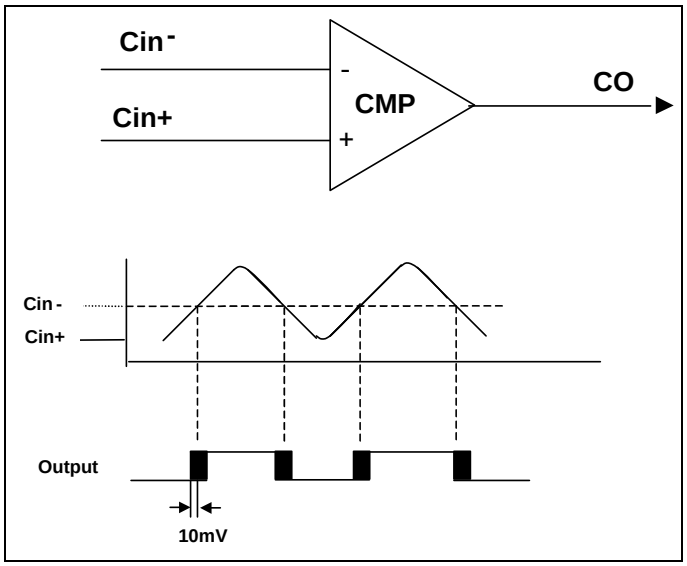


Figure 6-15 Comparator Operating Mode

6.10.1 External Reference Signal

The analog signal that is presented at Cin– compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

NOTE

- *The reference signal must be between Vss and Vdd.*
- *The reference voltage can be applied to either pin of the comparator.*
- *Threshold detector applications may be of the same reference.*
- *The comparator can operate from the same or different reference sources.*

6.10.2 Comparator Outputs

- The compared result is stored in the CMPOUT of IOC80.
- The comparator outputs are sent to CO (P64) by programming Bit 4 and Bit 3 <COS1, COS0> of the IOC80 register to <1,0>. See table under Section 6.2.4, *IOC80 (Comparator and TCCA Control Registers)* for Comparator/OP select bits function description.

The following figure shows the Comparator Output block diagram.

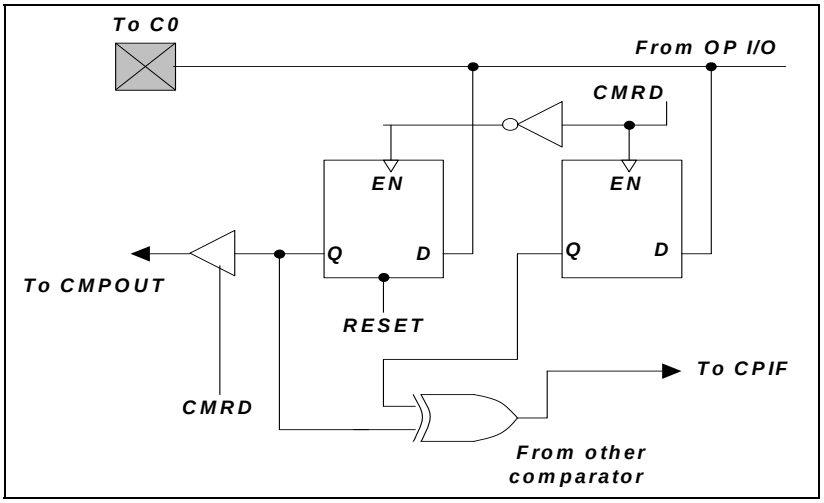


Figure 6-16 Comparator Output Configuration

6.10.3 Using Comparator as an Operation Amplifier

The comparator can be used as an operation amplifier if a feedback resistor is externally connected from the input to the output. In this case, the Schmitt trigger function can be disabled for power saving purposes, by setting Bit 4, Bit 3 <COS1, COS0> of the IOC80 register to <1,1>. See table under Section 6.2.4, *IOC80 (Comparator and TCCA Control Registers)* for Comparator/OP select bits function description.

NOTE

Under Operation Amplifier:

- *The CMPIE (IOCE0.4), CMPWE (RE.2), and CMPIF (RE.4) bits are invalid.*
- *The comparator interrupt is invalid.*
- *The comparator wake-up is invalid.*

6.10.4 Comparator Interrupt

- CMPIE (IOCE0.4) must be enabled for the "ENI" instruction to take effect.
- Interrupt is triggered whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CMPOUT, IOC80<5>.
- CMPIF (RE.4), the comparator interrupt flag, can only be cleared by software.

6.10.5 Wake-up from Sleep Mode

- If the CMPWE bit of the RE register is set to "1," the comparator remains active and the interrupt remains functional, even under Sleep mode.
- If a mismatch occurs, the change will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

The Comparator is considered completed as determined by**:**

1. COS1 and COS0 bits of IOC80 register setting selects Comparator.
2. CMPIF bit of RE register is set to "1".
3. CMPWE bit of RE register is set to "1". Wakes up from Comparator (where it remains in operation during sleep/idle mode).
4. Waking-up and executing the next instruction, if CMPIE bit of IOCE0 is enabled and the "DISI" instruction is executed.
5. Waking-up and entering into Interrupt vector (Address 0x00F), if CMPIE bit of IOCE0 is enabled and the "ENI" instruction is executed.
6. Entering into Interrupt vector (Address 0x00F), if CMPIE bit of IOCE0 is enabled and the "ENI" instruction is executed.

6.11 Oscillator

6.11.1 Oscillator Modes

The EM78P342N can be operated in six different oscillator modes, such as High Crystal Oscillator Mode 1 (HXT1), High Crystal Oscillator Mode 2 (HXT2), Low Crystal Oscillator Mode 1 (LXT1), Low Crystal Oscillator Mode 2 (LXT2), External RC Oscillator Mode (ERC), and RC Oscillator Mode with Internal RC Oscillator Mode (IRC). You can select one of them by programming the OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P70/OSCO acts as P70	0	0	0
ERC[1] (External RC oscillator mode); P70/OSCO acts as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P70/OSCO acts as P70	0	1	0
IRC[2] (Internal RC oscillator mode); P70/OSCO acts as OSCO	0	1	1
LXT1[3] (Frequency range of XT mode is 1MHz ~ 100kHz)	1	0	0
HXT1[3] (Frequency range of XT mode is 16MHz ~ 6MHz)	1	0	1
LXT2[3] (Frequency range of XT mode is 32kHz)	1	1	0
HXT2[3] (Frequency range of XT mode is 6MHz ~ 1MHz) (default)	1	1	1

[1] In ERC mode, OSCI is used as oscillator pin. OSCO/P70 is defined by code option Word 0 Bit 6 ~ Bit 4.

[2] In IRC mode, P55 is normal I/O pin. OSCO/P70 is defined by code option Word 0 Bit 6 ~ Bit 4.

[3] In LXT1, LXT2, HXT1 and HXT2 modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

The maximum operating frequency limit of crystal/resonator at different VDDs, are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.1V	4
	3.0V	8
	4.5V	16

6.11.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P342N can be driven by an external clock signal through the OSCI pin as illustrated below.

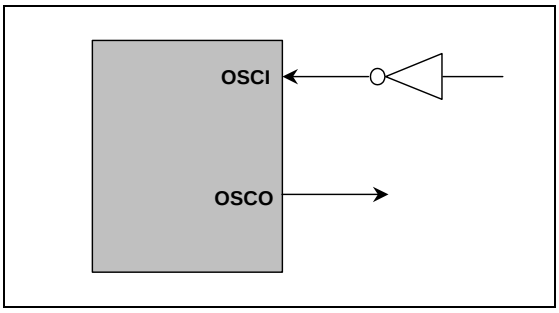


Figure 6-17 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-18 below depicts such a circuit. The same applies to the HXT1 mode, HTX2 mode, LXT1 mode and LXT2 mode.

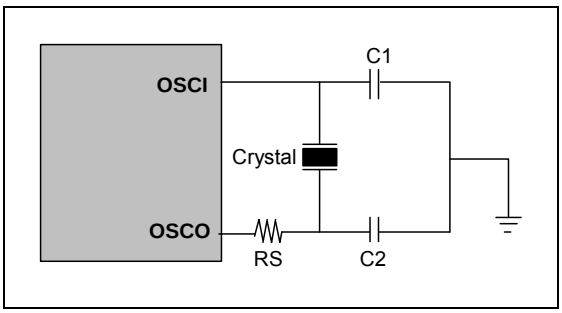


Figure 6-18 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, user should refer to the resonator specifications for the appropriate values of C1 and C2. RS, a serial resistor, maybe required for AT strip cut crystal or low frequency mode. Figure 6-21 is PCB layout suggestion. **When the system works in Crystal mode (16 MHz), a 10 KΩ is connected between OSCI and OSCO.**

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT (100 K ~ 1 MHz)	100kHz	67 pF	67 pF
		200kHz	30 pF	30 pF
		455kHz	30 pF	30 pF
		1 MHz	30 pF	30 pF
	MXT (1 M ~ 6 MHz)	1.0 MHz	30 pF	30 pF
		2.0 MHz	30 pF	30 pF
		4.0 MHz	30 pF	30 pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	40 pF	40 pF
	LXT1 (100 K ~ 1 MHz)	100kHz	67 pF	67 pF
		200kHz	30 pF	30 pF
		455kHz	30 pF	30 pF
		1 MHz	30 pF	30 pF
	HXT2 (1~6 MHz)	455kHz	30 pF	30 pF
		1.0 MHz	30 pF	30 pF
		2.0 MHz	30 pF	30 pF
		4.0 MHz	30 pF	30 pF
		6.0 MHz	30 pF	30 pF
	HXT1 (6~16 MHz)	6.0 MHz	30 pF	30 pF
		8.0 MHz	30 pF	30 pF
		10.0 MHz	30 pF	30 pF
		12.0 MHz	30 pF	30 pF
		16.0 MHz	15 pF	15 pF

Circuit diagrams for serial and parallel modes Crystal/Resonator:

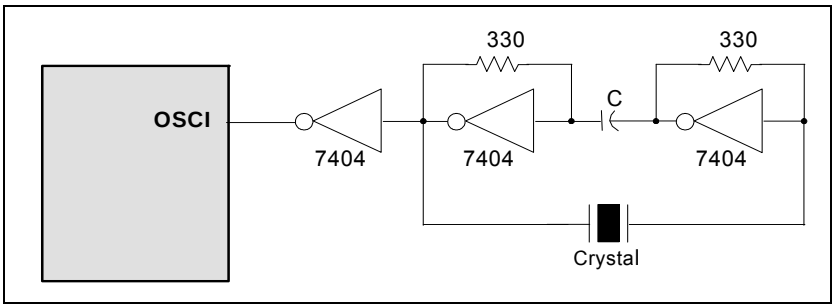


Figure 6-19 Serial Mode Crystal/Resonator Circuit Diagram

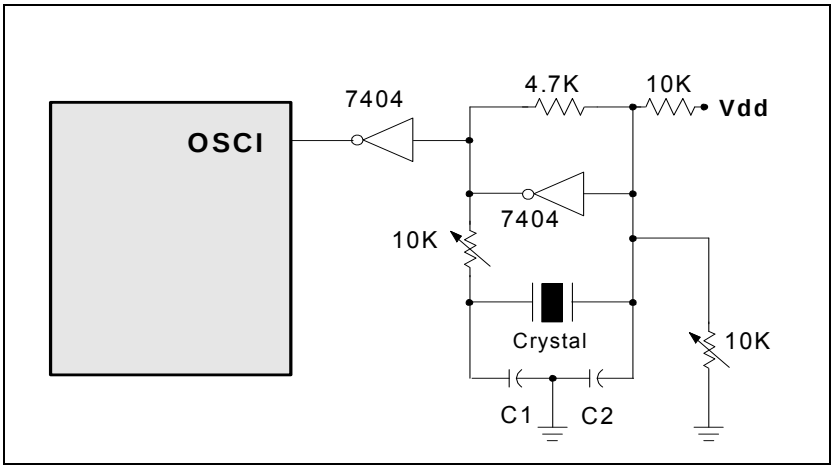


Figure 6-20 Parallel Mode Crystal/Resonator Circuit Diagram

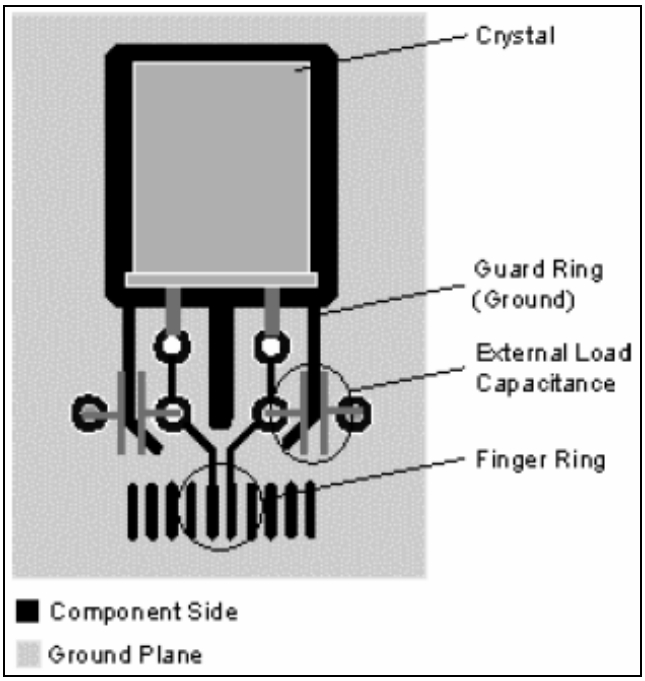


Figure 6-21 Parallel Mode Crystal/Resonator Circuit Diagram

6.11.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 6-22) could offer an effective cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

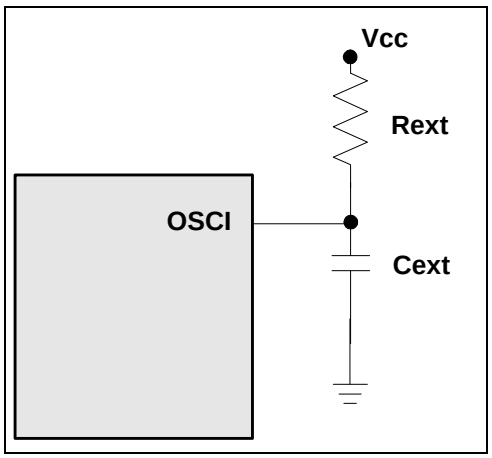


Figure 6-22 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should be no less than 20 pF, and the value of Rext should not be greater than 1 MΩ. If the frequency cannot be kept within this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot correctly discharge the capacitance current.

Based on the above reasons, it must be kept in mind that all supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout have certain effects on the system frequency.

The RC Oscillator frequencies:

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.0 MHz
	5.1k	2.4 MHz	2.2 MHz
	10k	1.27 MHz	1.24 MHz
	100k	140kHz	143kHz
100 pF	3.3k	1.21 MHz	1.18 MHz
	5.1k	805 kHz	790kHz
	10k	420kHz	418kHz
	100k	45 kHz	46kHz
300 pF	3.3k	550kHz	526kHz
	5.1k	364kHz	350kHz
	10k	188kHz	185kHz
	100k	20kHz	20kHz

Note: [1]: Measured based on DIP packages.
[2]: The values are for design reference only.
[3]: The frequency drift is ± 30%

6.11.4 Internal RC Oscillator Mode

The EM78P342N offers a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (16 MHz, 1 MHz, and 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The Table below describes the EM78P342N internal RC drift with voltage, temperature, and process variations.

Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40℃ ~+85℃)	Voltage (2.3V~3.9V~5.5V)	Process	Total
4 MHz	±5%	±5%	±4%	±14%
16 MHz	±5%	±5%	±4%	±14%
1 MHz	±5%	±5%	±4%	±14%
455kHz	±5%	±5%	±4%	±14%

Note: Theoretical values are for reference only. Actual values may vary depending on the actual process.

6.12 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply stabilizes in steady state. The EM78P342N POR voltage range is 1.6V ~ 1.8V. Under customer application, when power is switched OFF, Vdd must drop below 1.6V and remains at OFF state for 10μs before power can be switched ON again. Subsequently, the EM78P342N will reset and work normally. The extra external reset circuit will work well if Vdd rises fast enough (50ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.12.1 Programmable WDT Time-out Period

The Option word (WDTPS) is used to define the WDT time-out period (18ms[5] or 4.5ms[6]). Theoretically, the range is from 4.5ms or 18ms. For most crystal or ceramic resonators, the lower the operation frequency is, the longer is the required set-up time.

6.12.2 External Power-on Reset Circuit

The circuit shown in the following figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow the Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time. Because

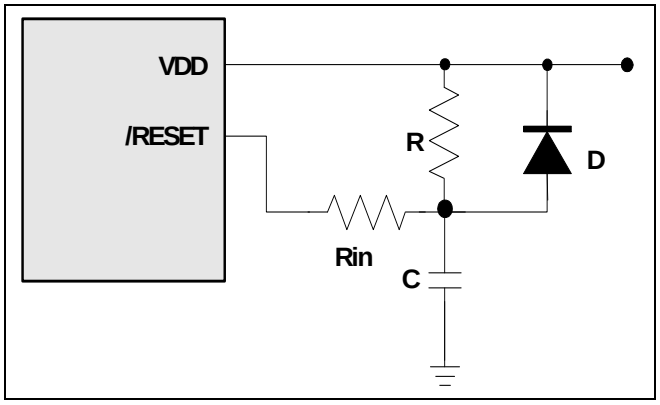


Figure 6-23 External Power-on Reset Circuit

the current leakage from the /RESET pin is about ± 5μA, it is recommended that R should not be greater than 40KΩ. This way, the voltage at Pin /RESET is held below 0.2V. The diode (D) functions as a short circuit at power-down. The "C" capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

[5] *VDD=5V, WDT time-out period = 16.5ms ± 30%.*
VDD=3V, WDT time-out period = 18ms ± 30%.

[6] *VDD=5V, WDT time-out period = 4.2ms ± 30%.*
VDD=3V, WDT time-out period = 4.5ms ± 30%.

6.12.3 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-24 and Figure 6-25 show how to create a protection circuit against residual voltage.

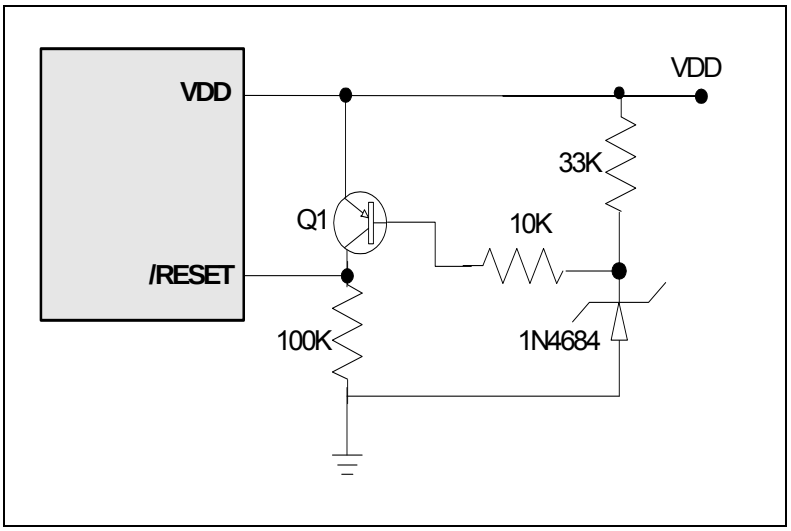


Figure 6-24 Residual Voltage Protection Circuit 1

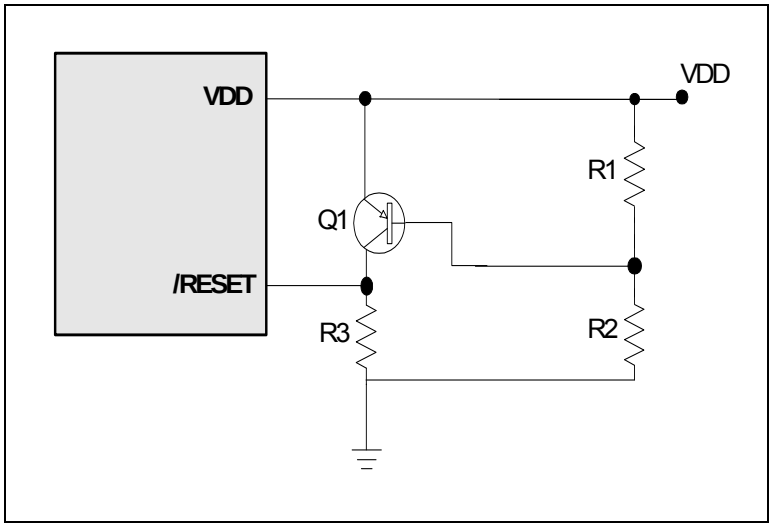


Figure 6-25 Residual Voltage Protection Circuit 2

6.13 Code Option

EM78P342N has two Code Option Words and one Customer ID word that are not part of the normal program memory.

Word 0	Word1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit12 ~ Bit 0

6.13.1 Code Option Register (Word 0)

Word 0													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	LVR1	LVR0	TYPE1	TYPE0	CLKS	ENWDTB	OSC2	OSC1	OSC0	–	Protect		
1	High	High	High	High	4clocks	Disable	High	High	High	–	Disable		
0	Low	Low	Low	Low	2clocks	Enable	Low	Low	Low	–	Enable		

Bits 12~11 (LVR1 ~ LVR0): Low Voltage Reset enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (Default)	
10	2.4V	2.6V
01	3.5V	3.7V
00	4.0V	4.2V

Bits 10~9 (TYPE1 ~ TYPE0): Type selection for EM78P342N.

TYPE 1, TYPE 0	MCU Type
00	Not used
01	EM78P342N-14Pin
10	EM78P342N-16Pin EM78P342N-18Pin
11	EM78P342N-20Pin (Default)

Bit 8 (CLKS): Instruction period option bit

0 = two oscillator periods

1 = four oscillator periods (default)

Refer to Section 6.15 for Instruction Set

Bit 7 (ENWDTB): Watchdog timer enable bit

0 = Enable

1 = Disable (default)

Bits 6, 5 and 4 (OSC2, OSC1 and OSC0): Oscillator Modes Selection bits

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P70/OSCO acts as P70	0	0	0
ERC[1] (External RC oscillator mode); P70/OSCO acts as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P70/OSCO acts as P70	0	1	0
IRC[2] (Internal RC oscillator mode); P70/OSCO acts as OSCO	0	1	1
LXT1[3] (Frequency range of XT, mode is 1MHz ~ 100kHz)	1	0	0
HXT1[3] (Frequency range of XT mode is 16MHz ~ 6MHz)	1	0	1
LXT2[3] (Frequency range of XT mode is 32kHz)	1	1	0
HXT2[3] (Frequency range of XT mode is 6MHz ~ 1MHz) (default)	1	1	1

[1] In ERC mode, OSCI is used as oscillator pin. OSCO/P54 is defined by code option Word 0 Bit 6 ~ Bit 4.

[2] In IRC mode, P54 is normal I/O pin. OSCO/P54 is defined by code option Word 0 Bit 6 ~ Bit 4.

[3] In LXT1, LXT2, HXT1 and HXT2 modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

Bit 3: Not used, (reserved). This bit is set to "0" all the time.

Bits 2 ~ 0 (Protect**):** Protect Bit

Protect Bits	Protect
0	Enable
1	Disable (default)

6.13.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	–	RCOUT	NRHL	NRE	–	C3	C2	C1	C0	RCM1	RCM0
1	–	–	–	System_clk	32/fc	Enable	–	High	High	High	High	High	High
0	–	–	–	Open_drain	8/fc	Disable	–	Low	Low	Low	Low	Low	Low

Bit 12: Not used, (reserved). This bit is set to "0" all the time.

Bits 11~10: Not used, (reserved). These bits are set to "1" all the time.

Bit 9 (RCOUT): Instruction clock output enable bit in IRC or ERC mode

0 : OSCO pin is open drain

1 : OSCO output instruction clock (default)

Bit 8 (NRHL): Noise rejection high/low pulses define bit. INT pin is falling or rising edge trigger

0 : Pulses equal to 8/fc is regarded as signal

1 : Pulses equal to 32/fc is regarded as signal (default)

NOTE

The noise rejection function is turned off in the LXT2 and sleep mode.

Bit 7 (NRE): Noise rejection enable

0 : disable noise rejection

1 : enable noise rejection (default), but in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bit 6: Not used, (reserved). This bit is set to "1" all the time.

Bits 5, 4, 3, and Bit 2 (C3, C2, C1, C0): Calibrator of internal RC mode

C3, C2, C1, and C0 must be set to "1" only (auto-calibration).

Bit 1 and Bit 0 (RCM1, RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (Default)
1	0	16
0	1	1
0	0	455kHz

6.13.3 Customer ID Register (Word 2)

Word 2													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	–	NRM	RESET ENB	–	WDT PS	ID5	ID4	ID3	ID2	ID1	ID0
1	–	–	–	MOD1	P71	–	18ms	High	High	High	High	High	High
0	–	–	–	MOD2	/RESET	–	4.5ms	Low	Low	Low	Low	Low	Low

Bits 12 ~ 11: Not used (reserved). These bits are set to "1" all the time.

Bit 10: Not used, (reserved). This bit is set to "0" all the time.

Bit 9 (NRM): **0 :** Noise Reject Mode 2

For multi-time circuit use, such as key scan and LED output.

1 : Noise reject Mode 1. For General input or output use **(Default)**

Bit 8 (RESETENB): RESET/P71 Pin Select Bit

0 : P71 set to /RESET pin

1 : P71 is general purpose input pin or open-drain for output Port (default)

Bit 7: Not used (reserved). This bit is set to "1" all the time.

Bit 6 (WDTPS): WDT Time-out Period Selection bit

WDT Time	Watchdog Timer*
1	18 ms (Default)
0	4.5 ms

**Theoretical values, for reference only.*

Bits 5 ~ 0: Customer's ID code

6.14 Low Voltage Detector/Low Voltage Reset

The Low Voltage Reset (LVR) and the Low Voltage Detector (LVD) are designed for unstable power situation, such as external power noise interference or in EMS test condition.

When LVR is enabled, the system supply voltage (Vdd) drops below Vdd reset level (V_{RESET}) and remains at 10μs, a system reset will occur and the system will remain in reset status. The system will remain at reset status until Vdd voltage rises above Vdd release level. Refer to Figure 6-26.

If Vdd drops below the low voltage detector level, /LVD (Bit 7 of RE) is cleared to "0' to show a low voltage signal when LVD is enabled. This signal can be used for low voltage detection.

6.14.1 Low Voltage Reset

LVR property is set at Bits 12 and 11 of Code Option Word 0. Detailed operation mode is as follows:

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVR1	LVR0	TYPE1	TYPE0	CLKS	ENWDTB	OSC2	OSC1	OSC0	–	Protect		

Bits 12~11 (LVR1 ~ LVR0): Low Voltage Reset enable bits.

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.4V	2.6V
01	3.5V	3.7V
00	4.0V	4.2V

6.14.2 Low Voltage Detector

LVD property is set and Register detailed operation mode is as follows:

6.14.2.1 IOCD1 (LVD Control Register)

Bit	7	6	5	4	3	2	1	0
EM78P342N	-	-	-	-	LVDIE	LVDEN	LVD1	LVD0
ICE341N	TYPE1	TYPE0	LVR1	LVR0	LVDIE	LVDEN	LVD1	LVD0

NOTE

- *IOCD1< 3 > register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in the IOCD1< 4 > to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*

Bit 3 (LVDIE): Low voltage Detector interrupt enable bit.

0 : Disable Low voltage Detector interrupt

1 : Enable Low voltage Detector interrupt

When the detect low level voltage state is used to enter an interrupt vector or enter next instruction, the LVDIE bit must be set to “Enable“.

Bit 2 (LVDEN): Low Voltage Detector Enable bit

0 : Low voltage detector disable

1 : Low voltage detector enable

Bits 1~0 (LVD1:0): Low Voltage Detector level bits.

LVDEN	LVD1, LVD0	LVD voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	NA	0

6.14.2.2 RE (Interrupt Status 2 and Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/LVD	LVDIF	ADIF	CMPIF	ADWE	CMPWE	ICWE	LVDWE

NOTE

- *RE < 6, 5, 4 > can be cleared by instruction but cannot be set.*
- *IOCE0 is the interrupt mask register.*
- *Reading RE will result to "logic AND" of RE and IOCE0.*

Bit 7 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0 : Low voltage is detected.

1 : Low voltage is not detected or LVD function is disabled.

Bit 6 (LVDIF): Low Voltage Detector Interrupt Flag

LVDIF reset to “0” by software or hardware.

Bit 0 (LVDWE): Low Voltage Detect Wake-up Enable bit.

0 : Disable Low Voltage Detect wake-up.

1 : Enable Low Voltage Detect wake-up.

When the Low Voltage Detect is used to enter an interrupt vector or to wake up the IC from sleep/idle with Low Voltage Detect running, the LVDWE bit must be set to “Enable“.

6.14.3 Programming Process

Follow these steps to obtain data from the LVD**:**

1. Write to the two bits (LVD1: LVD0) on the LVDCR register to define the LVD level.
2. Set the LVDWE bit, if the wake-up function is employed.
3. Set the LVDIE bit, if the interrupt function is employed.
4. Write “ENI” instruction, if the interrupt function is employed.
5. Set LVDEN bit to 1
6. Write “SLEP” instruction or Polling /LVD bit.
7. Clear the low voltage detector interrupt flag bit (LVDIF) when Low Voltage Detector interrupt occurred.

The LVD module uses the internal circuit. When LVDEN (Bit 2 of IOCD1) is set to “1”, the LVD module is enabled.

When LVDWE (Bit 0 of RE) is set to “1”, the LVD module will continue to operate during sleep/idle mode. If Vdd drops slowly and crosses the detect point (V**LVD**), the LVDIF (Bit 6 of RE) will be set to ”1”, the /LVD (Bit 7 of RE) will be cleared to “0”, and the system will wake up from Sleep/Idle mode. When a system reset occurs, the LVDIF will be cleared.

When Vdd remains above VLVD, LVDIF is kept at “0” and /LVD is kept at “1”. When Vdd drops below VLVD, LVDIF is set to “1” and /LVD is kept at “0”. If ENI instruction is executed, LVDIF will be set to “1”, and the next instruction will branch to interrupt Vector 021H. The LVDIF is cleared to “0” by software. Refer Figure 6-26 below.

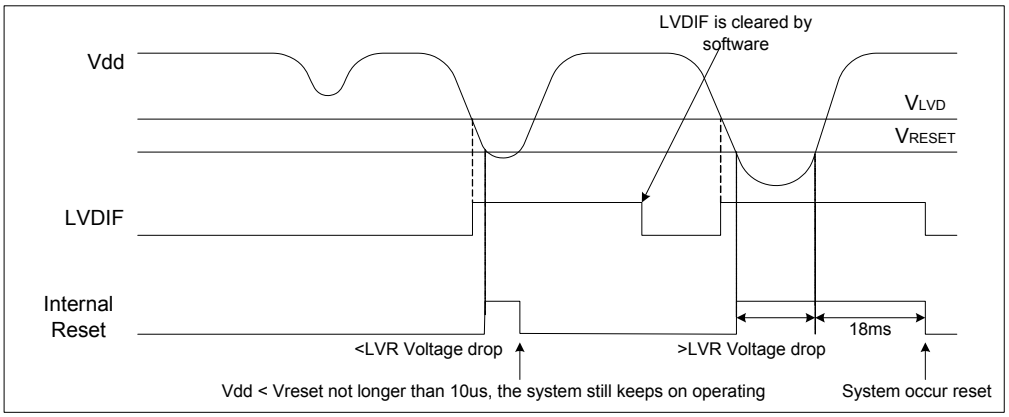


Figure 6-26 LVD/LVR Waveform Situation

6.15 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator time periods), unless the program counter is changed by instructions "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.).

In addition, the instruction set has the following features:

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

The following symbols are used in the Instruction Set table:

Convention:

R = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*
Bits 6 and 7 in R4 determine the selected register bank.

b = *Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k = *8 or 10-bit constant or literal value*

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 1001 000k	1E9k	BANK k	k →R4(6)	None
1 1110 1010 kkkk k kkkk kkkk kkkk	1EAK	LCALL k	PC+1→[SP], k→PC	None
1 1110 1011 kkkk k kkkk kkkk kkkk	1EBK	LJMP k	k→PC	None

Note: *[1] This instruction is applicable to IOC50~IOCF0, IOC51 ~ IOCF1 only.*
[2] This instruction is not recommended for RF operation.
[3] This instruction cannot operate under RF.

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.3V	to	5.5V
Working Frequency	DC	to	16 MHz

8 DC Electrical Characteristics

Ta= 25°C, VDD= 5.0V, VSS= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768k	4	16	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	760	950	1140	kHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7	0.7Vdd	–	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7	-0.3V	–	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7Vdd	–	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	–	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC,INT	0.7Vdd	–	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC,INT	-0.3V	–	0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5, 6, 7)	VOH = 0.9VDD	–	-10	–	mA
IOL1	Output Low Voltage (Ports 5, 6,7)	VOL = 0.1VDD	–	20	–	mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOL2	Output Low Voltage (Ports 60, 61,62, 63)	VOL = 0.3VDD	–	70	–	mA
LVR1	Low voltage reset level	Ta = 25°C	–	2.4	–	V
		Ta = -40 ~ 85°C	–	2.4	–	V
LVR2		Ta = 25°C	3.1	3.5	3.92	V
		Ta = -40 ~ 85°C	2.73	3.5	4.25	V
LVR3		Ta = 25°C	3.56	4.0	4.43	V
		Ta = -40 ~ 85°C	3.16	4.0	4.81	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	–	-90	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	20	–	60	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	–	–	2.0	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled	–	–	10	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	15	20	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type,CLKS="0"), output pin floating, WDT enabled	–	15	25	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	–	1.5	1.7	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	2.8	3.0	mA

Note: *1. These parameters are hypothetical (not tested) and are provided for design reference use only.*

2. Data under Minimum, Typical, and Maximum (Min, Typ, and Max) columns are based on hypothetical results at 25°C. These data are for design reference only.

Internal RC Electrical Characteristics (Ta=25°C, VDD=5 V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.84 MHz	4 MHz	4.16 MHz
16 MHz	25°C	5V	15.36 MHz	16 MHz	16.64 MHz
1 MHz	25°C	5V	0.96 MHz	1 MHz	1.04 MHz
455kHz	25°C	5V	436.8kHz	455kHz	473.2kHz

Internal RC Electrical Characteristics (Ta=-40 ~85°C, VDD=2.2~5.5 V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40°C ~85°C	2.2V~5.5V	3.44 MHz	4 MHz	4.56 MHz
16 MHz	-40°C ~85°C	2.2V~5.5V	13.76 MHz	16 MHz	18.24 MHz
1 MHz	-40°C ~85°C	2.2V~5.5V	0.86 MHz	1 MHz	1.14 MHz
455kHz	-40°C ~85°C	2.2V~5.5V	391.3kHz	455kHz	518.7kHz

8.1 AD Converter Characteristics

Vdd=2.5V to 5.5V, Vss=0V, Ta=-40 to 85°C

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from Vdd)	750	850	1000	μA
	Ivref			-10	0	+10	μA
IAI2	Ivdd	Analog supply current	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from VREF)	500	600	820	μA
	IVref			200	250	300	μA
IOP		OP current	VDD=5.0V, OP used Output voltage swing from 0.2V to 4.8V	450	550	650	μA
RN1		Resolution	ADREF=0, Internal VDD VDD=5.0V, VSS = 0.0V	–	9	–10	Bits
RN2		Resolution	ADREF=1, External VREF VDD=VREF=5.0V, VSS = 0.0V	–	11	12	Bits
LN1		Linearity error	VDD = 2.5 to 5.5V Ta=25°C	0	± 4	±8	LSB
LN2		Linearity error	VDD= 2.5 to 5.5V Ta=25°C	0	± 2	±4	LSB
DNL		Differential nonlinear error	VDD = 2.5 to 5.5V Ta=25°C	0	± 0.5	±0.9	LSB
FSE1		Full scale error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	±0	± 4	±8	LSB
FSE2		Full scale error	VDD=VREF=5.0V, VSS = 0.0V	±0	± 2	±4	LSB
OE		Offset error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	±0	± 2	±4	LSB
ZAI		Recommended impedance of analog voltage source	–	0	8	10	KΩ
TAD		ADC clock duration	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	4	–	–	μs
TCN		AD conversion time	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	15	–	15	TAD
ADIV		ADC OP input voltage range	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	0	–	V_{AREF}	V
ADOV		ADC OP output voltage swing	VDD=V_{AREF}=5.0V, V_{ASS} =0.0V, RL=10KΩ	0	0.2	0.3	V
				4.7	4.8	5	
ADSR		ADC OP slew rate	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	0.1	0.3	–	V/μs
PSR		Power Supply Rejection	VDD=5.0V±0.5V	±0	–	±2	LSB

Note: *1. These parameters are hypothetical (not tested) and provided for design reference use only.*

2. There is no current consumption when ADC is off other than minor leakage current.

3. AD conversion result will not decrease when an increase of input voltage and no missing code will result.

4. These parameters are subject to change without further notice.

8.2 Comparator (OP) Characteristics

Vdd = 5.0V, Vss=0V, Ta=-40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SR	Slew rate	–	0.1	0.2	–	V/us
Vos	Input offset voltage	–	–	–	10	mV
IVR	Input voltage range	Vdd =5.0V, V_{SS} = 0.0V	0	–	5	V
OVS	Output voltage swing	Vdd =5.0V, V_{SS} = 0.0V, RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
Iop	Supply current of OP	–	250	350	500	μA
Ico	Supply current of Comparator	–	–	300	–	μA
PSRR	Power-supply Rejection Ratio for OP	Vdd= 5.0V, V_{SS} = 0.0V	50	60	70	dB
Vs	Operating range	–	2.5	–	5.5	V

Note: *1. These parameters are hypothetical (not tested) and provided for design reference use only.*

2. These parameters are subject to change without further notice.

8.3 Device Characteristics

The graphs below were derived based on a limited number of samples and they are provided for reference only. Hence, the device characteristic shown herein cannot be guaranteed as fully accurate. In these graphs, the data may be out of the specified operating warranted range.

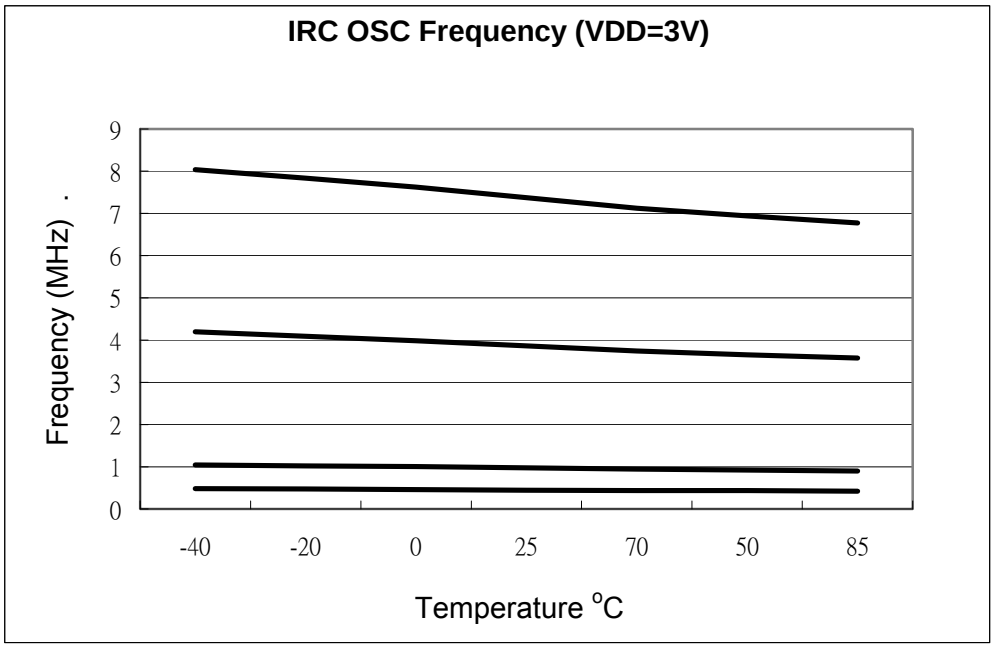


Figure 8-1 Internal RC OSC Frequency vs. Temperature, VDD=3V

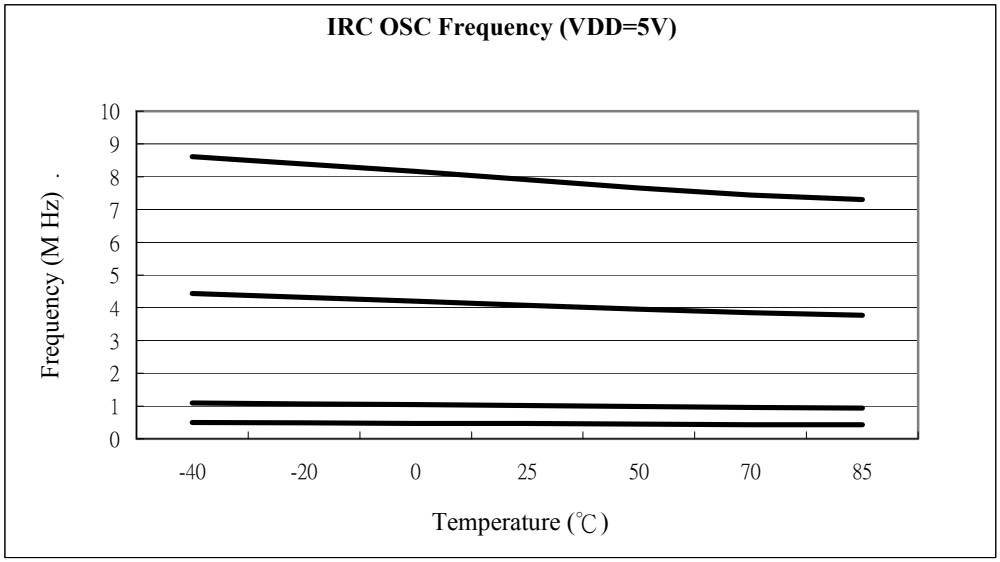


Figure 8-2 Internal RC OSC Frequency vs. Temperature, VDD=5V

9 AC Electrical Characteristics

Ta=-40 to 85°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input time period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer duration	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns
Tdrc	ERC delay time	Ta = 25°C	1	3	5	ns

Note: *1. *N = selected prescaler ratio*

2. Twdt1: The Option Word 1 (WDTPS) is used to define the oscillator set-up time. WDT timeout length is the same as set-up time (18ms).

3. Twdt2: The Option word1 (WDTPS) is used to define the oscillator set-up time. WDT timeout length is the same as set-up time (4.5ms).

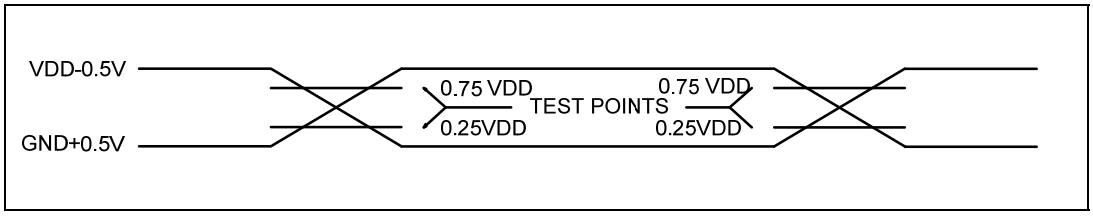
4. These parameters are hypothetical (not tested) and are provided for design reference only.

5. Data under Minimum, Typical, and Maximum (Min., Typ., and Max.) columns are based on hypothetical results at 25°C. These data are for design reference use only.

6. The Watchdog timer duration is determined by Code Option Word1 (WDTPS).

10 Timing Diagrams

AC Test Input/Output Waveform



Note: *AC Testing: Input is driven at VDD-0.5V for logic "**1**", and GND+0.5V for logic "**0**"*
*Timing measurements are made at 0.75V for logic "**1**", and 0.25VDD for logic "**0**"*

Figure 10-1a AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK = "0")

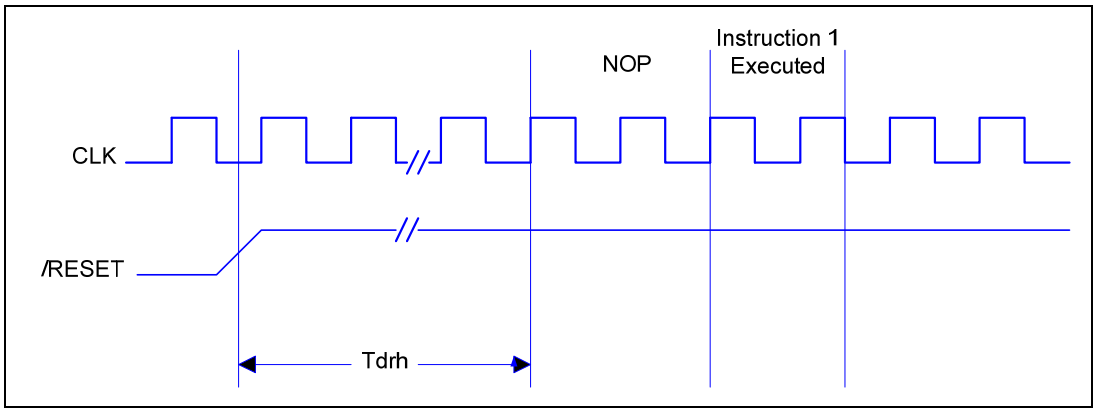


Figure 10-1b Reset Timing Diagram

TCC Input Timing (CLKS = "0")

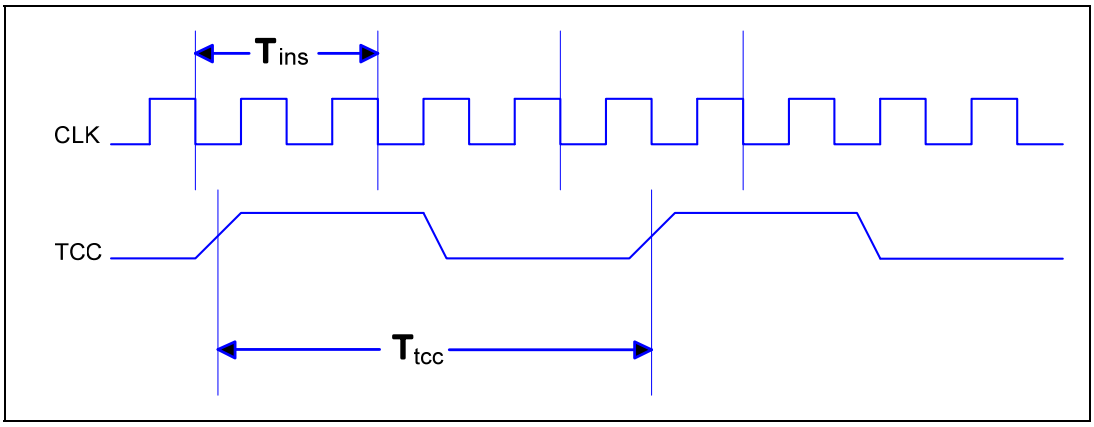


Figure 10-1c TCC Input Timing Diagram

APPENDIX

A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P342ND14J/S	DIP	14	300 mil
EM78P342NSO14J/S	SOP	14	150 mil
EM78P342NSO16AJ/S	SOP	16	150 mil
EM78P342ND18J/S	DIP	18	300 mil
EM78P342NSO18J/S	SOP	18	300 mil
EM78P342ND20J/S	DIP	20	300 mil
EM78P342NSO20J/S	SOP	20	300 mil
EM78P342NSS20J/S	SSOP	20	209 mil

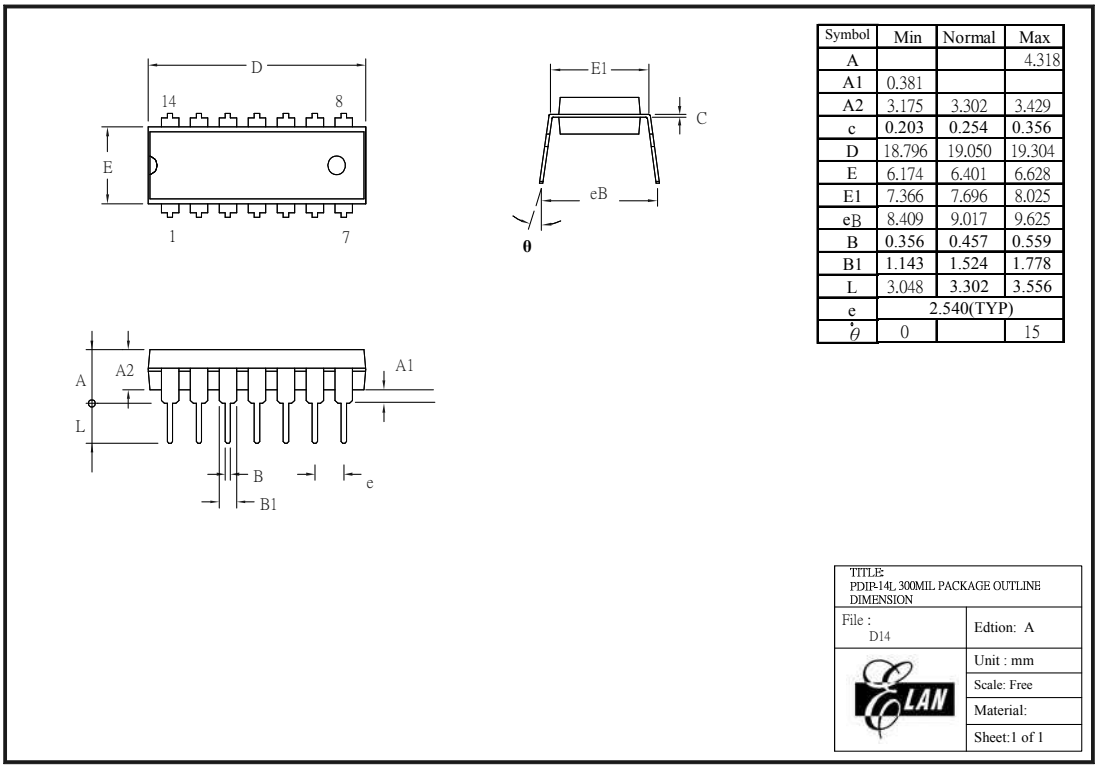
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78P342NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Packaging Configuration

B.1 EM78P342ND14

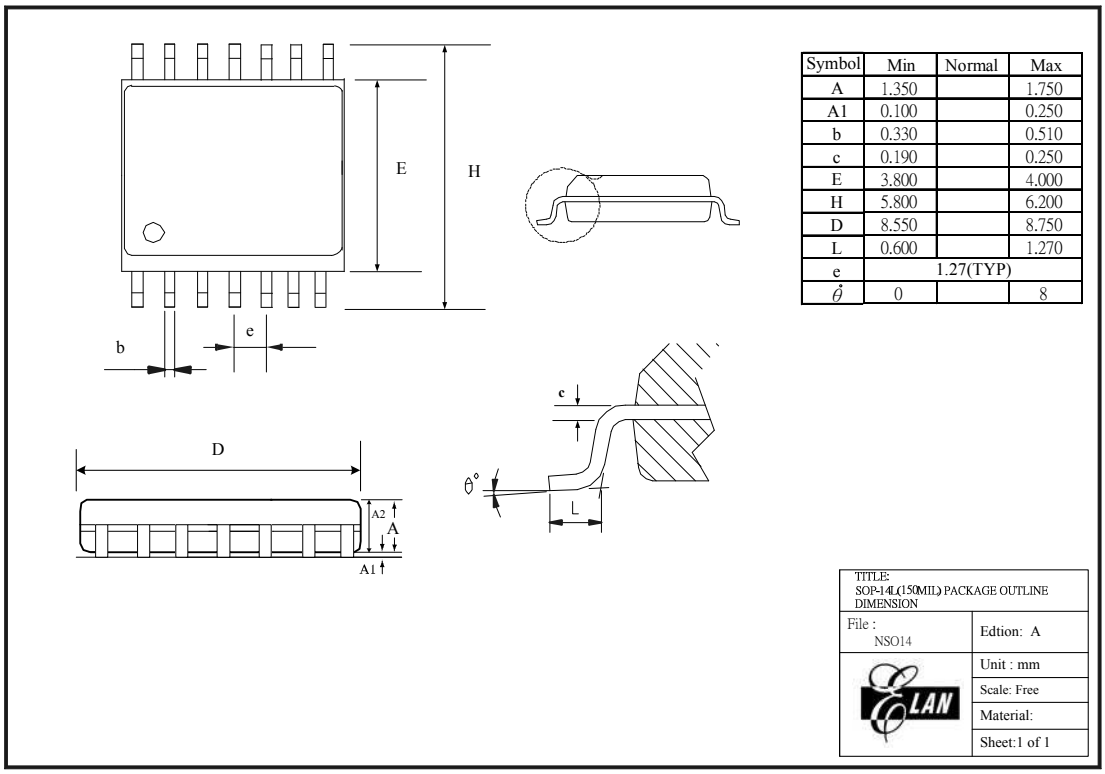


Symbol	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	18.796	19.050	19.304
E	6.174	6.401	6.628
E1	7.366	7.696	8.025
eB	8.409	9.017	9.625
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-14L 300MIL PACKAGE OUTLINE DIMENSION	
File : D14	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78P342N 14-pin PDIP Package Type

B.2 EM78P342NSO14



Symbol	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e	1.27(TYP)		
θ	0		8

TITLE:
SOP-14L(150MIL) PACKAGE OUTLINE DIMENSION

File : NSO14 | Edtion: A

Unit : mm

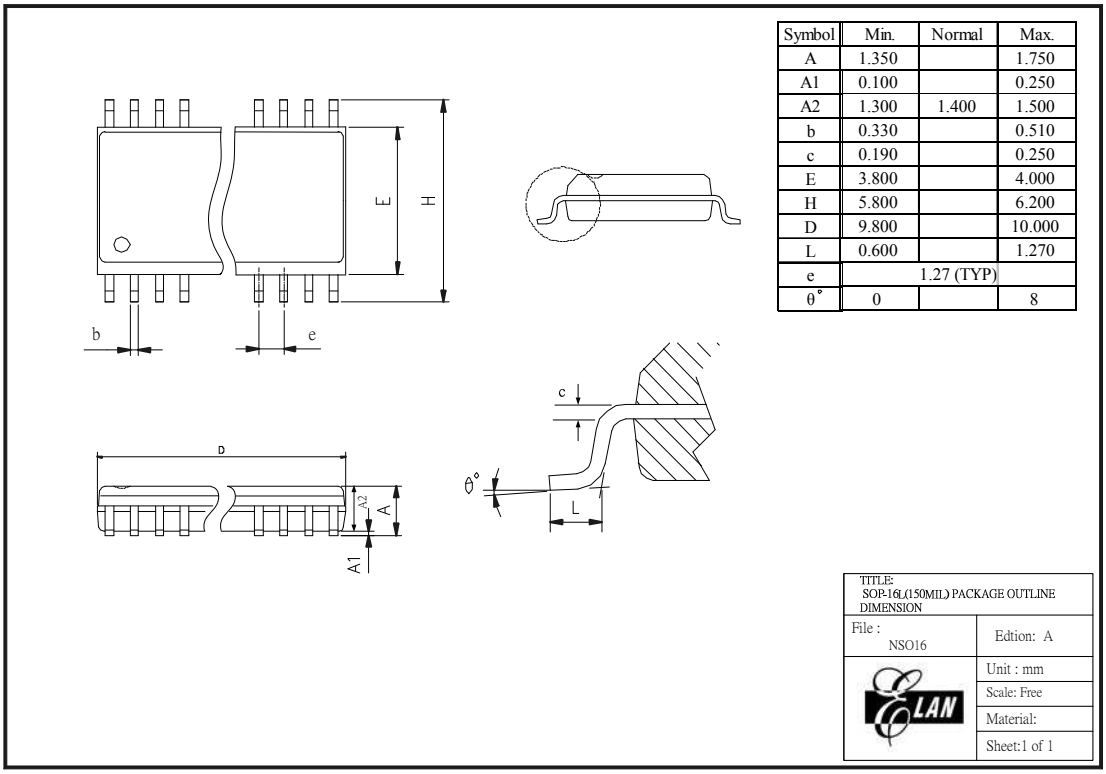
Scale: Free

Material:

Sheet:1 of 1

Figure B-2 EM78P342N 14-pin SOP Package Type

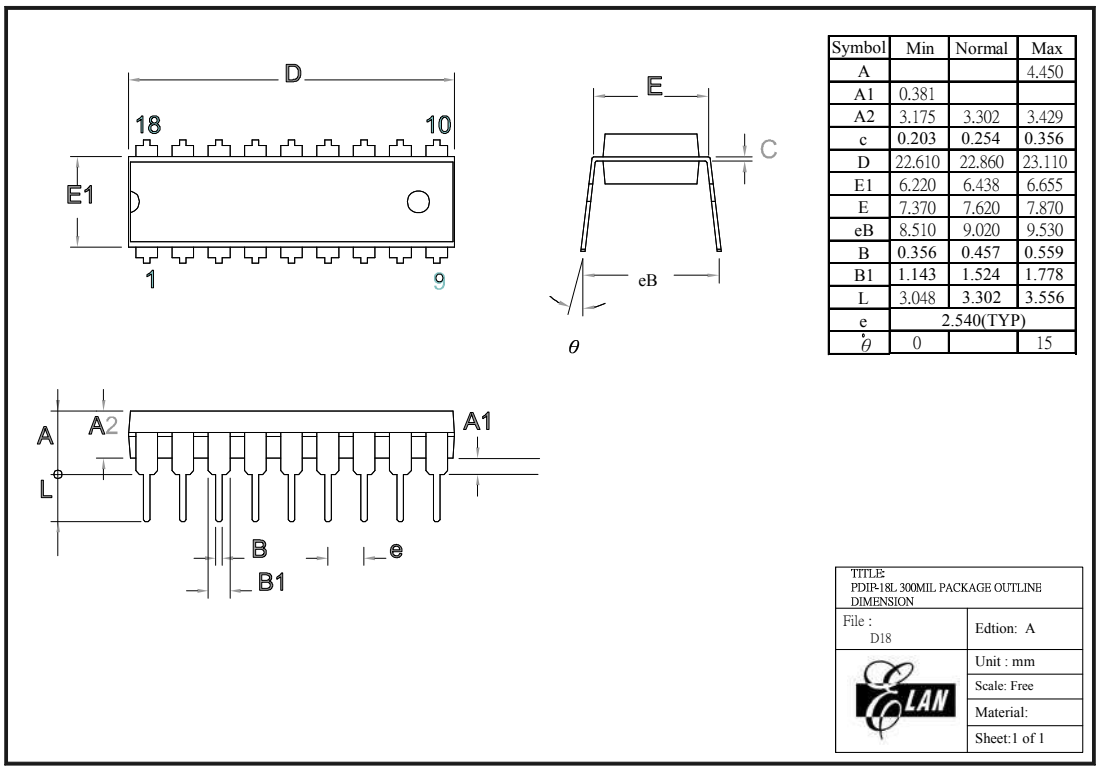
B.3 EM78P342NSO16A



Symbol	Min.	Normal	Max.
A	1.350		1.750
A1	0.100		0.250
A2	1.300	1.400	1.500
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	9.800		10.000
L	0.600		1.270
e		1.27 (TYP)	
θ°	0		8

Figure B-3 EM78P342N 16-pin SOP Package Type

B.4 EM78P342ND18

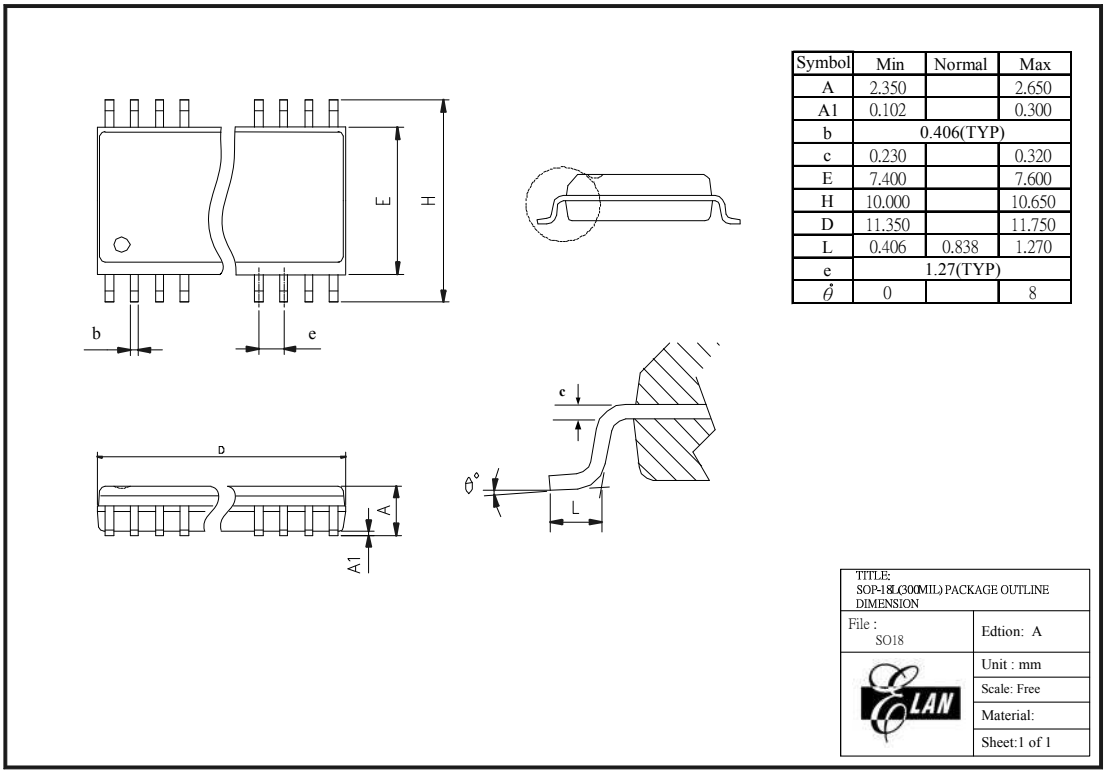


Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-18L 300MIL PACKAGE OUTLINE DIMENSION	
File : D18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-4 EM78P342N 18-pin PDIP Package Type

B.5 EM78P342NSO18



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e		1.27(TYP)	
θ	0		8

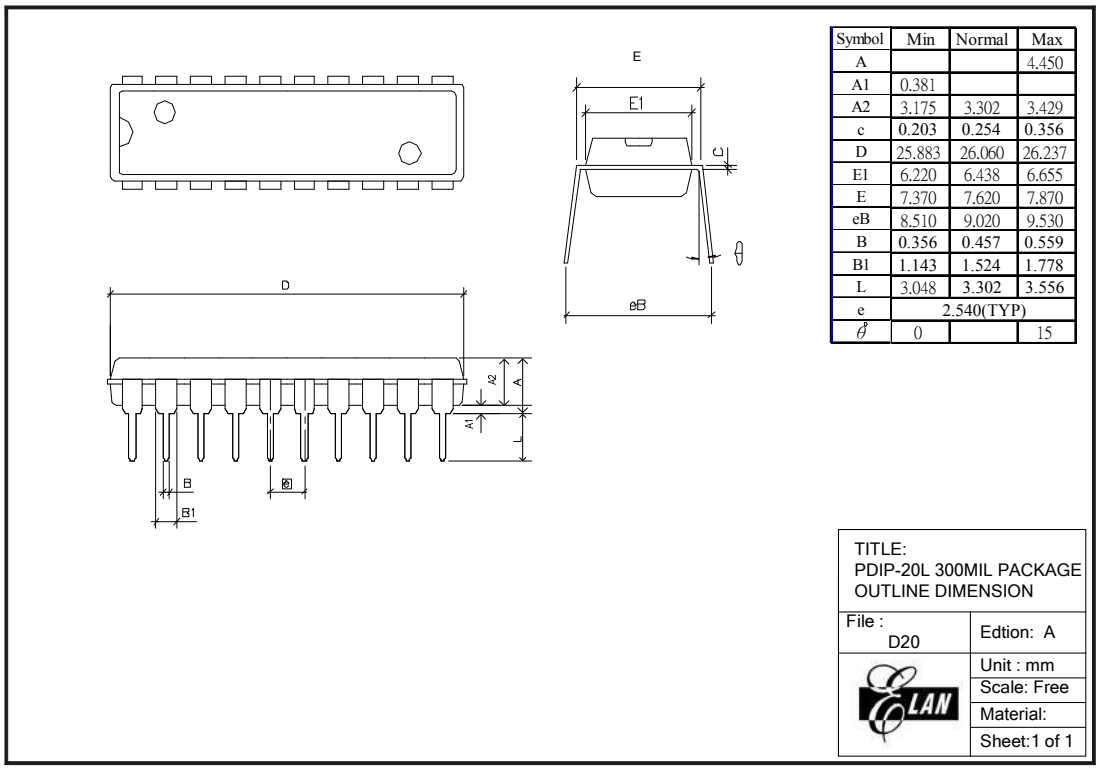
TITLE:
SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION

File : SO18 | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure B-5 EM78P342N 18-pin SOP Package Type

B.6 EM78P342ND20

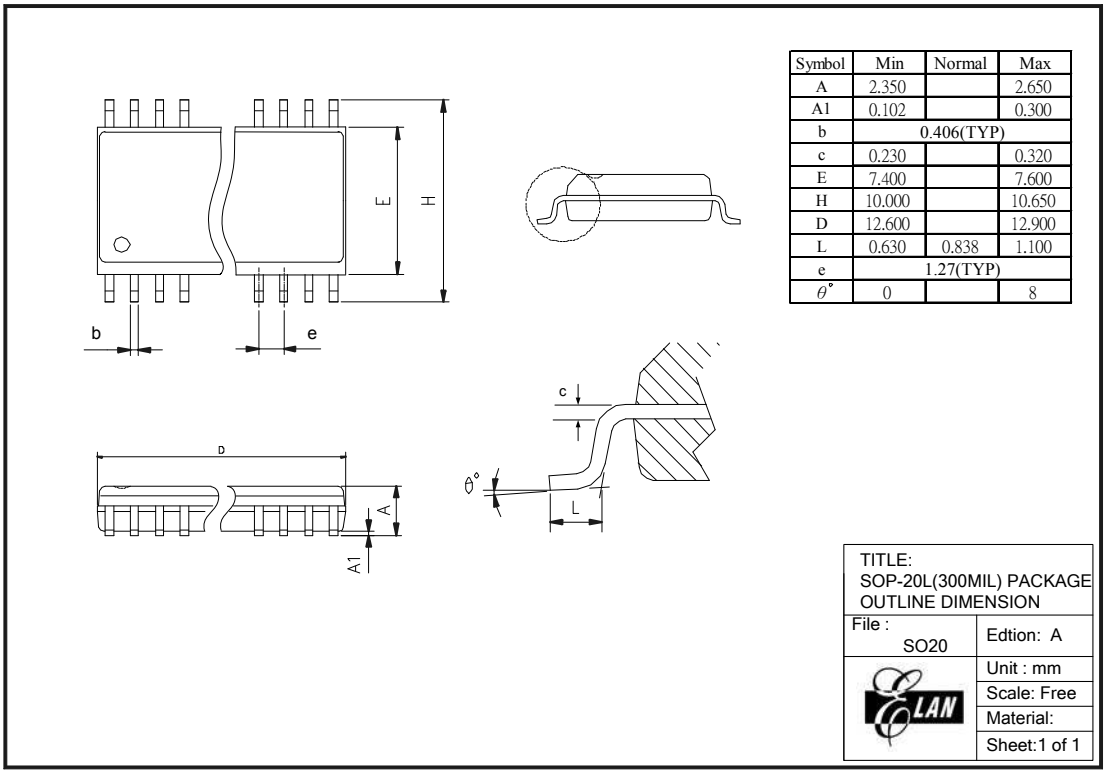


Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

TITLE: PDIP-20L 300MIL PACKAGE OUTLINE DIMENSION	
File : D20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-6 EM78P342N 20-pin PDIP Package Type

B.7 EM78P342NSO20

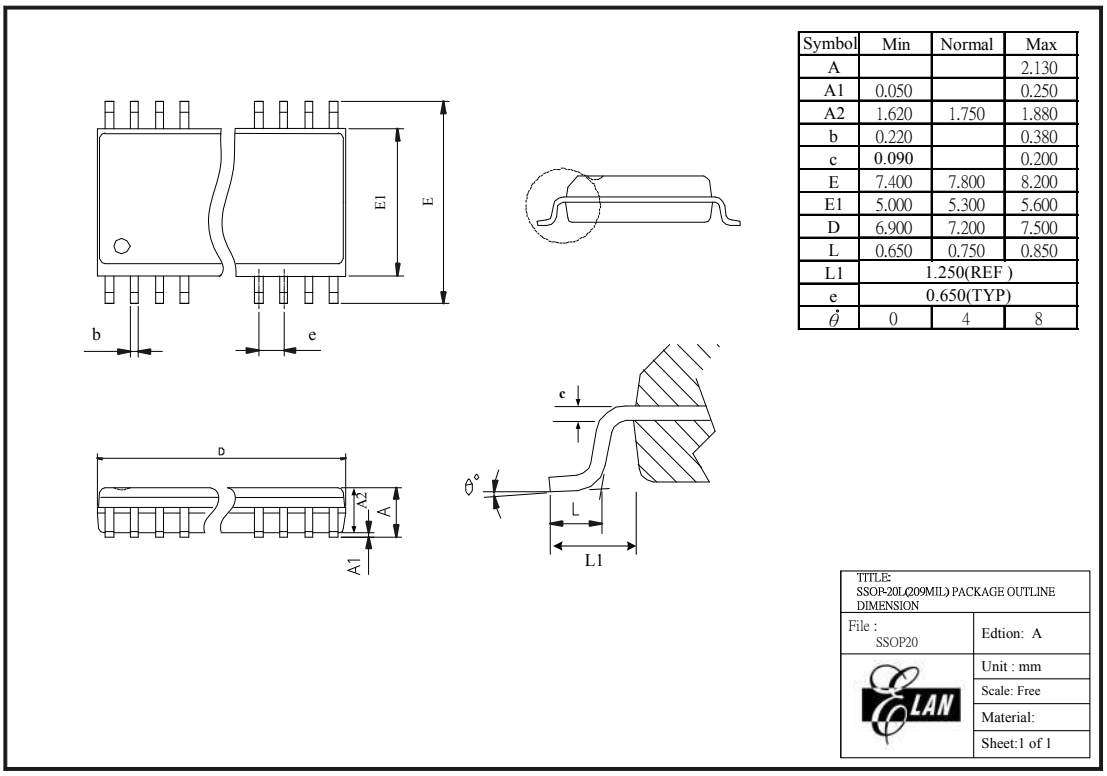


Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-7 EM78P342N 20-pin SOP Package Type

B.8 EM78P342NSS20



Symbol	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250(REF)		
e	0.650(TYP)		
θ	0	4	8

TITLE: SSOP-20L(209MIL) PACKAGE OUTLINE DIMENSION

File : SSOP20 | Edtion: A

Unit : mm

Scale: Free

Material:

Sheet:1 of 1

Figure B-8 EM78P342N 20-pin SSOP Package Type

C Quality Assurance and Reliability

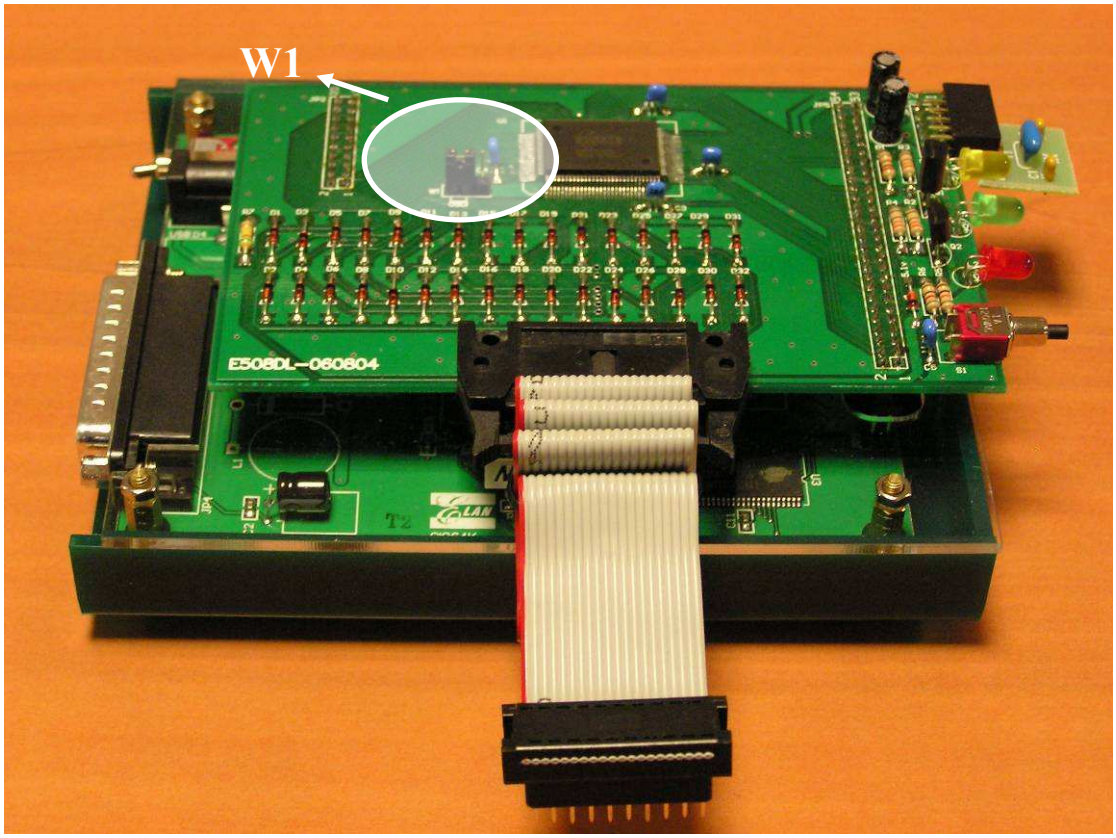
Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15mins)~150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (durance)=24 hrs	
	Step 3: Soak at 30°C /60% , TD (durance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm^3 ----225 ± 5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm^3 ----240 ± 5°C)	
Temperature cycle test	-65° (15mins)~150°C (15mins), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (durance) = 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85% , TD (durance)=168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (durance)=500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC=Max. operating voltage, TD (durance) =168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC=Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥ | ± 3KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-)mode
ESD (MM)	TA=25°C, ≥ | ± 300V |	

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.

D How to Use the ICE 341N

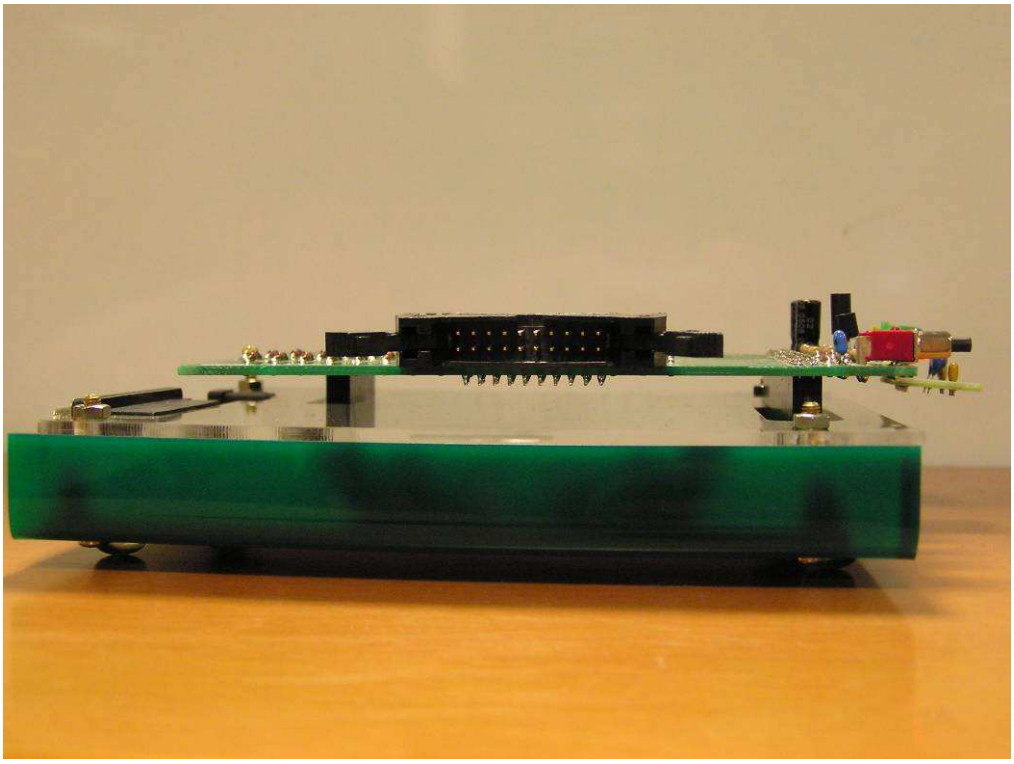
ICE 341 for EM78P342N



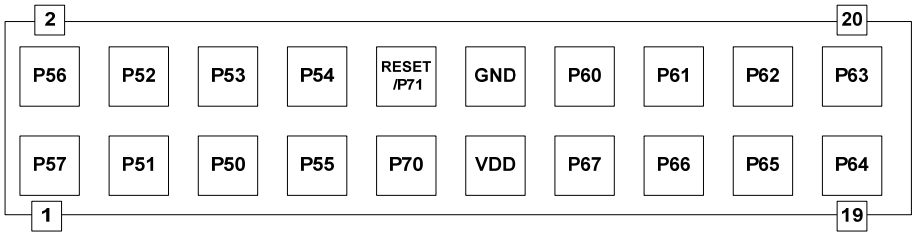
W1	P55/OSCI Pin Select
OSCI P55 	I/O Port (P55)
OSCI P55 	Crystal, ERC (OSCI)

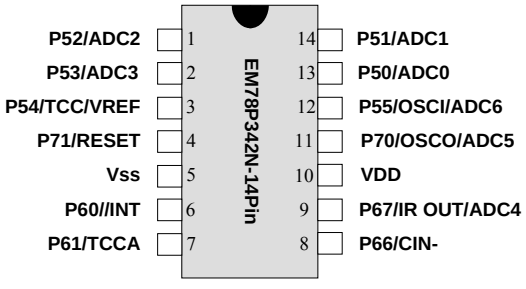
Oscillator IRC Modes select **I/O Port (P55)**

Oscillator Crystal, ERC Modes select **Crystal (OSCI)**

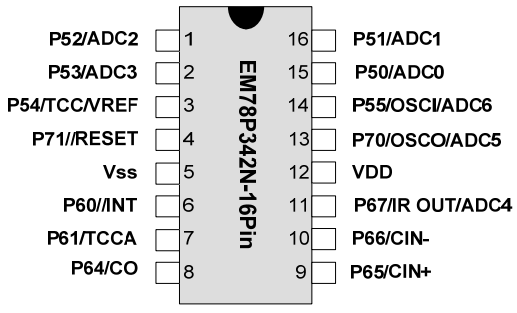


JP3

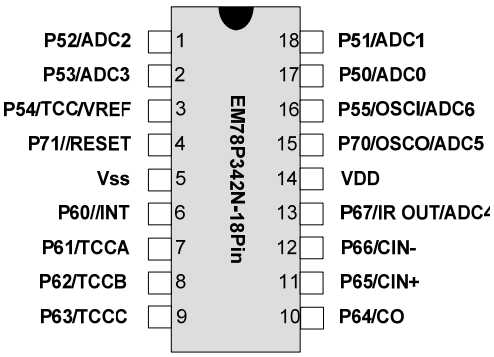




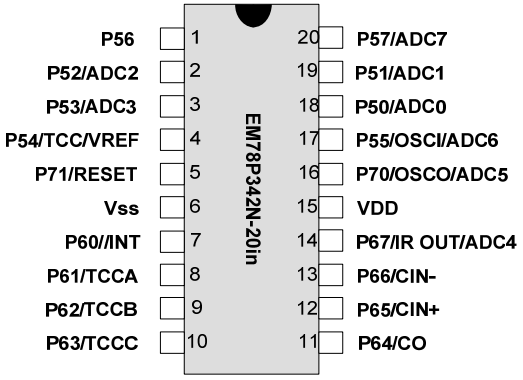
EM78P342ND14/SO14



EM78P342NSO16A

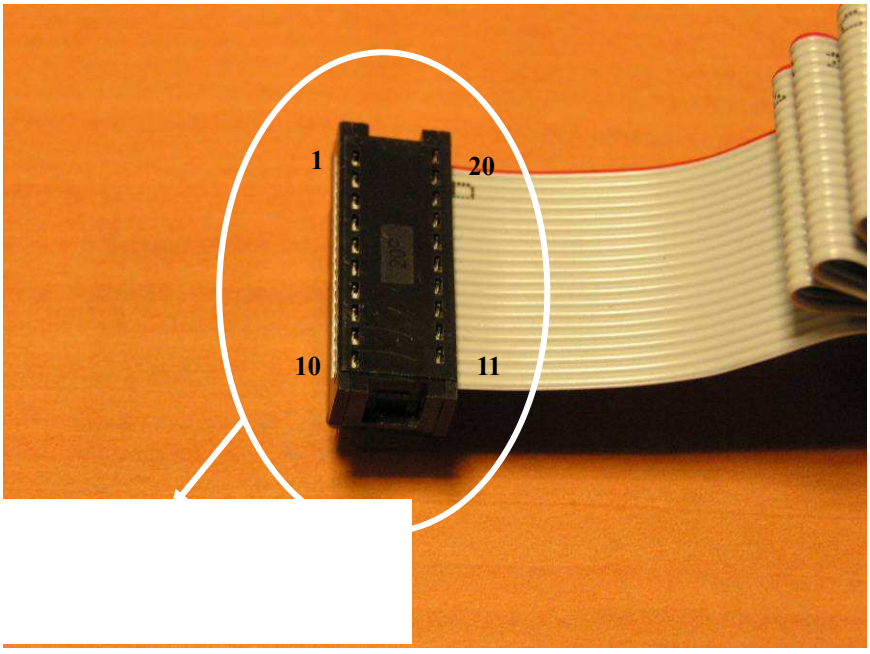


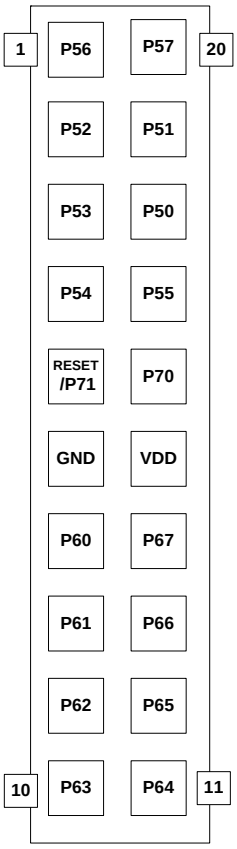
EM78P342ND18/SO18



EM78P342ND20/SO20/SS20

DIP IDC PLUG

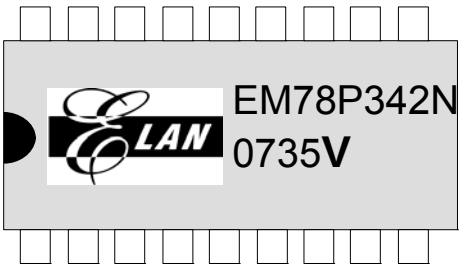




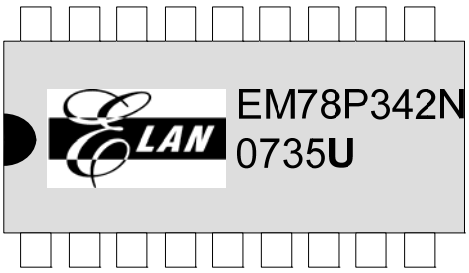
E Comparison between V-Package and U-Package Versions

This microcontroller device is comprised of the older V-package version and the newer U-package version. In the newer U-package version, a Code Option NRM is added and various features such as Crystal mode Operating frequency range and IRC mode wake-up time from sleep mode to normal mode, have been modified to favorably meet users' requirements. The following table is provided for quick comparison between the two package version and for user convenience in the choice of the most suitable product for their application.

Item	EM78P342N-V	EM78P342N-U
Level Voltage Reset	4.0V, 3.5V, 2.7V	4.0V, 3.5V, 2.4V
Crystal mode Operating frequency range at 0°C~ 70°C	DC ~ 12 MHz, 4.5V DC ~ 8 MHz, 3.0V DC ~ 4 MHz, 2.1V	DC ~ 16 MHz, 4.5V DC ~ 8 MHz, 3.0V DC ~ 4 MHz, 2.1V
IRC mode wake-up time (Sleep → Normal) Condition: 5V, 4MHz	80μs	10μs
Code Option	×	Added a Code Option NRM



EM78P342N-V Package



EM78P342N-U Package