
EM78P220N

**8-Bit Microcontroller
with OTP ROM**

Product Specification

DOC. VERSION 1.3


ELAN MICROELECTRONICS CORP.

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Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2007/03/20
1.0	Initial released version	2007/10/19
1.1	Renamed the Product as EM78P220N from EM78P221N, EM78P222N	2008/01/24
1.2	*1. Retrieved ICE220N, Updated with ICE210N. *2. For ICE210N and EM78P220N, added Green mode and Idle mode.	2008/04/23
1.3	Added LVR specifications	2013/04/22

*ICE210N vs ICE220N Comparison Table

Item	ICE220N	ICE210N
P72, P73 Function (when used as output pins)	Open drain pins	General Output pins
P81 Function (when used as output pins)	General Output pins	Open drain pins
Port 6 High Drive Function	×	o
Port 5 High Sink Function	×	o
Port 6 High Sink Function	×	o
Type Selection in Bank 3-R7 Register	×	o
Operating Mode	Sleep, Normal	Sleep, Idle, Green, Normal

Note: “o” = function is available if enabled “x” = function is not available



1 General Description

The EM78P220N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has as an on-chip 4K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Two Code option bits are also available to meet user's requirements.

With its enhanced OTP-ROM features, the device provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development code.

2 Features

- CPU configuration
 - 4K×13 bits on-chip OTP-ROM
 - 144×8 bits on-chip registers (SRAM)
 - 8-level stacks for subroutine nesting
 - 3 programmable Level Voltage Reset (LVR) : 4.0V, 3.0V, 2.5V
 - Less than 1.5 mA at 5V/4MHz
 - Typically 15 μ A, at 3V/32kHz
 - Typically 2 μ A, during sleep mode
- I/O port configuration
 - Four bidirectional I/O ports: P5, P6, P7 and P8
 - Wake-up port : P6
 - 26 I/O pins
 - Eight programmable pull-down I/O pins
 - Eight programmable pull-high I/O pins
 - Eight programmable open-drain I/O pins
 - Eight Programmable high drive current I/O pins
 - 16 Programmable high sink current I/O pins
 - External interrupt : P77, P71
- Operating voltage range:
 - OTP version:
 - Operating voltage: 2.1V~5.5V (commercial)
 - Operating voltage: 2.3V~5.5V (industrial)
- Operating temperature range:
 - Operating temperature: 0°C~70°C (commercial)
 - Operating temperature: -40°C~85°C (industrial)
- Operating frequency range
 - Crystal mode:
 - DC~16 MHz/2 clks @ 4.5V; DC~125ns inst. cycle @ 4.5V
 - DC~8 MHz/2 clks @ 3V; DC~250ns inst. Cycle @ 3V
 - ERC mode:
 - DC~16 MHz/2 clks @ 4.5V; DC~125ns inst. cycle @ 5V
 - DC~8 MHz/2 clks @ 3V; DC~250ns inst Cycle @ 3V
 - IRC mode:
 - Oscillation mode: 16MHz, 4 MHz, 1 MHz, 455kHz
 - Process deviation: Typ \pm 3%, Max. \pm 5%
 - Temperature deviation: \pm 5% (-40°C~85°C)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~85°C)	Voltage (2.1V~5.5V)	Process	Total
4 MHz	\pm 5%	\pm 5%	\pm 4%	\pm 14%
16 MHz	\pm 5%	\pm 5%	\pm 4%	\pm 14%
1 MHz	\pm 5%	\pm 5%	\pm 4%	\pm 14%
455kHz	\pm 5%	\pm 5%	\pm 4%	\pm 14%

All the four main frequencies can be trimmed by programming with four calibrated bits in the ICE210N Simulator. OTP is auto trimmed by ELAN Writer (DWTR).

- Fast set-up time requires only 800 μ s (VDD:5V, Crystal: 4MHz, C1/C2: 30pF) in HXT2 mode and 10 μ s in IRC mode (VDD: 5V IRC: 4 MHz)
- Peripheral configuration
 - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
 - One comparator (can act as an OP) (offset voltage is smaller than 10mV)
- Five available interrupts
 - TCC overflow interrupt
 - Input-port status changed interrupt (wake up from sleep mode)
 - Two External interrupts
 - Comparator high/low interrupt
- Special Features
 - Programmable free running Watchdog Timer
 - Two clocks per instruction cycle
 - Power-on voltage detector available (1.8 V \pm 0.1V)
 - High EFT immunity (better performance at 4MHz or below)
 - Power saving Sleep mode
 - Selectable Oscillation mode
- Package Type:
 - 24-pin skinny DIP 300mil : EM78P220NK24J/S
 - 24-pin SOP 300mil : EM78P220NSO24J/S
 - 24-pin SSOP 209mil : EM78P220NSS24AJ/S
 - 28-pin skinny DIP 300mil : EM78P220NK28J/S
 - 28 pin SOP 300mil : EM78P220NSO28J/S
 - 28 pin SSOP 209mil : EM78P220NSS28J/S

Note: Green products do not contain hazardous substances.

3 Pin Assignment

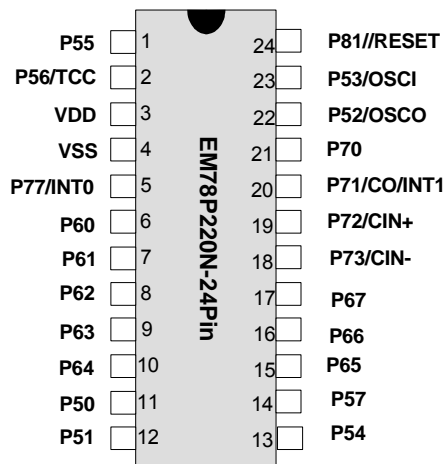


Figure 3-1 EM78P220NK24/SO24/SS24A

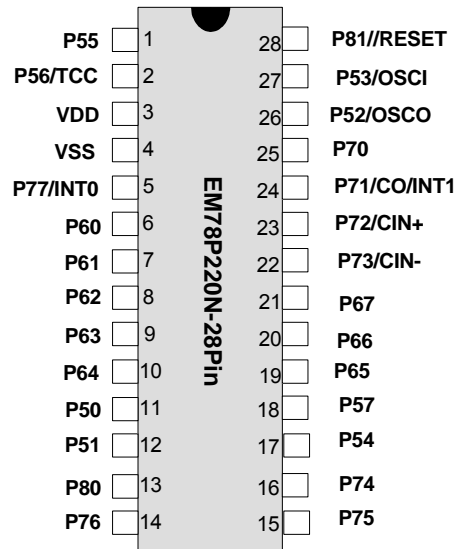


Figure 3-2 EM78P220NK28/SO28/SS28



4 Pin Description

4.1 EM78P220NK24/SO24/SS24A

Symbol	Pin No.	Type	Function
P50~P57	1~2 11~14 22~23	I/O	8-bit General purpose input/output pins. Pull-high (P50~P53) / Open-drain function. High sink function. Default value at power-on reset.
P60~P67	6 ~ 10 15~17	I/O	8-bit General purpose input/output pins. Pull-high (P64~P67) / Pull-down function. High drive / High sink function. Wake-up from sleep mode when the pin status changes. Default value at power-on reset.
P70~P73 P77	21 ~ 18 5	I/O	5-bit General purpose input/output pins. Default value at power-on reset.
P81	24	I/O	1-bit General purpose input or output open-drain pin. Default value at power-on reset.
CIN- CIN+ CO	18 19 20	I I O	"-" : input pin of Vin- of the comparator "+" : input pin of Vin+ of the comparator Pin CO is the comparator output Defined by CMPCON (Bank 1-RA) <3:4>
OSCI	23	I	Crystal type: Crystal input terminal RC type: RC oscillator input pin
OSCO	22	O	Crystal type: Output terminal for crystal oscillator. RC type: Clock output with a duration of one instruction cycle time. External clock signal input.
/RESET	24	I	If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
INT0~INT1	5, 20	I	External interrupt pin
VDD	3	-	Power supply
VSS	4	-	Ground

4.2 EM78P220NK28SO28/SS28

Symbol	Pin No.	Type	Function
P50~P57	1~2 11~12 17~18 26~27	I/O	8-bit General purpose input/output pins. Pull-high (P50~P53) / Open-drain function. High sink Function. Default value at power-on reset.
P60~P67	6 ~ 10 19 ~21	I/O	8-bit General purpose input/output pins. Pull-high (P64~P67) / Pull-down function. High drive / High sink function. Wake up from sleep mode when the pin status changes. Default value at power-on reset.
P70~P77	5 14 ~ 16 22~25	I/O	8-bit General purpose input/output pins. Default value at power-on reset.
P80, P81	13, 28	I/O	2-bit General purpose input or output open-drain pin. Default value at power-on reset. P81 is define as General purpose input or output open-drain pin.
CIN- CIN+ CO	22 23 24	I I O	"-" : input pin of Vin- of the comparator "+" : input pin of Vin+ of the comparator Pin CO is the comparator output. Defined by CMPCON (Bank 1-RA) <3:4>
OSCI	27	I	Crystal type: Crystal input terminal RC type: RC oscillator input pin
OSCO	26	O	Crystal type: Output terminal for crystal oscillator. RC type: Clock output with a duration of one instruction cycle time. External clock signal input.
/RESET	28	I	If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
INT0~INT1	5, 24	I	External interrupt pin
VDD	3	-	Power supply
VSS	4	-	Ground

5 Block Diagram

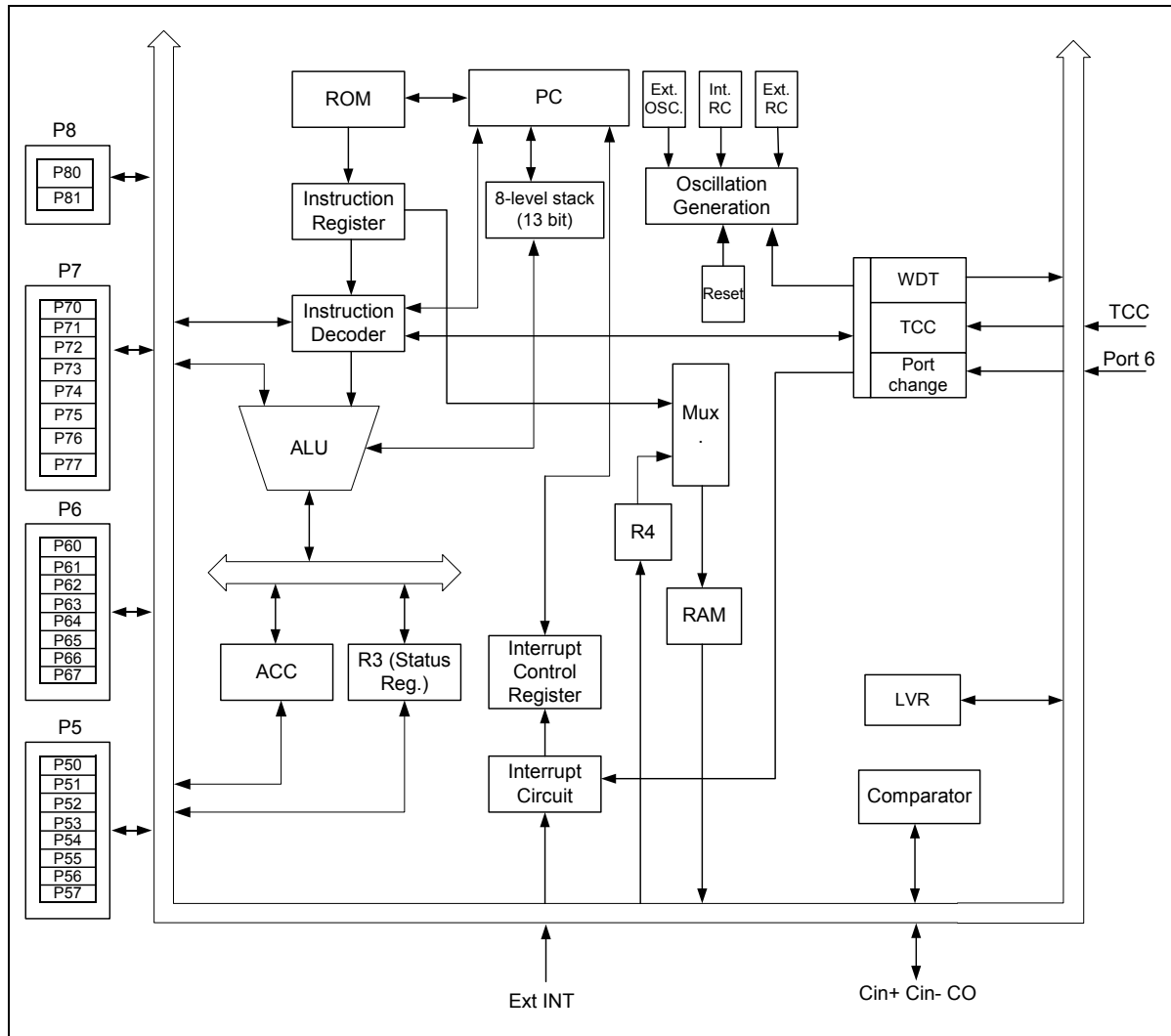


Figure 5 EM78P220N Functional Block Diagram

6 Functional Description

6.1 Register Configuration

Addr	Bank 0 Registers	Bank 1 Registers	Bank 2 Registers	Bank 3 Registers
00	R0 (Indirect Addressing Register)			
01	R1 (Memory switch register)			
02	R2 (Program Counter)			
03	R3 (Status Register)			
04	R4 (Select Indirect Address)			
05	R5 (Port 5)	R5 (I/O Port Control Register)	R5 (High Drive Control Register for Port 6)	R5 (Time Clock / Counter)
06	R6 (Port 6)	R6 (I/O Port Control Register)	R6 (High Sink Control Register for Port 5)	R6 (IRC control Register) *
07	R7 (Port 7)	R7 (I/O Port Control Register)	R7 (High Sink Control Register for Port 6)	R7 (Noise and LVR Control Register) *
08	R8 (Port 8)	R8 (I/O Port Control Register)	R8 (Operating mode Control Register)	Reserve
09	Reserve	Reserve	Reserve	Reserve
0A	Reserve	RA (Comparator Control Register)	Reserve	Reserve
0B	Reserve	RB (Pull-down Control Register)	Reserve	Reserve
0C	Reserve	RC (Open-drain Control Register)	Reserve	Reserve
0D	Reserve	RD (Pull-high Control Register)	Reserve	Reserve
0E	RE (Wake-up Control Register)	RE (WDT Control Register)	Reserve	Reserve
0F	RF (Interrupt Status Register)	RF (Interrupt Mask Register)	Reserve	Reserve
10 : 1F	General Registers (16×8 bits)			
20 : 3F	General Registers (32×8 bits)	General Registers (32×8 bits)	General Registers (32×8 bits)	General Registers (32×8 bits)

Note: 1. All registers are 8 bits.

2. When using ICE, some registers code options are set. Refer to Section 6.2 for detailed register description.

3. Registers with asterisk * can only be used in ICE210N simulator.

6.2 Registers Description

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

- 0 = interrupt occurs at a rising edge on the INT0 and INT1 pin
- 1 = interrupt occurs at a falling edge on the INT0 and INT1 pin

Bit 6 (INT): Interrupt enable flag

- 0 = masked by DISI or hardware interrupt
- 1 = enabled by the ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC signal source

- 0 = internal instruction cycle clock. If P56 is used as I/O pin, TS must be 0.
- 1 = transition on the TCC pin

Bit 4 (TE): TCC signal edge

- 0 = increment if the transition from low to high takes place on the TCC pin
- 1 = increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

- 0 = prescaler disable bit. TCC rate is 1:1
- 1 = prescaler enable bit. TCC rate is set as Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note: Tcc time-out period $[1/Fosc \times \text{prescaler} \times (256 - Tcc \text{ cnt}) \times 1]$
Fosc: Oscillator (Crystal, ERC, IRC) frequency

6.2.3 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.2.4 R1 (Memory Switch Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	"0"	"0"	BS1	BS0

Bits 7~2: not used, fixed to 0 all the time.

Bits 1~0: is used to select Banks 0 ~ 3 for R20~R3F and select Banks 0~3 for control register.

See the table under Section 6.2 *Registers Configuration* for the data memory configuration.

6.2.5 R2 (Program Counter) and Stack

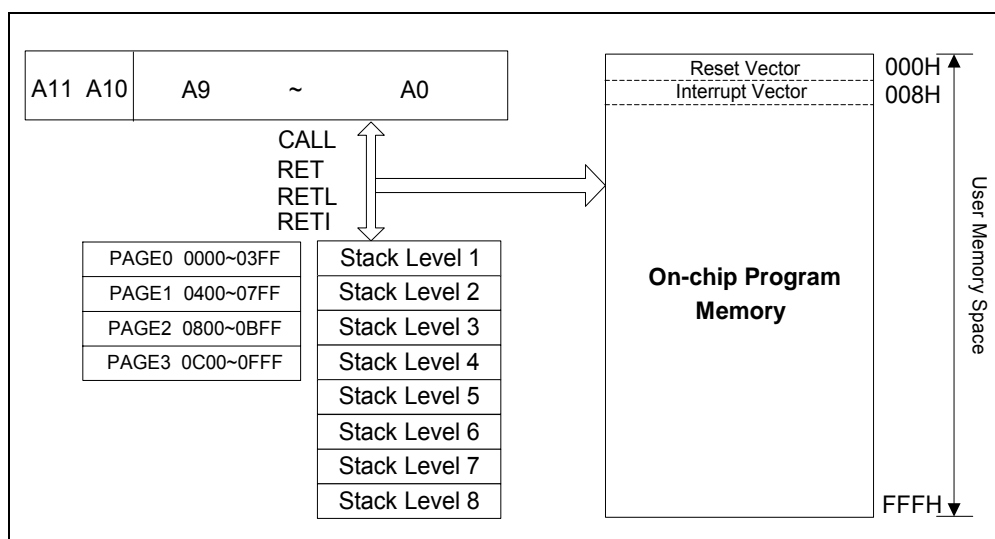


Figure 6-1 Program Counter Organization

R2 and hardware stacks are 12-bit wide. The structure is depicted in the table under Section 6.1 *Register Configuration*.

Generates 4K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

The contents of R2 are all set to "0"s when a reset condition occurs.



"JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to jump to any location within a Page (1K).

"CALL" instruction loads the lower 10 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page (1K).

"LJMP" instruction allows direct loading of the lower 11 program counter bits. Therefore, "LJMP" allows the PC to jump to any location within 4K (2^{12}).

"LCALL" instruction loads the lower 12 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12}).

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of the stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will be incremented progressively.

"MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will remain unchanged.

Any instruction (except "ADD R2,A") that is written to R2 (e.g., "MOV R2, A", "BC R2, 6" etc.) will cause the ninth bit and above bits of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2) except "LCALL" and "LJMP" instructions. The "LCALL" and "LJMP" instructions need two instruction cycles.

6.2.6 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T	P	Z	DC	C

Bits 7~5: not used, fixed to 0 all the time.

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power-on and reset to 0 by WDT time-out.

Bit 3 (P): Power-down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

NOTE

Bit 4 and Bit 3 (T and P) are read only.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag



6.2.7 R4 (Select Indirect Address)

Bits 7~6: not used, fixed to 0 all the time.

Bits 5 ~ 0: used to select registers (Address: 00 ~ 3F) in indirect addressing mode.

6.2.8 Bank 0-R5 (Port 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	P53	P52	P51	P50

Bits 7 ~ 0 (P57 ~ P50): I/O data bits

6.2.9 Bank 0-R6 (Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Bits 7 ~ 0 (P67 ~ P60): I/O data bits

6.2.10 Bank 0-R7 (Port 7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70

Bits 7 ~ 0 (P77 ~ P70): I/O data bits

6.2.11 Bank 0-R8 (Port 8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	NREN	0	0	0	P81	P80

Bits 7~6, 4~2, 0: not used, fixed to 0 all the time.

Bit 5 (NREN): Noise rejection enable
 0 = disable noise rejection (Default)
 1 = enable noise rejection. However in crystal oscillator mode (LXT2), the noise rejection circuit is always disabled.

Bits 1~0 (P81~P80): I/O data bit.

[Note]: P80 is General input or output, but P81 is input or open-drain for output pin.

6.2.12 Bank 0-R9~RD (Reserve)

Bits 7~0: not used, fixed to "0" all the time.

6.2.13 Bank 0-RE (WUCR: Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EX1IF	0	0	ICWE	0	CMPWE	0	CMPIF

Bit 7 (EX1IF): External interrupt flag. Set by INT1 pin, reset by software.

- 0 = no interrupt occurs
- 1 = with interrupt request

Bits 6~5, 3, 1: not used, fixed to 0 all the time

Bit 4 (ICWE): Port 6 input change to wake-up status enable bit

- 0 = Disable Port 6 input change to wake-up status
- 1 = Enable Port 6 input change wake-up status

When the Port 6 Input Status Change is used to enter an interrupt vector or to wake-up the EM78P220N from sleep mode, the ICWE bit must be set to "Enable".

Bit 2 (CMPWE): Comparator wake-up enable bit

- 0 = Disable Comparator wake-up
- 1 = Enable Comparator wake-up

When the Comparator output status change is used to enter an interrupt vector or to wake-up from sleep mode, the CMPWE bit must be set to "Enable".

Bit 0 (CMPIF): Comparator Interrupt Flag. Set when a change occurs in the Comparator output. Reset by software.

- 0 = no interrupt occurs
- 1 = with interrupt request

NOTE

- Bank 0-RE <7, 0> can be cleared by instruction but cannot be set.
- Bank 1-RE <0> is an interrupt mask register.
- Interrupt results from "logic AND" of Bank 0-RE <7, 0> and Bank 1-RE <0>, with instruction "ENI".

6.2.14 Bank 0-RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	EX0IF	ICIF	TCIF

Bits 7~3: not used, fixed to 0 all the time

Bit 2 (EX0IF): External interrupt flag. Set by INT0 pin. Reset by software.

- 0 = no interrupt occurs
- 1 = with interrupt request



Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.

- 0 = no interrupt occurs
- 1 = with interrupt request

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

- 0 = no interrupt occurs
- 1 = with interrupt request

NOTE

- Bank 0-RF <2, 1, 0> can be cleared by instruction but cannot be set.
- Bank 1-RF <2, 1, 0> is an interrupt mask register.
- Interrupt results from "logic AND" of Bank 0-RF <2, 1, 0> and Bank 1-RF <2, 1, 0> with instruction "ENI".

6.2.15 Bank 1-R5 ~R7 (I/O Port Control Register)

Bits 7~0: 0 = defines the relative I/O pin as output
1 = puts the relative I/O pin into high impedance

Bank 1-R5, R6 and R7 registers are all readable and writable.

6.2.16 Bank 1-R8 (I/O Port Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	C81	C80

Bits 7~2: not used, fixed to "0" all the time

Bits 1~0 (C81~C80): 0 = defines the relative I/O pin as output
1 = puts the relative I/O pin into high impedance

[Note]: P80 is General input or output, but P81 is input or open-drain for output pin.

6.2.17 Bank 1-R9 (Reserve)

Bits 7~0: not used, fixed to 0 all the time

6.2.18 Bank 1-RA (CMPCON: Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIS1	EIS0	CMPOUT	CMPCOS1	CMPCOS0	0	0	0

Bit 7 (EIS1): Control bit used to define the function of the P71 (/INT1) pin
0 = P71, normal I/O pin
1 = /INT1, external interrupt pin. In this case, the I/O control bit of P71 (Bit 1 of Bank 1-R7) must be set to "1".

Bit 6 (EIS0): Control bit used to define the function of the P77 (/INT0) pin
0 = P77, normal I/O pin
1 = /INT0, external interrupt pin. In this case, the I/O control bit of P77 (Bit 7 of Bank 1-R7) must be set to "1"

NOTE

- When EIS is "0," the path of /INT is masked. When EIS is "1," the status of /INT pin can also be read by way of reading Port 7 (Bank 0-R7). Refer to Figure 6-4 (I/O Port and I/O Control Register Circuit for P77 (/INT0) and P71 (/INT1) under Section 6.4 (I/O Ports).
- EIS0 and EIS1 are both readable and writable.
- The highest priority of P71/INT1/CO is INT1. When EIS1=0, the working type of P71/INT1/CO is determined by CMPCOS1 and CMPCOS0.

Bit 5 (CMPOUT): The result of the comparator output

Bit 4 ~ Bit 3 (CMPCOS1 ~ CMPCOS0): Comparator Select bits

CMPCOS1	CMPCOS0	Function Description
0	0	Comparator is not used. P72, P73, and P71 are normal I/O pins.
0	1	P72 and P73 are Comparator input pins and P71 is normal I/O pin.
1	0	P72 and P73 are Comparator input pins and P71 is Comparator output pin (CO)
1	1	Used as OP and P71 is OP output pin (CO)

Bits 2~0: not used, fixed to 0 all the time

6.2.19 Bank 1-RB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bank 1-RB register is both readable and writable

Bit 7 (/PD7): Control bit used to enable pull-down of the P67 pin
0 = Enable internal pull-down
1 = Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable pull-down of the P66 pin

Bit 5 (/PD5): Control bit used to enable pull-down of the P65 pin

Bit 4 (/PD4): Control bit used to enable pull-down of the P64 pin

Bit 3 (/PD3): Control bit used to enable pull-down of the P63 pin

Bit 2 (/PD2): Control bit used to enable pull-down of the P62 pin

Bit 1 (/PD1): Control bit used to enable pull-down of the P61 pin

Bit 0 (/PD0): Control bit used to enable pull-down of the P60 pin



6.2.20 Bank 1-RC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OD7	/OD6	/OD3	/OD2	/OD5	/OD4	/OD1	/OD0

Bank 1-RC register is both readable and writable.

Bit 7 (OD7): Control bit used to enable open-drain of the P57 pin.

0 = Enable open-drain output

1 = Disable open-drain output

Bit 6 (OD6): Control bit used to enable open-drain output of the P56 pin.

Bit 5 (OD5): Control bit used to enable open-drain output of the P55 pin.

Bit 4 (OD4): Control bit used to enable open-drain output of the P54 pin.

Bit 3 (OD3): Control bit used to enable open-drain output of the P53 pin.

Bit 2 (OD2): Control bit used to enable open-drain output of the P52 pin.

Bit 1 (OD1): Control bit used to enable open-drain output of the P51 pin.

Bit 0 (OD0): Control bit used to enable open-drain output of the P50 pin.

6.2.21 Bank 1-RD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

Bank 1-RD register is both readable and writable.

Bit 7 (/PH7): Control bit used to enable the pull-high function of the P67 pin.

0 = Enable internal pull-high

1 = Disable internal pull-high

Bit 6 (/PH6): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH5): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH4): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH3): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH2): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH1): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH0): Control bit used to enable pull-high of the P60 pin.

6.2.22 Bank 1-RE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	0	PSWE	PSW2	PSW1	PSW0	0	CMPIE

NOTE

- Bank 1-RE <0> register is both readable and writable
- Individual interrupt is enabled by setting its associated control bit in the Bank 1-RF <0 > to "1".
- Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).

Bit 7 (WDTE): Control bit is used to enable Watchdog Timer

0 = Disable WDT

1 = Enable WDT

WDTE is both readable and writable.

Bits 6, 1: Not used, fixed to 0 all the time

Bit 5 (PSWE): Prescaler enable bit for WDT

0 = prescaler disable bit. WDT rate is 1:1

1 = prescaler enable bit. WDT rate is set as Bit 4~Bit 2

Bit 4 ~ Bit 2 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 0 (CMPIE): CMPIF interrupt enable bit

0 = Disable CMPIF interrupt

1 = Enable CMPIF interrupt

When the Comparator output status change is used to enter an interrupt vector or to enter next instruction, the CMPIE bit must be set to "Enable". But actually the comparator output must be read to latch the status first. Then the output of the comparator is compared to this latch to produce the information of output status change.



6.2.23 Bank 1-RF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	EXIE	ICIE	TCIE

NOTE	
■	RF register is both readable and writable
■	Individual interrupt is enabled by setting its associated control bit in the RF to "1."
■	Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).

- Bits 7~3:** Not used, fixed to 0 all the time
- Bit 2 (EXIE):** EX0IF and EX1IF interrupts enable bit
0 = Disable EX0IF and EX1IF interrupts
1 = Enable EX0IF and EX1IF interrupts
- Bit 1 (ICIE):** ICIF interrupt enable bit
0 = Disable ICIF interrupt
1 = Enable ICIF interrupt
 If Port 6 Input Status Change Interrupt is used to enter an interrupt vector or to enter next instruction, the ICIE bit must be set to "Enable".
- Bit 0 (TCIE):** TCIF interrupt enable bit
0 = Disable TCIF interrupt
1 = Enable TCIF interrupt

6.2.24 Bank 2-R5 (HDCR: High Drive Control Register for Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HD67	HD66	HD65	HD64	HD63	HD62	HD61	HD60

- Bit 7 (HD67):** Output High Drive Current Select for P67
- Bit 6 (HD66):** Output High Drive Current Select for P66
- Bit 5 (HD65):** Output High Drive Current Select for P65
- Bit 4 (HD64):** Output High Drive Current Select for P64
- Bit 3 (HD63):** Output High Drive Current Select for P63
- Bit 2 (HD62):** Output High Drive Current Select for P62
- Bit 1 (HD61):** Output High Drive Current Select for P61
- Bit 0 (HD60):** Output High Drive Current Select for P60

HDxx	VDD = 5V, Drive Current
0	9 mA (in 0.9VDD)
1	27 mA (in 0.7VDD)



6.2.25 Bank 2-R6 (HSCR1: High Sink Control Register for Port 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HS57	HS56	HS55	HS54	HS53	HS52	HS51	HS50

Bit 7 (HS57): Output High Sink Current Select for P57

Bit 6 (HS56): Output High Sink Current Select for P56

Bit 5 (HS55): Output High Sink Current Select for P55

Bit 4 (HS54): Output High Sink Current Select for P54

Bit 3 (HS53): Output High Sink Current Select for P53

Bit 2 (HS52): Output High Sink Current Select for P52

Bit 1 (HS51): Output High Sink Current Select for P51

Bit 0 (HS50): Output High Sink Current Select for P50

HDxx	VDD = 5V, Sink Current
0	18mA (in 0.1VDD)
1	75mA (in 0.3VDD)

6.2.26 Bank 2-R7 (HSCR2: High Sink Control Register for Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HS67	HS66	HS65	HS64	HS63	HS62	HS61	HS60

Bit 7 (HS67): Output High Sink Current Select for P67

Bit 6 (HS66): Output High Sink Current Select for P66

Bit 5 (HS65): Output High Sink Current Select for P65

Bit 4 (HS64): Output High Sink Current Select for P64

Bit 3 (HS63): Output High Sink Current Select for P63

Bit 2 (HS62): Output High Sink Current Select for P62

Bit 1 (HS61): Output High Sink Current Select for P61

Bit 0 (HS60): Output High Sink Current Select for P60

HDxx	VDD = 5V, Sink Current
0	18 mA (in 0.1VDD)
1	75 mA (in 0.3VDD)

6.2.27 Bank 2-R8 (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TIMERSC	CPUS	IDLE	0	0	0	0

Bit 7: Not used, fixed to "0" all the time.

Bit 6 (TIMERSC): TCC clock sources.

0 = Fs: sub frequency for WDT internal RC time base 16kHz ± 30% (fs)

1 = Fm: main-oscillator clock (fosc)

Bit 5 (CPUS): CPU Oscillator Source Select

0 : sub-oscillator (fs)

1 : main oscillator (fosc)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit

From SLEP instruction, this bit will determine as to which mode to choose.

0 : IDLE = '0' + SLEP instruction → sleep mode

1 : IDLE = '1' + SLEP instruction → idle mode

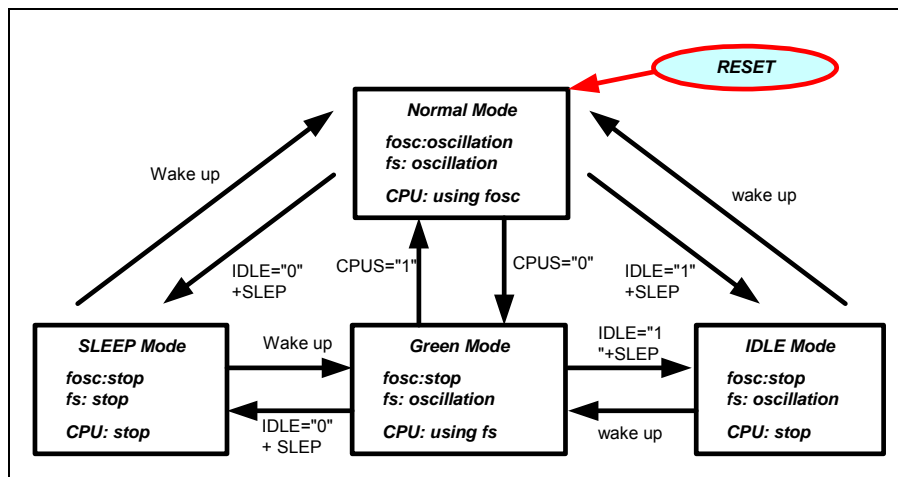


Figure 6-2 CPU Operation Mode Diagram

Bits 3~0: Not used, fixed to "0" all the time.

6.2.28 Bank 2-R9~RF (Reserve)

Bits 7~0: Not used, fixed to "0" all the time

6.2.29 Bank 3-R5 (Timer Clock/Counter)

- Incremented by an external signal edge through the TCC pin, or by the instruction cycle clock.
- External signal of TCC trigger pulse width must be greater than one instruction.
- The signals to increment the counter are determined by Bit 4 and Bit 5 of the CONT register.
- Writable and readable as any other registers.

6.2.30 Bank 3-R6 (IRC Control)-only for ICE

Bit	7	6	5	4	3	2	1	0
EM78P220N	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
ICE210N	C3	C2	C1	C0	RCM1	RCM0	'0'	'0'

Bits 7 ~ 2:

[With Simulator (C3~C0, RCM1~RCM0)]: IRC calibration bits in IRC oscillator mode.
In IRC oscillator mode of the ICE210N simulator, these are the IRC mode selection bits and IRC calibration bits.

[With EM78P220N]: Unimplemented, read as '0'.

Bits 7 ~ 4 (C3 ~ C0): Calibrator of internal RC mode

C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	$(1-36%) \times F$
0	0	0	1	$(1-31.5%) \times F$
0	0	1	0	$(1-27%) \times F$
0	0	1	1	$(1-22.5%) \times F$
0	1	0	0	$(1-18%) \times F$
0	1	0	1	$(1-13.5%) \times F$
0	1	1	0	$(1-9%) \times F$
0	1	1	1	$(1-4.5%) \times F$
1	1	1	1	F (default)
1	1	1	0	$(1+4.5%) \times F$
1	1	0	1	$(1+9%) \times F$
1	1	0	0	$(1+13.5%) \times F$
1	0	1	1	$(1+18%) \times F$
1	0	1	0	$(1+22.5%) \times F$
1	0	0	1	$(1+27%) \times F$
1	0	0	0	$(1+31.5%) \times F$

1. Frequency values shown are theoretical and taken at an instance of a high frequency mode. Hence, frequency values are shown for reference only. Definite values depend on the actual process.
2. Similar way of calculation is also applicable to low frequency mode.

Bits 3 ~ 2 (RCM1 ~ RCM0): IRC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (default)
1	0	16
0	1	1
0	0	455kHz

Bits 1 ~ 0: are not used, fixed to "0" all the time.



6.2.31 Bank 3-R7 (Noise and LVR Control) - only for ICE

Bit	7	6	5	4	3	2	1	0
EM78P220N	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
ICE210N	"0"	"0"	TYPE1	TYPE0	NRHL	NRE	LVR1	LVR0

[With EM78P220N]: Unimplemented, read as '0'.

[With Simulator]:

Bits 7 ~ 6: Not used, fixed to "0" all the time.

Bits 5 ~ 4 (TYPE1, TYPE0): Type selection for EM78P220N

TYPE1, TYPE0	MCU Type
00	Not used
01	
10	EM78P220N-24Pin
11	EM78P220N-28Pin

Bit 3 (NRHL): Noise rejection high/low pulse defined bit. The INT pin is a falling edge trigger.

0 = Pulses equal to $8/f_c$ [s] are regarded as signal.

1 = Pulses equal to $32/f_c$ [s] are regarded as signal (default)

NOTE

The noise rejection function is turned off in the LXT2 and in sleep mode.

Bit 2 (NRE): Noise Rejection Enable

0 = disable noise rejection

1 = enable noise rejection (default). However in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bits 1 ~ 0 (LVR1 ~ LVR0): Low Voltage Reset enable bits. If Vdd has a crossover at Vdd reset level as Vdd changes, the system will be reset.

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (default)	
10	2.5V	2.7V
01	3.0V	3.2V
00	4.0V	4.2V

6.2.32 Bank 3-R8~RF (Reserve)

Bits 7~0: are not used, fixed to "0" all the time.

6.2.33 R10 ~ R1F

All of these are 8-bit general-purpose registers.

6.2.34 Banks 0~3 - R20 ~ R3F

All of these are 8-bit general-purpose registers.

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT. The PST2~PST0 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PSW2~PSW0 bits of the Bank 1-RE register are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler are cleared by the “WDTC” and “SLEP” instructions. Figure 6-2 depicts the block diagram of TCC/WDT.

TCC (Bank 3-R5) is an 8-bit timer/counter. The TCC clock source can be internal clock (Fosc) or external signal input (edge selectable from the TCC pin). If the TCC signal source is from an external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at High or Low level) must be greater than 1CLK. 1 CLK is always Fosc/2. Refer to Figure 6-2.

NOTE

The internal TCC will stop running when in sleep mode.

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode through software programming. Refer to WDTE bit of Bank 1-RE register (Section 6.2.10 Bank 1-RE (WDT Control Register)). With no prescaler, the WDT time-out duration is approximately 18ms.¹

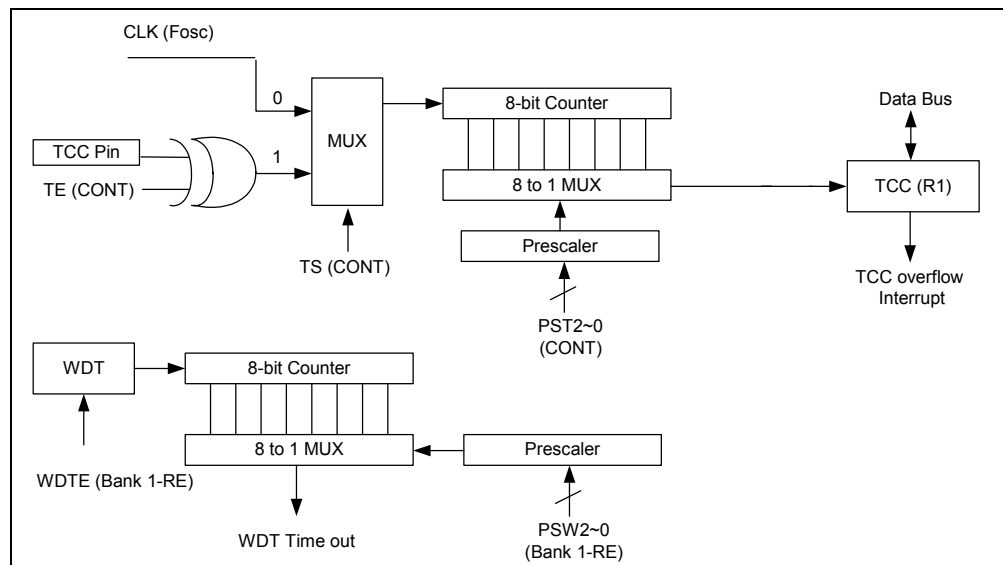
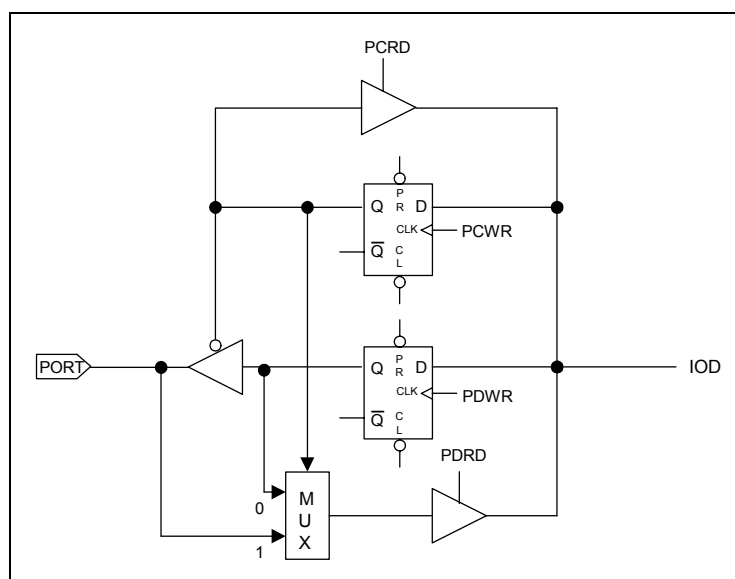


Figure 6-3 TCC and WDT Block Diagram

¹ VDD=5V, WDT Time-out period = 15.2ms ± 30%.
VDD=3V, WDT Time-out period = 18ms ± 30%.

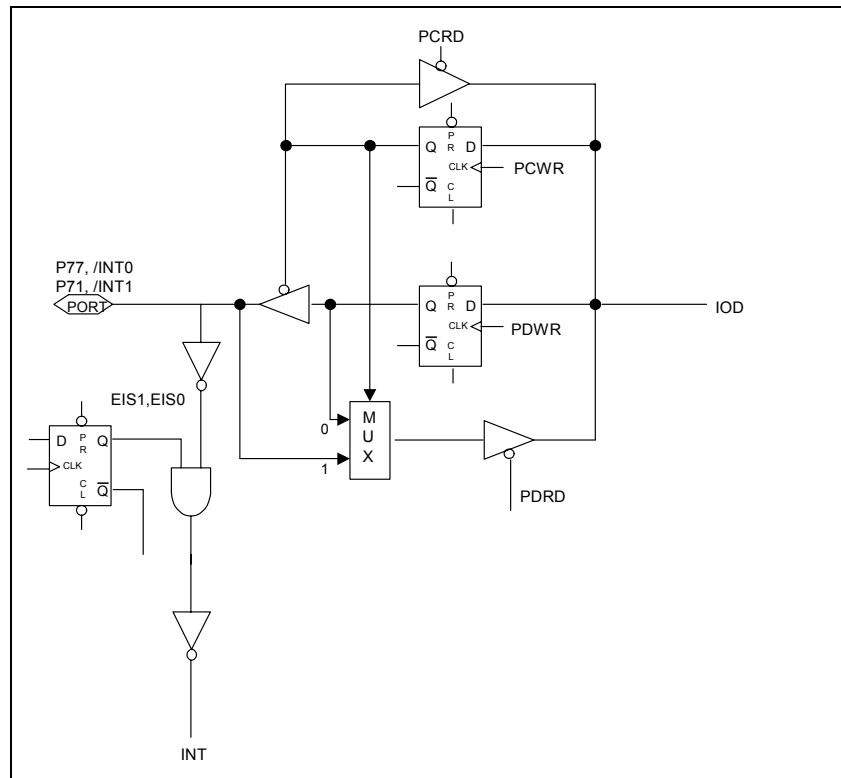
6.4 I/O Ports

The I/O registers (Port 5, Port 6, Port 7, and Port 8) are bidirectional tri-state I/O ports. The Pull-high, Pull-down, and Open-drain functions can be set internally by Bank 1-RB, Bank 1-RC, and Bank 1-RD respectively. The High drive and High Sink functions can be set internally by Bank 2-R5, Bank 2-R6, and Bank 2-R7 respectively. Port 6 features an input status change interrupt (or wake-up) function. Most I/O pin can be defined as "input" or "output" pin by the I/O control registers. The I/O registers and I/O control registers are both readable and writable. However, the initial states of these I/O ports (Port 5, Port 6, Port 7 and Port 8) are unknown input (high impedance). Then, if the I/O pin is pulled to a level at external circuit, the pin must induce a voltage. Hence, user must take into consideration whether the induced voltage causes a wrong action in the system. The I/O interface circuits for Port 5, Port 6, Port 7, and Port 8 are illustrated in Figures 6-4, 6-5, and 6-6 respectively. Port 6 with Input Change Interrupt/Wake-up is shown in Figure 6-7.



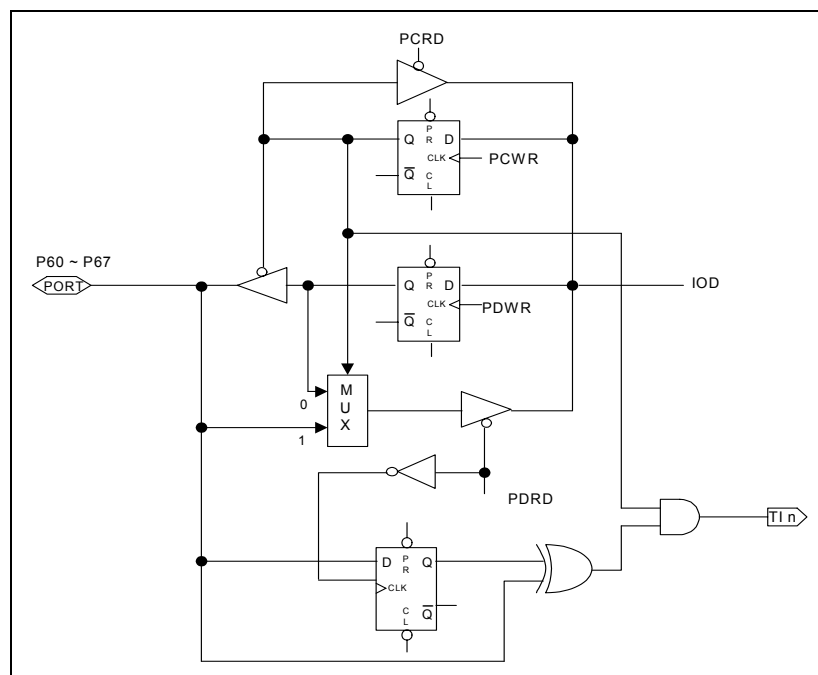
Note: Pull-high and Open-drain are not shown in the figure.

Figure 6-4 I/O Port and I/O Control Register Circuit for Port 5, Port 7 and Port 8



Note: CO, Pull-high and Open-drain are not shown in the figure.

Figure 6-5 I/O Port and I/O Control Register Circuit for P77 (/INT0) and P71 (/INT1)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-6 I/O Port and I/O Control Register Circuit for Port 6

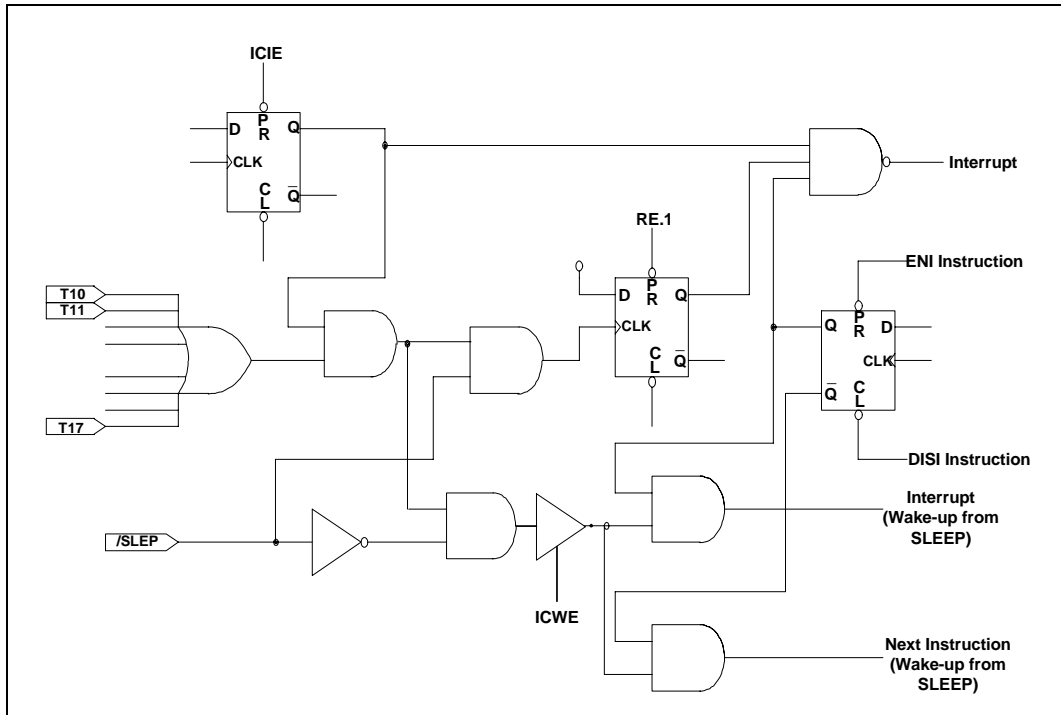


Figure 6-7 Port 6 Block Diagram with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(1) Wake-up	(2) Wake-up and Interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port 6 (MOV R6,R6)	2. Read I/O Port 6 (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set Bank 0-RE ICWE =1)	4. Enable wake-up bit (Set Bank 0-RE ICWE =1)
5. Execute "SLEEP" instruction	5. Enable interrupt (Set BANK1-RF ICIE =1)
(b) After wake-up	6. Execute "SLEEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (008H)
	2. IF "DISI" → Next instruction
(3) Interrupt	
(a) Before Port 6 pin change	
1. Read I/O Port 6 (MOV R6,R6)	
2. Execute "ENI" or "DISI"	
3. Enable interrupt (Set BANK1-RF ICIE =1)	
(b) After Port 6 pin changed (interrupt)	
1. IF "ENI" → Interrupt vector (008H)	
2. IF "DISI" → Next instruction	



6.5 Reset and Wake-up

6.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

A device is kept in a reset condition for the duration of approximately 18ms² after the reset is detected. When in LXT 2 mode, the reset time is 500ms. Once a reset occurs, the following functions are performed (the initial address is 000h):

- The oscillator continues running, or will be started (if in sleep mode)
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- When power is switched On, the Memory switch register (R1) is set to "0".
- The CONT register bits are set to all "0" except for Bit 6 (INT flag).
- Bank 0-RF register bits are set to all "0".
- Bank 1-RB register bits are set to all "1".
- Bank 1-RC register bits are set to all "1".
- Bank 1-RD register bits are set to all "1".
- Bank 1-RE register bits are set to all "0".
- Bank 1-RF register bits are set to all "0".

Executing the "SLEP" instruction will assert the sleep (power down) mode. While entering sleep mode, the Oscillator and TCC are stopped. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

- Case 1 External reset input on /RESET pin
- Case 2 WDT time-out (if enabled)
- Case 3 Port 6 input status changes (if ICWE is enabled)
- Case 4 Comparator output status changes (if CMPWE is enabled)

² VDD=5V, Setup time period = 16.5ms ± 30%.
VDD=3V, Setup time period = 18ms ± 30%.

The first two cases (1 and 2) will cause the EM78P220N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3 & 4 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEEP, the instruction will begin to execute from Address 0x8 after wake-up. If DISI is executed before SLEEP, the execution will restart from the instruction next to SLEEP after wake-up. All sleep mode wake up time is dependent on the oscillator mode, no matter what the oscillator type or mode is (except when it's in LXT2 mode). In LXT2 mode, wake-up time is 2~3 sec.

Although each of Cases 1 to 4 can be enabled, but not simultaneously, only one at a time can be enabled before entering sleep mode. That is:

Case [a] If WDT is enabled before SLEEP, all of the RE bit is disabled. Hence, the EM78P220N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 6.6) for further details.

Case [b] If Port 6 Input Status Change is used to wake -up EM78P220N and ICWE bit of Bank 0-RE register is enabled before SLEEP, WDT must be disabled. Hence, the EM78P220N can be awakened only with Case 3. Wake-up time is dependent on the oscillator mode. In RC mode (VDD: 5V, IRC: 4 MHz), wake-up time is 10 μ s (for stable oscillators). In HXT2 mode (VDD: 5V, Crystal: 4 MHz, C1/C2: 30pF), wake-up time is 800 μ s (for stable oscillators), and in LXT2 mode, wake-up time is 2~3 sec.

Case [c] If the Comparator output status change is used to wake-up the EM78P220N and the CMPWE bit of the RE register is enabled before SLEEP, WDT must be disabled by software. Hence, the EM78P220N can be awakened only with Case 4.

Wake-up time is dependent on the oscillator mode. In RC mode (VDD: 5V, IRC: 4MHz), wake-up time is 10 μ s (for stable oscillators). In HXT2 mode (VDD: 5V, Crystal: 4 MHz, C1/C2: 30pF), wake-up time is 800 μ s (for stable oscillators), and in LXT2 mode, wake-up time is 2~3 sec.



If Port 6 Input Status Change Interrupt is used to wake up the EM78P220N (as in Case b above), the following instructions must be executed before SLEEP:

```

MOV      A, @000110xxb    ; Select WDT prescaler and disable WDT
BANK    1
MOV      RE, A
WDTC    ; Clear WDT and prescaler
BANK    0
MOV      R6, R6           ; Read Port 6
ENI (or DISI)           ; Enable (or disable) global interrupt
MOV      A, @xxx1xxxxb   ; Enable Port 6 input change wake-up bit
MOV      RE
MOV      A, @00000x1xb   ; Enable Port 6 input change interrupt
BANK    1
MOV      RF, A
SLEEP   ; Sleep
  
```

Similarly, if the Comparator Interrupt is used to wake up the EM78P220N (as in Case [c] above), the following instructions must be executed before SLEEP:

```

MOV      A, @xxx01xxxb   ; Select Comparator and P71 functions as
                          ; general I/O pin
BANK    1
MOV      RA, A
MOV      A, @000110xxb   ; Select WDT prescaler and Disable WDT
MOV      RE, A
WDTC    ; Clear WDT and prescaler
ENI (or DISI)           ; Enable (or disable) global interrupt
MOV      A, @00000100b   ; Enable comparator output status change
                          ; wake-up bit
BANK    0
MOV      RE, A
BANK    1
MOV      A, @0x00000001b ; Enable Comparator output status change
                          ; interrupt
MOV      RE, A
SLEEP   ; Sleep
  
```

6.5.1.1 Wake-up and Interrupt Modes Operation Summary

All categories under Reset, Wake-up and Interrupt modes are summarized below.

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	×	Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
Port 6 pin change	If enable ICWE bit Wake-up + interrupt (if interrupt enable) + next instruction	If enable ICWE bit Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
TCC overflow interrupt	×	Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
Comparator interrupt	If enable CMPWE bit Wake-up + interrupt (if interrupt enable) + next instruction	If enable CMPWE bit Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
WDT Time out	Reset to Normal mode	Reset to Normal mode	Reset to Normal mode	Reset to Normal mode
Low Voltage Reset	Reset to Normal mode	Reset to Normal mode	Reset to Normal mode	Reset to Normal mode

After wake up:

1. If interrupt enable → interrupt+ next instruction
2. If interrupt disable → next instruction



The controller can be awakened from Sleep and Idle mode. The wake-up signals are listed as follows:

Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
INT0 INT1	N/A	DISI + Bank 1-RF (EXIE) Bit 2 = 1	DISI + Bank 1-RF (EXIE) Bit 2 = 1	DISI + Bank 1-RF (EXIE) Bit 2 = 1
		Wake-up+ Next Instruction + Set Bank 0-RF (EX0IF)=1	Next Instruction+ Set Bank 0-RF (EX0IF) = 1 or Set Bank 0-RE (EX1IF)=1	Next Instruction+ Set Bank 0-RF (EX0IF) = 1 or Set Bank 0-RE (EX1IF)=1
		ENI + Bank 1-RF (EXIE) Bit 2 = 1	ENI + Bank 1-RF (EXIE) Bit 2 = 1	ENI + Bank 1-RF (EXIE) Bit 2 = 1
		Wake-up+ Interrupt Vector (0x08)+ Set Bank 0-RF (EX0IF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (EX0IF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (EX0IF) = 1
Port 6 Input Status Change	Bank 0-RE (ICWE) Bit 4=0, Bank 1-RF (ICIE) Bit 1 = 0	Bank 0-RE (ICWE) Bit 4=0, Bank 1-RF (ICIE) Bit 1=0	Bank 1-RF (ICIE) Bit 1 = 0	Bank 1-RF (ICIE) Bit 1 = 0
	Oscillator and TCC are stopped. Port 6 input status changed wake-up is invalid.	Oscillator and TCC are stopped. Port 6 input status changed wake-up is invalid.	Port 6 input status change interrupt is invalid	Port 6 input status change interrupt is invalid
	Bank 0-RE (ICWE) Bit 4=0, Bank 1-RF (ICIE) Bit 1=1	Bank 0-RE (ICWE) Bit 4=0, Bank 1-RF (ICIE) Bit 1 = 1	N/A	N/A
	Set Bank 0-RF (ICIF) = 1, Oscillator and TCC are stopped. Port 6 input status changed wake-up is invalid.	Set Bank 0-RF (ICIF) = 1, Oscillator and TCC are stopped. Port 6 input status changed wake-up is invalid.	N/A	N/A
	Bank 0-RE (ICWE) Bit 4=1, Bank 1-RF (ICIE) Bit 1=0	Bank 0-RE (ICWE) Bit 4=1, Bank 1-RF (ICIE) Bit 1=0	N/A	N/A
	Wake-up+ Next Instruction Oscillator and TCC are stopped.	Wake-up+ Next Instruction Oscillator and TCC are stopped.	N/A	N/A
	Bank 0-RE (ICWE) Bit 4=1, DISI + Bank 1-RF (ICIE) Bit 1 = 1	Bank 0-RE (ICWE) Bit 4=1, DISI + Bank 1-RF (ICIE) Bit 1 = 1	DISI + Bank 1-RF (ICIE) Bit 1 = 1	DISI + Bank 1-RF (ICIE) Bit 1 = 1
	Wake-up+ Next Instruction+ Set Bank 0-RF (ICIF) = 1 Oscillator and TCC are stopped.	Wake-up+ Next Instruction+ Set Bank 0-RF (ICIF) = 1 Oscillator and TCC are stopped.	Next Instruction+ Set Bank 0-RF (ICIF) = 1	Next Instruction+ Set Bank 0-RF (ICIF) = 1
Bank 0-RE (ICWE) Bit 4=1, ENI + Bank 1-RF (ICIE) Bit 1 = 1	Bank 0-RE (ICWE) Bit 4=1, ENI + Bank 1-RF (ICIE) Bit 1 = 1	ENI + Bank 1-RF (ICIE) Bit 1 = 1	ENI + Bank 1-RF (ICIE) Bit 1 = 1	
Wake-up+ Interrupt Vector (0x08)+ Set Bank 0-RF (ICIF) = 1 Oscillator and TCC are stopped.	Wake-up+ Interrupt Vector (0x08)+ Set Bank 0-RF (ICIF) = 1 Oscillator and TCC are stopped.	Interrupt Vector (0x08)+ Set Bank 0-RF (ICIF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (ICIF) = 1	
TCC Overflow	N/A	DISI + Bank 1-RF (TCIE) Bit 0 = 1	DISI + Bank 1-RF (TCIE) Bit 0 = 1	DISI + Bank 1-RF (TCIE) Bit 0 = 1
		Wake-up+ Next Instruction + Set Bank 0-RF (TCIF)=1	Next Instruction+ Set Bank 0-RF (TCIF) = 1	Next Instruction+ Set Bank 0-RF (TCIF) = 1
		ENI + Bank 1-RF (TCIE) Bit 0 = 1	ENI + Bank 1-RF (TCIE) Bit 0=1	ENI + Bank 1-RF (TCIE) Bit 0=1
		Wake-up+ Interrupt Vector (0x08)+ Set Bank 0-RF (TCIF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (TCIF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (TCIF) = 1



Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
Comparator (Comparator Output Status Change)	Bank 0-RE (CMPWE) Bit 2 = 0 Bank 1-RE (CMPIE) Bit 0 = 0	Bank 0-RE (CMPWE) Bit 2 = 0 Bank 1-RE (CMPIE) Bit 0 = 0	Bank 1-RE (CMPIE) Bit 0 = 0	Bank 1-RE (CMPIE) Bit 0 = 0
	Comparator output status changed wake-up is invalid. Oscillator and TCC are stopped.	Comparator output status changed wake-up is invalid. Oscillator and TCC are stopped.	Comparator output status change interrupt is invalid.	Comparator output status change interrupt is invalid.
	Bank 0-RE (CMPWE) Bit 2 = 0 Bank 1-RE (CMPIE) Bit 0 = 1	Bank 0-RE (CMPWE) Bit 2 = 0 Bank 1-RE (CMPIE) Bit 0 = 1	N/A	N/A
	Set Bank 0-RE (CMPIF) = 1, Comparator output status changed wake-up is invalid. Oscillator and TCC are stopped.	Set Bank 0-RE (CMPIF)=1, Comparator output status changed wake-up is invalid. Oscillator and TCC are stopped.	N/A	N/A
	Bank 0-RE (CMPWE) Bit 2 = 1, Bank 1-RE (CMPIE) Bit 0 = 0	Bank 0-RE (CMPWE) Bit 2 = 1, Bank 1-RE (CMPIE) Bit 0 = 0	N/A	N/A
	Wake-up+ Next Instruction, Oscillator and TCC are stopped.	Wake-up+ Next Instruction, Oscillator and TCC are stopped.	N/A	N/A
	Bank 0-RE (CMPWE) Bit 2 = 1, DISI + Bank 1-RE (CMPIE) Bit 0 = 1	Bank 0-RE (CMPWE) Bit 2 = 1, DISI + Bank 1-RE (CMPIE) Bit 0 = 1	DISI + Bank 1-RE (CMPIE) Bit 0 = 1	DISI + Bank 1-RE (CMPIE) Bit 0 = 1
	Wake-up+ Next Instruction+ Set Bank 0-RE (CMPIF) Bit 0 = 1, Oscillator and TCC are stopped.	Wake-up+ Next Instruction+ Set Bank 0-RE (CMPIF) Bit 0 = 1, Oscillator and TCC are stopped.	Next Instruction+ Set Bank 0-RE (CMPIF) Bit 0 = 1	Next Instruction+ Set Bank 0-RE (CMPIF) Bit 0 = 1
Bank 0-RE (CMPWE) Bit 2 = 1, ENI + Bank 1-RE (CMPIE) Bit 0 = 1	Bank 0-RE (CMPWE) Bit 2 = 1, ENI + Bank 1-RE (CMPIE) Bit 0 = 1	ENI + Bank 1-RE (CMPIE) Bit 0 = 1	ENI + Bank 1-RE (CMPIE) Bit 0 = 1	
Wake-up+ Interrupt Vector (0x08)+ Set Bank 0- RE (CMPIF) Bit 0 = 1, Oscillator and TCC are stopped.	Wake-up+ Interrupt Vector (0x08)+ Set Bank 0- RE (CMPIF) Bit 0 = 1, Oscillator and TCC are stopped.	Interrupt Vector (0x08)+ Bank 0-RE (CMPIF) Bit 0 = 1	Interrupt Vector (0x08)+ Bank 0-RE (CMPIF) Bit 0 = 1	
WDT Time-out Bank 1-RE (WDTE) Bit 7=1	Wake-up+ Reset (Address 0x00)	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)	Reset (Address 0x00)
Low Voltage Reset	Wake-up+ Reset (Address 0x00)	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)	Reset (Address 0x00)



6.5.1.2 Register Initial Values after Reset

The following table summarizes the registers initialized values.

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (MSR)	Bit Name	-	-	-	-	-	-	BS1	BS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x08 or continue to execute the next instruction							
0x03	R3 (SR)	Bit Name	-	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET & WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4 (SIA)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET & WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 0-R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 0-R6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	Bank 0-R7	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	Bank 0-R8	Bit Name	-	-	NREN	-	-	-	P81	P80
		Power-on	0	0	0	0	0	0	U	U
		/RESET & WDT	0	0	0	0	0	0	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09~0xD	Bank 0-R9~RD (Reserve)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xE	Bank 0-RE (WUCR)	Bit Name	EX1IF	-	-	ICWE	-	CMPWE	-	CMPIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xF	Bank 0-RF (ISR)	Bit Name	-	-	-	-	-	EX0IF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 1-R5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 1-R6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	Bank 1-R7	Bit Name	C77	C76	C75	C74	C73	C72	C71	C70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x8	Bank 1-R8	Bit Name	-	-	-	-	-	-	C81	C80
		Power-on	0	0	0	0	0	0	1	1
		/RESET & WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9	Bank 1-R9 (Reserve)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xA	Bank 1-RA (CMPCON)	Bit Name	EIS1	EIS0	CMP OUT	CMP COS1	CMP COS0	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xB	Bank 1-RB (PDCR)	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xC	Bank 1-RC (ODCR)	Bit Name	/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xD	Bank 1-RD (PHCR)	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xE	Bank 1-RE (WDTCR)	Bit Name	WDTE	-	PSWE	PSW2	PSW1	PSW0	-	CMPIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P



Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF	Bank 1-RF (IMR)	Bit Name	-	-	-	-	-	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 2-R5 (HDCR)	Bit Name	HD67	HD66	HD65	HD64	HD63	HD62	HD61	HD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 2-R6 (HSCR1)	Bit Name	HS57	HS56	HS55	HS54	HS53	HS52	HS51	HS50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	Bank 2-R7 (HSCR2)	Bit Name	HS67	HS66	HS65	HS64	HS63	HS62	HS61	HS60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x8	Bank 2-R8 (OMCR)	Bit Name	-	TIMERSC	CPUS	IDLE	-	-	-	-
		Power-on	U	1	1	1	U	U	U	U
		/RESET & WDT	P	1	1	1	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9 ~ 0xF	Bank 2-R9 (RF)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 3-R5 (TCC)	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 3-R6 (IRC) (only for ICE)	Bit Name	C3	C2	C1	C0	RCM1	RCM0	-	-
		Power-on	1	1	1	1	1	1	U	U
		/RESET & WDT	1	1	1	1	1	1	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

6.5.2 The T and P Status under Status Register

A reset condition is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
LVR during Operating mode,	*P	*P
LVR wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous status before reset

The following shows the events that may affect the status of T and P.

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during Sleep mode	1	0

* P: Previous value before reset

6.6 Interrupt

The EM78P220N has four interrupts as listed below:

1. TCC overflow interrupt
2. Port 6 Input Status Change Interrupt
3. External Interrupt INT0, INT1
4. When the Comparator output status changes

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6, R6") is necessary. Each Port 6 pin will have this feature if its status changes. Port 6 Input Status Change Interrupt will wake up the EM78P220N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP. When wake-up occurs, the controller will continue to execute the succeeding program if the global interrupt is disabled. If enabled, it will branch out to the Interrupt Vector 008H.

The external interrupt has a built-in digital noise rejection circuit (if the input pulse is less than 8 system clock times, it is eliminated as noise. Edge selection is possible with /INT. Refer to Word 1 Bits 8~7 (Section 6.13.2, *Code Option Register (Word 1)*) for digital noise rejection definition.

During a power source unstable situation, like during external power noise interference or EMS test condition, it will cause the power to vibrate fiercely. While Vdd is still unsettled, the supply voltage may be below the working voltage. When the system supply voltage Vdd is below the working voltage, the IC kernel must automatically keep all register status.

Bank 0-RE and Bank 0-RF are the interrupt status register that records the interrupt requests in the relative flags/bits. Bank 1-RE and Bank 1-RF are interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in Bank 0-RE and Bank 0-RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

When interrupt mask bits are "Enabled", the flag in the Interrupt Status Register (RF) is set regardless of the ENI execution. Note that the result of Bank 0-RE/RF will be the logic AND of Bank 0-RE/RF and Bank 1-RE/RF (refer to Figure 6-8). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

When any interrupt occurs, the contents of ACC, R1 (Bits 5, 4, 1, 0), R3 (Bits 2 ~0), R4 registers are pushed to the corresponding stack (Figure 6-9). After the RETI instruction is executed, the contents of the corresponding stack are popped to ACC, R1 (Bits 5, 4, 1, 0), R3 (Bits 2 ~0), R4 registers.

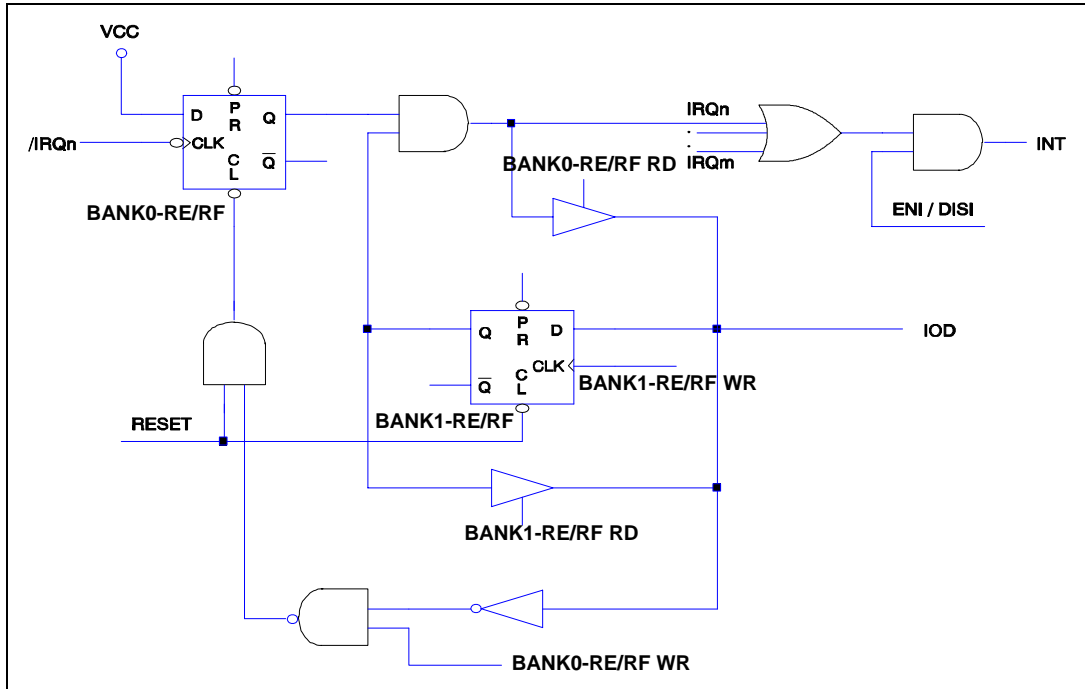


Figure 6-9 Interrupt Input Circuit

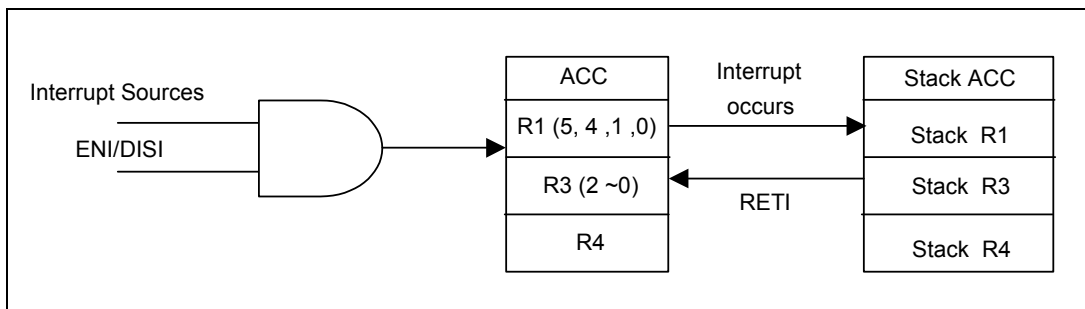


Figure 6-10 Interrupt Backup Diagram

6.7 Comparator

The EM78P220N has one comparator comprising of two analog inputs and one output. The comparator can be utilized to wake up the EM78P220N from sleep mode. The comparator circuit diagram is depicted in the figure below.

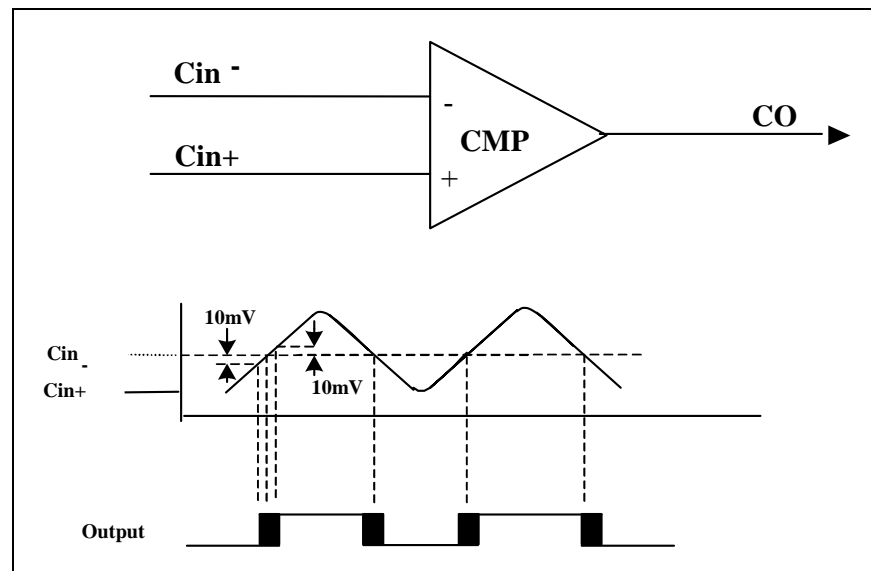


Figure 6-11 Comparator Circuit Diagram and Operating Mode

6.7.1 External Reference Signal

The analog signal presented at $Cin-$ compares to the signal at $Cin+$, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

NOTE

- The reference signal must be between V_{ss} and V_{dd} .
- The reference voltage can be applied to either pin of the comparator.
- Threshold detector applications may be of the same reference.
- The comparator can operate from the same or different reference sources.

6.7.2 Comparator Outputs

- The compared result is stored in the CMPOUT of Bank 1-RA.
- Bits 3 ~ 4 <CMPCOS1, CMPCOS0> of the Bank 1-RA register. See Section 6.2.18, *Bank 1-RA (CMPCON: Comparator Control Register)* for Comparator select bits function description.

NOTE

- The highest priority of P71/INT1/CO is INT1. When EIS1=0, the working type of P71/INT1/CO is determined by CMPCOS1 and CMPCOS2.
- The CO and P71 of the P71/CO pins cannot be used at the same time.
- The P71/CO pin priority is as follows:

P71/INT1/CO Pin Priority		
High	Medium	Low
/INT1	CO	P71

The following figure shows the Comparator Output Block Diagram.

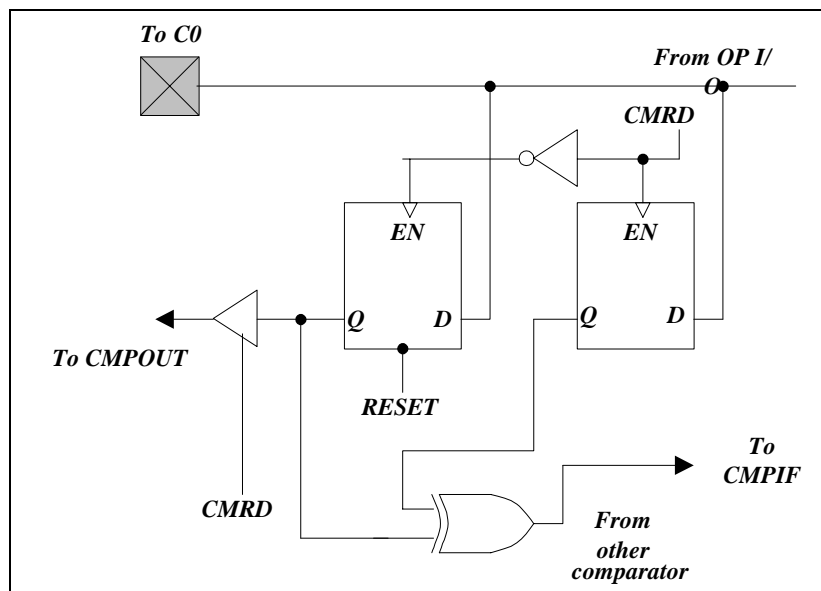


Figure 6-12 Comparator Output Configuration

6.7.3 Using a Comparator as an Operation Amplifier

6.7.3.1 Bank 0-RE (WUCR: Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EX1IF	0	0	ICWE	0	CMPWE	0	CMPIF

Bit 2 (CMPWE): Comparator wake-up enable bit
0 = Disable Comparator wake-up
1 = Enable Comparator wake-up

When the Comparator output status change is used to enter an interrupt vector or to wake-up the EM78P220N from sleep, the CMPWE bit must be set to "Enable".

Bit 0 (CMPIF): Comparator Interrupt Flag. Set when a change occurs in the Comparator output. Reset by software

6.7.3.2 Bank 1-RA (CMPCON: Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIS1	EIS0	CMPOUT	CMPCOS1	CMPCOS0	0	0	0

Bit 5 (CMPOUT): The result of the Comparator output

Bit 4 ~ Bit 3 (CMPCOS1 ~ CMPCOS0): Comparator Select bits

CMPCOS1	CMPCOS0	Function Description
0	0	Comparator is not used. P72, P73, and P71 are normal I/O pins
0	1	P72 and P73 are Comparator input pins and P71 is normal I/O pin
1	0	P72 and P73 are Comparator input pins and P71 is Comparator output pin (CO)
1	1	Used as OP and P71 is OP output pin (CO)

6.7.3.3 Bank 1-RE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	0	PSWE	PSW2	PSW1	PSW0	0	CMPIE

Bit 0 (CMPIE): CMPIF interrupt enable bit
0 = Disable CMPIF interrupt
1 = Enable CMPIF interrupt

When the Comparator output status change is used to enter an interrupt vector or to enter the next instruction, the CMPIE bit must be set to "Enable". But actually the comparator output must be read to latch the status at first. Then the comparator output is compared to this latch to produce the information of output status change.

6.7.4 Comparator Interrupt

- CMPIE must be enabled for the "ENI" instruction to take effect
- Interrupt is triggered whenever a change occurs on the comparator output pin
- The actual change on the pin can be determined by reading the Bit CMPOUT
- CMPIF the comparator interrupt flag, can only be cleared by software

6.7.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.8 Oscillator

6.8.1 Oscillator Modes

The EM78P220N can be operated in six different oscillator modes, such as High Crystal oscillator mode (HXT 1, 2), Low Crystal oscillator mode (LXT 1, 2), External RC oscillator mode (ERC), and RC oscillator mode with Internal RC oscillator (IRC). Select one of such modes by programming the OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC2	OSC1	OSC0
ERC ¹ (External RC oscillator mode); P52/OSCO act as P52	0	0	0
ERC ¹ (External RC oscillator mode); P52/OSCO act as OSCO	0	0	1
IRC ² (Internal RC oscillator mode); P52/OSCO act as P52	0	1	0
IRC ² (Internal RC oscillator mode); P52/OSCO act as OSCO	0	1	1
LXT1 ³ (Frequency range of XT mode is 1MHz~100kHz)	1	0	0
HXT1 ³ (Frequency range of XT mode is 16MHz~6MHz)	1	0	1
LXT2 ³ (Frequency range of XT mode is 32kHz)	1	1	0
HXT2 ³ (Frequency range of XT mode is 6MHz~1MHz) (default)	1	1	1

¹ In ERC mode, OSC1 is used as oscillator pin. OSCO/P52 is defined by code option Word 0 Bit 6 ~ Bit 4.

² In IRC mode, P53 is normal I/O pin. OSCO/P52 is defined by code option Word 0 Bit 6 ~ Bit 4.

³ In LXT1, LXT2, HXT1 and HXT2 modes; OSC1 and OSC0 are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

The maximum operating frequency limit of the crystal/resonator at different VDDs, are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.1	4
	3.0	8
	4.5	16

6.8.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P220N can be driven by an external clock signal through the OSCO pin as illustrated below.

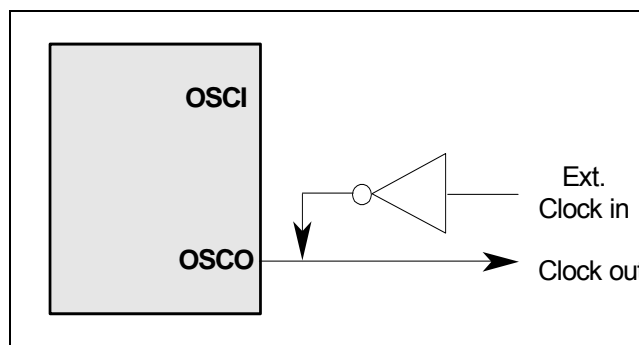


Figure 6-13 External Clock Input Circuit

In most applications, Pin OSC1 and Pin OSC0 can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-17 below depicts such circuit. The same applies to the HXT 1, 2 modes and the LXT 1, 2 modes.

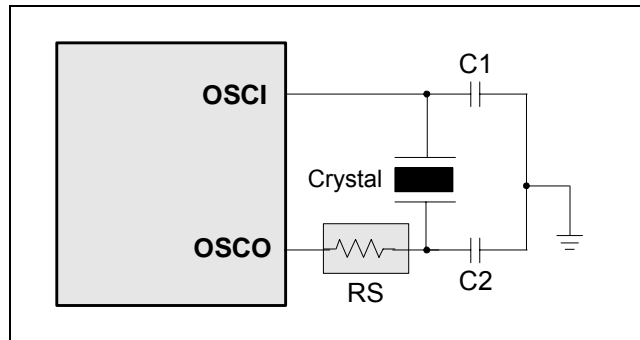


Figure 6-14 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, user should refer to the resonator specifications for appropriate values of C1 and C2. RS, a serial resistor, may be required for AT strip cut crystal or low frequency mode. Figure 6-13-1 is PCB layout suggestion. When the system works in Crystal mode (16 MHz), a 10 KΩ is connected between OSC1 and OSC0.

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT (100K~1 MHz)	100kHz	67pF	67pF
		200kHz	30pF	30pF
		455kHz	30pF	30pF
		1 MHz	30pF	30pF
	HXT (1~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	20pF	20pF
	LXT1 (100K~1 MHz)	100kHz	67pF	67pF
		200kHz	30pF	30pF
		455kHz	30pF	30pF
		1 MHz	30pF	30pF
	HXT2 (1~6 MHz)	455kHz	30pF	30pF
		1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	30pF	30pF
		6.0 MHz	30pF	30pF
		6.0 MHz	30pF	30pF
	HXT1 (6~16 MHz)	8.0 MHz	30pF	30pF
		12.0 MHz	30pF	30pF
		16.0 MHz	15pF	15pF
16.0 MHz		15pF	15pF	

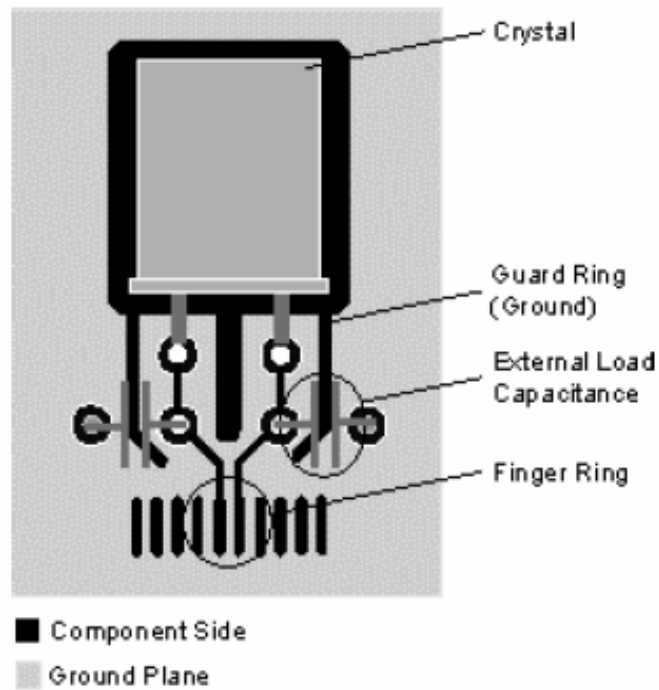


Figure 6-15 Parallel Mode Crystal/Resonator Circuit Diagram

6.8.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 6-16) could offer a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

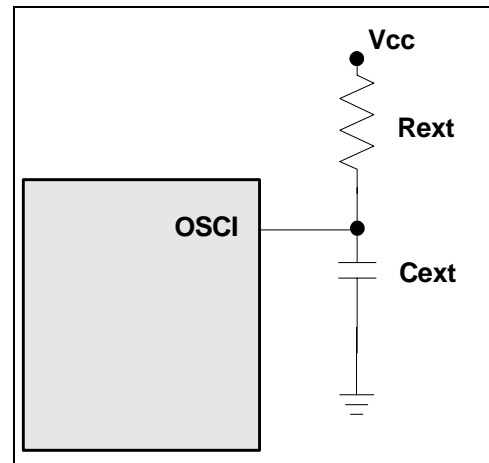


Figure 6-16 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and the value of Rext should not be greater than 1MΩ. If the frequency cannot be kept within this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot discharge the capacitance current correctly.

Based on the above reasons, it must be kept in mind that all the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB is layout, have certain effect on the system frequency.

The RC Oscillator frequencies:

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140kHz	140kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850kHz	820kHz
	10k	450kHz	450kHz
	100k	48kHz	50kHz
300 pF	3.3k	560kHz	540kHz
	5.1k	370kHz	360kHz
	10k	196kHz	192kHz
	100k	20kHz	20kHz

Note: ¹: Measured based on DIP packages.
²: The values are for design reference only.
³: The frequency drift is ± 30%