EM78F602N

8-Bit Microprocessor

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Release version	2011/01/11

1 General Description

The EM78F602N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology and high noise immunity. It has an on-chip 2K×13-bit Electrical Flash Memory and 256×8-bit in-system programmable EEPROM. It provides three protection bits to prevent intrusion of user's Flash memory code. Some Code option bits are also available to meet user's requirements.

With its enhanced Flash-ROM features, the EM78F602N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the Writer to easily program his development code.

2 Features

- CPU configuration
  - 2K×13 bits on-chip Flash memory
  - 144×8 bits on-chip registers (SRAM)
  - 256 bytes in-system programmable EEPROM Endurance: 1,000,000 write/erase cycles
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - 3 programmable Level Voltage Reset LVR: 4.0V, 3.5V, 2.7V
  - Less than 1.5 mA at 5V / 4 MHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - 1 bidirectional I/O ports: P6
  - 6 I/O pins
  - Wake-up port: P6
  - 5 programmable pull-high I/O pins
  - 6 programmable pull-down I/O pins
  - 5 programmable open-drain I/O pins
  - External interrupt with Wake-up: P60
- Operating voltage range
  - 2.4V~5.5V at -40°C~85°C (Industrial)
  - 2.2V~5.5V at 0°C~70°C (Commercial)
- Operating frequency range (base on two clocks)
  - IRC modes:DC~4MHz @ 2.2V~5.5V,
    DC~8 MHz @ 3V~5.5V,
    DC~16 MHz @ 4.5V~5.5V

Internal RC Frequency	Drift Rate			
	Temperature (-40℃~85℃)	Voltage (2.4V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 2.5%	± 10.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16.5kHz	± 3%	± 5%	± 4.5%	± 12.5%

- Fast power-on set-up time requires only 2ms in 4 MHz IRC mode from initial power-on condition
- Fast wake-up time requires only 3μs in 4 MHz IRC mode from sleep mode to normal mode
- Six available interrupts
  - Internal interrupt: 3
  - External interrupt: 3
- One set of comparator (offset voltage: smaller than 5 mV)
- One 8-bit Timer/Counter
  - TC3: Timer/Counter/PDO (programmable divider output)/PWM (pulse width modulation)
- One 16-bit Timer/Counter
  - TC2: Timer/Counter/Window
- Peripheral configuration
  - 8-bit real time clock (TCC) with overflow interrupt
  - External interrupt input pin
  - CPU operation modes: Normal, Green, Idle, and Power down (Sleep)
  - High EFT immunity
  - Table read (TBRD) instruction
- Six available interrupts
  - TCC, TC2, TC3 overflow interrupt
  - External interrupt
  - Port 6 pin status changed interrupt
  - Comparator status change interrupt
- Single instruction cycle command with 2 clocks.
- Special Features
  - Programmable free running Watchdog Timer
  - Power-on voltage detector available (2.0V ~ 2.1V)
- Package Type:
  - 10-pin MSOP 118 mil : EM78F602NMS10AJ/S

Note: *These are Green products which do not contain hazardous substances.*

3 Pin Assignment

(1) 10-Pin MSOP

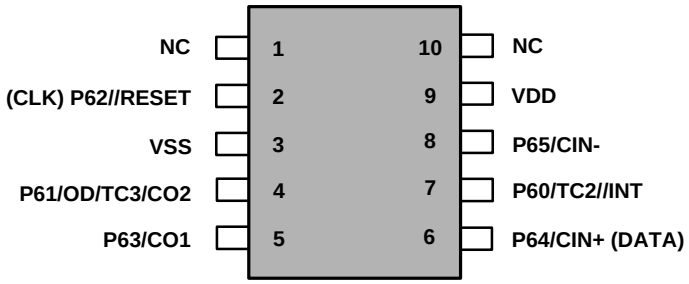


Figure 3-1 10-Pin EM78F602N

4 Pin Description

Name	Function	Input Type	Output Type	Description
P60/TC2//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TC2	ST	–	Timer 2 clock input
	/INT	ST	–	External interrupt pin
P61/OD/TC3/CO2	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pin change wake-up
	OD	–	CMOS	Internal open-drain output pin
	TC3	ST	–	Timer 3 clock input
	CO2	–	CMOS	Output 2 of Comparator
P62//RESET	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	/RESET	ST	–	Internal pull-high reset pin
(CLK)	**(CLK)**	ST	–	Clock pin for Writer programming
P63/CO1	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	CO1	–	CMOS	Output 1 of Comparator
P64/CIN+	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	CIN+	AN	–	Non-inverting end of Comparator
(DATA)	**(DATA)**	ST	CMOS	DATA pin for Writer programming
P65/CIN-	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	CIN-	AN	–	Inverting end of Comparator
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

Legend: ST: Schmitt Trigger input AN: Analog pin
CMOS: CMOS output

5 Block Diagram

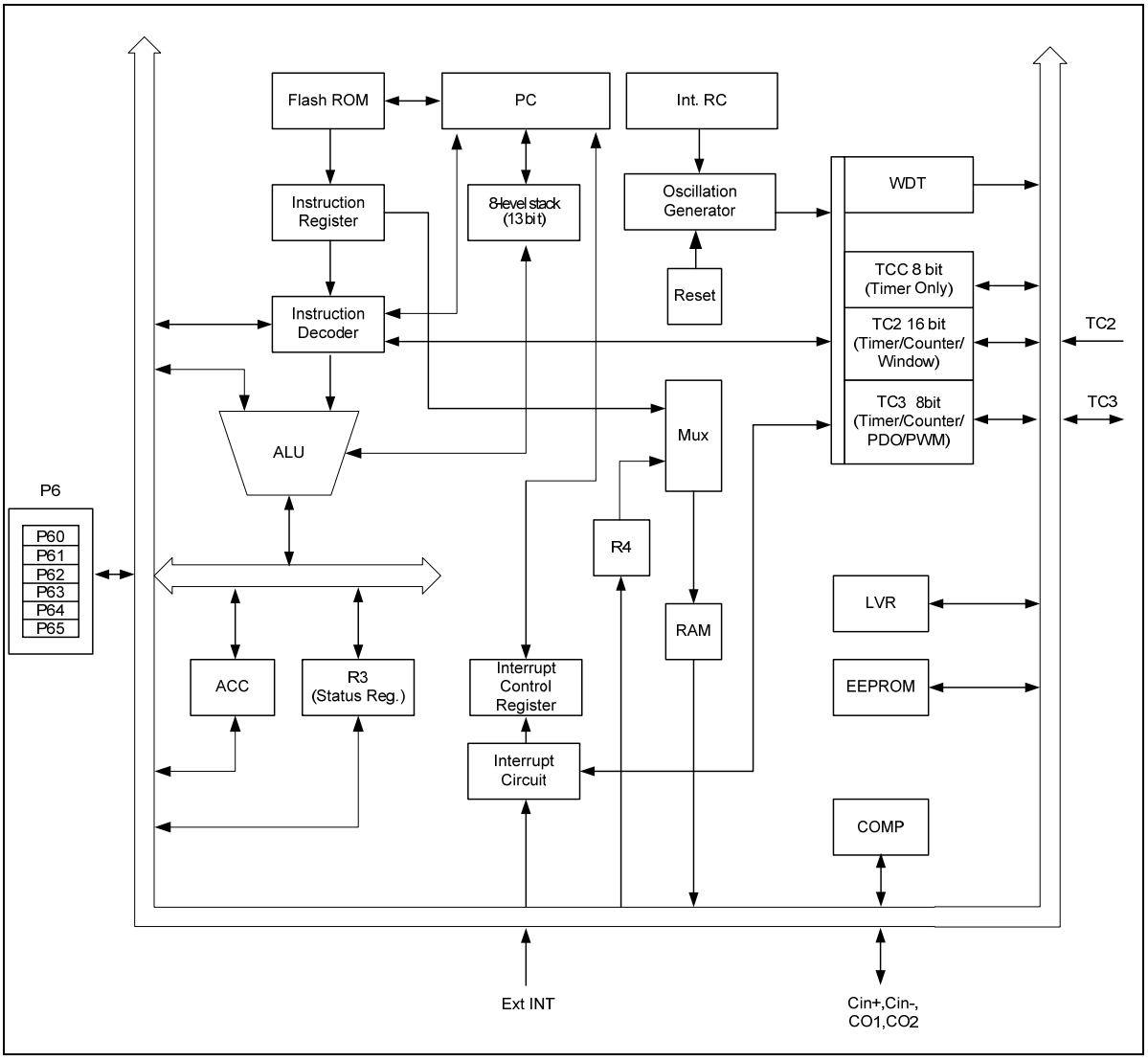


Figure 5-1 EM78F602N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock)

R1 is incremented by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC If the PSTE bit (CONT-3) is reset. The content of the prescaler counter is cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter and Stack)

- Depending on the device type, R2 and hardware stack are 11-bit wide. The structure is depicted in Figure 6-1 below.
- The configuration structure generates 2K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all **"0"**s when under a reset condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 11 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 2K (2^{11}).
- "LCALL" instruction loads the lower 11 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 2K (2^{11}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC will remain unchanged.

- Any instruction (except “ADD R2,A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6") will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

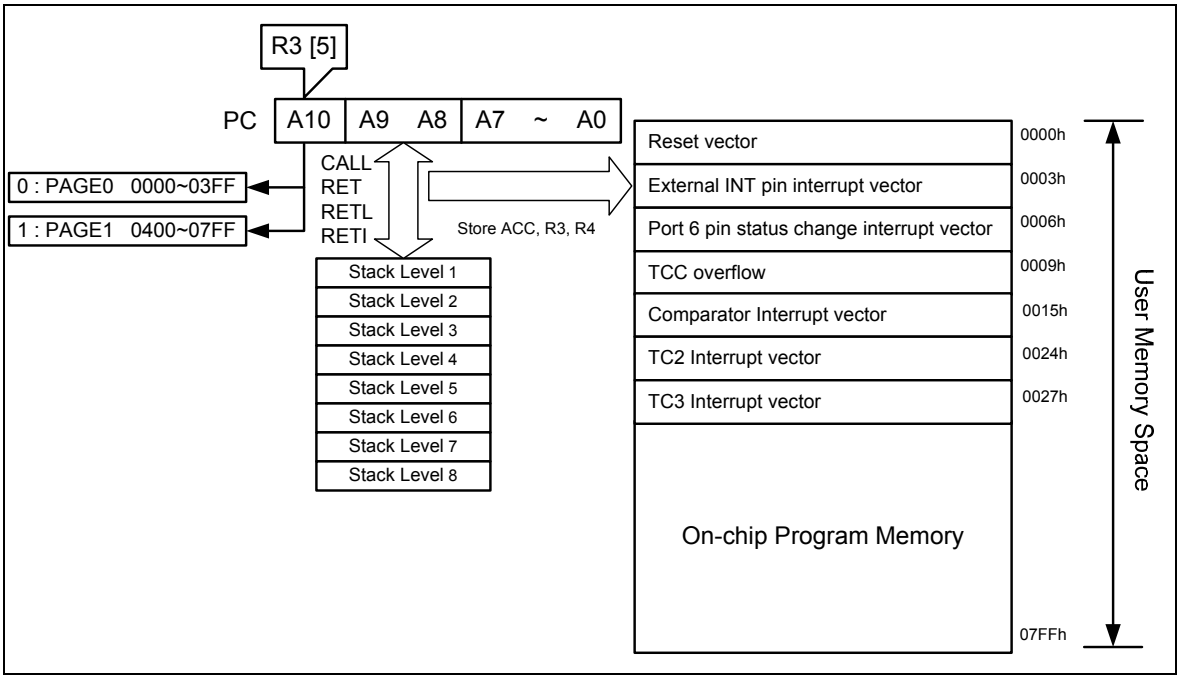


Figure 6-1 Program Counter Organization

6.1.3.1 Data Memory Configuration

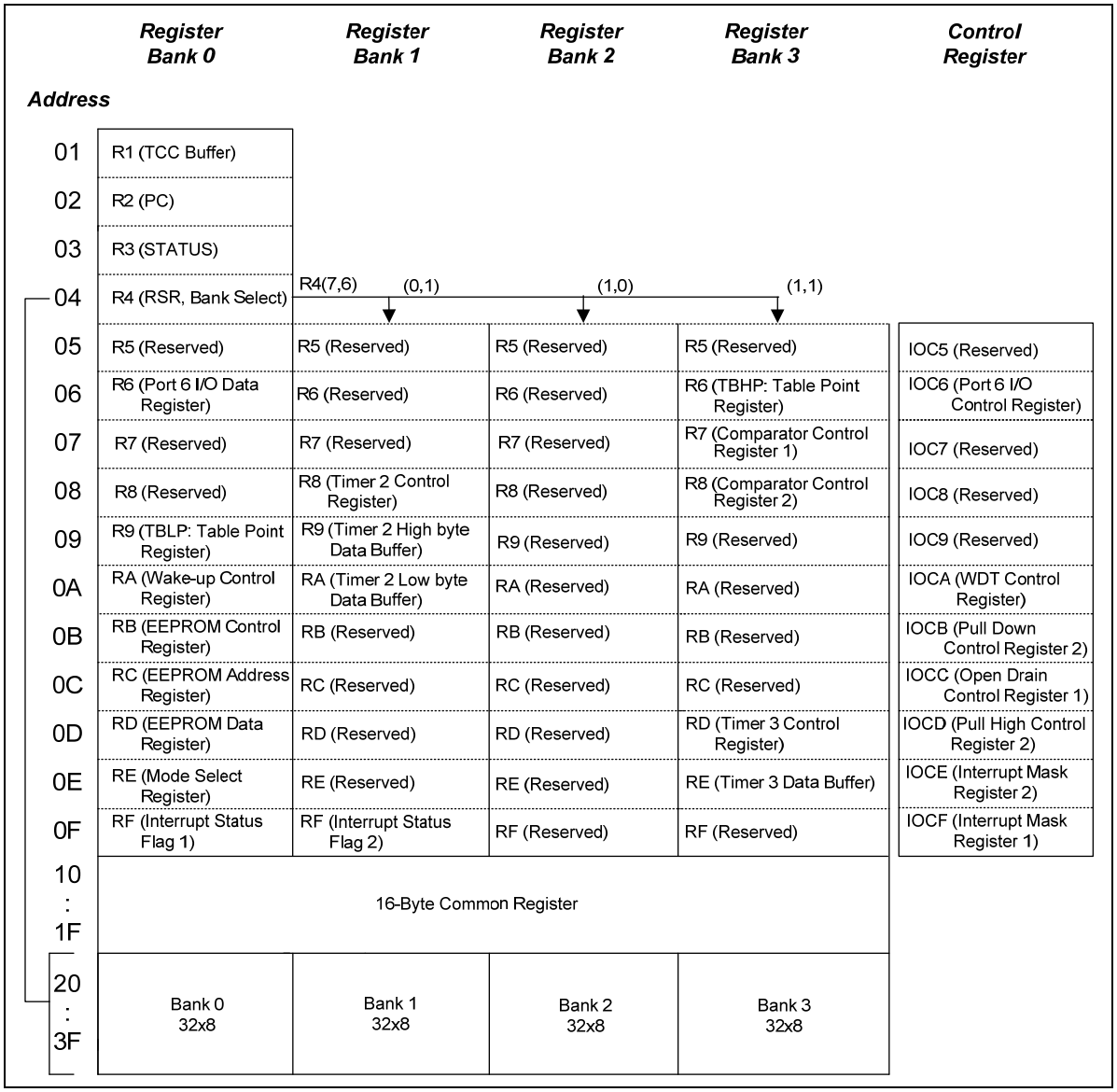


Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PS0	T	P	Z	DC	C

Bits 7 ~ 6: Not used. Set to "**0**" at all time.

Bit 5 (PS0): Page bits (Read Only)

PS0	Program Memory Page [Address]
0	Page 0 [0000-03FF]
1	Page 1 [0400-07FF]

Bit 4 (T): Time-out bit

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to "**1**" during power-on or by a "WDTC" command and reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

Bits 5 ~ 0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data memory configuration in Figure 6-2.

6.1.6 Bank 0 R6 (Port 6)

R6 are I/O registers.

6.1.7 Bank 0 R9 (TBLP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

Bits 7 ~ 0: These are the least 8 significant bits of address for program code.

NOTE

- *Bank 0 R9 overflow will carry to Bank 3 R6.*
- *Bank 0 R9 underflow will borrow from Bank 3 R6.*

6.1.8 Bank 0 RA (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPWE	ICWE	–	EXWE	–	–	–	–

Bit 7 (CMPWE): Wake-up enable bit

0: Disable Comparator wake-up

1: Enable Comparator wake-up

When the Comparator output status change is used to enter an interrupt vector or to wake-up the EM78F602N from Sleep mode, the CMPWE bit must be set to "Enable."

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0: Disable Port 6 input status change wake-up

1: Enable Port 6 input status change wake-up

Bit 5: Not used. Set to "**0**" at all time.

Bit 4 (EXWE): External /INT wake-up enable bit

0: Disable External /INT pin wake-up

1: Enable External /INT pin wake-up

Bits 3 ~ 0: Not used. Set to "**0**" at all time.

6.1.9 Bank 0 RB (EEPROM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	–	–	–

Bit 7 (RD): Read control register

0: Does not execute EEPROM read

1: Read EEPROM contents (RD can be set by software. RD is cleared by hardware after Read instruction is completed).

Bit 6 (WR): Write control register

0: Write cycle to the EEPROM is completed.

1: Initiates a write cycle (WR can be set by software. WR is cleared by hardware after Write cycle is completed).

Bit 5 (EEWE): EEPROM Write Enable bit.

0: Prohibits write to the EEPROM

1: Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detect Flag

0: Write cycle is completed

1: Write cycle is unfinished

Bit 3 (EEPC): EEPROM power-down control bit

0: Switch off the EEPROM

1: EEPROM is operating

Bits 2 ~ 0: Not used. Set to "**0**" at all time.

6.1.10 Bank 0 RC (256 Bytes EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_A7	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 7 ~ 0: 256 bytes EEPROM address

6.1.11 Bank 0 RD (256 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 256 bytes EEPROM data

6.1.12 Bank 0 RE (Mode Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CPUS	IDLE	TCCSS	-	TC2SS	TC3SS

Bits 7 ~ 6: Not used. Set to "**0**" at all time.

Bit 5 (CPUS): CPU Oscillator Source Select.

0: Fs : Sub frequency for WDT internal RC time base

1: Fm : Main-oscillator clock

When CPUS=0, the CPU oscillator selects the Sub-oscillator and the Main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit.

0: IDLE="0" + SLEP instruction → Sleep mode

1: IDLE="1" + SLEP instruction → Idle mode

■ **CPU Operation Mode**

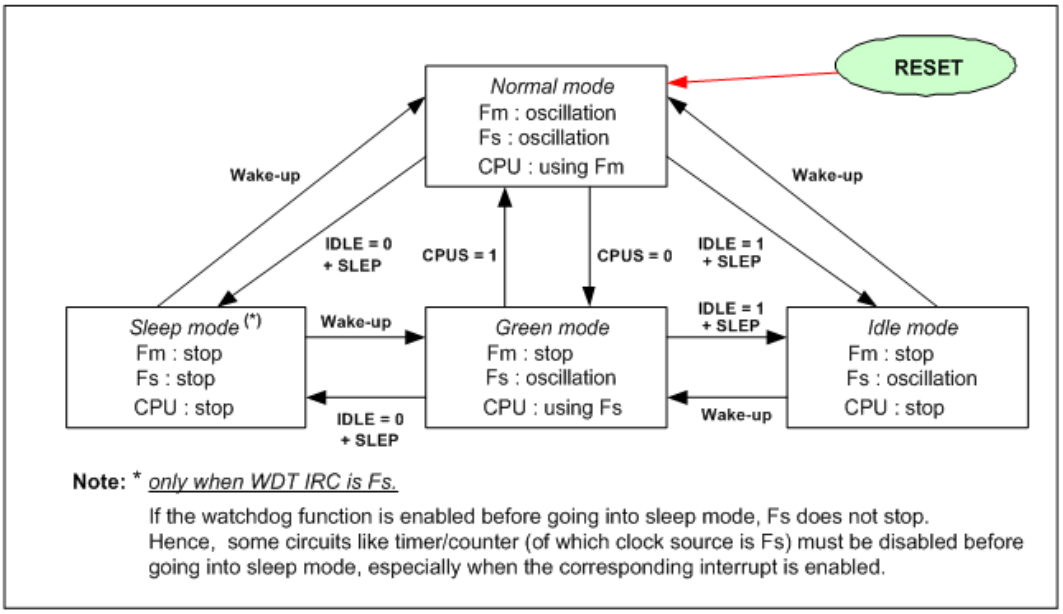


Figure 6-3 CPU Operation Mode

Oscillator (Normal Mode Source)	CPU Mode Status	Oscillator Stable Time (S) [1]	Count from Normal/Green (CLK) [2]
IRC ; 4M, 8M, 16 MHz	Sleep/Idle → Normal	< 2 µs	8 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	

[1] *The oscillator stable time depends on the oscillator characteristics.*

[2] *After the oscillator has stabilized, the CPU will count 8 CLK in Normal or Green mode and continue to work in Normal or Green mode respectively.*

Ex 1: The 4 MHz IRC wakes-up from Sleep mode to Normal mode. The total wake-up time is 2 µs + 8 CLK @ 4 MHz.

Ex 2: The 4 MHz IRC wakes-up from Sleep mode to Green mode. The total wake-up time is 100 µs + 8 CLK @ 16.5kHz.

Bit 3 (TCCSS): TCC clock source select.

0: Fs is used as Fc

1: Fm is used as Fc

Bit 2: Not used, set to "0" at all time.

Bit 1 (TC2SS):TC2 clock source select.

0: Fs is used as Fc

1: Fm is used as Fc

Bit 0 (TC3SS):TC3 clock source select.

0: Fs is used as Fc

1: Fm is used as Fc

6.1.13 Bank 0 RF (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

Bits 7 ~ 3: Not used, set to "**0**" at all time

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, reset by software.

0: No interrupt occurs

1: Interrupt request

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

0: No interrupt occurs

1: Interrupt request

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

0: No interrupt occurs

1: Interrupt request

NOTE

- *RF can be cleared by instruction but cannot be set.*
- *IOCF is the interrupt mask register.*
- *The result of reading RF is the "logic AND" of RF and IOCF.*

6.1.14 R10 ~ R3F

All are 8-bit general-purpose registers.

6.1.15 Bank 1 R8 TC2CR (Timer 2 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCM1	RCM0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bits 7 ~ 6 (RCM1: 0): IRC mode select bits

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	x	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
16 MHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6 μs
	0	1	16 MHz ± 2.5%	4.5V ~ 5.5V	< 1.25 μs
	1	x	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
8 MHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	x	8 MHz ± 2.5%	3.0V ~ 5.5V	< 2.5 μs

NOTE

- *The initial values of Bank 1 R8<7,6> are kept the same as EEWORD0<7,6>.*
- *If you change the IRC frequency from **A**-frequency to **B**-frequency, the MCU needs to wait for some time for it to work. The waiting time corresponds to the **B**-frequency.*

Example:

1st Step**:** When user selects the 4 MHz at the Writer, the initial values of Bank 1 R8<7,6> would be “00”, the same as the value of EEWORD0<7,6> is “00”. If the MCU is free-running, it will work at 4 MHz ± 2.5%. Refer to the table below.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	x	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs

2nd Step: If it is desired to set Bank 1 as R8<7,6> = "**01**" while the MCU is working at 4 MHz ± 2.5%, the MCU needs to hold for 1.5 μs, then it will continue to work at 16 MHz ± 10%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 μs
	0	**1**	**16 MHz ± 10%**	4.5V ~ 5.5V	< 1.5 μs
	1	x	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs

3rd Step: If it is desired to set Bank 1 as R8<7,6> = "**1x**" while the MCU is working at 16 MHz ± 10%, the MCU needs to hold for 3 μs, then it will continue to work at 8 MHz ± 10%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	**x**	**8 MHz ± 10%**	3.0V ~ 5.5V	< 3 μs

4th Step: If it is desired to set Bank 1 R8<7,6> = "**00**" while the MCU is working at 8 MHz ± 10%, the MCU needs to hold for 5 μs, then it will continue to work at 4 MHz ± 2.5%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	x	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs

Bit 5 (TC2ES): TC2 signal edge

0: Increment if a transition from low to high (rising edge) takes place on the TC2 pin.

1: Increment if a transition from high to low (falling edge) takes place on the TC2 pin.

Bit 4 (TC2M): TC2 mode select

0: Timer/Counter mode

1: Window mode

Bit 3 (TC2S): TC2 start control

0: Stop and counter clear

1: Start

Bit 2 ~ Bit 0 (TC2CK2 ~ TC2CK0): TC2 clock source select

TC2CK2	TC2CK1	TC2CK0	Clock Source	Resolution	Max. Time	Resolution	Max. Time
			Normal	Fc=4M	Fc=4M	Fc=16.5K	Fc=16.5K
0	0	0	Fc/223	2.1 sec	38.2 hr	508.4 s	9255 hr
0	0	1	Fc/213	2.048 ms	134.22 sec	496.48 ms	32537.3 s
0	1	0	Fc/28	64 μs	4.194 sec	15.515 ms	1016.79 s
0	1	1	Fc/23	2 μs	131.072 ms	0.484 ms	31719 ms
1	0	0	Fc	250 ns	16.384 ms	0.0606 ms	3971 ms
1	0	1	–	–	–	–	–
1	1	0	–	–	–	–	–
1	1	1	External clock (TC2 pin)	–	–	–	–

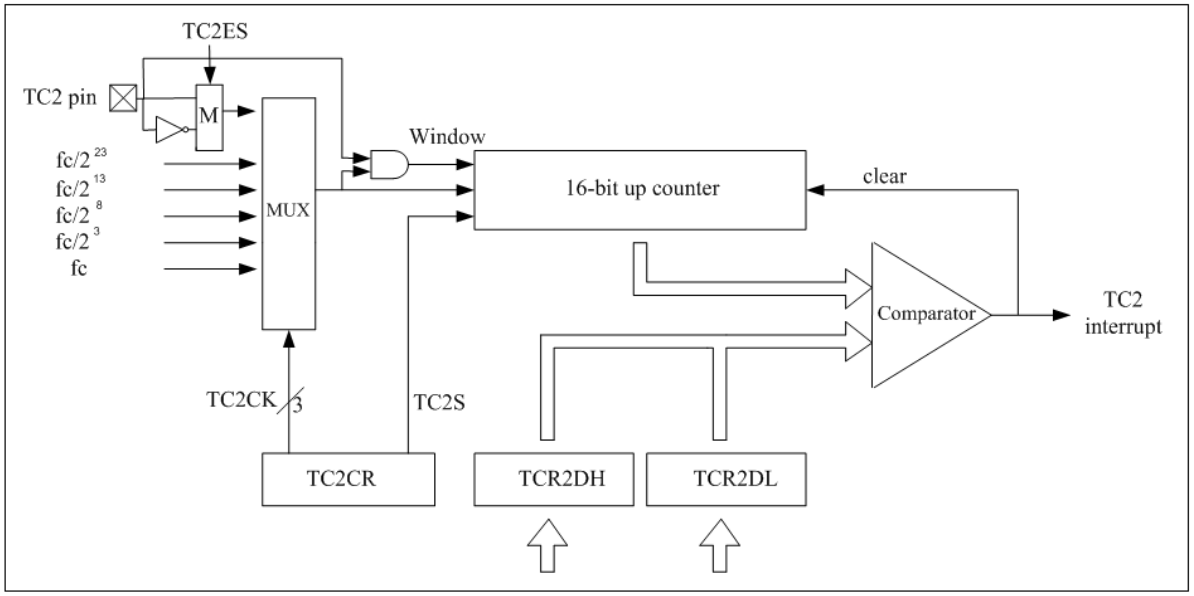


Figure 6-4 TC2 Configuration

In **Timer mode,** counting up is performed using an internal clock. When the contents of the up-counter match the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

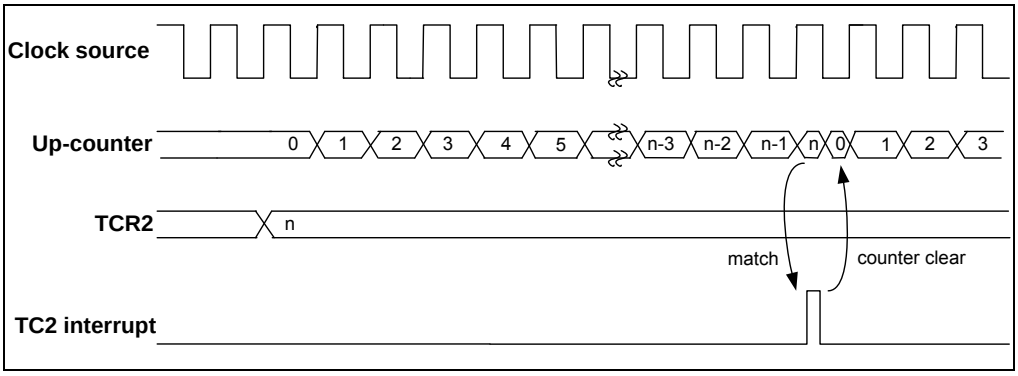


Figure 6-5 Timer Mode Timing Chart

In **Counter mode,** counting up is performed using an external clock input pin (TC2) and either rising or falling edge can be selected by setting TC2ES. When the contents of the up-counter match the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

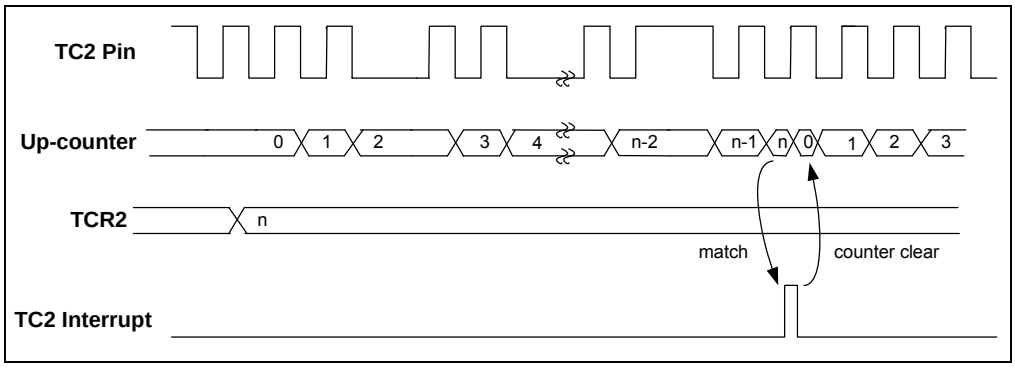


Figure 6-6 Counter Mode Timing Chart

In **Window mode,** counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of the up-counter match with the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

In Writing to the TCR2DL, comparison is inhibited until TCR2DH is written.

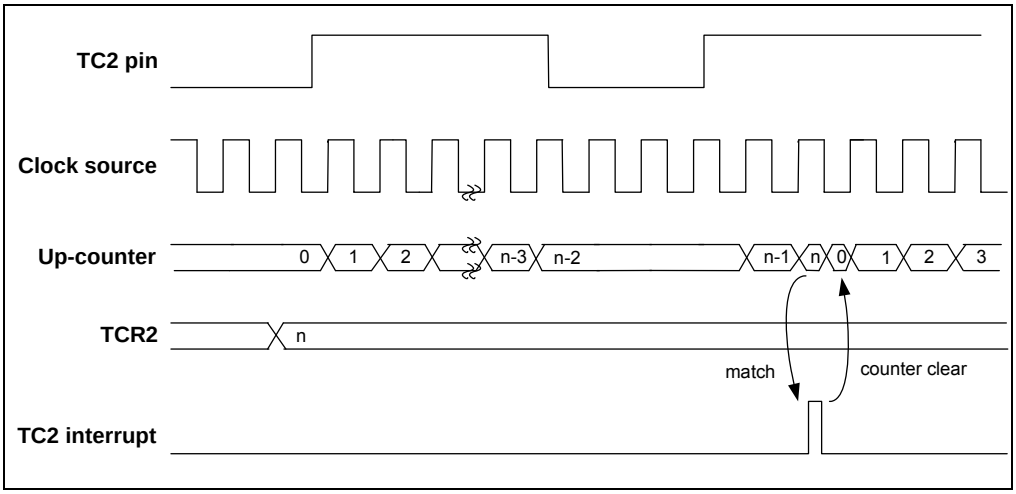


Figure 6-7 Window Mode Timing Chart

6.1.16 Bank 1 R9 TC2DH (Timer 2 High Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8

Bit 7 ~ Bit 0 (TCR2D15 ~ TCR2D8): High byte data buffer of 16-bit TC2

6.1.17 Bank 1 RA TC2DL (Timer 2 Low Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0

Bit 7 ~ Bit 0 (TC2D7 ~ TC2D0): Low byte data buffer of 16-bit TC2

6.1.18 Bank 1 RF (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIF	-	TC3IF	TC2IF	-	-	-	-

Bit 7 (CMPIF): Comparator Interrupt Flag. Set when a change occurs in the Comparator output, reset by software.

Bit 6: Not used, set to "**0**" at all time

Bit 5 (TC3IF): 8-bit TC3 Interrupt Flag

Bit 4 (TC2IF): 16-bit TC2 Interrupt Flag

Bits 3 ~ 0: Not used, set to "**0**" at all time

NOTE

The Interrupt flag is automatically set by hardware. It must be cleared by software.

6.1.19 Bank 3 R6 (TBHP: Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	-	RBit10	RBit9	RBit8

Bit 7 (MLB): Select MSB or LSB machine code to be moved to register. The machine code is pointed by TBLP and TBHP register.

Bits 6 ~ 3: Not used, set to "**0**" at all time.

Bits 2 ~ 0: These are the 3 most significant bits of address for program code.

6.1.20 Bank 3 R7 (CMPCON1: Comparator Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	COS1	COS0	CO2EN	CO1EN

Bits 7 ~ 4: Not used, set to "**0**" at all time.

Bits 3~2 (COS1: 0): Comparator Select bits

COS1	COS0	Function Description
0	0	Comparator OFF. P64/CIN+, P65/CIN-, P63/CO1, P61/CO2, 4 pins act as normal I/O pin. CO2EN and CO1EN, two bits fixed to "0".
0	1	Act as Comparator. Comparator inverting input connects to 1/2*VDD. Comparator non-inverting input connects to P64/CIN+ pin. P65/CIN- pin act as normal I/O pin. For the two pins P63/CO1, P61/CO2, refer to the two bits CO2EN and CO1EN descriptions below.
1	0	Act as Comparator. Comparator inverting input connects to 1/4*VDD. Comparator non-inverting input connects to P64/CIN+ pin. P65/CIN- pin act as normal I/O pin. For the two pins P63/CO1, P61/CO2, refer to the two bits CO2EN and CO1EN descriptions below.
1	1	Act as Comparator. Comparator inverting input connects to P65/CIN- pin. Comparator non-inverting input connects to P64/CIN+ pin. For the two pins P63/CO1, P61/CO2, refer to the two bits CO2EN and CO1EN descriptions below.

Bit 1 (CO2EN): Control bit is used to enable the comparator output of P61/CO2 pin.

0: P61/CO2 pin act as normal I/O pin

1: P61/CO2 pin act as comparator output pin

NOTE

*When COS1:0 = 00, this bit is fixed to "**0**"*

Bit 0 (CO1EN): Control bit is used to enable the comparator output of P63/CO1 pin.

0: P63/CO1 pin act as normal I/O pin

1: P63/CO1 pin act as comparator output pin

NOTE

*When COS1:0 = 00, this bit is fixed to "**0**"*

6.1.21 Bank 3 R8 (CMPCON2: Comparator Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	CPOUT	-	-	-	-

Bits 7 ~ 5: Not used, set to "**0**" at all time.

Bit 4 (CPOUT): The result of Comparator output (Read Only)

Bits 3 ~ 0: Not used, set to "**0**" at all time.

6.1.22 Bank 3 RD TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7 ~ 6 (TC3FF1 ~ TC3FF0): TC3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): TC3 start control

0: Stop and clear the counter

1: Start

Bits 4 ~ 2 (TC3CK2 ~ TC3CK0): TC3 clock source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time	Resolution	Max. Time
			Normal	Fc=4M	Fc=4M	Fc=16.5K	Fc=16.5K
0	0	0	Fc/211	512 µs	131072 µs	124 ms	31744 ms
0	0	1	Fc/27	32 µs	8192 µs	7.75 ms	1984 ms
0	1	0	Fc/25	8 µs	2048 µs	1.93 ms	494 ms
0	1	1	Fc/23	2 µs	512 µs	484 µs	123.9 ms
1	0	0	Fc/22	1 µs	256 µs	242 µs	61.95 ms
1	0	1	Fc/21	500 ns	128 µs	121 µs	30.97 ms
1	1	0	Fc	250 ns	64 µs	60.6 µs	15.51 ms
1	1	1	External clock (TC3 pin)	-	-	-	-

Bits 1 ~ 0 (TC3M1 ~ TC3M0): TC3 operating mode select

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider Output
1	1	Pulse Width Modulation Output

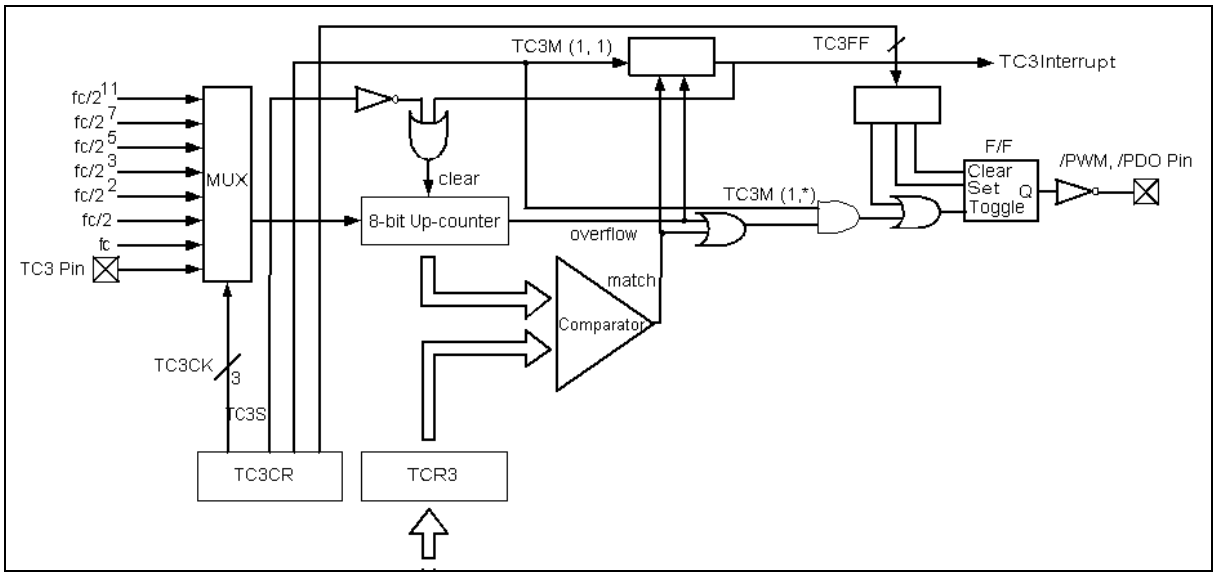


Figure 6-8 TC3 Configuration

In Timer mode, counting up is performed using internal clock (rising edge trigger). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using external clock input pin (TC3 pin). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by the program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

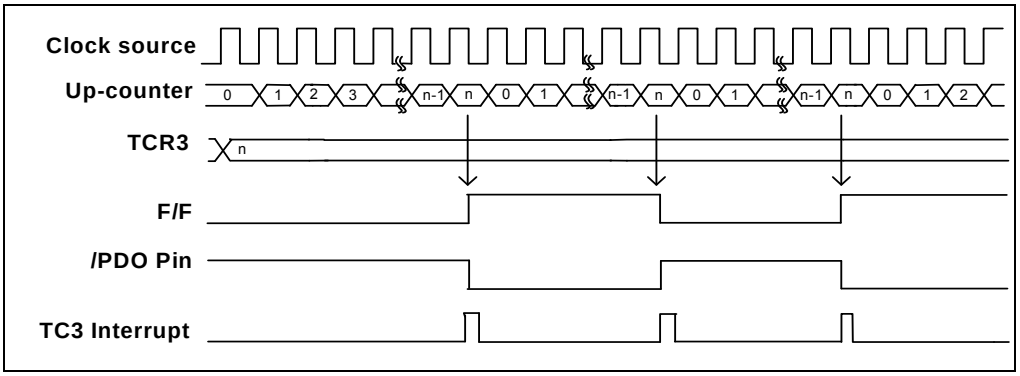


Figure 6-9 PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output Mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. The counter continues counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. Also, after data is loaded to TCR3, the TCR3 (Bit 5) has to be shifted first by setting TC3S to "**1**".

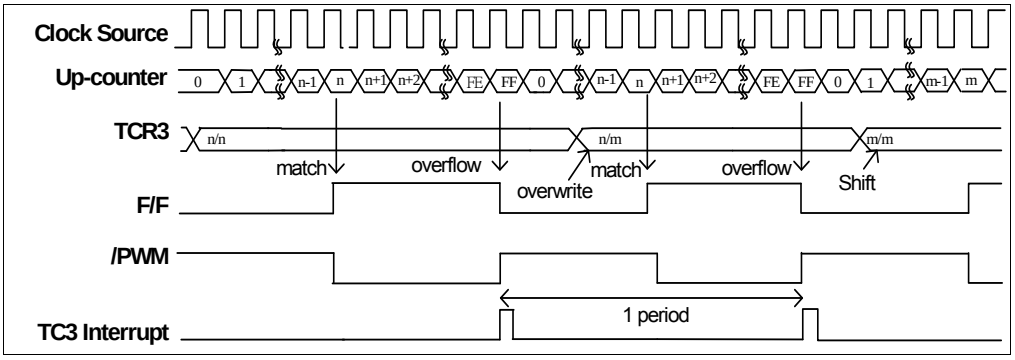


Figure 6-10 PWM Mode Timing Chart

6.1.23 Bank 3 RE TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bits 7 ~ 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit TC3

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand on hold, usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/INT	-	-	PSTE	PST2	PST1	PST0

Bit 7: Not used, set to "**0**" at all time.

Bit 6 (/INT): Interrupt enable flag

0: Masked by DISI or hardware interrupt

1: Enabled by ENI/RETI instructions

Bits 5~4: Not used, set to "**0**" at all time.

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit, TCC rate is 1:1.

1: Prescaler enable bit, TCC rate is set as Bit 2~Bit 0.

Bit 2 ~ Bit 0 (PST 2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

NOTE

The CONT register is both readable and writable.

6.2.3 IOC6 (I/O Port Control Register)

A value of "**1**" sets the relative I/O pin into high impedance, while "**0**" defines the relative I/O pin as output.

IOC6 registers are both readable and writable.

6.2.4 IOC5, IOC7~9

Reserved registers

6.2.5 IOCA (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	INTE1	INTE0	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of P60 (/INT) pin

0: P60, bidirectional I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "**1**".

When EIS is "**0**", the path of /INT is masked. When EIS is "**1**", the status of the /INT pin can also be read by way of reading Port 6 (R6).

The EIS is both readable and writable.

Bits 5 ~ 4 (INTE1:0): INT signal edge

INTE1	INTE0	Function Description
0	x	Interrupt occurs at a rising edge of the P60/INT pin
1	0	Interrupt occurs at a falling edge of the P60/INT pin
1	1	Interrupt occurs at a rising and falling edge of the P60/INT pin

Bit 3 (PSWE): Prescaler enable bit for WDT

0: prescaler disable bit, WDT rate is 1:1

1: prescaler enable bit, WDT rate is set at Bit 0 ~ Bit 2

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.6 IOCB (Pull-down Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	/PD65	/PD64	/PD63	/PD62	/PD61	/PD60

Bits 7 ~ 6: Not used, set to "**0**" at all time.

Bit 5 (/PD65): Control bit used to enable pull-down of the P65 pin

0: Enable internal pull-down

1: Disable internal pull-down

Bit 4 (/PD64): Control bit used to enable pull-down of the P64 pin.

Bit 3 (/PD63): Control bit used to enable pull-down of the P63 pin.

Bit 2 (/PD62): Control bit used to enable pull-down of the P62 pin.

Bit 1 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 0 (/PD60): Control bit used to enable pull-down of the P60 pin.

The IOCB Register is both readable and writable.

6.2.7 IOCC (Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	OD65	OD64	OD63	OD62	-	OD60

Bits 7 ~ 6: Not used, set to "**0**" at all time.

Bit 5 (OD65): Control bit used to enable open-drain output of the P65 pin

0: Disable open-drain output

1: Enable open-drain output

Bit 4 (OD64): Control bit used to enable open-drain output of the P64 pin

Bit 3 (OD63): Control bit used to enable open-drain output of the P63 pin

Bit 2 (OD62): Control bit used to enable open-drain output of the P62 pin

Bit 1: Not used, set to "0" at all time.

Bit 0 (OD60): Control bit used to enable open-drain output of the P60 pin

The IOCC Register is both readable and writable.

6.2.8 IOCD (Pull-high Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	/PH65	/PH64	/PH63	/PH62	-	/PH60

Bits 7 ~ 6: Not used, set to "**0**" at all time.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1: Not used, set to "**0**" at all time.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

6.2.9 IOCE (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIE	-	TC3IE	TC2IE	-	-	-	-

Bit 7 (CMPIE): CMPIF interrupt enable bit

0: Disable CMPIF interrupt

1: Enable CMPIF interrupt

When the Comparator output status changed is used to enter an interrupt vector or enter the next instruction, the CMPIE bit must be set to “Enable“.

Bit 6: Not used, set to “**0**” at all time

Bit 5 (TC3IE): Interrupt enable bit

0: Disable TC3IF interrupt

1: Enable TC3IF interrupt

Bit 4 (TC2IE): Interrupt enable bit

0: Disable TC2IF interrupt

1: Enable TC2IF interrupt

Bits 3~0: Not used, set to “**0**” at all time.

NOTE

■*User must set to “0” Bit 6 of the IOCE register.*

■*The IOCE register is both readable and writable.*

6.2.10 IOCF (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	ICIE	TCIE

Bits 7 ~ 3: Not used, set to “**0**” at all time.

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: Disable TCIF interrupt

1: Enable TCIF interrupt

NOTE

- *You must set Bit 7 of the IOCF register to "**0**".*
- *Individual interrupt is enabled by setting its associated control bit in the IOCF to "**1**".*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.*
- *The IOCF register is both readable and writable.*

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST2~PST0 bits of the CONT register are used to determine the ratio of the TCC prescaler . Likewise, the PSW2~PSW0 bits of the IOCA register are used to determine the prescaler of WDT. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler are cleared by the "WDTC" and "SLEP" instructions. Figure 6-11 below depicts the circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer. The clock source of TCC is internal clock. TCC will be incremented by 1 at Fc clock (without prescaler). **The TCC will stop running when Sleep mode occurs.**

The Watchdog Timer is a free running on-chip WDT RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to the WDTE bit of the IOCA register (Section 6.2.5, *IOCA* (*WDT Control Register)*). With no prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

[1] VDD=5V, WDT time-out period = 15.5ms ± 7.5%
VDD=3V, WDT time-out period = 18ms ± 7.5%.

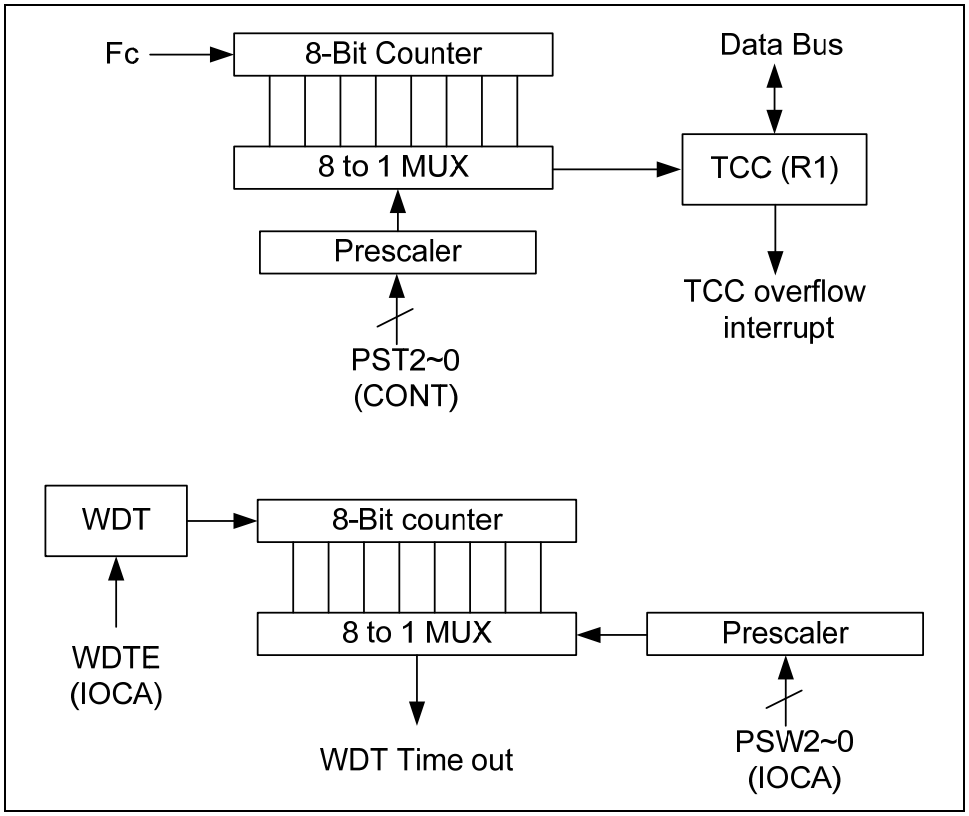


Figure 6-11 TCC and WDT Block Diagram

6.4 I/O Ports

The I/O register, Port 6 is bidirectional tri-state I/O port. P60, P62~P65 can be pulled high internally by software. In addition, P60, P62~P65 can also have open-drain output by software. Port 6 has input status change interrupt (or wake-up) function. P60~P65 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC6).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 6 are shown in Figures 6-12, 6-13 (a), 6-13 (b), and 6-14.

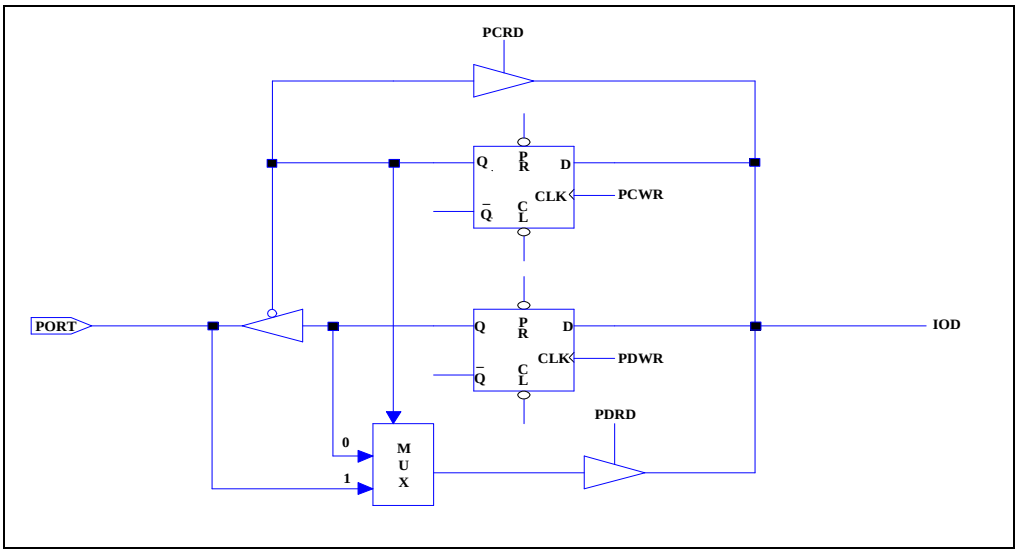


Figure 6-12 I/O Port and I/O Control Register Circuit for Ports 6

Note: Pull-down is not shown in the figure

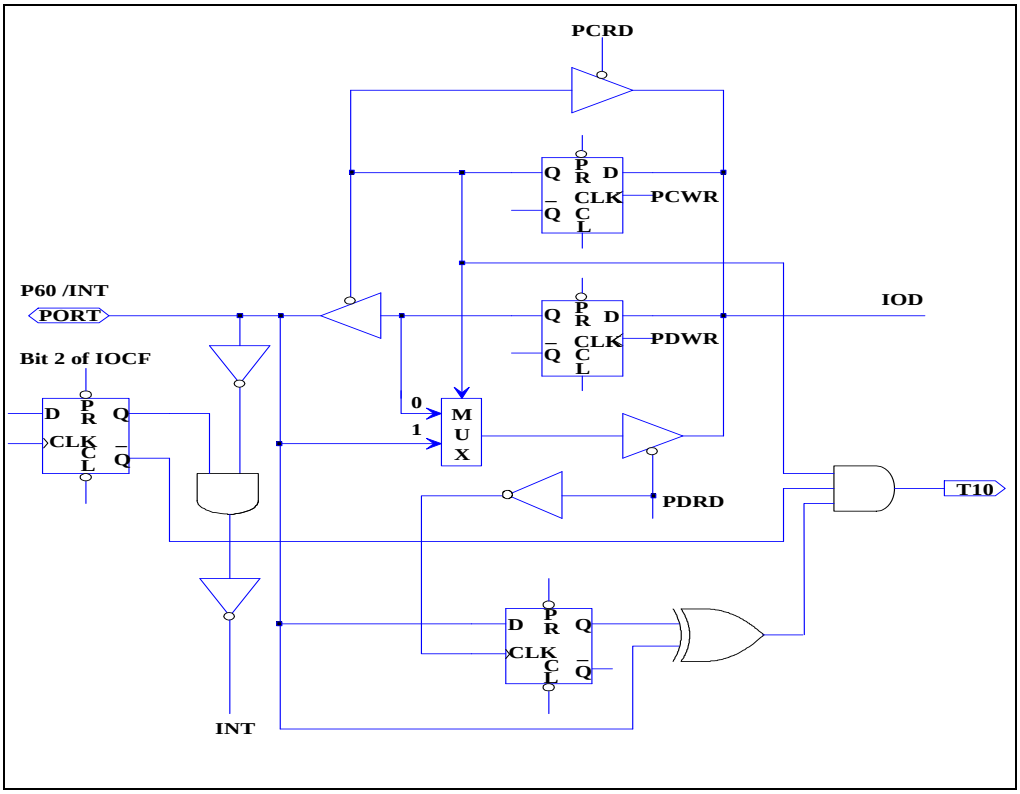


Figure 6-13 (a) I/O Port and I/O Control Register Circuit for P60 (/INT)

Note: Pull-high (down) and Open-drain are not shown in the figure.

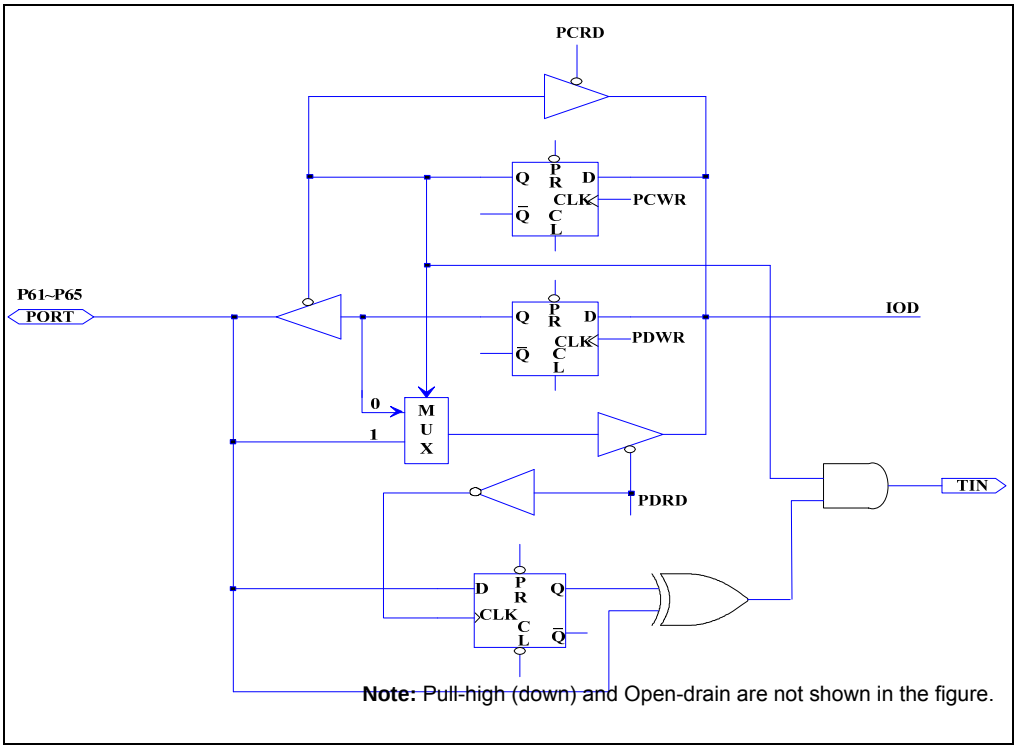


Figure 6-13 (b) I/O Port and I/O Control Register Circuit for P61~P65

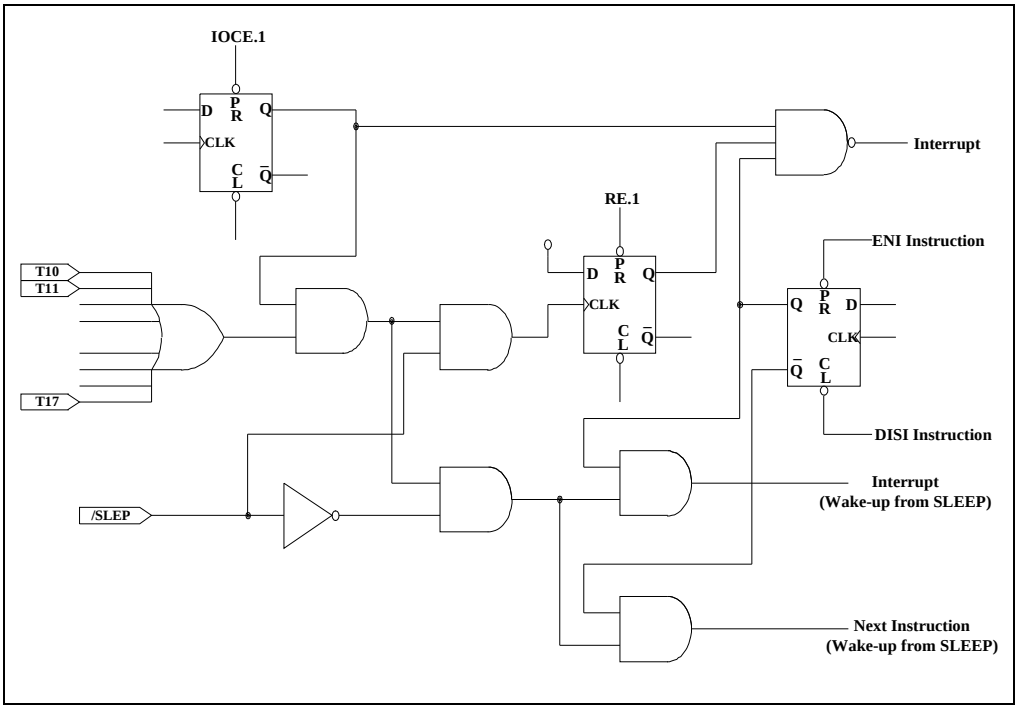


Figure 6-14 Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

1. Wake-up from Port 6 Input Status Change	2 Port 6 Input Status Change Interrupt
a) Before Sleep 1. Disable WDT[2] (use this very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3 a. Enable interrupt (Set IOCF.1). After wake-up, if “ENI”, switch to interrupt vector (006H). If “DISI”, excute next instruction. b. Disable interrupt (Set IOCF.1). Always execute next instruction. 4. Enable wake-up enable bit (Set RA.6) 5. Execute "SLEP" instruction **b) After wake-up** 1. IF "ENI" → Interrupt Vector (006H) 2. IF "DISI" → Next instruction	1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt Vector (006H)

6.5 Reset and Wake-up

6.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events:

(1) Power-on reset

(2) /RESET pin input "low"

(3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 2 ms[3] (one IRC oscillator start-up timer period) after a reset is detected.

- The IRC oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 are cleared.
- The bits of the RB, RC, and RD registers are set to their previous status.
- The bits of the CONT register are set to all "**0**".

[2] The Software disables WDT (Watchdog Timer) but the hardware must be enabled before applying Port 6 Change Wake-Up function (IOCA Bit 7 (WDTE) is set to “**0**”).

[3] Vdd = 5V, set up time period = 2ms ± 10%
Vdd = 3V, set up time period = 2ms ± 10%

- The bits of the IOCA register are set to all "**0**".
- The bits of the IOCB register are set to all "**1**".
- The bits of the IOCC register are set to all "**0**".
- The bits of the IOCD register are set to all "**1**".
- The bits of the IOCE register are set to all "**0**".
- The bits of the IOCF register are set to all "**0**".

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While going into Sleep mode, the WDT (if enabled) is cleared but keeps on running. When waking-up in RC mode, the Wake-up time is 3 μs.

The controller can be awakened by one of the following events:

Event 1: External reset input on /RESET pin

Event 2: WDT time-out (if enabled)

Event 3: Port 6 input status changes (if enabled)

Event 4: Comparator output status change (if CMPWE is enabled)

Event 5: External (P60, /INT) pin changes (if EXWE is enabled)

The first two events (Event1 & 2) will cause the EM78F602N to reset. The T and P flags of R3 can be used to determine the source of the reset (Wake-up). Events 3, 4, and 5 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a Wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Addresses 0×6, 0×15, 0×3 after Wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. When waking-up in RC mode, the Wake-up time is 3 μs.

One or more of Events 2 to 5 can be enabled before entering into Sleep mode. That is**:**

[a] If WDT is enabled before SLEP, all of the RE bits are disabled. Hence, the EM78F602N can be awakened only by Event 1 or Event 2 condition. Refer to the Section 6.6, *Interrupt;* for further details.

[b] If Port 6 Input Status Change is used to Wake-up the EM78F602N and the ICWE bit of the RA register is enabled before SLEP, the WDT must be disabled. Hence, the EM78F602N can be waken-up only by Event 3 condition.

[c] If the Comparator output status change is used to wake-up the EM78F602N and the CMPWE bit of RA register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78F602N can be awaken-up only by Event 4 condition.

[d] If External (P60/INT) pin change is used to wake-up the EM78F602N and the EXWE bit of the RA register is enabled before SLEP, the WDT must be disabled. Hence, the EM78F602N can be waken-up only by Event 5 condition.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78F602N, (as in Condition [b] above), the following instructions must be executed before SLEP:

```
MOV             A, @0xxx1000b   ; Select WDT prescaler and
                                ; disable the WDT
IOW             IOCA
WDTC                            ; Clear WDT and prescaler
MOV             R6, R6          ; Read Port 6
ENI (or DISI)                   ; Enable (or disable) global
                                ; interrupt
BC              R4, 7           ; Select Bank0
BC              R4, 6
MOV             A, @0100xxxxb   ; Enable Port 6 input change
                                ; wake-up bit
MOV             RA,A
MOV             A, @xxxxxx1xb   ; Enable Port 6 input change
                                ; interrupt
IOW             IOCF
SLEP                            ; Sleep
```

Similarly, if the Comparator Interrupt is used to Wake up the EM78F602N (as in Condition [c] above), the following instructions must be executed before SLEP:

```
BS              R4, 7           ; Select Bank 3
BS              R4, 6
MOV             A, @xxxx1111b   ; Select a comparator and P63,
                                ; P61 acts as CO pin
MOV             R7,A
MOV             A, @000xxxxxb   ; CPOUT do not latch with
                                ; /INT pin.
MOV             R8,A
MOV             A, @0xxx1000b   ; Select WDT prescaler and
                                ; disable the WDT
IOW             IOCA
WDTC                            ; Clear WDT and prescaler
ENI (or DISI)                   ; Enable (or disable) global
                                ; interrupt
BC              R4, 7           ; Select Bank 0
BC              R4, 6
MOV             A, @1000xxxxb   ; Enable comparator output status
                                ; change wake-up bit
MOV             RA,A
MOV             A, @10000000b   ; Enable comparator output status
                                ; change interrupt
IOW             IOCE
SLEP                            ; Sleep
```

6.5.1.1 Wake-up and Interrupt Modes Operation Summary

All categories in Wake-up and Interrupt modes are summarized below.

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	If enable EXWE bit: Wake-up+ interrupt (if interrupt enable)+ next instruction	If enable EXWE bit: Wake-up+ interrupt (if interrupt enable)+ next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
Port 6 pin change	If enable ICWE bit: Wake-up+ interrupt (if interrupt enable)+ next instruction	If enable ICWE bit: Wake-up+ interrupt (if interrupt enable)+ next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
TCC overflow interrupt	X	Wake-up+ interrupt (if interrupt enable)+ next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
Comparator (Comparator Output Status Change)	If enable CMPWE bit: Wake-up+ interrupt (if interrupt enable)+ next instruction	If enable CMPWE bit: Wake-up+ interrupt (if interrupt enable)+ next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
TC2 interrupt	X	Wake-up+ interrupt (if interrupt enable)+ next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
TC3 interrupt	X	Wake-up+ interrupt (if interrupt enable)+ next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
WDT Time out	RESET	RESET	RESET	RESET
Low Voltage Reset	RESET	RESET	RESET	RESET

NOTE

After wake up:

1. *If interrupt enabled → interrupt + next instruction*
2. *If interrupt disabled → next instruction*

6.5.1.2 Registers Initialized Values after Reset

The following summarizes the registers initialized values.

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC6	Bit Name	-	-	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	-	INT	-	-	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to interrupt vector address or continue to execute next instruction.							
0×03	R3 (SR)	Bit Name	-	-	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	Bank 1	Bank 0	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×06	R6 (Bank 0)	Bit Name	-	-	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R9 (Bank 0)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 0)	Bit Name	CMPWE	ICWE	-	EXWE	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (ECR) (Bank 0)	Bit Name	RD	WR	EEWE	EEDF	EEPC	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 0)	Bit Name	EE_A7	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 0)	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 0)	Bit Name	-	-	CPUS	IDLE	TCCSS	-	TC2SS	TC3SS
		Power-on	0	0	1	1	1	0	1	1
		/RESET and WDT	0	0	1	1	1	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR) (Bank 0)	Bit Name	-	-	-	-	-	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×08	R8 (Bank 1)	Bit Name	RCM1	RCM0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-on	EEWORD0<7,6>		0	0	0	0	0	0
		/RESET and WDT	EEWORD0<7,6>		0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 1)	Bit Name	TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 1)	Bit Name	TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (Bank 1)	Bit Name	CMPIF	-	TC3IF	TC2IF	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (Bank 3)	Bit Name	MLB	-	-	-	-	RBit10	RBit9	RBit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 3)	Bit Name	-	-	-	-	COS1	COS0	CO2EN	CO1EN
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 3)	Bit Name	-	-	-	CPOUT	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 3)	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 3)	Bit Name	TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0A	IOCA	Bit Name	WDTE	EIS	INTE1	INTE0	PSWE	PSW2	PSW1	PSW0
		Power-un	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	IOCB	Bit Name	-	-	/PD65	/PD64	/PD63	/PD62	/PD61	/PD60
		Power-on	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	IOCC	Bit Name	-	-	OD65	OD64	OD63	OD62	-	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	IOCD	Bit Name	-	-	/PH65	/PH64	/PH63	/PH62	-	/PH60
		Power-on	0	0	1	1	1	1	0	1
		/RESET and WDT	0	0	1	1	1	1	0	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	IOCE	Bit Name	CMPIE	-	TC3IE	TC2IE	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	IOCF	Bit Name	-	-	-	-	-	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×10 : 0×3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: **"×"** = not used **"P"** = previous value before reset

"u" = unknown or don't care **"t"** = check Table 6-5-2-1

6.5.2 Status of T and P of the Status Register

A reset condition is initiated by one of the following events**:**

1) Power-on condition
2) High-low-high pulse on /RESET pin
3) Watchdog timer time-out

The values of T and P as listed in the following table are used to check how the processor wakes up.

Reset Type	T	P
Power on	1	1
/RESET during Operation mode	P*	P*
/RESET wake-up during Sleep mode	1	0
WDT during Operation mode	0	P*
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* *P: Previous status before reset*

The following shows the events that may affect the Status of T and P:

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	P*
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* *P: Previous status before reset*

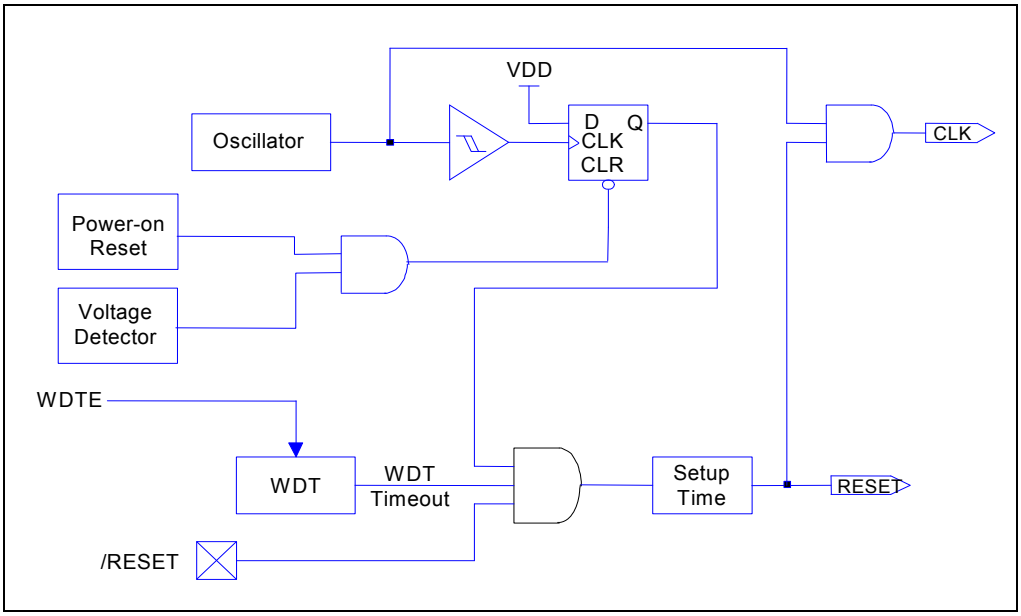


Figure 6-15 Controller Reset Block Diagram

6.6 Interrupt

The EM78F602N has 6 interrupts (3 external and 3 internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
External	Comparator	ENI+CMPIE=1	CMPIF	0015	4
Internal	TC2	ENI + TC2IE=1	TC2IF	0024	5
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	6

RE and RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. IOCE and IOCF are the interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF and RE) is set regardless of the status of its mask bit or of the ENI execution. The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

The external interrupt has an on-chip digital noise rejection circuit (input pulse less than **8 system clock time** is eliminated as noise), but under **Green mode (WDT RC oscillator), the noise rejection circuit is disabled.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC, R3, and R4 are restored.

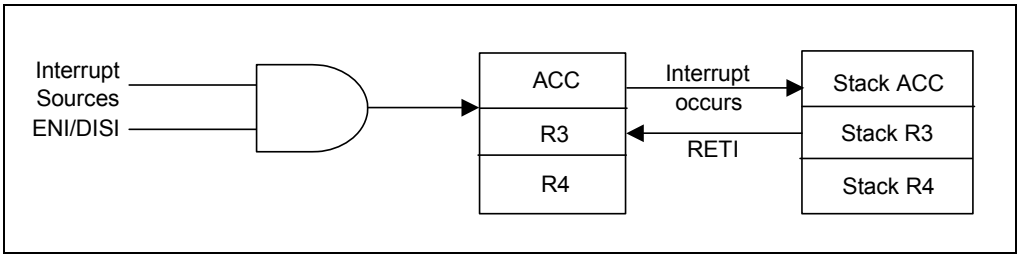


Figure 6-16 Interrupt Back-up Diagram

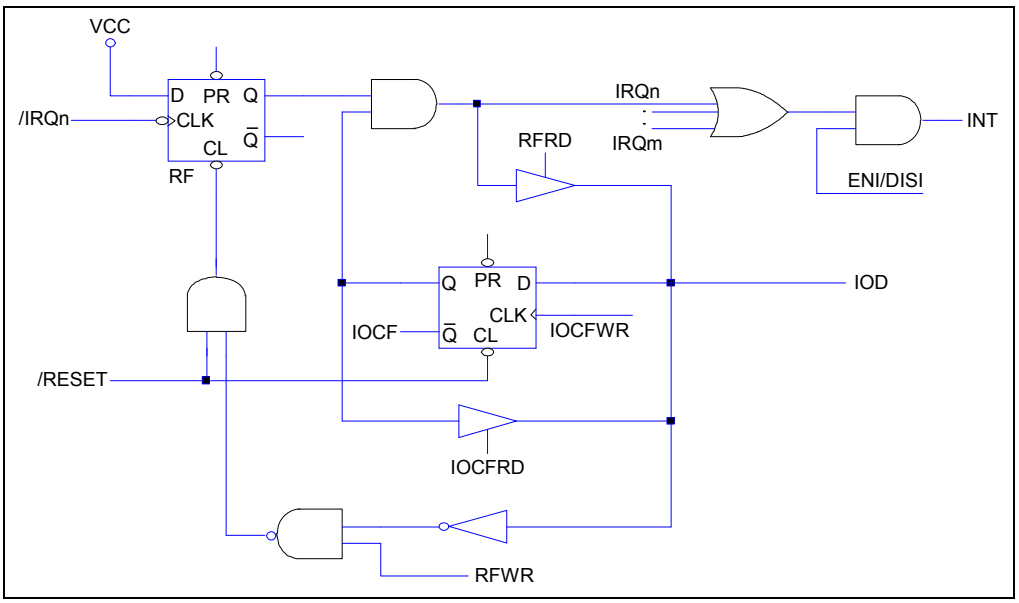


Figure 6-17 Interrupt Input Circuit

6.7 Data EEPROM

The Data EEPROM is readable and writable during normal operation over the whole Vdd range. The operation for Data EEPROM is base on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provides high erase and write cycles. A byte write automatically erases the location and writes the new value.

6.7.1 Data EEPROM Control Register

6.7.1.1 RB (EEPROM Control Register)

The EECR (EEPROM Control Register) is the control register for configuring and initiating the control register status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7: Read control register

0: Does not execute EEPROM read

1: Read EEPROM content, (RD can be set by software and is cleared by hardware after Read instruction is completed)

Bit 6: Write control register

0: Write cycle to EEPROM is completed.

1: Initiate a write cycle (WR can be set by software and is cleared by hardware after Write cycle is completed).

Bit 5: EEPROM Write Enable bit

0: Write to the EEPROM not allowed

1: Allows EEPROM write cycles

Bit 4: EEPROM Detect Flag

0: Write cycle is completed.

1: Write cycle is unfinished.

Bit 3: EEPROM power-down control bit

0: Switch off the EEPROM.

1: EEPROM is running.

Bits 2 ~ 0: Not used, set to "**0**" at all time.

6.7.1.2 RC (256 Bytes EEPROM Address)

When accessing the EEPROM data memory, the RC (256 bytes EEPROM address register) holds the address to be accessed. In accordance with the operation, the RD (256 bytes EEPROM Data register) holds the data to be written, or the data read, at the address in RC.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_A7	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 7 ~ 0: 256 bytes EEPROM address

6.7.1.3 RD (256 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 256 bytes EEPROM data

6.7.2 Programming Steps / Demonstration Example

6.7.2.1 Programming Steps

Follow the following steps to write or read data from the EEPROM**:**

1) Set the RB.EEPC bit to "**1**" to enable the EEPROM power.

2) Write the address to RC (256 bytes EEPROM address).

   a) Set the RB.EEWE bit to "**1**", if the write function is employed.

   b) Write the 8-bit data value to be programmed in the RD (256 bytes EEPROM data).

   c) Set the RB.WR bit to "**1**", then, execute write function.

   d) Set the RB.READ bit to "**1**", after which, execute read function.

3) a) Wait for the RB.EEDF or RB.WR to be cleared.

   b) Wait for the RB.EEDF to be cleared.

4) For the next conversion, go to Step 2 as required.

5) If user wants to save power and to make sure the EEPROM data is not used, clear the RB.EEPC.

6.7.2.2 Demonstration Program Example

```
; To define the control register
; Write data to EEPROM
RC == 0x0C
RB == 0x0B
RD == 0x0D
Read == 0x07
WR == 0x06
EEWE == 0x05
EEDF == 0x04
EEPC == 0x03

BS RB, EEPC      ; Set the EEPROM power on
MOV A,@0x0A
MOV RC,A         ; Assign the address from EEPROM
BS RB, EEWE      ; Enable the EEPROM write function
MOV A,@0x55
MOV RD,A         ; Set the data for EEPROM
BS RB,WR         ; Write value to EEPROM
JBC RB,EEDF      ; Check the EEPROM bit whether complete or not
JMP $-1
```

6.8 Timer/Counter 2

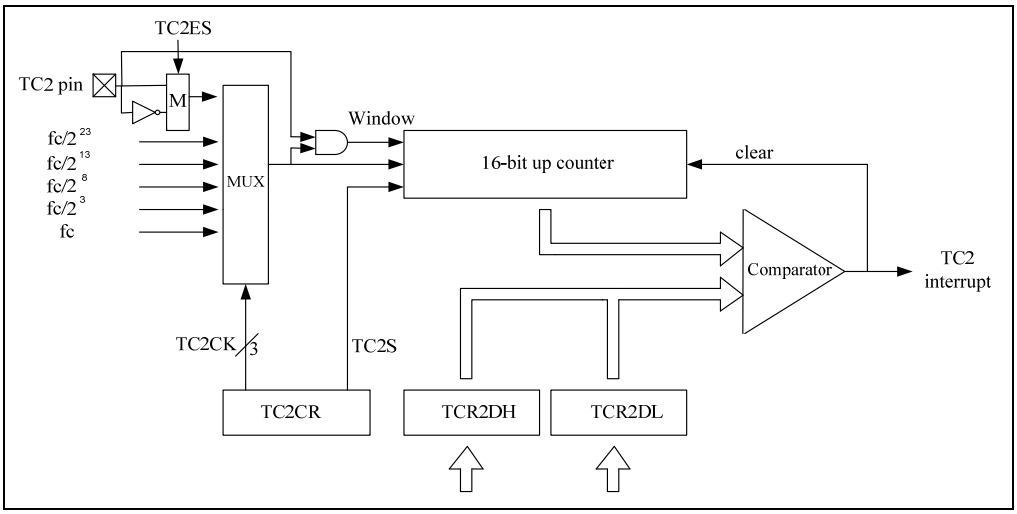


Figure 6-18 Configuration of Timer/Counter 2

In **Timer mode,** counting up is performed using the internal clock. When the contents of the up-counter match the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

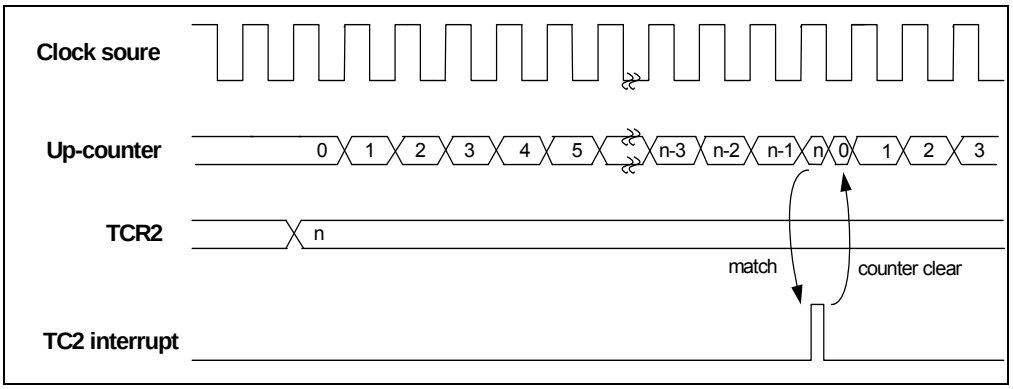


Figure 6-19 Timer Mode Timing Chart

In **Counter mode,** counting up is performed using an external clock input pin (TC2) and either rising or falling can be selected by setting TC2ES. When the contents of the up-counter match the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

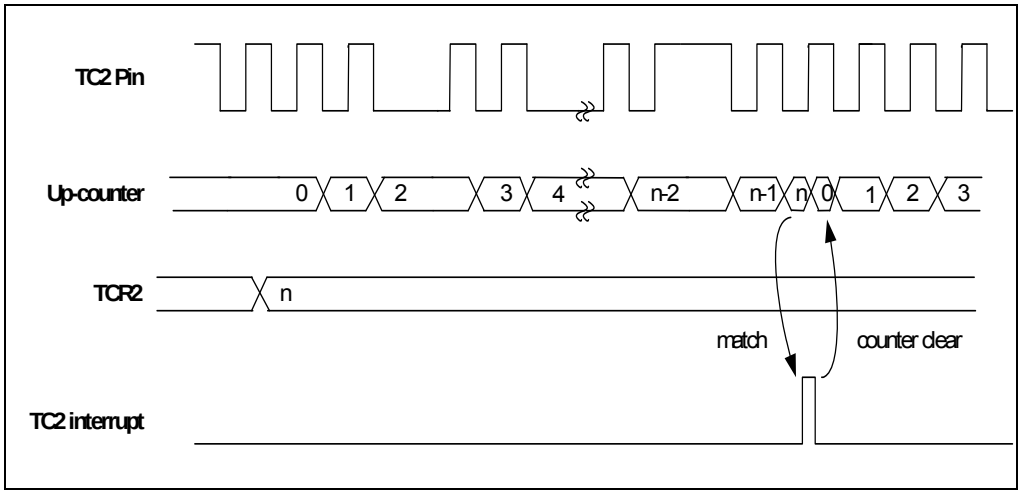


Figure 6-20 Counter Mode Timing Chart

In **Window mode,** counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of the up-counter match with the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

While writing to the TCR2DL, the comparison is inhibited until TCR2DH is written.

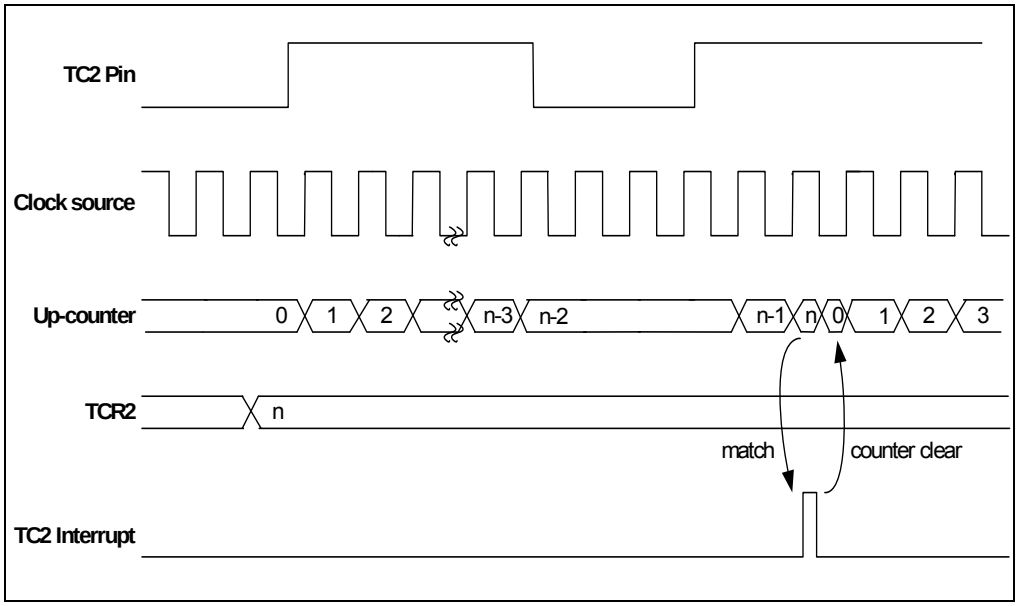


Figure 6-21 Window Mode Timing Chart

6.9 Timer/Counter 3

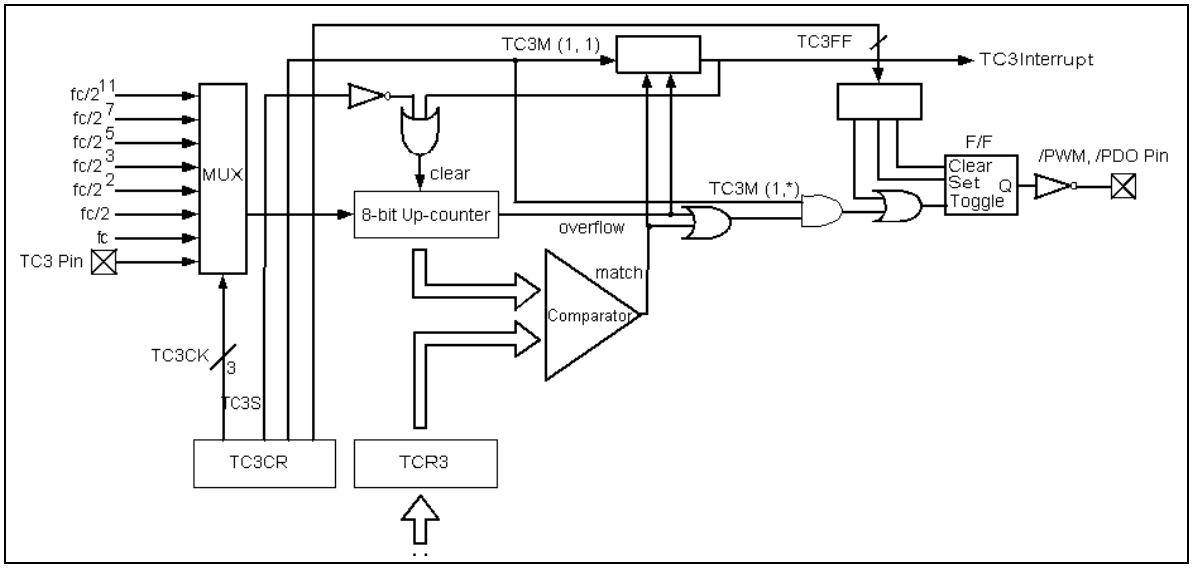


Figure 6-22 Timer/Counter 3 Configuration

In **Timer mode,** counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter match with the contents of TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In **Counter mode,** counting up is performed using the external clock input pin (TC3). When the contents of the up-counter match with the contents of TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In **Programmable Divider Output (PDO) mode,** counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

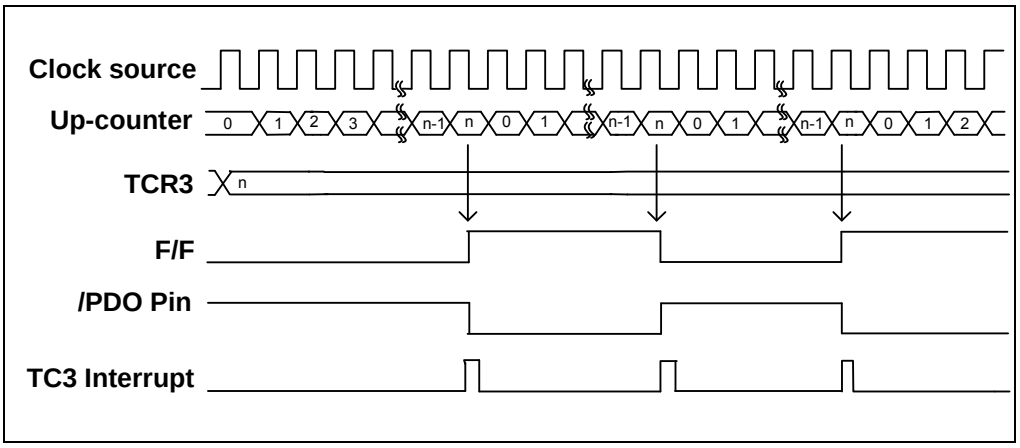


Figure 6-23 PDO Mode Timing Chart

In **Pulse Width Modulation (PWM) Output mode,** counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. While the counter is counting, the F/F is toggled again when the counter overflows, the counter is cleared. The F/F output is inverted and output to the /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Hence, the output can be changed continuously. Also, after data is loaded to TCR3, the TCR3 (Bit 5) has to be shifted first by setting TC3S to "**1**".

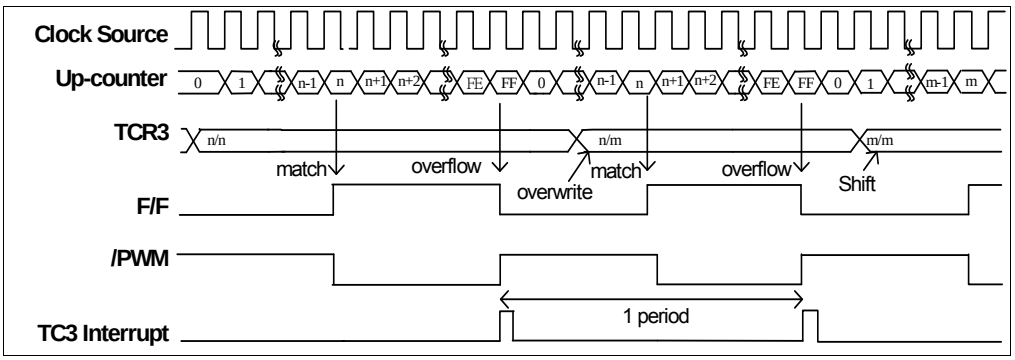


Figure 6-24 PWM Mode Timing Chart

6.10 Comparator

The EM78F602N has one comparator, which has two analog inputs and two outputs. The comparator can be employed to wake up from Sleep mode. Figure 6-25 illustrates the comparator circuit.

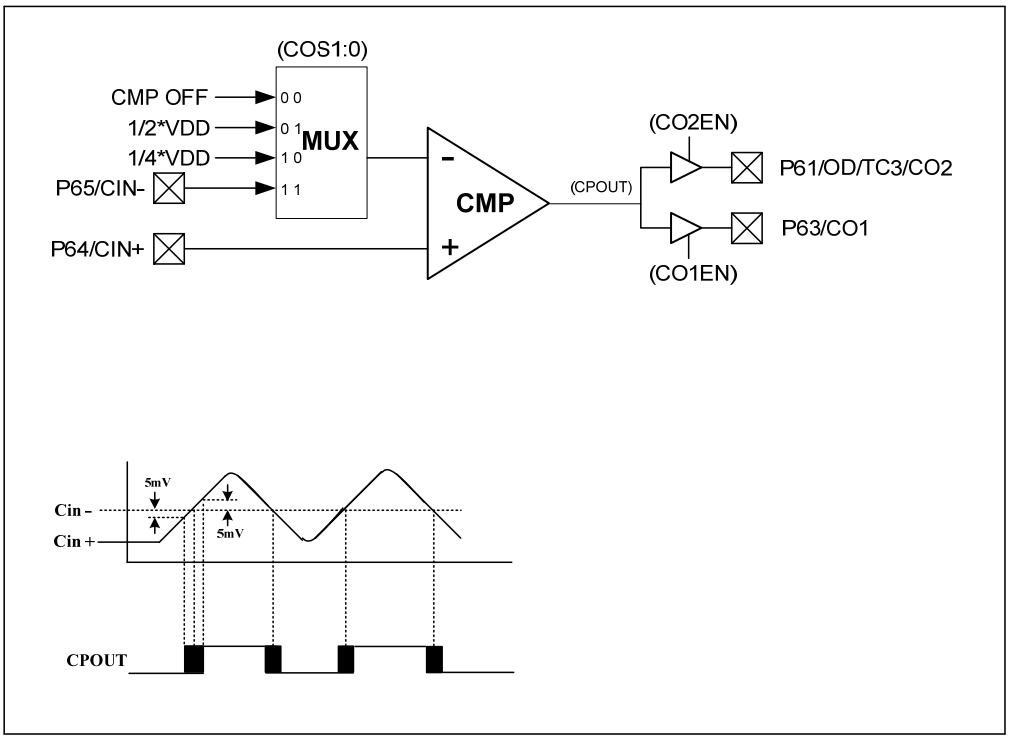


Figure 6-25 Comparator Operating Mode

6.10.1 External Reference Signal

The analog signal that is presented at Cin- compares to the signal at Cin+, and the digital output (CPOUT) of the comparator is adjusted accordingly.

- The reference signal must be between Vss and Vdd.
- The reference voltage can be applied to either pin of the comparator.
- Threshold detector applications may be of the same reference.
- The comparator can operate from the same or different reference source.

6.10.2 Comparator Output

- The compared result is stored in the CPOUT of R8 Bit 4 of Bank 3.
- The comparator is output to CO1 and CO2 (P63, P61) by programming the Bit 3~0 <COS1, COS0, COS2EN, COS1EN> of Register R7 Bank 3.

- The Figure below shows the comparator output block diagram.

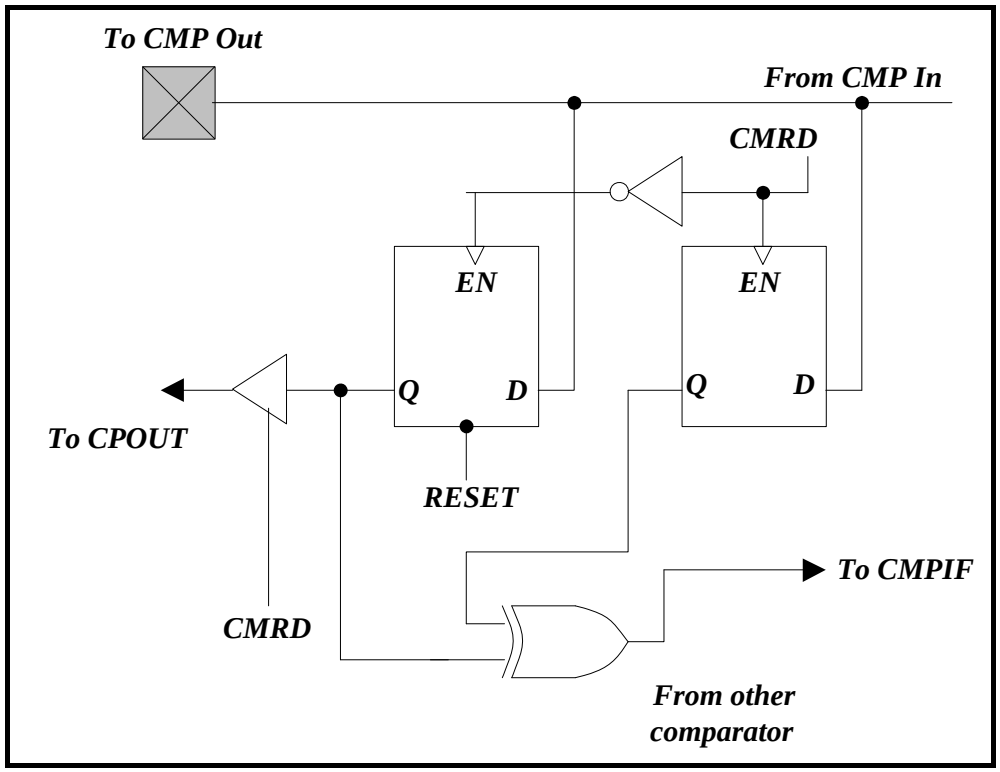


Figure 6-26 Comparator Output Configuration

6.10.3 Interrupt

- CMPIE (IOCE.7) and the “ENI” instruction execution must be enabled.
- Interrupt occurs whenever a change occurs on the output pin of the comparator.
- The actual change on the pin can be determined by reading the Bit CPOUT, R8 Bit 4 of Bank 3.
- CMPIF (RF.7 Bank 1), the comparator interrupt flag, can only be cleared by software.

6.10.4 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will Wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before going into sleep mode.

6.11 Oscillator

6.11.1 Internal RC Oscillator Mode

The EM78F602N offers a versatile internal RC mode with default frequency value of 4 MHz. The internal RC oscillator mode has other frequencies (8 and 16 MHz) that can be set by EEWORD0<7,6> or switch by Bank1 R8<7,6>. All these three main frequencies can be calibrated by programming the EEWORD0<4~0>, C4~C0 (auto calibration).

Internal RC Drift Rate (Ta=25°C, VDD=5 V± 5%, VSS=0V)

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.4V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 2.5%	± 10.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16.5kHz	± 3%	± 5%	± 4.5%	± 12.5%

6.12 ROM Code Option Register

The EM78F602N has a ROM Code option word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

ROM Code Option Register arrangement distribution**:**

ROM Word 1
Bit 12~Bit 0

6.12.1 ROM Code Option Register (ROM Word 1)

ROM Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	–	–	–	–	–	–	LVR1	LVR0	PR2	PR1	PR0
1	–	–	–	–	–	–	–	–	High	High	High	High	High
0	–	–	–	–	–	–	–	–	Low	Low	Low	Low	Low

Bits 12 ~ 6: Not used, set to "**0**" at all time

Bit 5: Not used, set to "**1**" at all time

Bit 4 ~ 3 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1	LVR0	Reset Level	Release Level
0	0	NA	NA
0	1	2.7V	2.9V
1	0	3.5V	3.7V
1	1	4.0V	4.2V

LVR1, LVR0="00"**:** LVR disable, power-on reset point of EM78F602N is 2.0~2.1V (default)

LVR1, LVR0="01"**:** If Vdd < 2.7V, the EM78F602N will reset.

LVR1, LVR0="10"**:** If Vdd < 3.5V, the EM78F602N will reset.

LVR1, LVR0="11"**:** If Vdd < 4.0V, the EM78F602N will reset.

Bits 2 ~ 0 (Protect): Protect Bit. Protect type is as follows:

Protect	Protect
1	Enable
0	Disable

6.13 EEPROM Code Option Register

The EM78F602N has an EEPROM Code option word that is also not part of the normal program memory. The option bits cannot be accessed during normal program execution.

EEPROM Code Option Register arrangement distribution**:**

EEWord 0	EEWord 1
Bit 7~Bit 0	Bit 7~Bit 0

6.13.1 EEPROM Code Option Register (EEWord 0)

EE Word 0								
Bit	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	RCM1	RCM0	–	C4	C3	C2	C1	C0
1	High	High	–	High	High	High	High	High
0	Low	Low	–	Low	Low	Low	Low	Low

Bit 7 ~ 6 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
0	0	4 (default)
0	1	16
1	x	8

Bit 5: Not used, set to "**0**" at all time.

Bits 4 ~ 0 (C4 ~ C0): Internal RC mode calibration bits. C4 ~ C0 must be set to "0" only (auto-calibration).

6.13.2 EEPROM Code Option Register (EEWord 1)

EE Word 1								
Bit	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	NRHL	NRE	RESETENB	–	SC3	SC2	SC1	SC0
1	8/fc	Disable	/RESET	–	High	High	High	High
0	32/fc	Enable	P62	–	Low	Low	Low	Low

Bit 7 (NRHL): Noise rejection high/low pulse defined bit. The INT pin is a falling edge trigger.

0: Pulses equal to 32/fc [s] is regarded as signal (default)

1: Pulses equal to 8/fc [s] is regarded as signal

NOTE

The noise rejection function is turned off during Green mode (WDT RC Oscillator), Idle mode, and Sleep mode.

Bit 6 (NRE): Noise rejection enable. The INT pin is a falling edge trigger.

1: Disable noise rejection

0: Enable noise rejection (default). But in Green mode (WDT RC Oscillator), the noise rejection circuit is always disabled.

Bit 5 (RESETENB): Reset Pin Enable Bit

1: Enable, P62//RESET → RESET pin

0: Disable, P62//RESET → P62 (default)

Bit 4: Not used, set to "**0**" at all time.

Bits 3 ~ 0 (SC3 ~ SC0): Calibrator of sub frequency (WDT frequency is 16.5kHz, auto calibration)

6.14 Power-on Considerations

Any microcontroller is not guaranteed to start and operate properly before the power supply has stabilized. The EM78F602N has an on-chip Power-on Voltage Detector (POVD) with a detection level of 2.0V~2.1V. It will work well if Vdd can rise quickly enough (2ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.15 External Power-on Reset Circuit

The circuit diagram shown below uses an internal R and external C to produce a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operational voltage. This circuit is used when the power supply has a slow rising time. Since the current leakage from the /RESET pin is ± 5 μA, the internal R is about 100 KΩ. Under this condition, the /RESET pin voltage is held below 0.2V. The diode (D) functions as a short circuit at the moment of power down.

The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing into the /RESET pin.

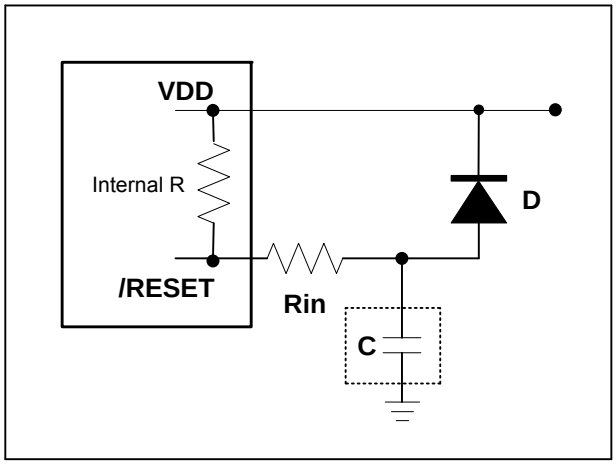


Figure 6-27 External Power-up Reset Circuit

NOTE

The R-C charge time will cause fast power-on, set-up time is not 2 ms.

6.16 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instructions "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this particular case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try to modify the instruction as follows**:**

a) Change one instruction cycle to consist of four oscillator periods.

b) "LJMP", "LCALL", "RET", "RETL", "RETI", "TBRD", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Note that once the two oscillator periods occur within one instruction cycle, the internal clock source to TCC should be CLK=Fosc/2.

In addition, the instruction set has the following features:

- Every bit of any register can be set, cleared, or tested directly.
- The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

■ EM78F602N Instruction Set Table

In the following Instruction Set table, the following symbols are used:

"**R**" *represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.*

"**b**" *represents a bit field designator that selects the value for the bit which is located in the register "**R**", and affects operation.*

"**k**" *represents an 8 or 10-bit constant or literal value.*

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z

[1] *This instruction is applicable to IOC6, IOCA ~ IOCF only.*

(Continuation)

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None[3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z

[2] *This instruction is not recommended for interrupt status register operation.*

[3] *This instruction cannot operate under interrupt status register.*

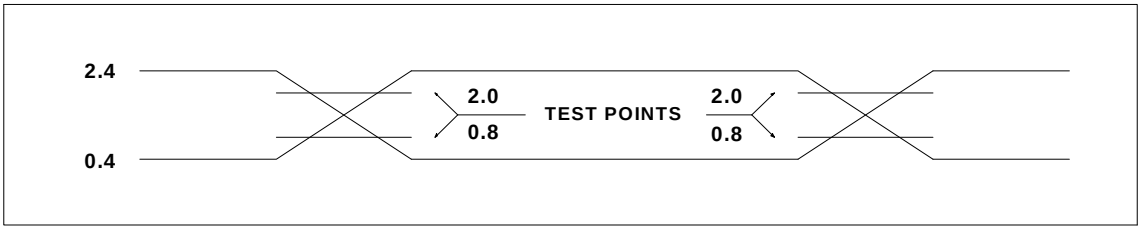
(Continuation)

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC
1 1110 1001 kkkk	1E9k	BANK k	K → R4(7:6)	None
1 1110 1010 kkkk k kkkk kkkk kkkk	1EAk	LCALL k	Next instruction : k kkkk kkkk kkkk PC+1 → [SP], k → PC	None [4]
1 1110 1011 kkkk k kkkk kkkk kkkk	1EBk	LJMP k	Next instruction: k kkkk kkkk kkkk k → PC	None [4]
1 1110 11rr rrrr	1Err	TBRD R	If Bank 3 R6.7=0, machine code (7:0) → R Else Bank 3 R6.7=1, machine code (12:8) → R(4:0), R(7:5)=(0,0,0)	None

[4] *This instruction will modify R3 (5) bit.*

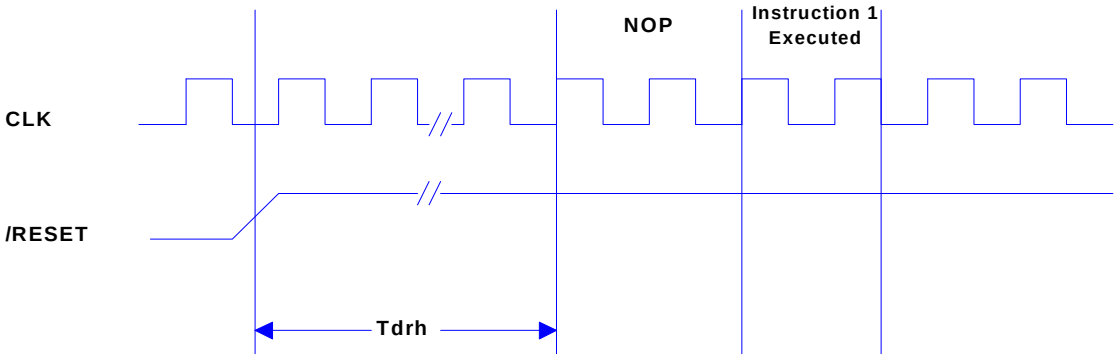
7 Timing Diagram

AC Test Input/Output Waveform



AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")

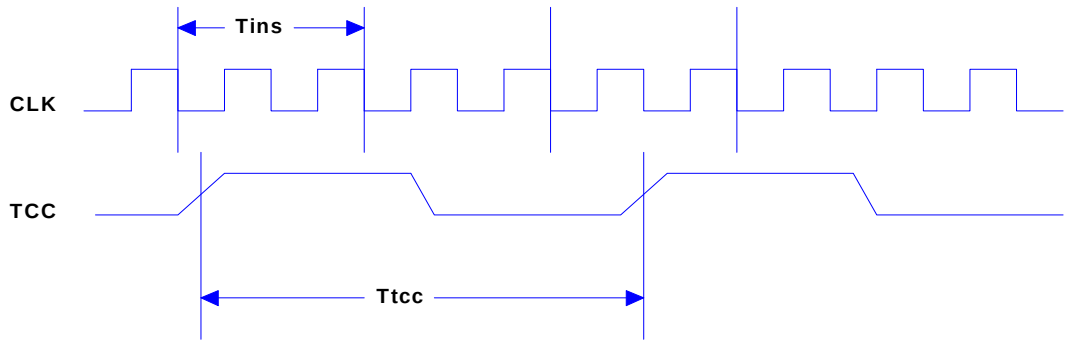


Figure 7-1 EM78F602N Timing Diagram

8 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.2	to	5.5V
Working frequency	DC	to	16 MHz
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

Note: These parameters are theoretical values and have not been tested.

9 DC Electrical Characteristics

■ **Ta=25°C, VDD=5.0V±5%, VSS=0V**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	IRC: VDD to 5 V	4 MHz, 8 MHz, 16 MHz	F-2.5%	F	F+2.5%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
VIH1	Input High Voltage (Schmitt Trigger)	P60, P62 ~ P65	0.7 * VDD	–	VDD + 0.3V	V
		P61	0.75 * VDD	–	VDD + 0.3V	
VIL1	Input Low Voltage (Schmitt Trigger)	P60, P62 ~ P65	-0.3V	–	0.3 * VDD	V
		P61	-0.3V	–	0.25 * VDD	
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7 * VDD	–	VDD + 0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.3 * VDD	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	INT	0.7 * VDD	–	VDD + 0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	INT	-0.3V	–	0.3 * VDD	V
IOH1	Output High Voltage (P60, P62~P65)	VOH = 0.9VDD	-3.2	-4.2	–	mA
IOL1	Output Low Voltage (P60, P62~P65)	VOL = 0.1VDD	10	12	–	mA
IOL2	Output Low Voltage (P61 is open-drain for output)	VOL = 0.1VDD	10	12	–	mA
IPH	Pull-high current	Pull-high active, Input pin at VSS	–	-70	-80	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	–	20	30	μA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	2	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	8	10	μA
ICC1	Operating supply current at two clocks	/RESET = 'High', IRC = 4 MHz Output pin floating, WDT enabled	–	1.1	1.5	mA
ICC2	Operating supply current at two clocks	/RESET = 'High', IRC = 8 MHz Output pin floating, WDT enabled	–	1.5	2.0	mA

NOTE

- *These parameters are hypothetical (not tested) and are provided for design reference use only.*
- *Data under Minimum, Typical, and Maximum (Min., Typ., and Max.) columns are based on hypothetical results at 25°C. These data are for design reference only.*

■ Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.5~ 5.5V Temperature = -40°C ~ 85°C	–	4.0	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	1000K	–	cycles

■ Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	–	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

■ **Comparator Electrical Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	RL = 5.1K (Note[1])	–	–	5	mV
Vcm	Input common-mode voltage range	(Note[2])	GND	–	VDD	V
$V_{1/2VDD}$	Comparator inverting input from internal voltage source.	1/2*VDD.	–	–	±5	%
$V_{1/4VDD}$		1/4*VDD.				
Tr	Response time, overdrive=30mV (Note[3])	CIN- = VDD ~ VDD-1	-	350	500	ns
		CIN- = VDD-1 ~ VSS+1	-	250	350	
		CIN- = VSS+1 ~ VSS	-	350	550	
VS	Operating range	–	2.5	–	5.5	V

[1] *The output voltage is in unit gain circuitry and over the full input common-mode range.*

[2] *The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.*

[3] *The response time specified is a 100 mV input step with 30 mV overdrive.*

10 AC Electrical Characteristics

■ 0 ≤ Ta ≤ 70°C, VDD=5V, VSS=0V

■ -40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (2 CLK)	RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	1.8	2.0	2.2	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	13.5	15.5	17.5	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload = 20 pF	–	50	–	ns

**N = Selected prescaler ratio*

NOTE

- *These parameters are hypothetical (not tested) and are provided for design reference use only.*
- *Data under Minimum, Typical, and Maximum (Min., Typ., and Max.) columns are based on hypothetical results at 25°C. These data are for design reference only.*

APPENDIX

A Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F602NMS10AJ/S	MSOP	10	118 mil

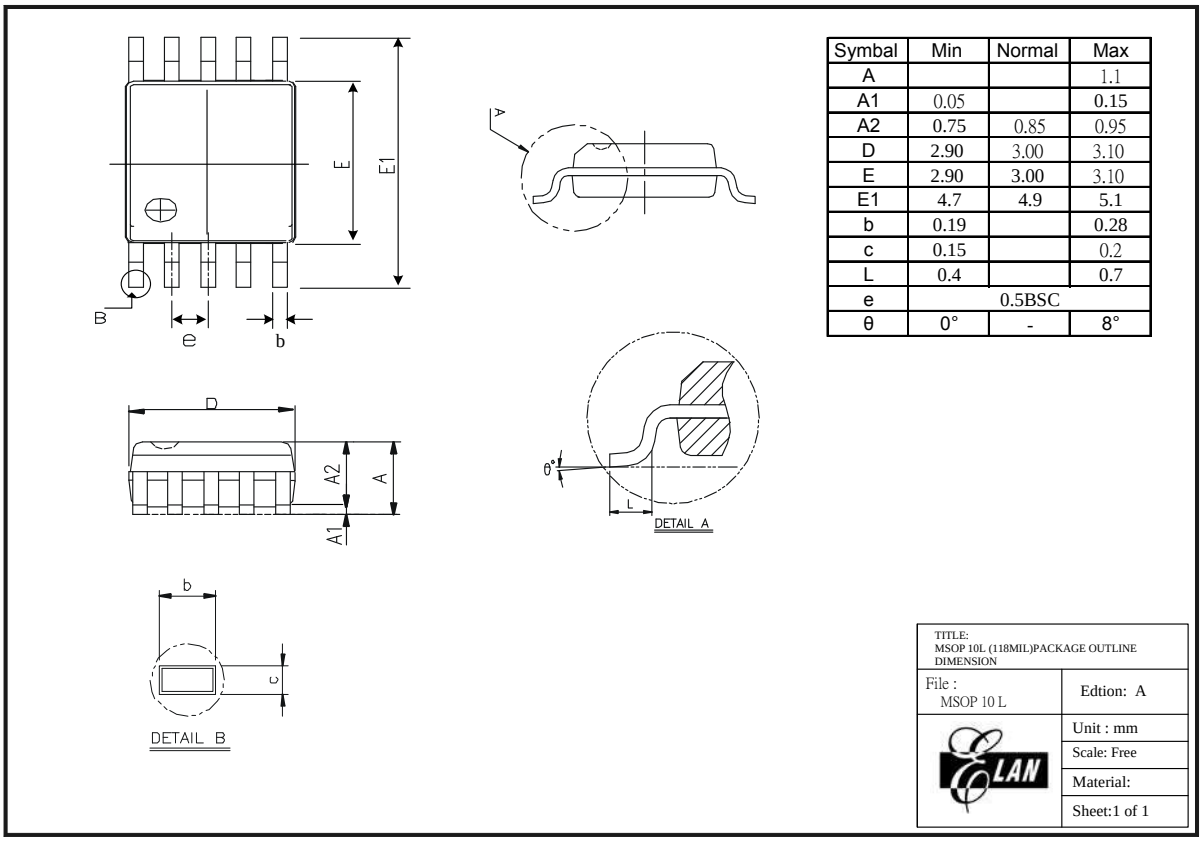
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

The Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78F602NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Packaging Configuration

B.1 EM78F602NMS10A



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e	0.5BSC		
θ	0°	-	8°

Figure B-1 EM78F602N 10-pin MSOP Package Type

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5°C)	
Temperature cycle test	-65°C (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.