EM78F665N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

July 2011

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2011/07/13

1 General Description

The EM78F665N series are 8-bit microprocessors designed and developed with low-power, high-speed CMOS technology. They have on-chip 4K×15-bit Electrical Flash Memory, 128×8-bit In-system programmable EEPROM, two 8-bit timers, two 10-bit PWM, 8 channels AD with 12 bits resolution and I^2C.

With enhanced Flash-ROM features, the EM78F665N offers a convenient way of developing and verifying users' programs. Moreover, users can avail of the EMC Writer to easily program his development code.

2 Features

- CPU configuration
  - **Support 4K×15** bits program ROM
  - **304×8** bits on-chip registers (SRAM)
  - **128** bytes in-system programmable EEPROM
    *Endurance: 1000,000 write/erase cycles
  - More than 10 years data retention
  - **8** level stacks for subroutine nesting
  - Typically 2 μA, during sleep mode
  - Four operation modes

Mode	CPU	Main clock	WDT clock
Sleep mode	Turn off	Turn off	Turn off
Idle Mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- I/O port configuration
  - 4 bidirectional I/O ports: P5, P6, P7, P8
  - Pin change wake-up port : P6
  - **30** programmable pull-down I/O pins
  - **30** programmable pull-high I/O pins
  - **30** programmable open-drain I/O pins
  - **30** programmable high-sink/drive I/O pins
  - External interrupt : P60
- Operating voltage range:
  - 2.4V~5.5V at 0°C~70°C (commercial)
  - 2.6V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on 2 clocks):
  - IRC mode
    DC ~ 16 MHz at 4.5V~5.5V
    DC ~ 8 MHz at 3V~5.5V
    DC ~ 4 MHz at 2.4V~5.5V
  - Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40℃ +85℃)	Voltage (2.2V~5.5V)	Process	Total
4 MHz	±2%	±2%	±2%	±6%
8 MHz	±2%	±2%	±2%	±6%
16 MHz	±2%	±2%	±2%	±6%

- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Two Pulse Width Modulation (PWMA, PWMB) with 10-bit resolution shared with Timers A and B
  - One 8-bit Timer/Counter:
    TC3: Timer/Counter/PWM/PDO(programmable divider output) mode select
  - **8** channels Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - Power-down (Sleep) mode
  - High EFT immunity (4 MHz, 4 clocks)
  - I^2C function with 7/10 bits address and 8 bits data transmit/receive mode
- 10 available interrupts (3 external, 7 internal)
  - External interrupt (P60)
  - TCC overflow interrupt
  - TC3 overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - ADC completion interrupt
  - PWMA, PWMB period match completion
  - I^2C transfer/receive/stop interrupt
- Programmable free running Watchdog Timer
  - Watchdog Timer: 16.5ms ± 5% with Vdd =5V at 25°C, Temperature range ± 5% (-40°C ~+85°C)
  - Watchdog Timer: 18ms ± 5% with Vdd = 3V at 25°C
  - Temperature range ± 5% (-40°C~+85°C)
  - Two clocks per instruction cycle
- Single instruction cycle commands
- Package Type:
  - 32 pin QFN : EM78F665NQN32J/S
  - 28 pin SKDIP : EM78F665NK28J/S
  - 28 pin SOP : EM78F665NSO28J/S

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Configuration

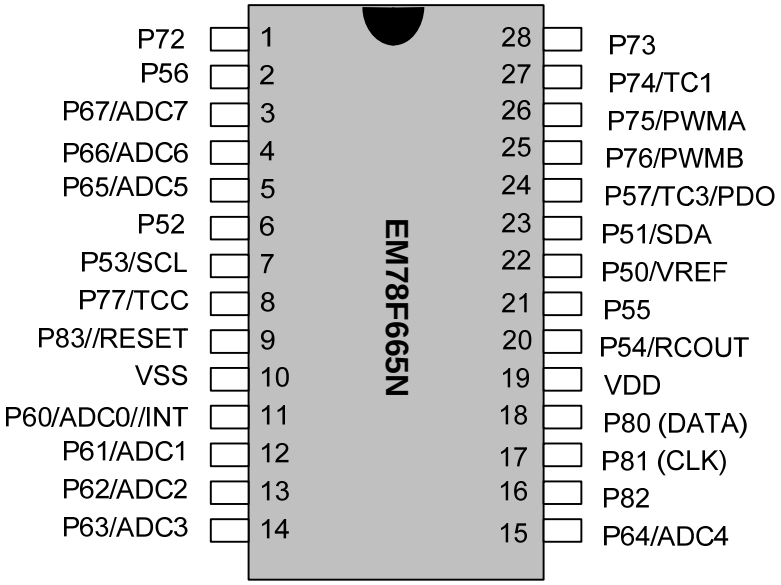


Figure 3-1 28-pin SKDIP/SOP

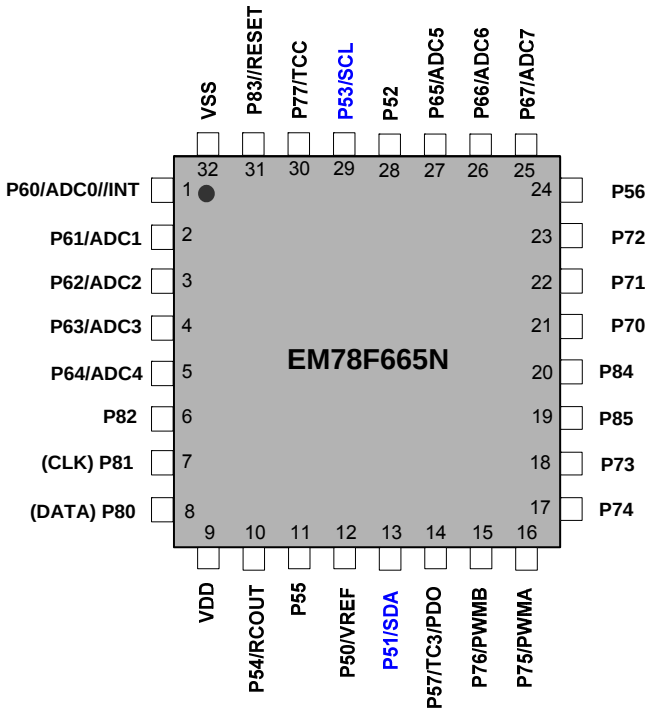


Figure 3-2 32-pin QFN Pin Assignment

4 Pin Description

Name	Function	Input Type	Output Type	Description
P50/VREF	VDD	Power	–	Power
	VSS	Power	–	Ground
	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	VREF	AN	–	Voltage reference for ADC
P51/SDA	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SDA	ST	CMOS	I2C serial data line. It is open-drain
P52	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P53/SCL	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SCL	ST	CMOS	I2C serial clock line. It is open-drain.
P54/RCOUT	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	RCOUT	–	CMOS	Clock output of internal RC oscillator
P55	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P56	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P57/TC3/PDO	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TC3	ST	–	Timer 3 clock input
	PDO	–	CMOS	programmable divider output
P60/ADC0//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC0	AN	–	ADC Input 0
	/INT	ST	–	External interrupt pin
P61/ADC1	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC1	AN	–	ADC Input 1
P62/ADC2	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC2	AN	–	ADC Input 2
P63/ADC3	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC3	AN	–	ADC Input 3
P64/ADC4	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC4	AN	–	ADC Input 4
P65/ADC5	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC5	AN	–	ADC Input 5
P66/ADC6	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC6	AN	–	ADC Input 6
P67/ADC7	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC7	AN	–	ADC Input 7

Name	Function	Input Type	Output Type	Description
P70	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P71	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P72	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P73	P73	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P74	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P75/PWMA	P75	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMA	–	CMOS	PWMA output
P76/PWMB	P76	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMB	–	CMOS	PWMB output
P77/TCC	P77	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TCC	ST	–	Real Time Clock/Counter clock input
P80	P80	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P81	P81	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P82	P82	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P83//RESET	P83	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
	/RESET	ST	–	External pull-high reset pin
P84	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P85	P85	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain

5 Functional Block Diagram

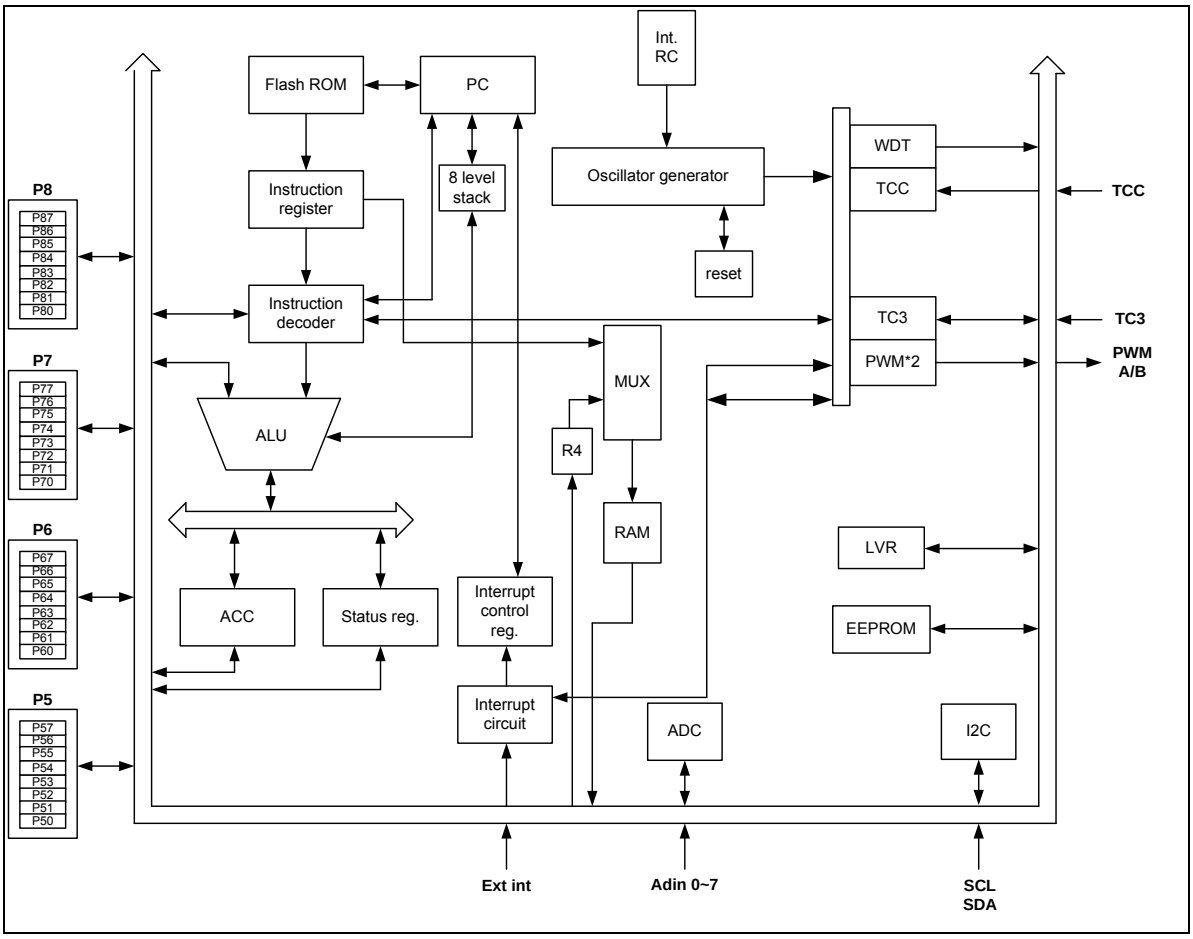


Figure 5-1 Functional Block Diagram of EM78F665N

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	SBS0	0	0	0	GBS0

Bits 7~5: Unused bits, fixed to "**0**" all the time.

Bit 4 (SBS0): Special register bank select bit. It is used to select Bank 0/1 of Special Registers R5~R4F.

0: Bank 0

1: Bank 1

Bits 3~1: Unused bits, fixed "**0**" all the time.

Bit 0 (GBS0): General register bank select bit. It is used to select Bank 0/1 of General Registers R80~RFF.

0: Bank 0

1: Bank 1

6.1.3 R2: PC (Program Counter)

- Depending on the device type, R2 and hardware stack are 12 bits wide. The structure is depicted in Figure 3.
- Generates 4K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "0"s when under Reset condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will increment by 1 and is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.

- "LJMP" instruction allows direct loading of the lower 13 program counter bits. Therefore, "LJMP" allows the PC to jump to any location within 4K (2^{12}).
- "LCALL" instruction loads the lower 13 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will remain unchanged.
- Any instruction except “ADD R2,A” that is written to R2 (e.g. "MOV R2, A", "BC R2, 6",·etc.) will cause the ninth bit and the above bits (A8~A11) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8, fclk/16). The instruction that would change the contents of R2 will need one more instruction cycle.

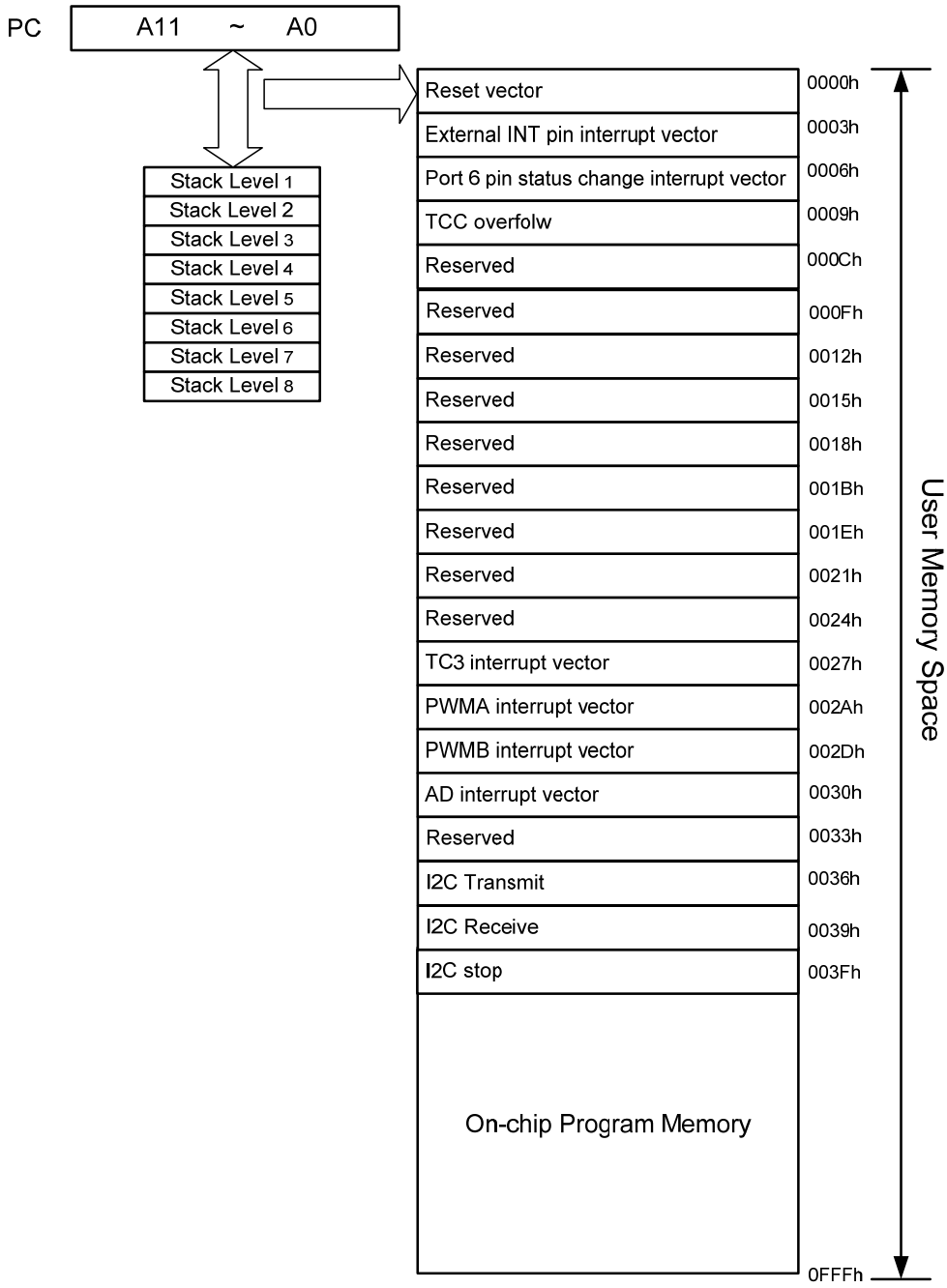


Figure 6-1 Program Counter Organization

Address	Bank 0	Bank 1
0X00	IAR (Indirect Addressing Register)	
0X01	BSR (Bank Selection Control Register)	
0X02	PC (Program Counter)	
0X03	SR (Status Register)	
0X04	RSR (RAM Select Register)	
0X05	Port 5	P5PHCR
0X06	Port 6	P6PHCR
0X07	Port 7	P7PHCR
0X08	Port 8	P8PHCR
0X09	-	-
0X0A	-	-
0x0B	OMCR (Operating Mode Control Register)	P5PLCR
0X0C	ISR1 (Interrupt Status Register 1)	P6PLCR
0X0D	ISR2 (Interrupt Status Register 2)	P7PLCR
0X0E	ISR3 (Interrupt Status Register 3)	P8PLCR
0X0F	-	-
0X10	EIESCR	-
0X11	WDTCR	P5HD/SCR
0X12	-	P6HD/SCR
0X13	TCCCR	P7HD/SCR
0X14	TCCDATA	P8HD/SCR
0X15	IOCR5	-
0X16	IOCR6	-
0X17	IOCR7	P5ODCR
0X18	IOCR8	P6ODCR
0X19	-	P7ODCR
0X1A	-	P8ODCR
0X1B	-	-
0X1C	IMR1 (Interrupt Mask Register 1)	-
0X1D	IMR2 (Interrupt Mask Register 2)	IRCS
0X1E	IMR3 (Interrupt Mask Register 3)	-
0X1F	-	EEROM Control
0X20	P5WUCR	EEPROM ADDR

Address	Bank 0	Bank 1
0X21	P5WUECR	EEPROM Data
0X22	P7WUCR	-
0X23	P7WUECR	I2CCR1 (I2C Status and Control Register 1)
0X24	ADCR1 (ADC Control Register 1)	I2CCR2 (I2C Status and Control Register 2)
0X25	ADCR2 (ADC Control Register 2)	I2CSA (I2C Slave Address Register)
0X26	ADICL (ADC Input Select Low Byte Register)	I2CDA (I2C Device Address Register)
0X27	-	I2CDB (I2C Data Buffer)
0X28	-	I2CA
0X29	ADDH (AD Data High 8-bit Register)	-
0X2A	ADDL (AD Data Low 4-bit Register)	PWMER (PWM Enable Control Register)
0x2B	-	TIMEN (Timer/PWM Enable Control Register)
0X2C	-	-
0X2D	-	-
0X2E	-	-
0X2F	WUCR1	PWMACR (PWM A control register)
0X30	-	PWMBCR (PWM B control register)
0X31	-	-
0X32	-	TACR (Timer A control register)
0X33	I2CSW (I2C Switch Control Register)	TBCR (Timer B control register)
0X34	-	-
0X35	-	TAPRD (Timer A Period buffer)
0X36	-	TBPRD (Timer B Period buffer)
0X37	TBPTL	-
0X38	TBPTH	TADT (Timer A Duty Buffer)
0X39	-	TBDT (Timer B Duty Buffer)
0X3A	-	-
0x3B	-	PRDxL
0X3C	-	DTxL
0X3D	-	-
0X3E	-	-
0X3F	-	-
0X40	-	-

Address	Bank 0	Bank 1
0X41	-	-
0X42	-	-
0X43	-	-
0X44	-	-
0X45	-	-
0X46	-	-
0X47	-	-
0X48	-	-
0X49	-	-
0X4A	-	-
0x4B	-	-
0X4C	-	-
0X4D	-	-
0X4E	TC3CR	-
0X4F	TCR3D	-
0X50	General Purpose Register	
0X51		
: :		
0X7F		
0X80	Bank 0	Bank 1
0X81		
: : :		
0XFE		
0XFF		

Figure 6-2 Data Memory Configuration

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	T	P	Z	DC	C

Bits 7~5: unused bits, fixed to “0” all the time.

Bit 4 (T): Time-out bit.

Set to “1” with the "SLEP" and "WDTC" commands, or during power up and reset to “0” by WDT time-out.

Bit 3 (P): Power down bit.

Set to “1” during power on or by a "WDTC" command and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bits 7~0 (RSR7~RSR0): these bits are used to select registers (Address: 00~FF) in indirect addressing mode. Users can see the configuration of the data memory in more details in Figure 4.

6.1.6 Bank 0 R5 ~ R8 (Port 5 ~ Port 8)

R5, R6, R7 and R8 are I/O data registers.

6.1.7 Bank 0 R9~RA *(Unused)*

6.1.8 Bank 0 RB OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	0	0	TC3SS	TASS	TBSS	0

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator for WDT internal RC time base

1: Fm: main-oscillator

When CPUS=0, the CPU oscillator select the sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will determine as to which mode to activate after SLEP instruction.

0: "IDLE=0"+SLEP instruction → sleep mode

1: "IDLE=1"+SLEP instruction → idle mode

CPU Operation Mode

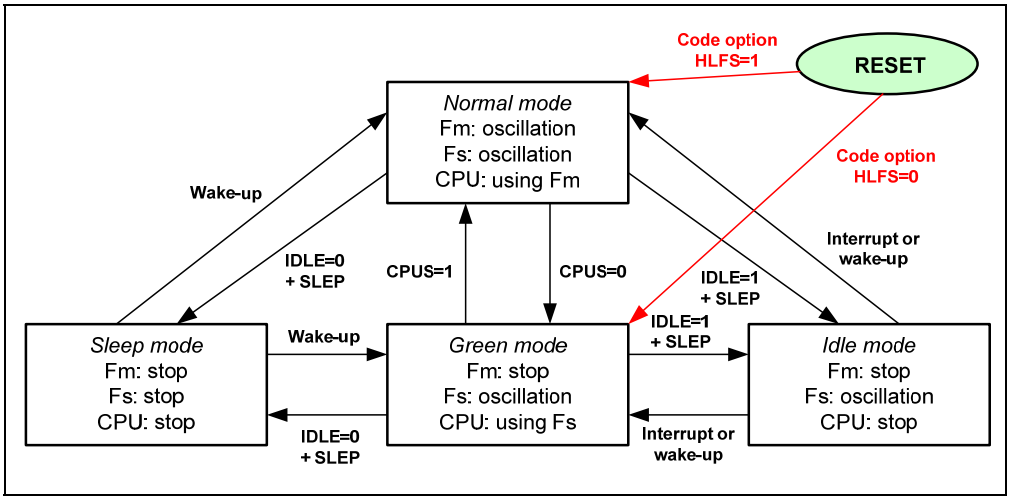


Figure 6-3 CPU Operation Mode

Bits 5~4: Unused bit, fixed to "0" all the time.

Bit 3 (TC3SS): TC3 clock source select bit

0: the Fs is used as Fc

1: the Fm is used as Fc

Bit 2 (TASS): Timer A clock source select bit

0: the Fs is used as Fc

1: the Fm is used as Fc

Bit 1 (TBSS): Timer B clock source select bit

0: the Fs is used as Fc

1: the Fm is used as Fc

Bit 0: unused bit, fixed to "0" all the time.

6.1.9 Bank 0 RC: ISR1 (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ADIF	0	PWMBIF	PWMAIF	EXIF	ICIF	TCIF

Note: *"**1**" means with interrupt request, "**0**" means no interrupt occurs.*

Bit 7: unused bit, fixed to "0" all the time.

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bit 5: unused bit, fixed to "0" all the time.

Bit 4 (PWMBIF): PWMB (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 3 (PWMAIF): PWMA (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 2 (EXIF): External interrupt flag.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

6.1.10 Bank 0 RD: ISR2 (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	TC3IF	0	0	0	0	0

Bits 7~6: Unused bits, fixed to "0" all the time.

Bit 5 (TC3IF): 8-bit Timer/Counter 3 interrupt flag. The Interrupt flag is cleared by software.

Bits 4~0: Unused bits, fixed to "0" all the time.

6.1.11 Bank 0 RE: ISR3 (Interrupt Status Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	I2CSTPIF	0	I2CRIF	I2CTIF

Bits 7~4: Unused bits, fixed to “0” all the time.

Bit 3 (I2CSTPIF): I2C slave received data stop interrupt flag.

Bit 2: Unused bit, fixed to “0” all the time.

Bit 1 (I2CRIF): I2C receive interrupt flag. Set when I2C receives 1 byte data and responds with ACK signal. Reset by firmware or I2C is disabled.

Bit 0 (I2CTIF): I2C transmit interrupt flag. Set when I2C transmits 1 byte data and receives a handshake signal (ACK or NACK). Reset by firmware or I2C is disabled**.**

6.1.12 Bank 0 RF: (Unused)

6.1.13 Bank 0 R10: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	EIES

Bits 7~1: Unused bit, fixed to 0 all the time.

Bit 0 (EIES): External interrupt edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

6.1.14 Bank 0 R11: WDTCR

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	INT	0	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Watchdog Timer Enable Bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bit 6 (EIS): P60/ /INT switch control bit

0: P60

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 must be set to "1". When EIS is "0", the path of /INT is masked. When EIS is "1", the status of the /INT pin can also be read by way of reading Port 6 (R6).

EIS is both readable and writable.

Bit 5 (INT): Interrupt enable flag

0: Interrupt is masked by DISI or hardware interrupt

1: Interrupt is enabled by ENI/DISI instructions

Bit 4: Unused bit, fixed to 0 all the time.

Bit 3 (PSWE): Prescaler Enable Bit for WDT

0: Disable Prescaler, WDT rate is 1:1

1: Enable Prescaler, WDT rate is set from Bits 2~0

Bits 2~0 (PSW2~PSW0): WDT Prescale Bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.15 Bank 0 R12: Unused register

6.1.16 Bank 0 R13: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TCCS	TS	TE	PSTE	PST2	PST1	PST0

Bit 7: Unused bit, set to 0 all the time.

Bit 6 (TCCS): TCC Clock Source Select Bit

0: Fs (sub clock)

1: Fm (main clock)

Bit 5 (TS): TCC Signal Source

0: Internal oscillator cycle clock. If P77 is used as I/O pin, TS must be 0.

1: Transition on the TCC pin

Bit 4 (TE): TCC Signal Edge

0: Increment if the transition from low to high takes place on the TCC pin.

1: Increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler Enable Bit for TCC

0: Disable prescaler, TCC rate is 1:1

1: Enable prescaler, TCC rate is set from Bits 2~0.

Bits 2~0 (PST2~PST0): TCC Prescaler Bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.17 Bank 0 R14: TCCDATA (TCC Data Register)

The TCC Data Register is incremented by an external signal edge through the TCC pin, or by the instruction cycle clock. The external signal of the TCC trigger pulse width must be greater than one instruction. The signals to increment the counter are determined by Bit 4 and Bit 5 of the TCCCR register. This register is writable and readable as any other registers.

6.1.18 Bank 0 R15~R18: (IOCR5~IOCR8)

These registers are used to control the I/O port direction. They are both readable and writable.

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance

6.1.19 Bank 0 R19~R1B: (Unused)

6.1.20 Bank 0 R1C: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ADIE	0	PWMBIE	PWMAIE	EXIE	ICIE	TCIE

Bit 7: Unused bit, fix to 0 all the time.

Bit 6 (ADIE): ADIF interrupt enable bit.

0: Disable ADIF interrupt

1: Enable ADIF interrupt.

When the ADC complete status is used to enter an interrupt vector or enter the next instruction, the ADIE bit must be set to “Enable“.

Bit 5: Unused bit, fixed to 0 all the time.

Bit 4 (PWMBIE): PWMBIF interrupt enable bit.

0: Disable PWMB interrupt

1: Enable PWMB interrupt

Bit 3 (PWMAIE): PWMAIF interrupt enable bit.

0: Disable PWMA interrupt

1: Enable PWMA interrupt

Bit 2 (EXIE): EXIF interrupt enable bit.

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit.

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit.

0: Disable TCIF interrupt

1: Enable TCIF interrupt

6.1.21 Bank 0 R1D: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	TC3IE	0	0	0	0	0

Bits 7~6: Unused bits, fixed to 0 all the time.

Bit 5 (TC3IE): Interrupt enable bit.

0: Disable TC3IF interrupt

1: Enable TC3IF interrupt

Bits 4~0: Unused bits, fixed to 0 all the time.

6.1.22 Bank 0 R1E: IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	I2CSTPIE	0	I2CRIE	I2CTIE

Bits 7~4: Unused bits, fixed to 0 all the time.

Bit 3 (I2CSTPIE): I2CSTPIF interrupt enable bit.

0: Disable I2CSTP interrupt

1: Enable I2CSTP interrupt

Bit 2: Unused bit, fixed to 0 all the time

Bit 1 (I2CRIE): I2C Interface Rx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 2 (I2CTIE): I2C Interface Tx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

6.1.23 Bank 0 R1F: (Unused)

6.1.24 Bank 0 R20: P5WUCR (Port 5 Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WU_P57	WU_P56	WU_P55	WU_P54	WU_P53	WU_P52	WU_P51	WU_P50

Bits 7~0 (WU_P57~WU_P50): Wake-up function control for Port 5.

0: Disable wake-up function

1: Enable wake-up function

6.1.25 Bank 0 R21: P5WUECR (Port 5 Wake-up Edge Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE_P57	WUE_P56	WUE_P55	WUE_P54	WUE_P53	WUE_P52	WUE_P51	WUE_P50

Bits 7~0 (WUE_P57~WUE_P50): Wake-up signal edge select for Port 5.

0: Falling edge trigger

1: Rising edge trigger

6.1.26 Bank 0 R22: P7WUCR (Port 7 Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WU_P77	WU_P76	WU_P75	WU_P74	WU_P73	WU_P72	WU_P71	WU_P70

Bits 7~0 (WU_P77~WU_P70): Wake-up function control for Port 7.

0: Disable Wake-up function

1: Enable Wake-up function

6.1.27 Bank 0 R23: P7WUECR (Port 7 Wake-up Edge Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE_P77	WUE_P76	WUE_P75	WUE_P74	WUE_P73	WUE_P72	WUE_P71	WUE_P70

Bits 7~0 (WUE_P77~WUE_P70): wake up signal edge selection for Port 7.

0: Falling edge trigger

1: Rising edge trigger

6.1.28 Bank 0 R24: ADCR1 (ADC Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	ADRUN	ADPD	0	0	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): Input source of the VREF of the ADC.

0: The Vref of the ADC is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1: The Vref of the ADC is connected to P50/VREF.

Note: Priority of the P50/VREF pin

P50/VREF Pin Priority	
High	Low
VREF	P50

Bit 6 (ADRUN): ADC starts to run

1: A/D conversion starts. This bit can be set by software

0: Reset on completion of the conversion. This bit cannot be reset though software

Bit 5 (ADPD): ADC Power-down mode

1: ADC is operating

0: Switch off the resistor reference to conserve power even while the CPU is operating.

Bits 4~3: Unused bits, set to 0 all the time.

Bits 2~0 (ADIS2~ADIS0): Analog Input Selection

ADIS2	ADIS1	ADIS0	Analog Input Pin
0	0	0	AD0/P60
0	0	1	AD1/P61
0	1	0	AD2/P62
0	1	1	AD3/P63
1	0	0	AD4/P64
1	0	1	AD5/P65
1	1	0	AD6/P66
1	1	1	AD7/P67

Note: *The AD channel can only be changed when the ADIF bit and the ADRUN bit are both Low.*

6.1.29 Bank 0 R25: ADCR2 (ADC Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF2	VOF1	VOF0	CKR2	CKR1	CKR0

Bit 7 (CALI): Calibration enable bit for A/D offset

0: Disable Calibration

1: Enable Calibration

Bit 6 (SIGN): Polarity bit of the offset voltage

0: Negative voltage

1: Positive voltage

Bits 5~3 (VOF2~VOF0): Offset voltage bits

VOF2	VOF1	VOF0	OFFSET
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bits 2~0 (CKR2~CKR0): The prescaler of oscillator clock rate of ADC

CKR2 CKR1 CKR0	Operation Mode	Max. System Operation Frequency
000 (default)	Fosc/4	4 MHz
001	Fosc/1	1 MHz
010	Fosc/2	2 MHz
011	Fosc/8	8 MHz
100	Fosc/16	16 MHz
101	Fosc/32	32 MHz
110	Fosc/64	64 MHz
111	Internal RC	–

6.1.30 Bank 0 R26: ADICL (ADC Input Select Low Byte Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P67 pin.

0: Disable ADC7, P67 act as I/O pin.

1: Enable ADC7 to act as analog input pin.

Bit 6 (ADE6): AD converter enable bit of P66 pin.

0: Disable ADC6, P66 act as I/O pin

1: Enable ADC6 to act as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin.

0: Disable ADC5, P65 act as I/O pin

1: Enable ADC5 to act as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin.

0: Disable ADC4, P64 act as I/O pin

1: Enable ADC4 to act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin.

0: Disable ADC3, P63 act as I/O pin

1: Enable ADC3 to act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin.

0: Disable ADC2, P62 act as I/O pin

1: Enable ADC2 to act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin.

0: Disable ADC1, P61 act as I/O pin

1: Enable ADC1 to act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin.

0: Disable ADC0, P60 act as I/O pin

1: Enable ADC0 to act as analog input pin

Note: The priority of the P60/ADC0//INT pins are as follows:

P60/ADC1//INT Pin Priority		
High	Medium	Low
/INT	ADC0	P60

6.1.31 Bank 0 R27~R28: (Unused)

6.1.32 Bank 0 R29: ADDH (AD Data High Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

Bits 7~0 (AD11~AD4): AD high 8-bit data buffer. When A/D conversion is complete, the result of high 8 bits is stored into ADDH; the low 4 bits is stored into ADDL. Then the ADRUN bit is cleared and the ADIF is set.

6.1.33 Bank 0 R2A: ADDL (AD Data Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	AD3	AD2	AD1	AD0

Bits 7~4: Unused bits, fixed to 0 all the time.

Bits 3~0 (AD3~AD0): AD low 4-bit data buffer.

6.1.34 Bank 0 R2B~R2E: Unused

6.1.35 Bank 0 R2F: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ICWE	ADWE	0	0	EXWE

Bits 7~5: unused bits, fixed to 0 all the time.

Bit 4 (ICWE): Port 6 Input Status Change Wake-up Enable bit.

0: Disable Port 6 input status change wake-up

1: Enable Port 6 input status change wake-up

When the Port 6 input status change is used to enter an interrupt vector or to wake-up the IC from sleep/idle, the ICWE bit must be set to “Enable“.

Bit 3 (ADWE): A/D Converter Wake-up Function Enable Bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When the AD Complete status is used to enter an interrupt vector or to wake-up the IC from sleep/idle with AD conversion running, the ADWE bit must be set to “Enable“.

Bits 2~1: Unused bits, fixed to 0 all the time.

Bit 0 (EXWE): External Interrupt Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status change is used to enter an interrupt vector or to wake up the IC from sleep, the EXWE bits must be set to "Enable".

6.1.36 Bank 0 R30~R31: (Unused)

6.1.37 Bank 0 R33: I2CSW (I2C Switch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SBIM1	SBIM0	0	0	0	0

Bits 7~6: unused bits, fixed to 0 all the time.

Bits 5~4 (SBIM1~SBIM0): Serial bus interface operating mode select

SBIM1	SBIM0	Operation Mode
0	0	I/O mode
0	1	Reserved
1	0	Reserved
1	1	I2C mode

Bits 3~0: Unused bits, fixed to 0 all the time.

6.1.38 Bank 0 R34~R36: (Unused)

6.1.39 Bank 0 R37: TBPTL (Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Bits 7~0 (TB7~TB0): Table Pointer Address Bits 7~0.

6.1.40 Bank 0 R38: TBPTH (Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8

Bit 7 (HLB): Take MLB or LSB at machine code.

Bits 6~5 (GP1~GP0): General Purpose read/write bits

Bits 4~0: Table Pointer Address Bits 12~8.

6.1.41 Bank 0 R39~R4D: Unused

6.1.42 Bank 0 R4E: TC3CR (Timer 3 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7~6 (TC3FF1~TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0: Stop and clear counter

1: Start

Bits 4~2 (TC3CK2~TC3CK0): Timer/Counter 3 clock source select.

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
			Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	$F_C/2^{11}$	256μs	65536μs	128ms	32768ms
0	0	1	$F_C/2^7$	16μs	4096μs	8ms	2048ms
0	1	0	$F_C/2^5$	4μs	1024μs	2ms	512ms
0	1	1	$F_C/2^3$	1μs	256μs	500μs	128ms
1	0	0	$F_C/2^2$	500ns	128μs	250μs	64ms
1	0	1	$F_C/2$	250ns	64μs	125μs	32ms
1	1	0	F_C	125ns	32μs	62.5μs	16ms
1	1	1	External clock (TC3 pin)	-	-	-	-

Bits 1~0 (TC3M1~TC3M0): Timer/Counter 3 operating mode select.

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider output
1	1	Pulse Width Modulation output

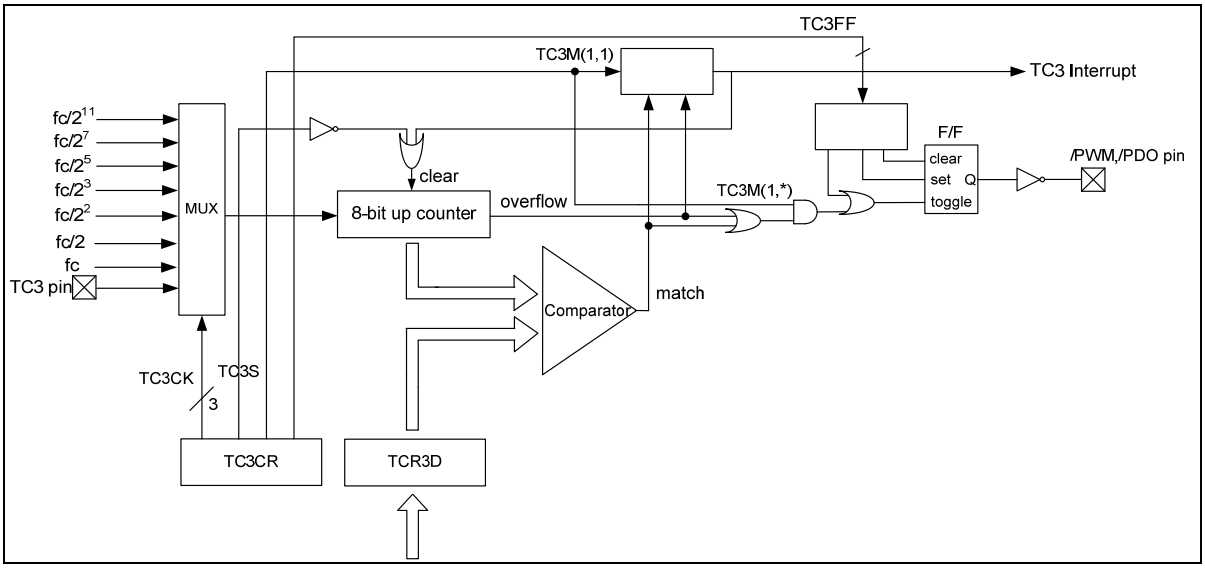


Figure 6-4 Timer/Counter 3 Configuration

In **Timer mode**, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter matched the TCR3D, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In **Counter mode**, counting up is performed using the external clock input pin (TC3 pin). When the contents of the up-counter matched the TCR3D, then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared.

In **Programmable Divider Output (PDO) mode**, counting up is performed using the internal clock. The contents of TCR3D are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by the program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

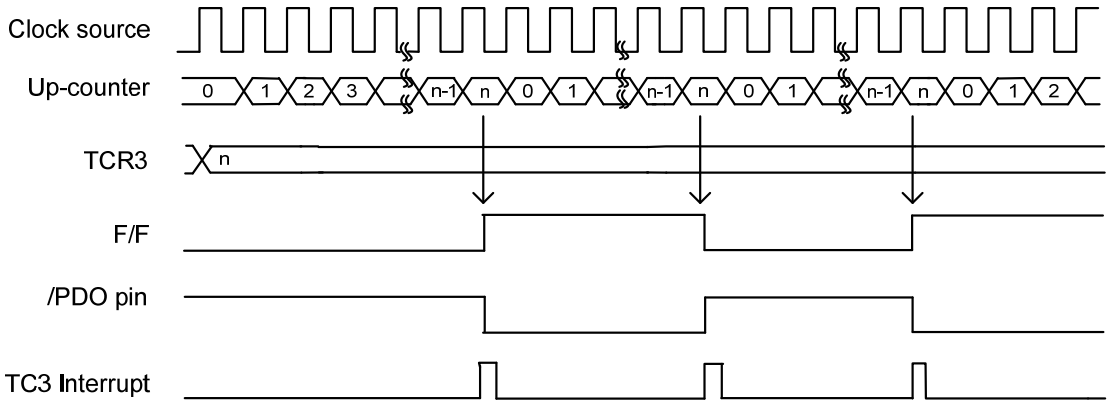


Figure 6-5 PDO Mode Timing Diagram

In **Pulse Width Modulation (PWM) Output mode**, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. The counter is still counting, the F/F is toggled again when the counter overflows, and the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and during output will not switch until one output cycle is completed even if TCR3 is overwritten**. Therefore, the output can be changed continuously. Also, the first time, TRC3 is shifted by setting TC3S to "1" after data is loaded to TCR3.

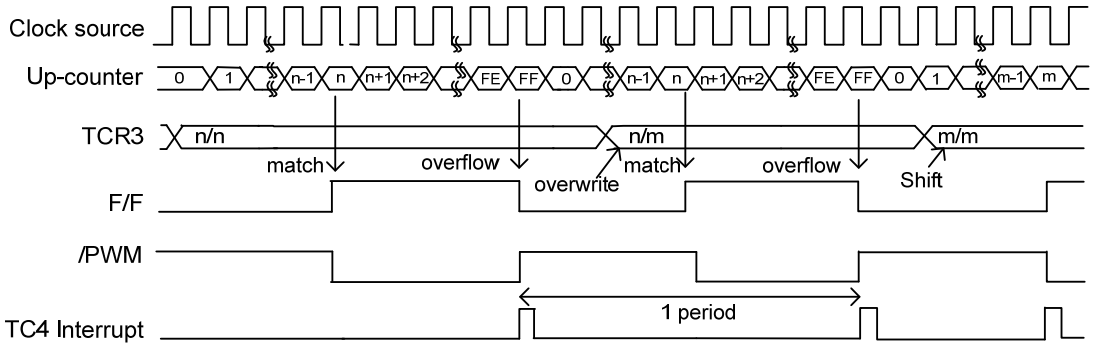


Figure 6-6 PWM Mode Timing Diagram

6.1.43 Bank 0 R4F: TCR3D (Timer 3 Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0

Bits 7~0 (TCR3D7~TCR3D0): Data Buffer of 8-bit Timer/Counter 3

6.1.44 Bank 1 R5: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

Bit 7 (/PH57): Control bit used to enable pull high of the P57 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH56): Control bit used to enable pull high of the P56 pin

Bit 5 (/PH55): Control bit used to enable pull high of the P55 pin

Bit 4 (/PH54): Control bit used to enable pull high of the P54 pin

Bit 3 (/PH53): Control bit used to enable pull high of the P53 pin

Bit 2 (/PH52): Control bit used to enable pull high of the P52 pin

Bit 1 (/PH51): Control bit used to enable pull high of the P51 pin

Bit 0 (/PH50): Control bit used to enable pull high of the P50 pin

6.1.45 Bank 1 R6: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit used to enable pull-high of the P67 pin

Bit 6 (/PH66): Control bit used to enable pull-high of the P66 pin

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin

6.1.46 Bank 1 R7: P7PHCR (Port 7 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70

Bit 7 (/PH77): Control bit used to enable pull-high of the P77 pin

Bit 6 (/PH76): Control bit used to enable pull-high of the P76 pin

Bit 5 (/PH75): Control bit used to enable pull-high of the P75 pin

Bit 4 (/PH74): Control bit used to enable pull-high of the P74 pin

Bit 3 (/PH73): Control bit used to enable pull-high of the P73 pin

Bit 2 (/PH72): Control bit used to enable pull-high of the P72 pin

Bit 1 (/PH71): Control bit used to enable pull-high of the P71 pin

Bit 0 (/PH70): Control bit used to enable pull-high of the P70 pin

6.1.47 Bank 1 R8: P8PHCR (Port 8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	/PH85	/PH84	/PH83	/PH82	/PH81	/PH80

Bits 7~6: Unused bits, set to "**1**" all the time

Bit 6 (/PH86): Control bit used to enable pull-high of the P86 pin

Bit 5 (/PH85): Control bit used to enable pull-high of the P85 pin

Bit 4 (/PH84): Control bit used to enable pull-high of the P84 pin

Bit 3 (/PH83): Control bit used to enable pull-high of the P83 pin

Bit 2 (/PH82): Control bit used to enable pull-high of the P82 pin

Bit 1 (/PH81): Control bit used to enable pull-high of the P81 pin

Bit 0 (/PH80): Control bit used to enable pull-high of the P80 pin

6.1.48 Bank 1 R9~RA: (Unused)

6.1.49 Bank 1 RB: P5PLCR (Port 5 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50

Bit 7 (/PL57): Control bit used to enable pull low of the P57 pin

0: enable internal pull-low

1: disable internal pull-low

Bit 6 (/PL56): Control bit used to enable pull low of the P56 pin

Bit 5 (/PL55): Control bit used to enable pull low of the P55 pin

Bit 4 (/PL54): Control bit used to enable pull low of the P54 pin

Bit 3 (/PL53): Control bit used to enable pull low of the P53 pin

Bit 2 (/PL52): Control bit used to enable pull low of the P52 pin

Bit 1 (/PL51): Control bit used to enable pull low of the P51 pin

Bit 0 (/PL50): Control bit used to enable pull low of the P50 pin

6.1.50 Bank 1 RC: P6PLCR (Port 6 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60

Bit 7 (/PL67): Control bit used to enable pull low of the P67 pin

Bit 6 (/PL66): Control bit used to enable pull low of the P66 pin

Bit 5 (/PL65): Control bit used to enable pull low of the P65 pin

Bit 4 (/PL64): Control bit used to enable pull low of the P64 pin

Bit 3 (/PL63): Control bit used to enable pull low of the P63 pin

Bit 2 (/PL62): Control bit used to enable pull low of the P62 pin

Bit 1 (/PL61): Control bit used to enable pull low of the P61 pin

Bit 0 (/PL60): Control bit used to enable pull low of the P60 pin

6.1.51 Bank 1 RD: P7PLCR (Port 7 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70

Bit 7(/PL77): Control bit used to enable pull low of the P77 pin

Bit 6(/PL76): Control bit used to enable pull low of the P76 pin

Bit 5(/PL75): Control bit used to enable pull low of the P75 pin

Bit 4(/PL74): Control bit used to enable pull low of the P74 pin

Bit 3(/PL73): Control bit used to enable pull low of the P73 pin

Bit 2(/PL72): Control bit used to enable pull low of the P72 pin

Bit 1(/PL71): Control bit used to enable pull low of the P71 pin

Bit 0(/PL70): Control bit used to enable pull low of the P70 pin

6.1.52 Bank 1 RE: P8PLCR (Port 8 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	/PL85	/PL84	/PL83	/PL82	/PL81	/PL80

Bits 7~6: Unused bits, set to "**1**" all the time

Bit 5 (/PL85): Control bit used to enable pull low of the P85 pin

Bit 4 (/PL84): Control bit used to enable pull low of the P84 pin

Bit 3 (/PL83): Control bit used to enable pull low of the P83 pin

Bit 2 (/PL82): Control bit used to enable pull low of the P82 pin

Bit 1 (/PL81): Control bit used to enable pull low of the P81 pin

Bit 0 (/PL80): Control bit used to enable pull low of the P80 pin

6.1.53 Bank 1 R9~R10: (Unused)

6.1.54 Bank 1 R11: P5HD/SCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H57	/H56	/H55	/H54	/H53	/H52	/H51	/H50

Bits 7~0 (H57~H50): P57~P50 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.55 Bank 1 R12: P6HD/SCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H67	/H66	/H65	/H64	/H63	/H62	/H61	/H60

Bits 7~0 (H67~H60): P67~P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.56 Bank 1 R13: P7HD/SCR (Port 7 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H77	/H76	/H75	/H74	/H73	/H72	/H71	/H70

Bits 7~0 (H77~H70): P77~P70 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.57 Bank 1 R14: P8HD/SCR (Port 8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	/H85	/H84	/H83	/H82	/H81	/H80

Bits 7~6: Unused bits, set to "**1**" all the time

Bits 5~0 (H85~H80): P85~P80 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.58 Bank 1 R15~R16: (Unused)

6.1.59 Bank 1 R17: P5ODCR (Port 5 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50

Bits 7~0 (OD57~OD50): Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.60 Bank 1 R18: P6ODCR (Port 6 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

Bits 7~0 (OD67~OD60): Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.61 Bank 1 R19: P7ODCR (Port 7 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70

Bits 7~0 (OD77~OD70): Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.62 Bank 1 R1A: P8ODCR (Port 8 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	OD85	OD84	OD83	OD82	OD81	OD80

Bits 7~6: Unused bits, set to "**0**" all the time

Bits 5~0 (OD85~OD80): Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.63 Bank 1 R1B~ R1C: (Unused)

6.1.64 Bank 1 R1D: IRCS (IRC Frequency Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RCM1	RCM0	0	0	0	0

Bits 7~6: Unused bits, fixed to 0 all the time.

Bits 5~4 (RCM1 ~ RCM0): IRC Mode Frequency Select Bits

RCM 1	RCM 0	Frequency (MHz)
0	0	4
0	1	16
1	0	8
1	1	Reserved

Word 1 COBS0 = 0 :

The R1D<5,4> of the initialized values will keep the same Word 1<6,5>.

The R1D<5,4> cannot change.

Word 1 COBS0 = 1 :

The R1D<5,4> of the initialized values will keep the same Word 1<6,5>.

The R1D<5,4> can change, when user wants to work on other IRC frequency.

ex. 4M → 16M

Bits 3~0: unused bits, fixed to 0 all the time.

6.1.65 Bank 1 R1E: (Unused)

6.1.66 Bank 1 R1F: EEPROM Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	0	0	0

Bit 7 (RD): Read control bit

0: Do not execute EEPROM read

1: Read EEPROM content (RD can be set by software. When read instruction is completed, RD will be cleared by hardware).

Bit 6 (WR): Write control bit

0: Write cycle to the EEPROM is completed.

1: Initiate a write cycle (WR can be set by software. When write cycle is completed, WR will be cleared by hardware).

Bit 5 (EEWE): EEPROM write enable bit

0: Prohibit write to the EEPROM

1: Allow EEPROM write cycles

Bit 4 (EEDF): EEPROM detective flag

0: Write cycle is completed

1: Write cycle is unfinished

Bit 3 (EEPC): EEPROM power down control bit

0: Switch of EEPROM

1: EEPROM is operating

Bits 2~0: Unused bit, fixed to 0 all the time.

6.1.67 Bank 1 R20: EEPROM ADDR

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0

Bit 7: Unused bit, fixed to 0 all the time

Bits 6~0 (EERA6~EERA0): EEPROM Address Registers

6.1.68 Bank 1 R21: EEPROM Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0

Bits 7~0 (EERD7~EERD0): EEPROM data register. Read only.

6.1.69 Bank 1 R22: (Unused)

6.1.70 Bank 1 R23: I2CCR1 (I2C Status and Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY

Bit 7 (Strobe/Pend): In Master mode, it is used as strobe signal to control the I2C circuit from sending SCL clock. Automatically resets after receiving or transmitting handshake signal (ACK or NACK).

In Slave mode, it is used as pending signal, user should clear it after writing data into the Tx buffer or retrieving data from the Rx buffer to inform the Slave I2C circuit to release an SCL signal.

Bit 6 (IMS): I2C Master/Slave mode select bit.

0: Slave

1: Master

Bit 5 (ISS): I2C Fast/Standard mode select bit. (If Fm is 4 MHz and I2CTS1~0<0,0>)

0: Standard mode (100kbit/s)

1: Fast mode (400kbit/s)

Bit 4 (STOP): In Master mode, if STOP=1 and R/nW=1 then the EM78F665N must return a nACK signal to the Slave device before sending a STOP signal. If STOP=1 and R/nW=0 then the EM78F665N sends a STOP signal after receiving an ACK signal. Reset when the EM78F665N sends a STOP signal to the Slave device.

In Slave mode, if STOP=1 and R/nW=0 then the EM78F665N must return a nACK signal to the Master device.

Bit 3 (SAR_EMPTY): Set when the EM78F665N transmits a "1" byte data from the I2C Slave Address Register and receives an ACK (or nACK) signal. Reset when the MCU writes a "1" byte data to the I2C Slave Address Register.

Bit 2 (ACK): The ACK condition bit is set to "1" by hardware when the device responds with an "acknowledge" (ACK) signal. Reset when the device responds with a "not-acknowledge" (nACK) signal.

Bit 1 (FULL): Set by hardware when the I2C Receive Buffer Register is full. Reset by hardware when the MCU reads data from the I2C Receive Buffer Register.

Bit 0 (EMPTY): Set by hardware when the I2C Transmit Buffer Register is empty and receives an ACK (or nACK) signal. Reset by hardware when the MCU writes new data to the I2C Transmit Buffer Register.

6.1.71 Bank 1 R24: I2CCR2 (I2C Status and Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CBF	GCEN	0	0	I2CTS1	I2CTS0	0	I2CEN

Bit 7 (I2CBF): I2C Busy Flag Bit

0: Clear to "0" in Slave mode, if the received STOP signal or the I2C Slave address does not match.

1: Set when I2C communicates with Master in Slave mode.

Bit 6 (GCEN): I2C General Call Function Enable Bit

0: Disable General Call Function

1: Enable General Call Function

Bits 5~4: Unused bits, fixed to 0 all the time.

Bits 3~2 (I2CTS1~I2CTS0): I2C Transmit Clock Source Select Bits (when I2CCS=0). When using different operating frequency Fm, these bits must be set correctly with the correct values in order for the SCL clock to be consistent in Standard/Fast mode.

I2CCR1 Bit 5 = 1, Fast mode

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/10	4
0	1	Fm/20	8
1	0	Fm/30	12
1	1	Fm/40	16

I2CCR1 Bit 5 = 0, Standard mode

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/40	4
0	1	Fm/80	8
1	0	Fm/120	12
1	1	Fm/160	16

Bit 1: Unused bit, fixed to 0 all the time.

Bit 0 (I2CEN): I2C Enable Bit

0: Disable I2C mode

1: Enable I2C mode

6.1.72 Bank 1 R25: I2CSA (I2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW

Bits 7~1 (SA6~SA0): When the EM78F665N is used as Master device for I2C application, these are the Slave device address register.

Bit 0 (IRW): When the EM78F665N is used as Master device for I2C application, this bit is Read/Write transaction control bit.

0: Write

1: Read

6.1.73 Bank 1 R26: I2CDA (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Bits 7~0 (DA7~DA0): When the EM78F665N is used as Slave device for I2C application, this register stores the address of the EM78F665N. It is used to identify the data on the I2C bus to extract the message delivered to the EM78F665N.

6.1.74 Bank 1 R27: I2CDB (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Bits 7~0 (DB7~DB0): I2C Receive/Transmit Data Buffer.

6.1.75 Bank 1 R28: I2CA (I2C Device High Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	DA9	DA8

Bits 7~2: Unused bits, fixed to 0 all the time.

Bits 1~0 (DA9~DA8): High Bits of Device Address.

6.1.76 Bank 1 R29: (Unused)

6.1.77 Bank 1 R2A: PWMER (PWM Enable Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	PWMBE	PWMAE

Bits 7~2: Unused bits, fixed to 0 all the time.

Bit 1 (PWMBE): PWM B Enable bit

0: PWM B is off (default value), and its related Pin P52 carries out the I/O pin function.

1: PWM B is on, and its related pin is automatically set to output.

Bit 0 (PWMAE): PWM A Enable bit.

0: PWM A is off (default value), and its related pin carries out the I/O pin function

1: PWM A is on, and its related pin is automatically set to output

6.1.78 Bank 1 R2B: TIMEN (Timer/PWM Enable Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	TBEN	TAEN

Bits 7~2: Unused bits, fixed to 0 all the time.

Bit 1 (TBEN): Timer B enable bit

0: Timer B is off (default)

1: Timer B is on

Bit 0 (TAEN): Timer A enable bit

0: Timer A is off (default)

1: Timer A is on

6.1.79 Bank 1 R2C~R2E: Unused

6.1.80 Bank 1 R2F: PWMACR (PWM A Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRCBA	0	0	0

Bits 7~4: Unused bits, fixed to "**0**" all the time

Bit 3 (TRCBA): Timer A Read Control Bit

0: When this bit set to "**0**", the values of PRDA[9]~PRDA[0] in PRDAL and PRDxH are PWMA period data.

1: When this bit set to "**1**", the values read from PRDA[9]~PRDA[0] in PRDAL and PRDxH are PWMA timer data.

Bits 2~0: Unused bits, fixed to "**0**" all the time

6.1.81 Bank 1 R30: PWMBCR (PWM B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRCBB	0	0	0

Bits 7~4: Unused bits, fixed to "**0**" all the time

Bit 3 (TRCBB): Timer B Read Control Bit

0: When this bit is set to 0, the values of PRDB[9]~PRDB[0] in PRDBL and PRDxH are PWMB period data.

1: When this bit is set to 1, the values of PRDB[9]~PRDB[0] in PRDBL and PRDxH are PWMB timer data.

Bits 2~0: Unused bits, fixed to "**0**" all the time.

6.1.82 Bank 1 R31: Unused

6.1.83 Bank 1 R32: TACR (Timer A Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	TAP2	TAP1	TAP0

Bits 7~3: Unused bit, fixed to "**0**" all the time.

TAP2	TAP1	T1AP0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.84 Bank 1 R33: TBCR (Timer B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	TBP2	TBP1	TBP0

Bits 7~3: Unused bits, fixed to "**0**" all the time.

Bits 2~0 (TBP2~TBP0): Timer B Prescaler Bits

TBP2	TBP1	TBP0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.85 Bank 1 R34: Unused

6.1.86 Bank 1 R35: TAPRDH (Timer A Period Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA[9]	PRDA[8]	PRDA[7]	PRDA[6]	PRDA[5]	PRDA[4]	PRDA[3]	PRDA[2]

Bits 7~0 (PRDA[9]~PRDA[2]): The contents of this register is a period of Timer A.

6.1.87 Bank 1 R36: TBPRDH (Timer B Period Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

Bits 7~0 (PRDB[9]~PRDB[2]): The contents of this register is a period of Timer B.

6.1.88 Bank 1 R37: Unused

6.1.89 Bank 1 R38: TADTH (Timer A Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]

Bits 7~0 (DTA[9]~ DTA[2]): The contents of this register is a duty of Timer A.

6.1.90 Bank 1 R39: TBDTH (Timer B Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]

Bits 7~0 (DTB[9]~DTB[2]): The contents of this register is a duty of Timer B.

6.1.91 Bank 1 R3A: Unused

6.1.92 Bank 1 R3B: PRDxL (PWM A/B Period Buffer Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	PRDB[1]	PRDB[0]	PRDA[1]	PRDA[0]

Bits 7~4: Unused bits, fixed to "**0**" all the time.

Bits 3~2 (PRDB[1]~PRDB[0]): PWM B period buffer low bits

Bits 1~0 (PRDA[1]~PRDA[0]): PWM A period buffer low bits

6.1.93 Bank 1 R3C: DTxL (PWM1/2 Duty Buffer Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	DTB[1]	DTB[0]	DTA[1]	DTA[0]

Bits 7~4: Unused bits, set to "**0**" all the time.

Bits 3~2 (DTB[1]~DTB[0]): PWM B duty buffer high bits

Bits 1~0 (DTA[1]~DTA[0]): PWM A duty buffer high bits

6.1.94 Bank 1 R3D~R4F: (Unused)

6.1.95 Bank 0 R50~R7F, Banks 0~1 R80~RFF

All of these are 8-bit general-purpose registers.

6.2 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the TCCCR register (Bank 0 R13) are used to determine the ratio of the TCC prescaler. Likewise, the PSW0~PSW2 bits of the WDTCR register (Bank 0 R11) are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Fig. 15 depicts the circuit diagram of TCC/WDT.

Bank 0 R14 (TCCDATA) is an 8-bit timer/counter. The TCC clock source of can be internal clock or external signal input (edge selectable from the TCC pin). If the TCC signal source is from the internal clock, the TCC will be incremented by 1 at every clock cycle (without prescaler), as illustrated in Figure 6-7. If the TCC signal source is from the external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (keep in High or low level) must be greater than 1CLK. **The TCC will stop running when sleep mode occurs.**

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or in sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of IOCE0 register. With no prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

[1] VDD=5V, WDT time-out period = 16.5ms ± 8%.
VDD=3V, WDT time-out period = 18ms ± 8%.

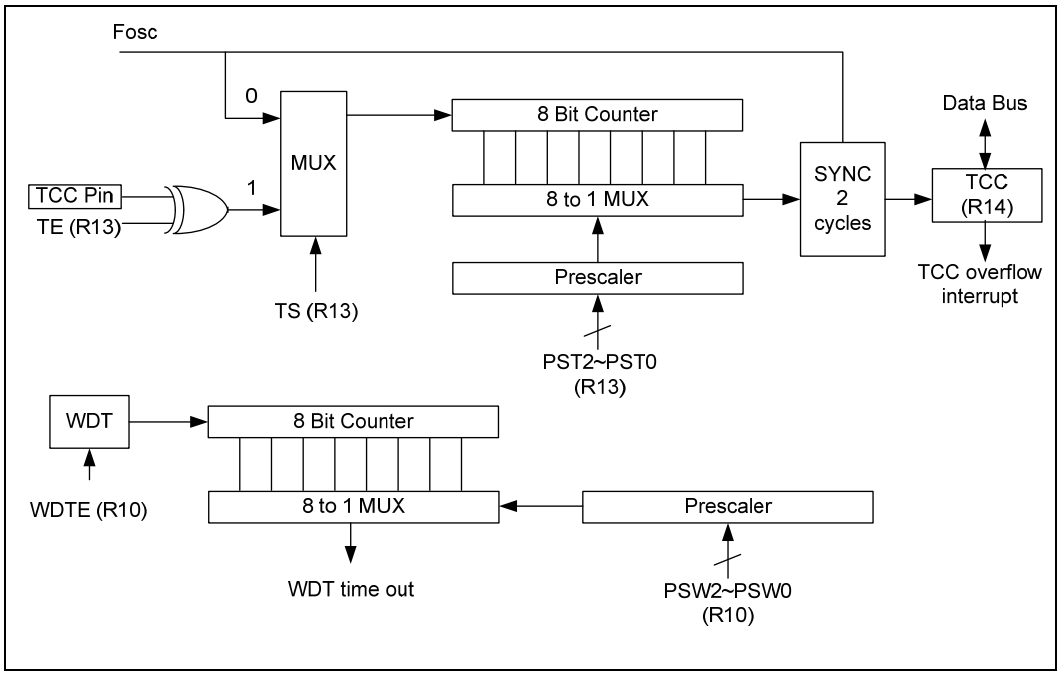


Figure 6-7 TCC and WDT Block Diagram

6.3 I/O Ports

The I/O registers Port 5~Port 8 are bi-directional tri-state I/O ports. All have high sink/drive setting by software. Port 5, Port 6 and Port 7 also have wake-up function. Further, Port 6 has input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable.

Table 1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change	(II) Port 6 Input Status Change Interrupt
(a) Before Sleep	1. Read I/O Port 6 (MOV R6,R6)
1. Disable WDT[2] (very carefully)	2. Execute "ENI"
2. Read I/O Port 6 (MOV R6,R6)	3. Enable interrupt
3. Enable interrupt, after wake-up if “ENI” switch to Interrupt Vector (006H), if “DISI” execute next instruction	4. If Port 6 change (interrupt) → Interrupt Vector (006H)
3. Disable interrupt, always execute next instruction	
4. Enable wake-up enable bit	
5. Execute "SLEP" instruction	
(b) After Wake-up	
1. IF "ENI" → Interrupt vector (006H)	
2. IF "DISI" → Next instruction	

6.4 I2C Function

R_Bank	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0X23	I2CCR1	Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X24	I2CCR2	0	0	0	0	I2CTS1	I2CTS0	I2CCS	I2CEN
			R	R	R	R	R/W	R/W	R/W	R/W
Bank 1	0X25	I2CSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X26	I2CDA	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X27	I2CDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X28	I2CA	0	0	0	0	0	0	DA9	DA8
			–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	ISR3	0	0	0	0	I2CDTPIF	0	I2CRIF	I2CTIF
			R	R	R	R	R	R/W	R/W	R/W
Bank 0	0x1E	IMR3	0	0	0	0	I2CDTPIE	0	I2CRIE	I2CTIE
			R	R	R	R	R	R/W	R/W	R/W

[2] **Note:** The Software disables the WDT (Watchdog Timer) but the hardware must be enabled before applying Port 6 Change Wake-up function. (Set Code Option Register and Bit 11 (ENWDTB-) to “1”).

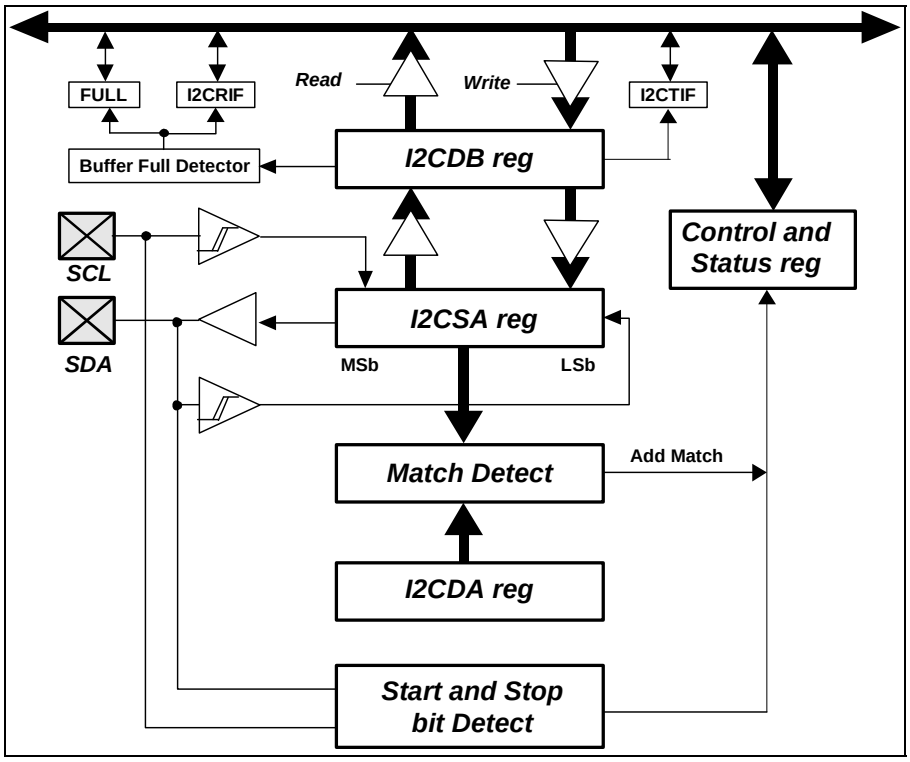


Figure 6-8 I2C Block Diagram

The EM78F665N supports a bidirectional, 2-wire bus, 7-bit and 10-bit addressing, as well as data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions. Both Master and Slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I2C-bus can be transferred at rates of up to 100kbit/s in Standard mode or up to 400kbit/s in Fast mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Within the procedure of the I2C bus, unique situations arise which are defined as START (S) and STOP (P) conditions.

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

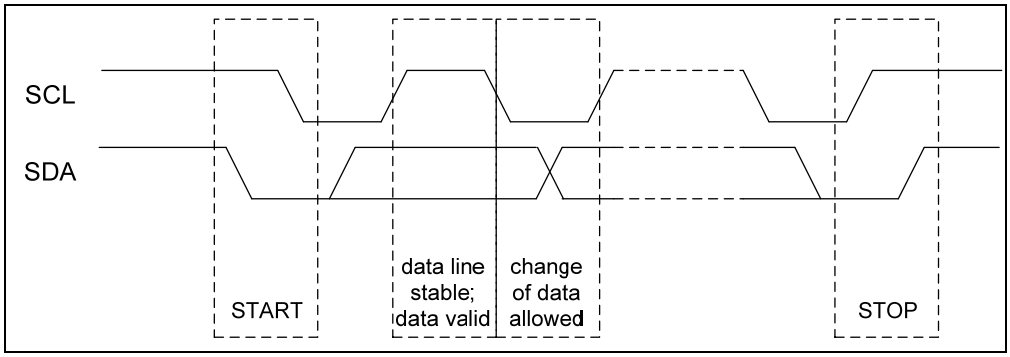


Figure 6-9 I2C Transfer Condition

7-Bit Slave Address:

Master-transmitter transmits to Slave-receiver. The transfer direction is not changed.

The Master reads the Slave immediately after the first byte. At the moment of the first acknowledge, the Master- transmitter becomes a Master- receiver and the Slave-receiver becomes a Slave-transmitter. This first acknowledge is still generated by the Slave. The STOP condition is generated by the Master, which has previously sent a not-acknowledge (A). The difference between Master transmitter with Master receiver is only in R//W bit, if the R//W bit is "0", the Master device would be a transmitter, the other way, the Master device would be a receiver. The Master transmitter is described in "Figure 6-10 (*7-Bit Slave Address in Master-transmitter Transmits to Slave-receiver)"*, and the Master receiver is described in the "Figure 6-11 (*7-Bit Slave Address in Master-receiver Reads Slave-transmitter)*".

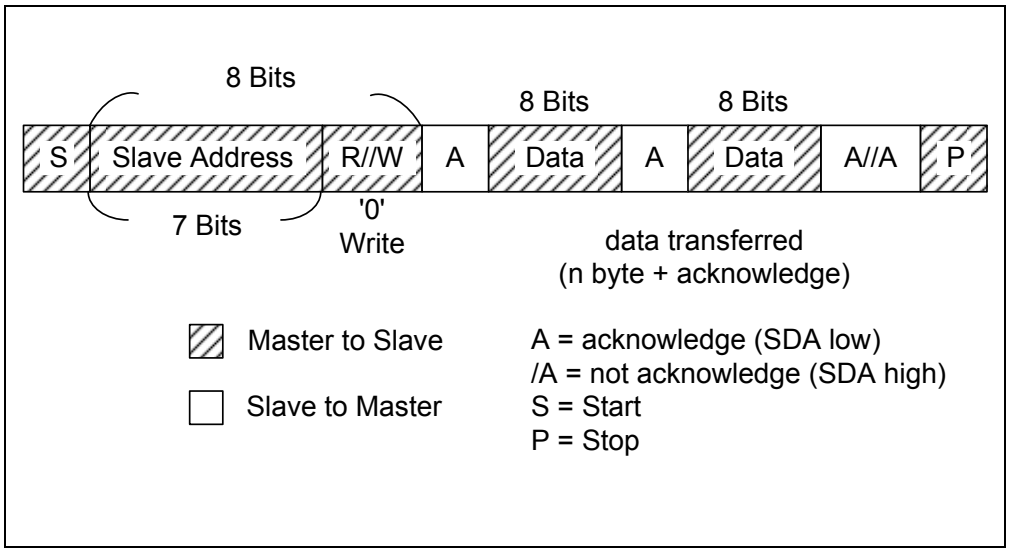


Figure 6-10 7-Bit Slave Address in Master-transmitter Transmits to Slave-receiver

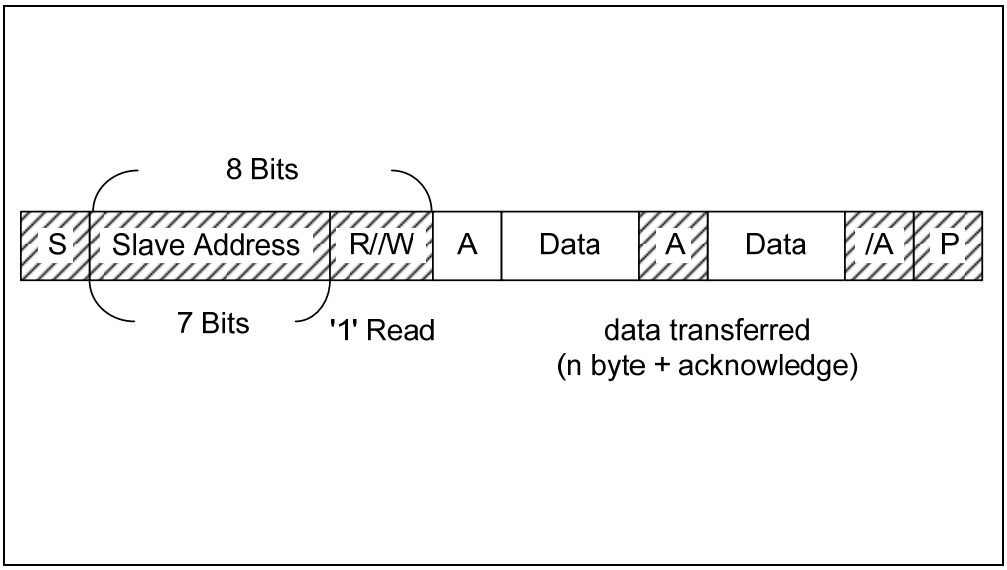


Figure 6-11 7-Bit Slave Address in Master-receiver Reads Slave-transmitter

10-Bit Slave Address:

In 10-Bit slave address mode, using 10-Bit for addressing exploits the reserved combination 11110XX for the first 7 bits of the first byte following a START (S) or repeated START (Sr) condition. The first 7 bits of the first byte are the combination 11110XX of which the last 2 bits (XX) are the two most-significant bits of the 10-bit address. If the R//W bit is "**0**", the second byte after acknowledge would be the 8 address bits of the10-bit slave address. On the other hand, the second byte would just only be the next transmitted data from a Slave to Master device. The first bytes 11110XX are transmitted by using the Slave address register (I2CSA), and the second bytes XXXXXXXX would be transmitted by using the data buffer (I2CDB).

There are few kinds of different formats that would be shown in Figure 6-12 ~ Figure 6-16 in the 10-bit slave address mode. The possible data transfer formats are:

- **Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address**

When the Slave has received the first byte after the START bit from the master, each slave device will compare the 7 bits of the first byte (11110XX) with their own address and the 8th bit, R//W, if the R//W bit is "0", the slave would return the acknowledge (A1) and that would be possible for more than 1 slave device to return it. Then all slave devices will continue to compare the second address (XXXXXXXX), if the slave device has matched, that would be only 1 slave device to return acknowledge. The matching slave device will remain addressed by the master until it receives a STOP condition or a repeated START condition followed by the different slave address.

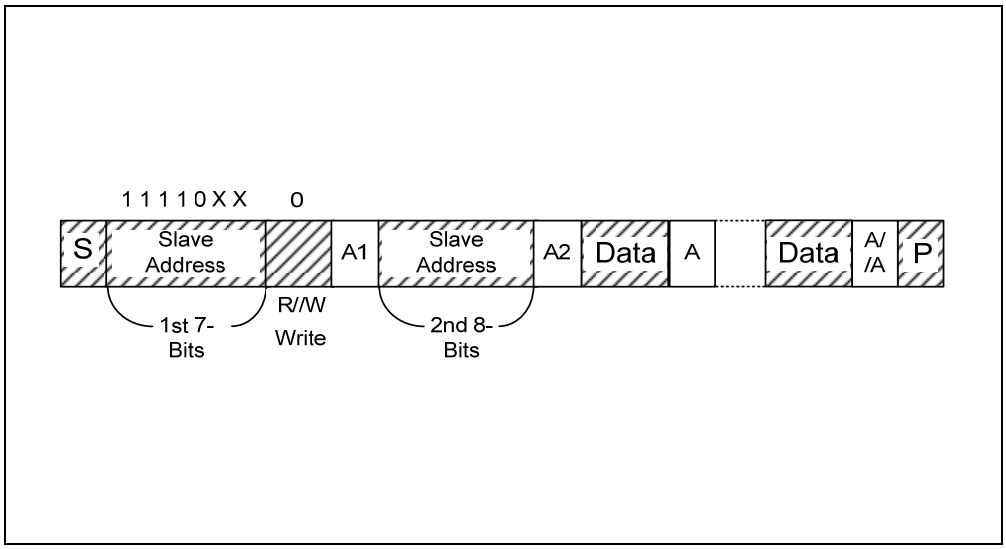


Figure 6-12 Master-transmitter Transmits to Slave-receiver with a 10-bit Slave Address

■ Master-Receiver Read Slave-Transmitter with a 10-bit Slave Address

Up to and including Acknowledge Bit A2, the procedure is the same as that described for Master-transmitter addressing a Slave receiver. After the Acknowledge A2, a repeated START condition (Sr) followed by 7 bits Slave address (11110XX) but the 8th bit R//W is “1”, the addressed Slave device will return an Acknowledge A3. If the repeated START (Sr) condition and the 7 bits of the first byte (11110XX) are received by the Slave device, all the Slave device would compare with their own address and test the 8th R//W, but none of the slave devices return an acknowledge because R//W=1.

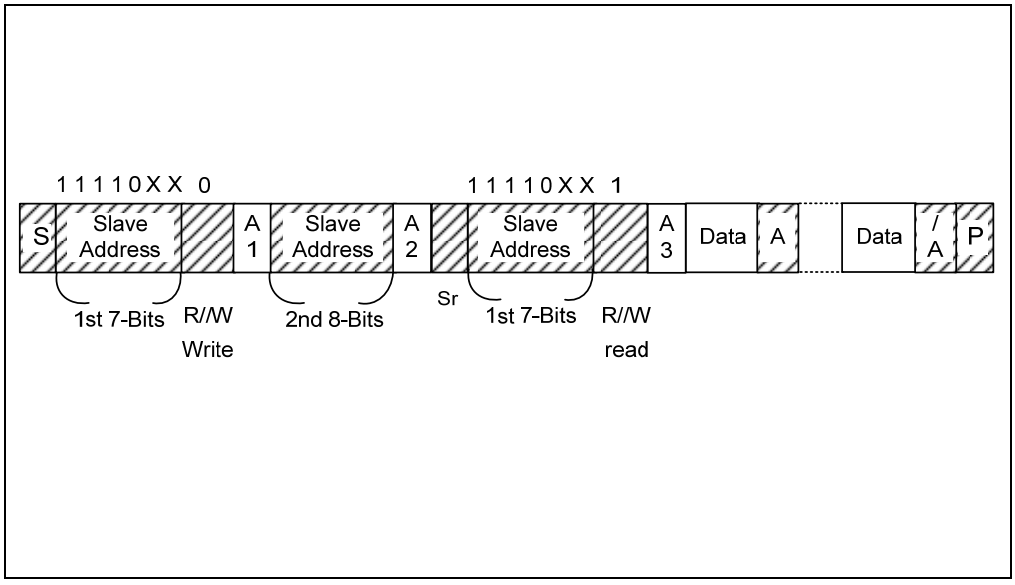


Figure 6-13 Master-receiver Reads Slave-transmitter with a 10-bit Slave Address

■ **Master Addresses a Slave with 10-Bit Addresses Transmits and Receives Data in the Same Slave Device.**

At first, the transmitter procedure is the same as the section of the “Master-transmitter transmits to slave-receiver with a 10-bit slave address”, then the master device can start to transmit the data to the slave device. If the slave device has received an Acknowledge or None Acknowledge which were followed by repeat START (Sr), repeat the procedure of the section of “Master-receiver read slave-transmitter with a 10-bit slave address”.

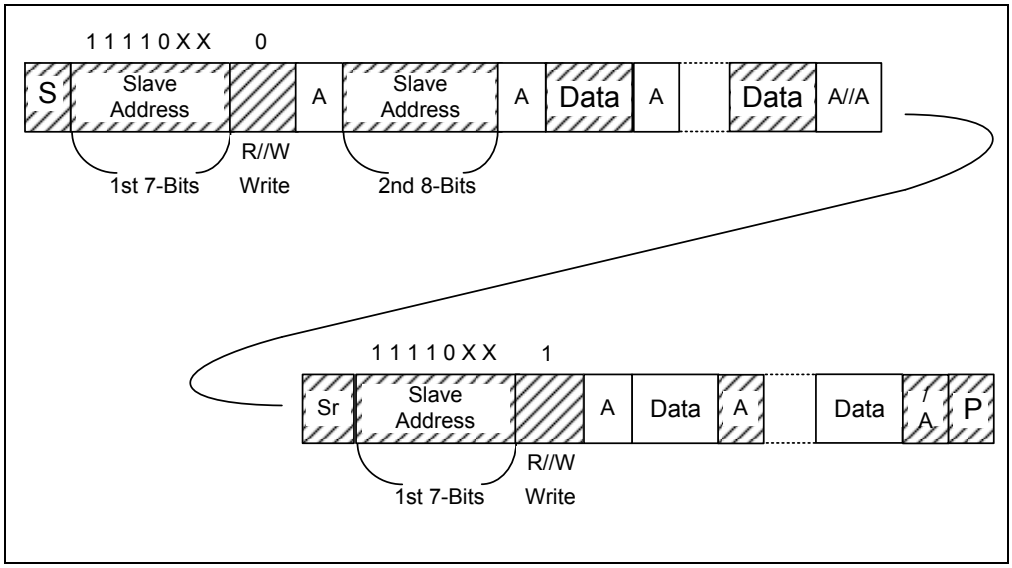


Figure 6-14 Master Addresses a Slave with 10-Bit addresses Transmits and Receives Data in the Same Slave Device.

■ **Master Device Transmits Data to Two or More Than Two Slave Devices**

The section on “Master-transmitter transmits to Slave-receiver with a 10-bit Slave address” describes the procedure on how to transmit the data to Slave device, if the Master device has finished the transmittal, and wants to transmit the data to another device, the Master would need to address the new Slave device, the address procedure is described in the section on “Master-transmitter transmits to Slave-receiver with a 10-Bit Slave address”. If the Master device wants to transmit data in 7-Bit Slave address mode and transmit the data in 10-Bit Slave address mode in serial transfer, after the START or repeat START conditions, a 7-Bit and 10-Bit address could be transmitted. Figure 6-16 shows how to transmit the data in 7-Bit and 10-Bit address mode in serial transfer.

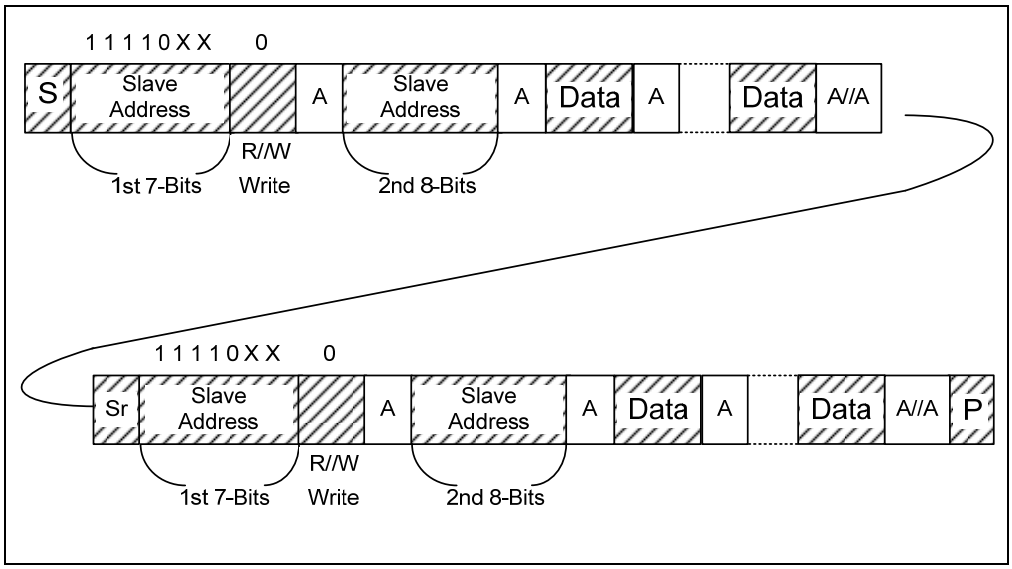


Figure 6-15 Transmit One more Device with a 10-bit Slave Address

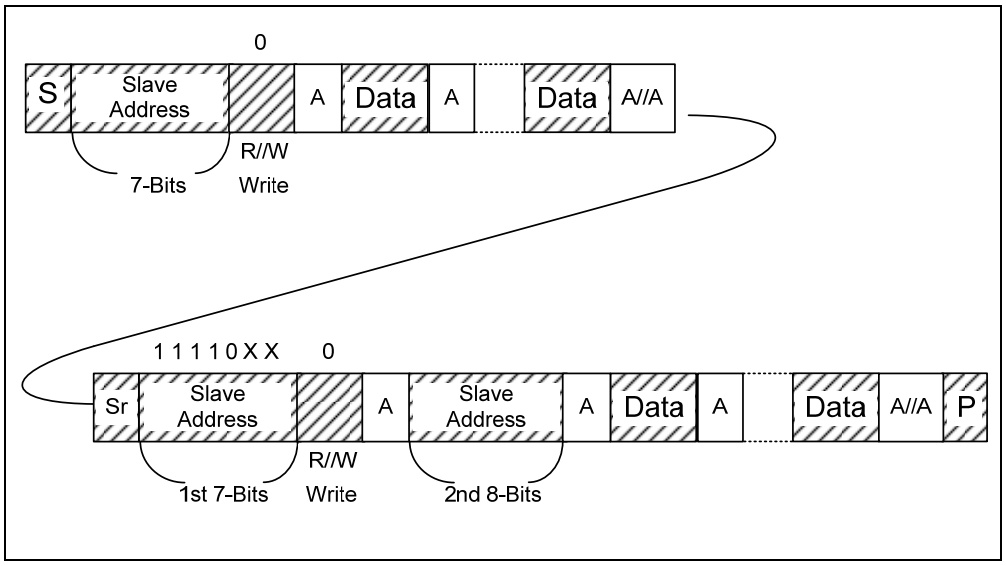


Figure 6-16 7-bit and 10-bit Slave Address Mode

6.4.1 Master Mode

In transmitting serial data, the I2C operates as follows:

1. Set I2CTS1~0, I2CCS and ISS bits to select I2C transmit clock source.
2. Set I2CEN and IMS bits to enable the I2C Master function.
3. Write the Slave address into the I2CSA register and IRW bit to select read or write.
4. Set strobe bit to start transmitting and then Check SAR_EMPTY bit.
5. Write the 1st data into the I2CDB register, set the strobe bit and Check EMPTY bit.
6. Write the 2nd data into the I2CDB register, set the strobe bit, STOP bit and Check the EMPTY bit.

6.4.2 Slave Mode

In receiving, the I2C operates as follows:

1. Set I2CTS1~0, I2CCS and ISS bits to select the I2C transmit clock source.
2. Set I2CEN and IMS bits to enable the I2C slave function.
3. Write the device address into the I2CDA register.
4. Check the FULL bit, read I2CDB register (address) and then clear the Pend bit.
5. Check the FULL bit, read I2CDB register (1st data) and then clear the Pend bit.
6. Check the FULL bit, read I2CDB register (2nd data) and then clear the Pend bit.

6.5 A/D Converter

Registers for AD Converter Circuit

R_Bank	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X24	ADCR1	VREFS	ADRUN	ADPD	0	0	ADIS2	ADIS1	ADIS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x25	ADCR2	CALI	SIGN	VOF2	VOF1	VOF0	CKR2	CKR1	CKR0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X26	ADICL	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X29	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
			R	R	R	R	R	R	R	R
Bank 0	0X2A	ADDL	0	0	0	0	ADD3	ADD2	ADD1	ADD0
			–	–	–	–	R	R	R	R
Bank 0	0X1C	IMR1	0	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0C	ISR1	0	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
			–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x2F	WUCR1	0	0	0	ICWE	ADWE	CMP2WE	CMP1WE	EXWE
			R	R	R	R/W	R/W	R/W	R/W	R/W

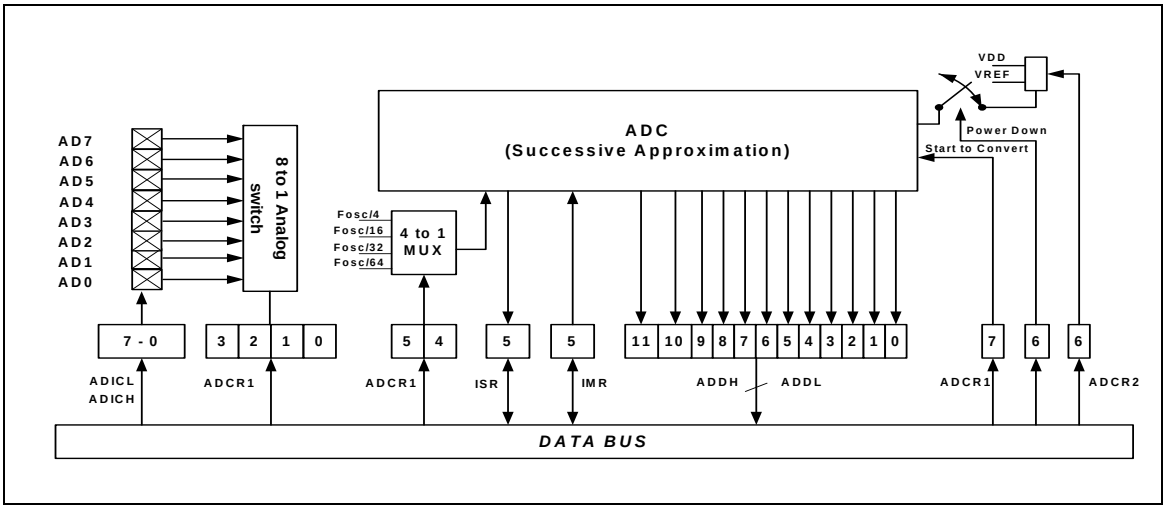


Figure 6-17 AD Converter

This is a 12-bit successive approximation type AD converter. The upper side of the analog reference voltage can select either internal VDD or external input Pin P50 (VREF) by setting the VREFS bit in ADCR1. Connecting to the external VREF is more accurate than connecting to the internal VDD.

6.5.1 ADC Data Register

When A/D conversion is completed, the result is loaded to the ADDH (8-bit) and ADDL (4-bit). The START/END bit is cleared, and the ADIF is set.

6.5.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μs for each KΩ of the analog source impedance and at least 2 μs for the low-impedance source. The maximum recommended impedance for the analog source is 10KΩ at VDD =5V. After the analog input channel is selected, this acquisition time must be done before A/D conversion can be started.

6.5.3 A/D Conversion Time

ADCK0 and ADCK1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at maximum frequency without sacrificing accuracy of the A/D conversion. For the EM78F665N, the conversion time per bit is 4 μs. Table 2 shows the relation between Tct and the maximum operating frequencies.

Table 2

CKR2~CKR0	Operation Mode	Max. Frequency (Fc)	Max. Conversion Rate per Bit	Max. Conversion Rate
000	Fosc/4	4 MHz	1 MHz (1 μs)	16 μs (62.5kHz)
001	Fosc/1	1 MHz	1 MHz (1 μs)	16 μs (62.5kHz)
010	Fosc/2	2 MHz	1 MHz (1 μs)	16 μs (62.5kHz)
011	Fosc/8	8 MHz	1 MHz (1 μs)	16 μs (62.5kHz)
100	Fosc/16	16 MHz	1 MHz (1 μs)	16 μs (62.5kHz)
101	Fosc/32	32 MHz	1 MHz (1 μs)	16 μs (62.5kHz)
110	Fosc/64	64 MHz	1 MHz (1 μs)	16 μs (62.5kHz)
111	Internal RC		1 MHz (1 μs)	16 μs (62.5kHz)

6.6 PWM

6.6.1 Overview

In PWM mode, PWMA, PWMB pins produce up to 10-bit resolution PWM output (see Figure 6-18 for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the period. Figure 6-19 depicts the relation between a period and a duty cycle.

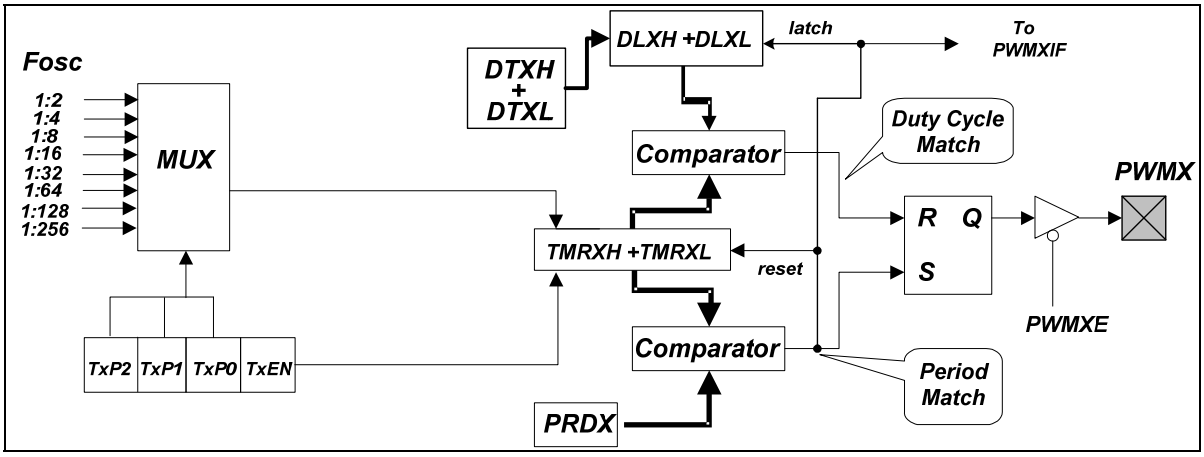


Figure 18 Functional Block Diagram of the Three PWMs

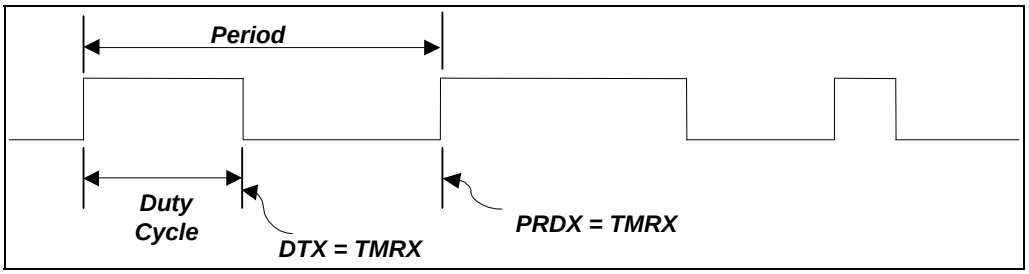


Figure 6-19 Output Timing of the PWM

6.6.2 Increment Timer Counter (TMRX: TMRAH/TWRAL or TMRBH/TWRBL)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. If employed, they can be turned down for power saving by setting TXEN bits to 0.

6.6.3 PWM Period (PRDX: PRDA, PRDB)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared.
- The PWMX pin is set to 1.
- The PWM duty cycle is latched from DTXL/DTXH to DLXL/DLXH.

Note: *The PWM output will not be set, if the duty cycle is "**0**"*;

- The PWMXIF pin is set to 1.

The following formula describes how to calculate the PWM period:

$$Period = (PRDX + 1) \times \left(\frac{1}{Fosc}\right) \times (TMRX \ \ prescaler\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz TMRX (0, 0, 0) = 1 : 2,

Then

$$Period = (49+1) \times \left(\frac{1}{4M}\right) \times 2 = 25\,\mu s$$

6.6.4 PWM Duty Cycle (DTX: DTXH/ DTXL; DLX: DLXH/DLXL)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle**:**

$$Duty\ cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ value)$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 2,

Then

$$Duty\ cycle = (10)\times\left(\frac{1}{4M}\right)\times 2 = 5\,\mu s$$

6.7 Reset and Wake-up

6.7.1 Reset

A reset is initiated by one of the following events -

(1) Power-on reset.

(2) /RESET pin input "low"

(3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 18 ms[3] (one oscillator start-up timer period) after the reset is detected. And if the /Reset pin goes “low” or WDT time-out is active, a reset is generated, in RC mode the reset time is 34 clocks, High XTAL mode reset time is 2 ms and 32 clocks. In low XTAL mode, the reset time is 500 ms. Once a reset occurs, the following functions are performed. Refer to Figure 6-17.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The bits of the control register are set.

The sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After wake-up generated, in RC mode the wake-up time is 34 clocks, High XTAL mode wake-up time is 2 ms and 32 clocks. In low XTAL mode, the wake-up time is 500 ms.

[3] Vdd = 5V, set up time period = 16.8ms ± 8%
Vdd = 3V, set up time period = 18ms ± 8%

The controller can be awakened by -

(1) External reset input on /RESET pin

(2) WDT time-out (if enabled)

(3) External (P60/INT) pin changes (if EXWE is enabled)

(4) Port 6 input status changes (if ICWE is enabled)

(5) A/D conversion completed (if ADWE is enabled)

(6) Port 5 / Port 7 input status changes (if corresponding control bits is enabled)

The first two cases will cause the EM78F665N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, 5, are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0x3, 0x6, 0X15, 0X30 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. Case 6 has no interrupt. All of the sleep mode, wake up time is 150 μs

Only one of Cases 2 to 6 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, the EM78F665N can be waken-up only by Case 1 or Case 2. Refer to the section on Interrupt for further details.

[b] If External (P60,/INT) pin change is used to wake-up the EM78F665N and the EXWE bit is enabled before SLEP, WDT must be disabled. Hence, the EM78F665N can be waken-up only by Case 3.

[c] If Port 6 Input Status Change is used to wake-up the EM78F665N and the corresponding wake-up setting is enabled before SLEP, WDT must be disabled. Hence, the EM78F665N can be waken-up only by Case 4.

[d] If AD conversion completed is used to wake-up the EM78F665N and the ADWE bit of Bank 0 R2F register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F665N can be waken-up only by Case 5.

All kinds of Wake-up mode and interrupt mode are shown below:

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0, EXIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	EXWE = 0, EXIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1, EXIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	EXWE = 1, EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 6 Pin change	ICWE = 0, ICIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ICWE = 0, ICIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWE = 1, ICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICWE = 1, ICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC overflow	TCIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC3 interrupt	TC3IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC3IE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM A/B (When TimerA/B Match PRDA/B)	PWMxIE = 0 (x = A or B)	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid.		Interrupt is invalid.	
	PWMxIE = 1 (x = A or B)	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C TX interrupt	I2CTIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	I2CTIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C RX interrupt	I2CRIE = 0	Wake-up if received correct address		Wake-up if received correct address		Interrupt is invalid		Interrupt is invalid	
	I2CRIE = 1	Wake-up if received correct address		Wake-up if received correct address		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C STOP interrupt	I2CSTPIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid.		Interrupt is invalid.	
	I2CSTPIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

After Wake up:

1. If interrupt enable → interrupt+ next instruction

2. If interrupt disable → next instruction

Table 3 Summary of the Registers Initial Values

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	0	0	0	SBS0	0	0	0	GBS0
		Power-on	0	0	0	U	0	0	0	U
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	P	0	0	0	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	0	0	0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	0	0	0	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X05	Bank 0, R5 (Port 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 0, R6 (Port 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	Bank 0, R7 (Port 7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	Bank 0, R8 (Port 8)	Bit Name	0	0	P85	P84	P83	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0B	Bank 0, RB (OMCR)	Bit Name	CPUS	IDLE	0	0	TC3SS	TASS	TBSS	0
		Power-on	1	1	0	0	0	0	0	0
		/RESET and WDT	1	1	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	Bank 0, RC (ISR1)	Bit Name	0	ADIF	0	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0D	Bank 0, RD (ISR2)	Bit Name	0	0	TC3IF	0	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	Bank 0, RE (ISR3)	Bit Name	0	0	0	0	I2CDTPIF	0	I2CRIF	I2CTIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x10	Bank 0, R10 EIESCR	Bit Name	0	0	0	0	0	0	0	EIES
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	0	0	P
0x11	Bank 0, R11 WDTCR	Bit Name	WDTE	EIS	INT	0	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	0	P	P	P	P
0X13	Bank 0, R13 TCCCR	Bit Name	0	TCCS	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0X14	Bank 0, R14 TCCDATA	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X15	Bank 0, R15 IOCR5	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X16	Bank 0, R16 IOCR6	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X17	Bank 0, R17 IOCR7	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X18	Bank 0, R18 IOCR8	Bit Name	1	1	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X1C	Bank 0, R1C IMR1	Bit Name	0	ADIE	0	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X1D	Bank 0, R1D IMR2	Bit Name	0	0	TC3IE	0	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X1E	Bank 0, R1E IMR3	Bit Name	0	0	0	0	I2CSTPIE	0	I2CRIE	I2CTIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X20	Bank 0, R20 P5WUCR	Bit Name	WU_P57	WU_P56	WU_P55	WU_P54	WU_P53	WU_P52	WU_P51	WU_P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X21	Bank 0, R21 P5WUECR	Bit Name	WUE_P57	WUE_P56	WUE_P55	WUE_P54	WUE_P53	WUE_P52	WUE_P51	WUE_P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X22	Bank 0, R22 P7WUCR	Bit Name	WU_P77	WU_P76	WU_P75	WU_P74	WU_P73	WU_P72	WU_P71	WU_P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X23	Bank 0, R23 P7WUECR	Bit Name	WUE_P77	WUE_P76	WUE_P75	WUE_P74	WUE_P73	WUE_P72	WUE_P71	WUE_P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X24	Bank 0, R24 ADCR1	Bit Name	VREFS	ADRUN	ADPD	0	0	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X25	Bank 0, R25 ADCR2	Bit Name	CALI	SIGN	VOF2	VOF1	VOF0	CKR2	CKR1	CKR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X26	Bank 0, R26 ADICL	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X29	Bank 0, R29 ADDH	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X2A	Bank 0, R2A ADDL	Bit Name	0	0	0	0	AD3	AD2	AD1	AD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0X2F	Bank 0, R2F WUCR1	Bit Name	0	0	0	ICWE	ADWE	CMP2WE	CMP1WE	EXWE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0X33	Bank 0, R33 I2CSW	Bit Name	0	0	SBIM1	SBIM0	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	P	0	0	0
0X37	Bank 0, R37 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X38	Bank 0, R38 TBPTH	Bit Name	HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X4E	Bank 0, R4E TC3CR	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X4F	Bank 0, R4F TC3RD	Bit Name	TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X05	Bank 1, R5 P5PHCR	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X06	Bank 1, R6 P6PHCR	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X07	Bank 1, R7 P7PHCR	Bit Name	/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X08	Bank 1, R8 P8PHCR	Bit Name	1	1	/PH85	/PH84	/PH83	/PH82	/PH81	/PH80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0B	Bank 1, RB P5PLCR	Bit Name	/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0C	Bank 1, RC P6PLCR	Bit Name	/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0D	Bank 1, RD P7PLCR	Bit Name	/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0E	Bank 1, RE P8PLCR	Bit Name	1	1	/PL85	/PL84	/PL83	/PL82	/PL81	/PL80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X11	Bank 1, R11 P5HD/SCR	Bit Name	/H57	/H56	/H55	/H54	/H53	/H52	/H51	/H50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X12	Bank 1, R12 P6HD/SCR	Bit Name	/H67	/H66	/H65	/H64	/H63	/H62	/H61	/H60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X13	Bank 1, R13 P7HD/SCR	Bit Name	/H77	/H76	/H75	/H74	/H73	/H72	/H71	/H70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X14	Bank 1, R14 P58HD/SCR	Bit Name	1	1	/H85	/H84	/H83	/H82	/H81	/H80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X17	Bank 1, R17 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X18	Bank 1, R18 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X19	Bank 1, R19 P7ODCR	Bit Name	OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1A	Bank 1, R1A P8ODCR	Bit Name	0	0	OD85	OD84	OD83	OD82	OD81	OD80
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X1D	Bank 1, R1D IRCS	Bit Name	0	0	RCM1	RCM0	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X1F	Bank 1, R21 EEPROM CONTROL	Bit Name	RD	WR	EEWE	EEDF	EEPC	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X20	Bank 1, R1F EEPROM ADDR	Bit Name	0	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X21	Bank 1, R20 EEPROM DATA	Bit Name	EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X23	Bank 1, R23 I2CCR1	Bit Name	Strobe/ Pend	IMS	ISS	STOP	SAR_ EMPTY	ACK	FULL	EMPTY
		Power-on	0	0	0	0	U	U	U	U
		/RESET & WDT	0	0	0	0	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X24	Bank 1, R24 I2CCR2	Bit Name	I2CBF	GCEN	0	0	I2CTS1	I2CTS0	0	I2CEN
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0X25	Bank 1, R25 I2CSA	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X26	Bank 1, R26 I2CDA	Bit Name	0	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X27	Bank 1, R27 I2CDB	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X28	Bank 1, R28 I2CA	Bit Name	0	0	0	0	0	0	DA9	DA8
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X2A	Bank 1, R2A PWMER	Bit Name	0	0	0	0	0	0	PWMBE	PWMAE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	P	P
0X2B	Bank 1, R2B TIMEN	Bit Name	0	0	0	0	0	0	TBEN	TAEN
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	P	P
0X2F	Bank 1, R2F PWMACR	Bit Name	0	0	0	0	TRCBA	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	0	0
0X32	Bank 1, R32 TACR	Bit Name	0	0	0	0	0	TAP2	TAP1	TAP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	P	P
0X33	Bank 1, R33 TBCR	Bit Name	0	0	0	0	0	TBP2	TBP1	TBP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	P	P
0X35	Bank 1, R35 TAPRDL	Bit Name	PRDA[9]	PRDA[8]	PRDA[7]	PRDA[6]	PRDA[5]	PRDA[4]	PRDA[3]	PRDA[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X36	Bank 1, R36 TBPRDL	Bit Name	PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X38	Bank 1, R38 TADT	Bit Name	DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X39	Bank 1, R38 TBDT	Bit Name	DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X3B	Bank 1, R3B PRDxL	Bit Name	0	0	0	0	PRDB[1]	PRDB[0]	PRDA[1]	PRDA[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	P	P	P	P
0X3C	Bank 1, R3C DTxL	Bit Name	0	0	0	0	DTB[1]	DTB[0]	DTA[1]	DTA[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	P	P	P	P

Legend: ***"u"*** *= unknown or don't care* ***"P"*** *= previous value before reset*
"t" *= Check Table 3*

6.7.2 Status of RST, T, and P of the Status Register

A reset condition is initiated by the following events:

1. A power-on condition,

2. A high-low-high pulse on /RESET pin, and

3. Watchdog timer time-out.

The values of T and P, listed in Table 3 are used to check how the processor wakes up. Table 4 shows the events that may affect the status of T and P.

Table 3 Values of RST, T and P after Reset

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

***P:** Previous status before reset

Table 4 Status of T and P Being Affected by Events

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

***P:** Previous status before reset

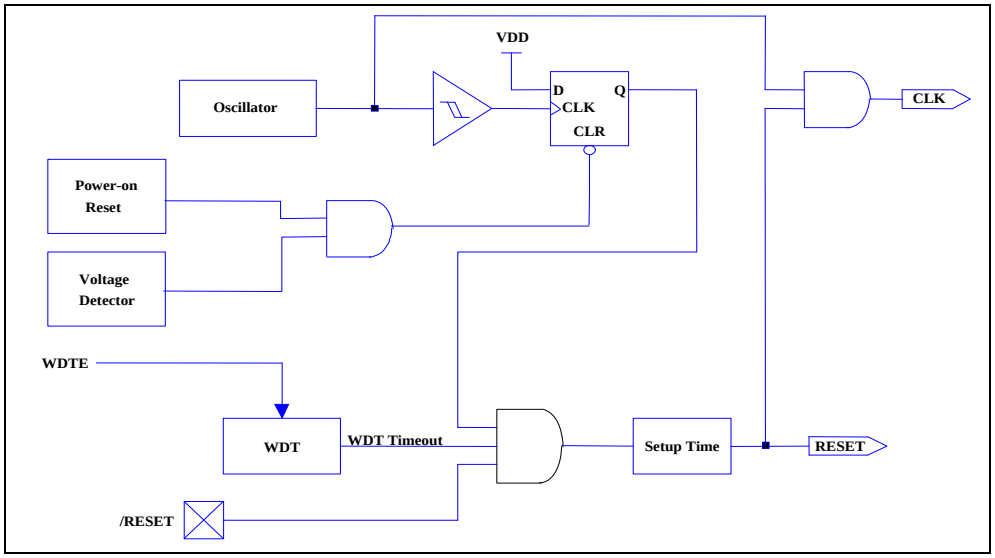


Figure 6-20 Block Diagram of Controller Reset

6.8 Interrupt

The EM78F665N has 10 interrupts (3 external, 7 internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	4
Internal	PWMA	ENI+PWMAIE=1	PWMAIF	002A	5
Internal	PWMB	ENI+PWMBIE=1	PWMBIF	002D	6
Internal	AD	ENI + ADIE=1	ADIF	0030	7
Internal	I2C Transmit	ENI + I2CTIE	I2CTIF	0036	8
Internal	I2C Receive	ENI + I2CRIE	I2CRIF	0039	9
Internal	I2C Stop	ENI + I2CSTPIE	I2CSTPIF	003F	10

Bank 0 RC~RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank 0 R1C~R1F is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse less than **8 system clocks time is eliminated as noise**) When an interrupt (falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC,R3 and R4 will be pushed back.

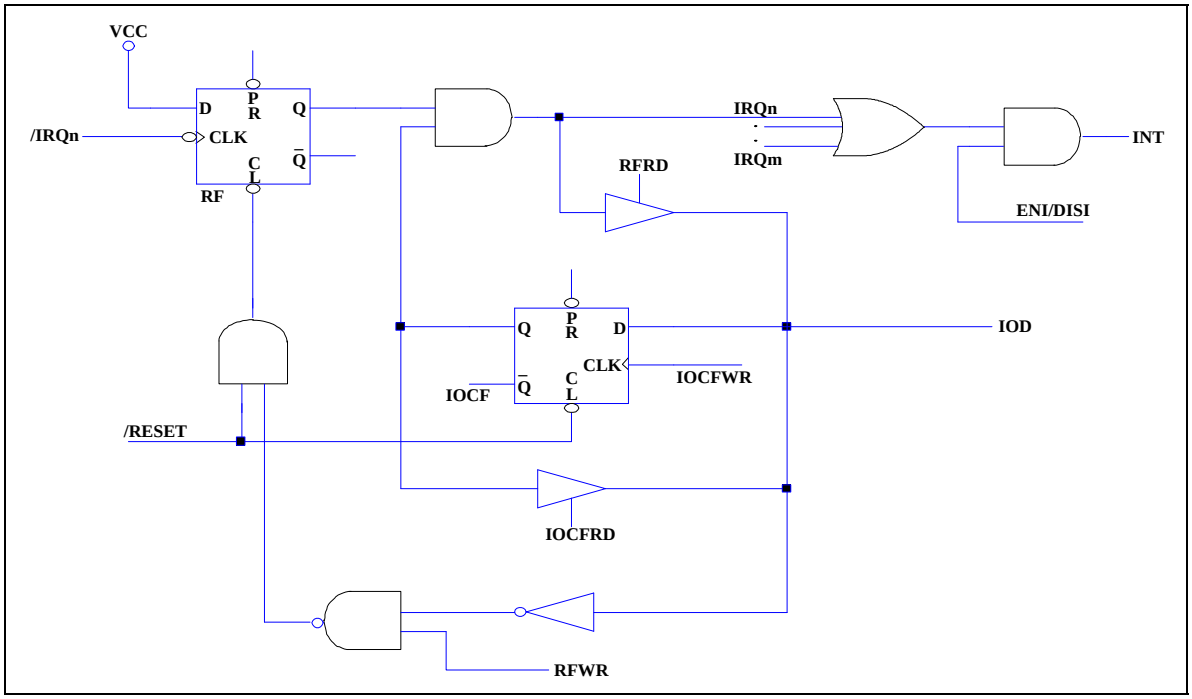


Figure 6-21 Interrupt Input Circuit

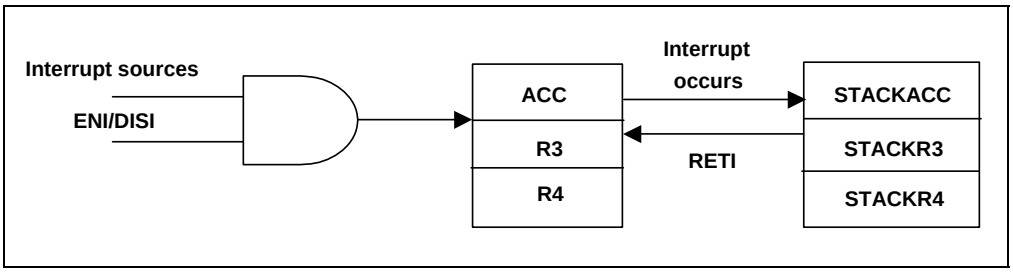


Figure 6-22 Interrupt Backup Diagram

6.9 Data EEPROM

The Data EEPROM is readable and writable during normal operation over the whole Vdd range. The operation for Data EEPROM is base on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provides high erase and write cycles. A byte write automatically erases the location and write the new value.

6.9.1 Data EEPROM Control Register

6.9.1.1 Bank 1 R1F (EEPROM Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	0	0	0

Bit 7(RD): Read control bit

0: Do Not execute EEPROM read

1: Read EEPROM content (RD can be set by software. When read instruction is completed, RD will be cleared by hardware.)

Bit 6 (WR): Write control bit

0: Write cycle to the EEPROM is completed.

1: Initiate a write cycle (WR can be set by software. When write cycle is completed, WR will be cleared by hardware.)

Bit 5 (EEWE): EEPROM write enable bit

0: Prohibit write to the EEPROM

1: Allow EEPROM write cycles

Bit 4 (EEDF): EEPROM detective flag

0: Write cycle is completed

1: Write cycle is unfinished

Bit 3 (EEPC): EEPROM power down control bit

0: Switch of EEPROM

1: EEPROM is operating

Bits 2~0: Unused bit, set to "**0**" all the time

6.9.1.2 Bank 1 R20 (128 Bytes EEPROM Address)

When accessing the EEPROM data memory, Bank 1 R20 (128 bytes EEPROM address register) holds the address to be accessed. According to the operation, Bank 1 R21 (128 bytes EEPROM Data register) holds the data to be written, or the data read, at the address in Bank 1 R20.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0

Bits 6~0 (EERA7~EERA0): EEPROM address register

6.9.1.3 Bank 1 R21 (128 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0

Bits 7~0 (EERD7~EERD0): EEPROM data register. Read only.

6.9.1.4 Programming Steps/Example Demonstration

The following are the steps to write or read data from the EEPROM:

1) Set the **EEPC** bit of Bank1 R1F to 1 for enable EEPROM power.

2) Write the address to EERA8~EERA0 (512 bytes EEPROM address).

3) a.1. Set the **EEWE** bit to 1, if the write function is employed.

   a.2. Write the 8-bit data value to be programmed in Bank 1 R21 (128 bytes EEPROM data)

   a.3. Set the **WR** bit to 1, then execute the write function

   b. Set the **RD** bit to 1, then execute the read function.

4) a. Wait for the **EEDF** or **WR** to be cleared

   b. Wait for the **EEDF** to be cleared

5) For the next conversion, go to Step 2 as required.

6) If it is desired to conserve power, make sure the EEPROM data is not used, and clear the **EEPC**.

6.10 Oscillator

6.10.1 Oscillator Modes

The EM78F665N can be operated in Internal RC oscillator mode.

Table 5 Oscillator Modes as defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
-	0	0	0
-	0	0	1
-	0	1	0
-	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
-	1	1	0
-	1	1	1

6.10.2 Internal RC Oscillator Mode

The EM78F665N offer a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (16 MHz and 8 MHz) that can be set by Code Option: RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option Bits: C4~C0. Table 7 describes a typical instance of the calibration.

Table 6 Internal RC Drift Rate (Ta=25°C, VDD=5 V± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40℃+85℃)	Voltage (2.2V~5.5V)	Process	Total
4 MHz	±2%	±2%	±2%	±6%
8 MHz	±2%	±2%	±2%	±6%
16 MHz	±2%	±2%	±2%	±6%

Table 7 Calibration Selections for Internal RC Mode

Trimming code					CLK Period	Frequency
C4	C3	C2	C1	C0		
1	1	1	1	1	Period* (1+32%)	F* (1-24.2%)
1	1	1	1	0	Period* (1+30%)	F* (1-23.1%)
1	1	1	0	1	Period* (1+28%)	F* (1-21.9%)
1	1	1	0	0	Period* (1+26%)	F* (1-20.6%)
1	1	0	1	1	Period* (1+24%)	F* (1-19.4%)
1	1	0	1	0	Period* (1+22%)	F* (1-18%)
1	1	0	0	1	Period* (1+20%)	F* (1-16.7%)
1	1	0	0	0	Period* (1+18%)	F* (1-15.3%)
1	0	1	1	1	Period* (1+16%)	F* (1-13.8%)
1	0	1	1	0	Period* (1+14%)	F* (1-12.3%)
1	0	1	0	1	Period* (1+12%)	F* (1-10.7%)
1	0	1	0	0	Period* (1+10%)	F* (1-9.1%)
1	0	0	1	1	Period* (1+8%)	F* (1-7.4%)
1	0	0	1	0	Period* (1+6%)	F* (1-5.7%)
1	0	0	0	1	Period* (1+4%)	F* (1-3.8%)
1	0	0	0	0	Period* (1+2%)	F* (1-2%)
0	0	0	0	0	Period (default)	F (default)
0	0	0	0	1	Period* (1-2%)	F* (1+2%)
0	0	0	1	0	Period* (1-4%)	F* (1+4.2%)
0	0	0	1	1	Period* (1-6%)	F* (1+6.4%)
0	0	1	0	0	Period* (1-8%)	F* (1+8.7%)
0	0	1	0	1	Period* (1-10%)	F* (1+11.1%)
0	0	1	1	0	Period* (1-12%)	F* (1+13.6%)
0	0	1	1	1	Period* (1-14%)	F* (1+16.3%)
0	1	0	0	0	Period* (1-16%)	F* (1+19%)
0	1	0	0	1	Period* (1-18%)	F* (1+22%)
0	1	0	1	0	Period* (1-20%)	F* (1+25%)
0	1	0	1	1	Period* (1-22%)	F* (1+28.2%)
0	1	1	0	0	Period* (1-24%)	F* (1+31.6%)
0	1	1	0	1	Period* (1-26%)	F* (1+35.1%)
0	1	1	1	0	Period* (1-28%)	F* (1+38.9%)
0	1	1	1	1	Period* (1-30%)	F* (1+42.9%)

* *1. These are theoretical values and for reference only. Actual values depend on the process.*
2. Similar way of calculation is also applicable for low frequency mode.

6.11 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply remains at its steady state. The EM78F665N is equipped with Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd is rising quick enough (50 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.12 External Power-on Reset Circuit

The circuit shown in Figure 6-23 implements an external RC that can produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is ± 5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. The current-limited resistor, Rin, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

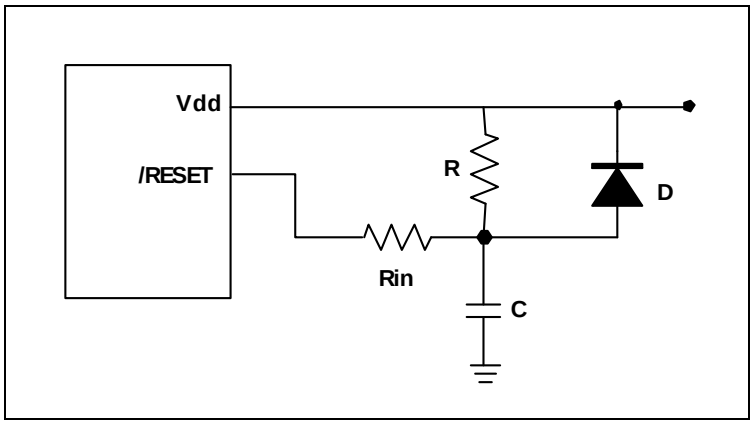


Figure 6-23 External Power-up Reset Circuit

6.13 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power on reset. Figure 6-24 and Figure 6-25 show how to build a residue-voltage protection circuit.

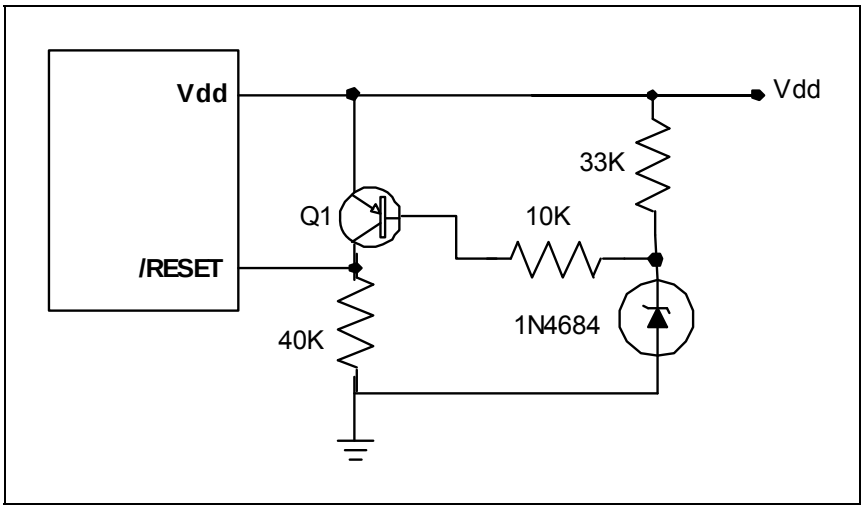


Figure 6-24 Residue Voltage Protection Circuit 1

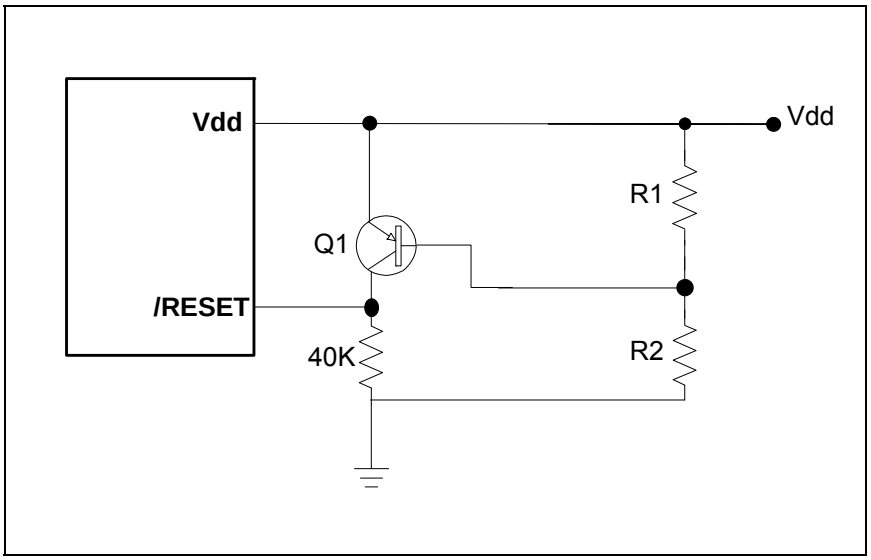


Figure 6-25 Residue Voltage Protection Circuit 2

6.14 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Change one instruction cycle to consist of 4 oscillator periods.

(B) "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the CODE Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the 4 oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc/ 2 as indicated in Fig. 5.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

Convention:

R *= Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b *= Bit field designator that selects the value for the bit located in the register* ***R*** *and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
000 0000 0000 0000	0000	NOP	No Operation	None
000 0000 0000 0001	0001	DAA	Decimal Adjust A	C
000 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
000 0000 0000 0100	0004	WDTC	0 → WDT	T, P
000 0000 0001 0000	0010	ENI	Enable Interrupt	None
000 0000 0001 0001	0011	DISI	Disable Interrupt	None
000 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
000 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
000 0001 rrrr rrrr	01rr	MOV R,A	A → R	None
000 0010 0000 0000	0200	CLRA	0 → A	Z
000 0011 rrrr rrrr	03rr	CLR R	0 → R	Z
000 0100 rrrr rrrr	04rr	SUB A,R	R-A → A	Z, C, DC
000 0101 rrrr rrrr	05rr	SUB R,A	R-A → R	Z, C, DC
000 0110 rrrr rrrr	06rr	DECA R	R-1 → A	Z
000 0111 rrrr rrrr	07rr	DEC R	R-1 → R	Z
000 1000 rrrr rrrr	08rr	OR A,R	A ∨ R → A	Z
000 1001 rrrr rrrr	09rr	OR R,A	A ∨ R → R	Z
000 1010 rrrr rrrr	0Arr	AND A,R	A & R → A	Z
000 1011 rrrr rrrr	0Brr	AND R,A	A & R → R	Z
000 1100 rrrr rrrr	0Crr	XOR A,R	A ⊕ R → A	Z

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
000 1101 rrrr rrrr	0Drr	XOR R,A	A ⊕ R → R	Z
000 1110 rrrr rrrr	0Err	ADD A,R	A + R → A	Z, C, DC
000 1111 rrrr rrrr	0Frr	ADD R,A	A + R → R	Z, C, DC
001 0000 rrrr rrrr	10rr	MOV A,R	R → A	Z
001 0001 rrrr rrrr	11rr	MOV R,R	R → R	Z
001 0010 rrrr rrrr	12rr	COMA R	/R → A	Z
001 0011 rrrr rrrr	13rr	COM R	/R → R	Z
001 0100 rrrr rrrr	14rr	INCA R	R+1 → A	Z
001 0101 rrrr rrrr	15rr	INC R	R+1 → R	Z
001 0110 rrrr rrrr	16rr	DJZA R	R-1 → A, skip if zero	None
001 0111 rrrr rrrr	17rr	DJZ R	R-1 → R, skip if zero	None
001 1000 rrrr rrrr	18rr	RRCA R	R(n) → A(n-1),R(0) → C, C → A(7)	C
001 1001 rrrr rrrr	19rr	RRC R	R(n) → R(n-1),R(0) → C, C → R(7)	C
001 1010 rrrr rrrr	1Arr	RLCA R	R(n) → A(n+1),R(7) → C, C → A(0)	C
001 1011 rrrr rrrr	1Brr	RLC R	R(n) → R(n+1),R(7) → C, C → R(0)	C
001 1100 rrrr rrrr	1Crr	SWAPA R	R(0-3) → A(4-7),R(4-7) → A(0-3)	None
001 1101 rrrr rrrr	1Drr	SWAP R	R(0-3) ↔ R(4-7)	None
001 1110 rrrr rrrr	1Err	JZA R	R+1 → A, skip if zero	None
001 1111 rrrr rrrr	1Frr	JZ R	R+1 → R, skip if zero	None
010 0bbb rrrr rrrr	2xrr	BC R,b	0 → R(b)	None <Note2>
010 1bbb rrrr rrrr	2xrr	BS R,b	1 → R(b)	None <Note3>
011 0bbb rrrr rrrr	3xrr	JBC R,b	if R(b)=0, skip	None
011 1bbb rrrr rrrr	3xrr	JBS R,b	if R(b)=1, skip	None
100 kkkk kkkk kkkk	4kkk	CALL k	PC+1 → [SP],(Page, k) → PC	None

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
101 kkkk kkkk kkkk	5kkk	JMP k	(Page, k) → PC	None
110 0000 kkkk kkkk	60kk	MOV A,k	k → A	None
110 0100 kkkk kkkk	64kk	OR A,k	A ∨ k → A	Z
110 1000 kkkk kkkk	68kk	AND A,k	A & k → A	Z
110 1100 kkkk kkkk	6Ckk	XOR A,k	A ⊕ k → A	Z
111 0000 kkkk kkkk	70kk	RETL k	k → A,[Top of Stack] → PC	None
111 0100 kkkk kkkk	74kk	SUB A,k	k-A → A	Z, C, DC
111 1100 kkkk kkkk	7Ckk	ADD A,k	k+A → A	Z, C, DC
111 1010 0000 kkkk	7A0k	SBANK k	K->R1(4)	None
111 1010 0100 kkkk	7A4k	GBANK k	K->R1(0)	None
111 1010 1000 kkkk kkk kkkk kkkk kkkk	7A8k kkkk	LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC	None
111 1010 1100 kkkk kkk kkkk kkkk kkkk	7ACk kkkk	LJMP k	Next instruction : k kkkk kkkk kkkk K→PC	None
111 1011 rrrr rrrr	7Brr	TBRD R	ROM[(TABPTR)] → R	None

6.15 Code Option Register

6.15.1 Code Option Register (Word 0)

Code Option from SRAM/ROM/OTP/Flash

Word 0											
Bit	**Bit 14**	**Bits 13~12**	**Bit 11**	**Bits 10~9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bits 2~0**
Mne-monic	COBS0	-	CLKS0	-	LVR1	LVR0	RESETEN	ENWDT	NRHL	NRE	Protect
1	register	-	2 clocks	-	High	High	/RESET	Enable	8/fc	Disable	Enable
0	option	-	4 clocks	-	Low	Low	P83	Disable	32/fc	Enable	Disable

Bit 14 (COBS0): IRC mode select bit

0: IRC frequency selection from code option

1: IRC frequency selection from register

Bit 13: Unused bit, set to "**1**" at all times

Bit 12: Unused bit, set to "**0**" at all times

Bits 11 (CLKS0): Instruction period option bits

Instruction Period	CLKS0
4 clocks	0
2 clocks	1

Bit 10: Unused bit, set to 1 at all times

Bit 9: Unused bit, set to 0 at all times.

Bits 8~7 (LVR1~LVR0): Low voltage reset enable bit.

LVR1, LVR0	VDD Reset Level	VDD Release Level
00	NA	NA
01	2.7V	2.9V
10	3.7V	3.9V
11	4.2V	4.4V

Bit 6 (RESETEN): P83//RESET pin selection bit

1: /RESET pin

0: P83 pin

Bit 5 (ENWDT): WDT enable bit

1: Enable

0: Disable

Bit 4 (NRHL): noise rejection high/low pulse define bit.

0: pulses equal to 32/fc [s] is regarded as signal

1: pulses equal to 8/fc [s] is regarded as signal

Bit 3 (NRE): Noise Rejection Enable bit

0: Enable Noise Rejection

1: Disable Noise Rejection

Bits 2~0 (PR2~PR0): Protect Bits

6.15.2 Code Option Register (Word 1)

Word 1															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit9**	**Bit8**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit 0**
Mnemonic	HLFS	-	SHE	C4	C3	C2	C1	C0	RCM1	RCM0	-	OSC2	OSC1	OSC0	RCOD
1	Green	-	Enable	High	High	High	High	High	High	High	-	High	High	High	Open drain
0	Normal	-	Disable	Low	Low	Low	Low	Low	Low	Low	-	Low	Low	Low	System clock

Bit 14 (HLFS): Initialized CPU mode

0: Normal mode

1: Green mode

Bit 13: Unused bit, set to "**1**" at all times

Bit 12 (SHE): System Halt Enable bit.

0: disable

1: enable

Bits 11~7 (C4~C0): IRC trim bits. This part will be auto set by writer.

Bits 6~5 (RCM1~RCM0): IRC frequency selection.

RCM1:RCM0	Frequency
00	4 MHz
01	16 MHz
10	8 MHz
11	Reserved

Bit 4: Unused bit, set to 1 at all times.

Bits 3~1(OSC2~OSC0): Oscillator mode selection bits.

Mode	OSC2	OSC1	OSC0
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1

Bit 0 (RCOD): A selecting bit of Oscillator output or I/O port.

RCOUT	Pin Function
1	OSCO pin is open drain
0	OSCO output system clock (default)

6.15.3 Code Option Register (Word 2)

Word 2															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	SC3	SC2	SC1	SC0	-	-	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	High	High	High	High	-	-	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	-	-	Low	Low	Low	Low	Low	Low	Low	Low	Low

7 DC Electrical Characteristics

Ta=25°C, VDD=5.0V±5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	IRC: VDD to 5V	4 MHz, 16 MHz, 8 MHz	F-5%	F	F+5%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	+1	μA
IRC1	IRC: VDD to 5V	RCM0:RCM1=0:0	3.92	4	4.08	MHz
IRC2	IRC: VDD to 5V	RCM0:RCM1=1:0	7.84	8	8.16	MHz
IRC3	IRC: VDD to 5V	RCM0:RCM1=0:1	15.68	16	16.32	MHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	3.9	4	4.1	V
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	0.7Vdd	-	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	-0.3V	-	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.56Vdd	-	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	-	0.44Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT	0.7Vdd	-	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT	-0.3V	-	0.3Vdd	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD - 0.1VDD	-	-4.5	-	mA
IOH2	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD - 0.1VDD	-	-8	-	mA
IOL1	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = GND + 0.1VDD	-	18	-	mA
IOL2	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = GND + 0.1VDD	-	32	-	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-	-75	-	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	-	40	-	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	-	2.0	-	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	-	7	-	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (IRC type, CLKS="0"), Output pin floating, WDT enabled	-	1.6	-	mA

Note: *These parameters are theoretical values and have not been tested.*

*****Data in the Minimum, Typical, Maximum ("Min.", "Typ.", "Max.") columns are based on characterization results at 25°C. These data are for design reference only and have not been tested.*

Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.5~ 5.5V Temperature = -40°C ~ 85°C	–	6	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	1000K	–	cycles

Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	4	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

A/D Converter Characteristics (Vdd=2.5V to 5.5V, Vss=0V, Ta=25°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VAREF	Analog reference voltage	VAREF-VASS= 2.5V to 5.5V	2.5	-	Vdd	V
VASS	–	–	-	Vss	-	V
VAI	Analog input voltage	–	VASS	-	VAREF	V
IAI1	Ivdd	VAREF = Vdd	1150	1300	1450	μA
	Ivref	–	-10	0	10	μA
IAI2	Ivdd	VAREF = VREF	700	800	900	μA
	Ivref	–	450	500	550	μA
RN	Resolution	VAREF=Vdd	8	9	-	Bits
LN	Linearity error	VAREF=Vdd	0	± 2	+/-4	LSB
DNL	Differential nonlinear error	VAREF=Vdd	0	± 0.5	+/-0.9	LSB
FSE	Full scale error	VAREF=Vdd	± 0	± 1	± 2	LSB
OE	Offset error	VAREF=Vdd	± 0	± 1	± 2	LSB
ZAI	Recommended impedance of analog voltage source	VAREF=Vdd	0	8	10	KΩ
TAD1	A/D clock period	VAREF=Vdd=2.5~5.5V Ta= -40~85°C	4	-	-	μs
TAD2	A/D clock period	VAREF=Vdd=3~5.5V Ta= -40~85°C	1	-	-	μs
TCN	A/D conversion time	VAREF=Vdd	14	-	14	TAD
PSR	Power supply rejection	Vdd=Vdd-10% to Vdd+10%	± 0	-	± 2	LSB

Note: 1. *The parameters are characterized but not tested.*
2. *These parameters are for design guidance only and are not tested.*
3. *It will not consume any current other than minor leakage current, when A/D is off.*
4. *The A/D conversion result never decreases with an increase in the input voltage, and has no missing code.*
5. *Specifications subject to change without notice.*

8 AC Electrical Characteristics

EM78F665N, 0≦Ta≦70°C, VDD=5V, VSS=0V

-40 ≦ Ta ≦ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS1:0="01")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	1000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload = 20 pF	–	50	–	ns

Note: *These parameters are theoretical values and have not been tested. Such parameters are for design reference only.*

Data in the Minimum, Typical, Maximum ("Min.", "Typ.", "Max.") columns are based on characterization results at 25°C.

*****N = selected prescaler ratio.*

APPENDIX

A Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F665NK28J/S	Skinny DIP	28	300 mil
EM78F665NSO28J/S	SOP	28	300 mil
EM78F665NQ32J/S	QFN	32	5 mm × 5 mm

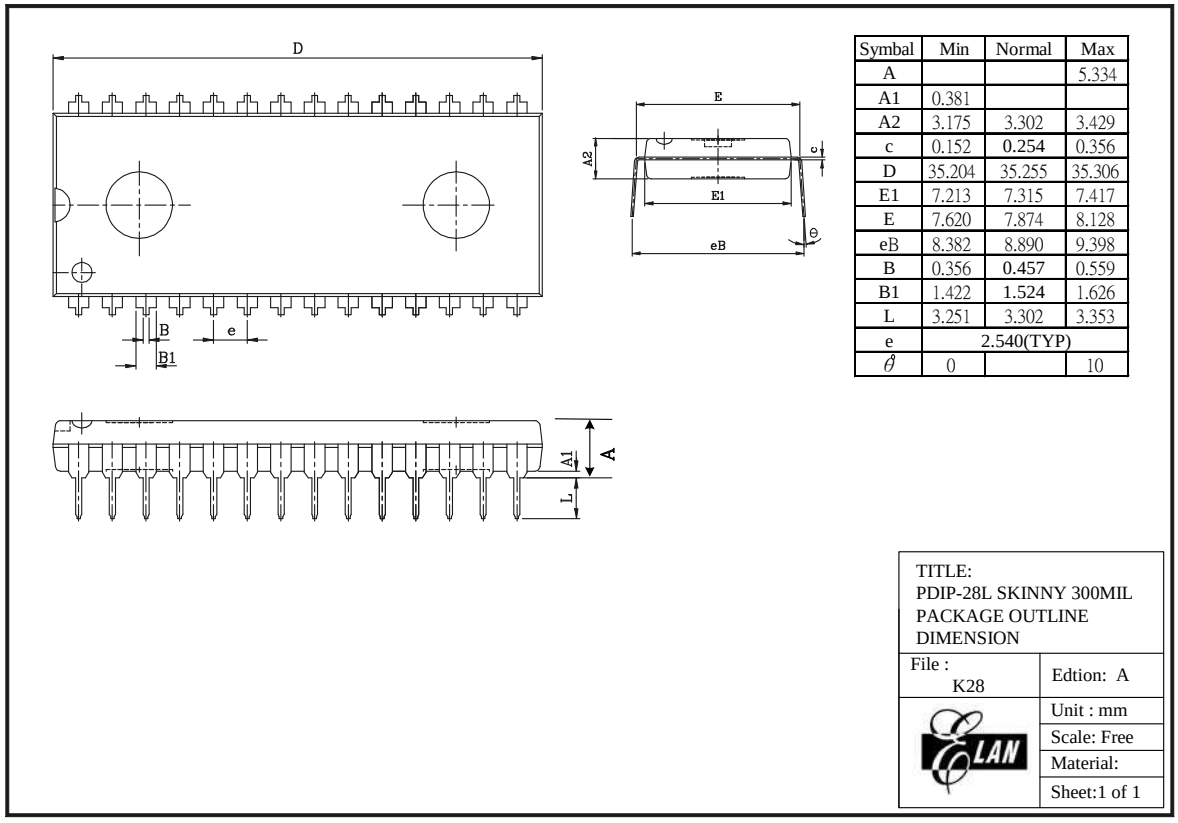
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb contents less is than 100ppm and complies with Sony specifications

Part No.	EM78F665NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Packaging Configuration

B.1 EM78F665NK28



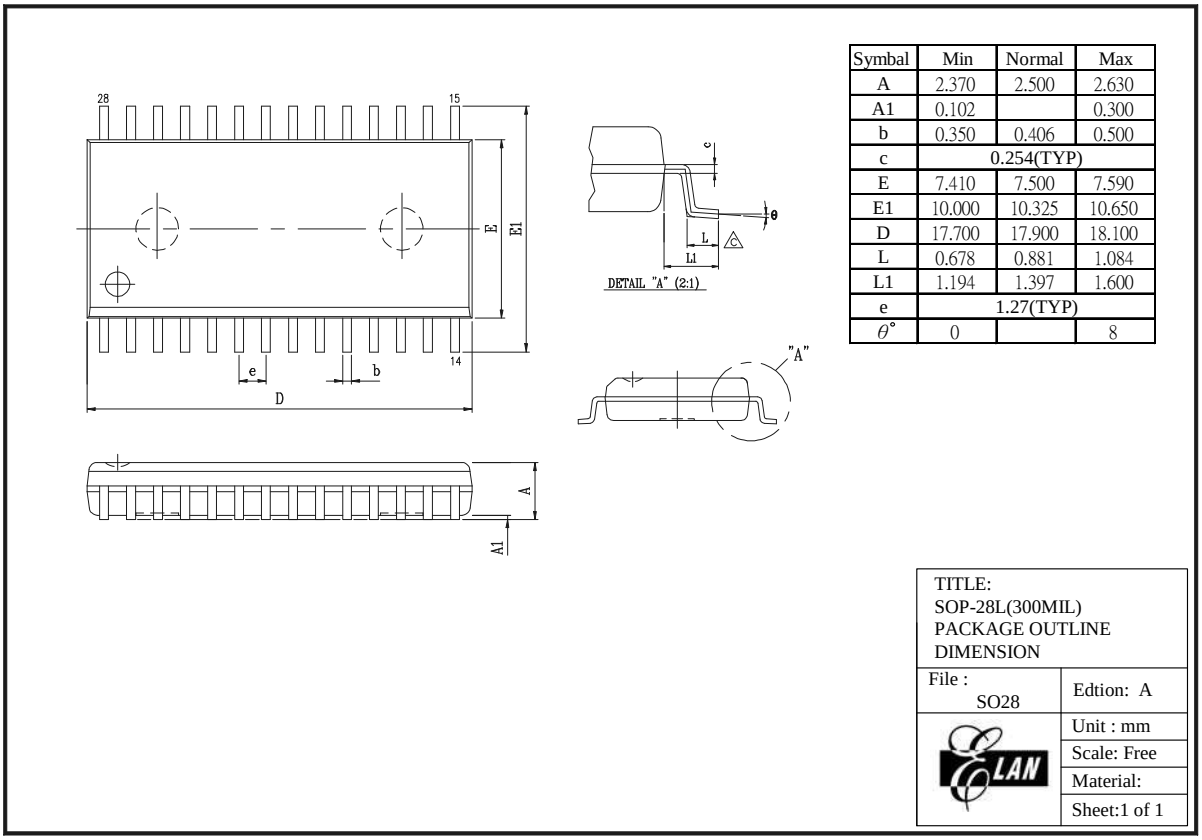
Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.152	**0.254**	0.356
D	35.204	35.255	35.306
E1	7.213	7.315	7.417
E	7.620	7.874	8.128
eB	8.382	8.890	9.398
B	0.356	**0.457**	0.559
B1	1.422	**1.524**	1.626
L	3.251	3.302	3.353
e	2.540(TYP)		
θ	0		10

TITLE:
PDIP-28L SKINNY 300MIL
PACKAGE OUTLINE
DIMENSION

File : K28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78F665N 28-pin Skinny DIP Package Type

B.2 EM78F665NSO28

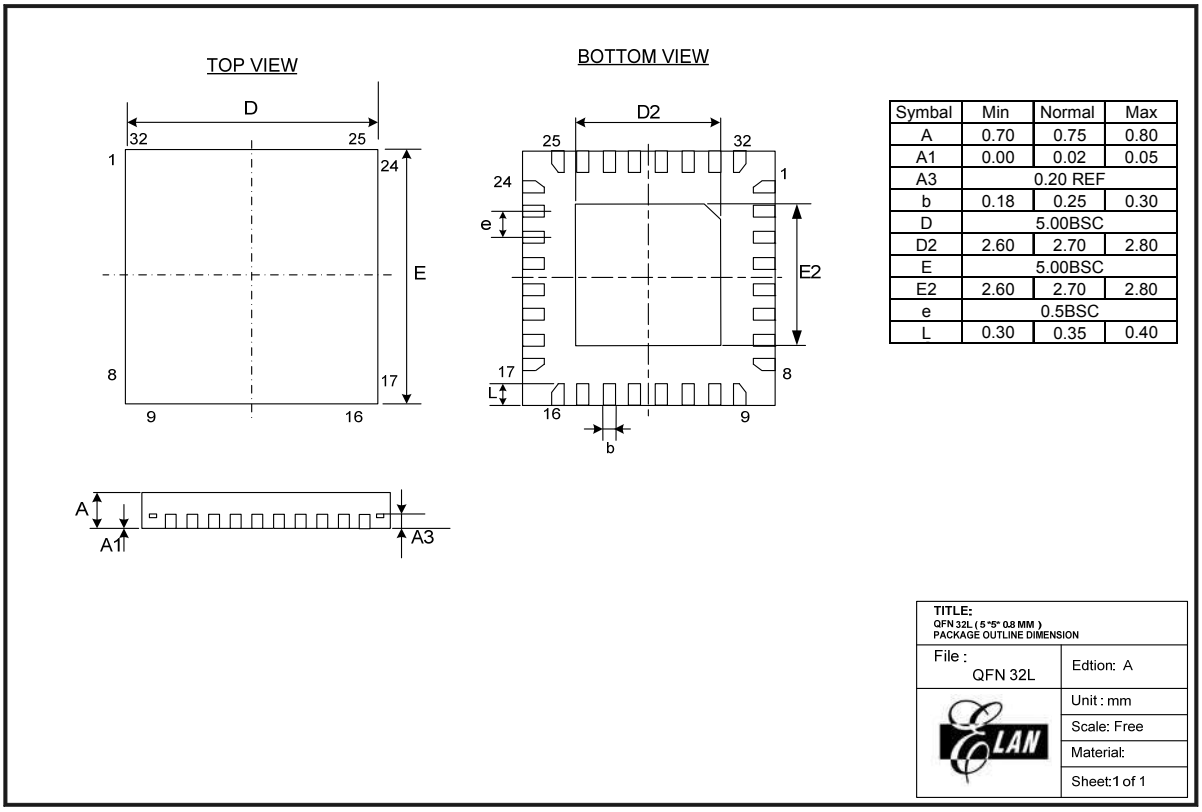


Symbal	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c	0.254(TYP)		
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-28L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-2 EM78F665N 28-pin SOP Package Type

B.3 EM78F665NQN32



Symbal	Min	Normal	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		5.00BSC	
D2	2.60	2.70	2.80
E		5.00BSC	
E2	2.60	2.70	2.80
e		0.5BSC	
L	0.30	0.35	0.40

Figure B-3 EM78F665N 32-pin QFN Package Type

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance) = 24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance) = 192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ---- 225 ± 5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ---- 240 ± 5°C)	
Temperature cycle test	-65°C (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure = 2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA = 85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA = 150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA = 125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA = 25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥ | ± 4KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ | ± 400V |	

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.