EM78F562N/F662N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial release version	2010/04/29
1.1	1. Modified the ICC1 and ICC2 current 2. Deleted the QFN16 package of EM78F562N. 3. Modified the EM78F662NQN16 to EM78F662NQN16A. 4. Fixed the Code Option Word 2 Bit 7 to “1”	2012/06/29
1.2	1. Added LVR characteristics in the DC Electrical Characteristics section. 2. Added SSOP package for EM78F662N.	2013/05/29

1 General Description

The EM78F562N/F662N devices are 8-bit microprocessors designed and developed with low-power, high-speed CMOS technology and high noise immunity. They have an on-chip 2K×13-bit Electrical Flash Memory and EM78F662N has 128×8-bit in system programmable EEPROM. It provides three protection bits to prevent intrusion of user's Flash memory code. Twelve Code option bits are also available to meet user's requirements.

With its enhanced Flash-ROM features, the EM78F562N/F662N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantage of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 2K×13 bits Flash memory
  - 144×8 bits on chip registers (SRAM)
  - 128 bytes in-system programmable EEPROM(Only for EM78F662N)
    *Endurance: 100,000 write/erase cycles
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - Less than 2 mA at 5V/4 MHz
  - Typically 20 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - Three bidirectional I/O ports
  - Wake-up port : P6
  - High sink port : P6
  - 12 Programmable pull-down I/O pins
  - Eight programmable pull-high I/O pins
  - Four programmable open-drain I/O pins
  - External interrupt : P60
- Operating voltage range:
  - Industrial: 2.4V~5.5V at -40℃ ~85℃
  - Commercial: 2.2V~5.5V ay 0℃ ~70℃
- Operating frequency range (base on two clocks):
  - Crystal mode:
    DC ~ 20 MHz @ 5V
    DC ~ 8 MHz @ 3V
    DC ~ 4 MHz @ 2.2V
  - ERC mode:
    DC ~ 20 MHz @ 5V
    DC ~ 8 MHz @ 3V
    DC ~ 4 MHz @ 2.2V
  - IRC Drift Rate (Ta=25℃, VDD=5V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40℃+85℃)	Voltage (2.2V~5.5V)	Process	Total
1 MHz	±3%	±4%	±2.5%	±9.5%
4 MHz	±3%	±4%	±2.5%	±9.5%
8 MHz	±3%	±5%	±2.5%	±10.5%
16 MHz	±3%	±5%	±2.5%	±10.5%

- One 16-bit Timer/Counter
  - TC2 : Timer/Counter/Window
- One 8-bit Timer/Counter
  - TC3 : Timer/Counter/PDO (Programmable Divider Output) / PWM (pulse width modulation)
- Comparator (CMP)
- Seven available interrupts:
  - Internal interrupt: 4
  - External interrupt: 3
- 8 channels Analog-to-Digital Converter with 10-bit resolution
- Peripheral configuration
  - 8-bit real timer clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Power down (Sleep) mode
  - Four programmable Level Voltage Reset (LVR)
    LVR : 4.0V, 3.5V, 2.7V, and POR
  - Three security registers to prevent intrusion of Flash memory codes
  - One configuration register to accommodate user's requirements
  - 2-/4-/8-/16 clocks per instruction cycle selected by code option
  - High EFT immunity
  - Two sub-frequency,128kHz and 16kHz, the 16kHz is provided by dividing 128kHz
- Single instruction cycle commands
- Four Crystal range in Oscillator Mode

Crystal Range	Oscillator Mode
20 MHz ~ 6 MHz	HXT
6 MHz ~ 1 MHz	XT
1 MHz ~ 100kHz	LXT1
32.768kHz	LXT2

- Programmable free running watchdog timer
- Package Type:
  - 16-pin DIP 300mil : EM78F562N/F662ND16
  - 16-pin SOP 300mil : EM78F562N/F662NSO16
  - 16-pin QFN 4x4mm : EM78F662NQN16A
  - 16-pin SSOP 150 mil: EM78F662NSS16
  - 18-pin DIP 300mil : EM78F562N/F662ND18
  - 18-pin SOP 300mil : EM78F562N/F662NSO18
  - 20-pin DIP 300 mil : EM78F562N/F662ND20
  - 20-pin SOP 300mil : EM78F562N/F662NSO20

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Assignment

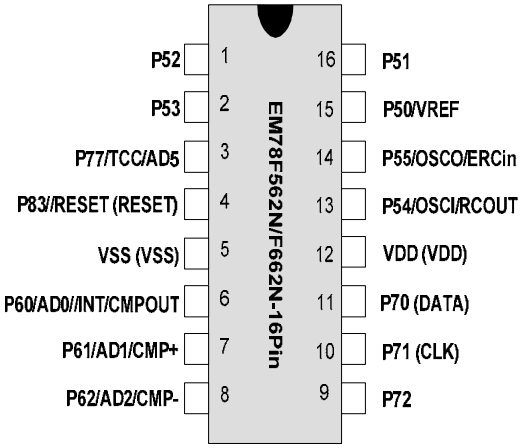

Figure 3-1 EM78F562N/F662ND16/SO16

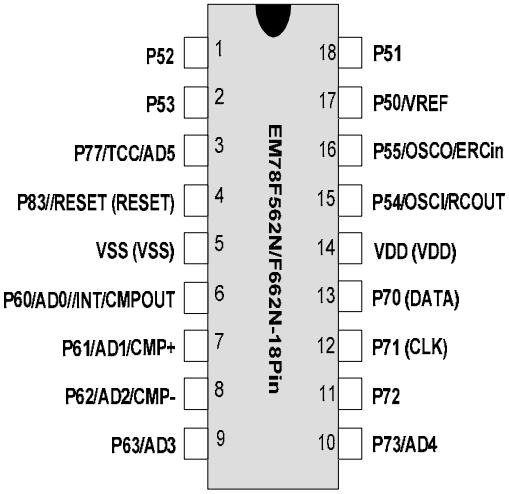

Figure 3-2 EM78F562/F662ND18/SO18

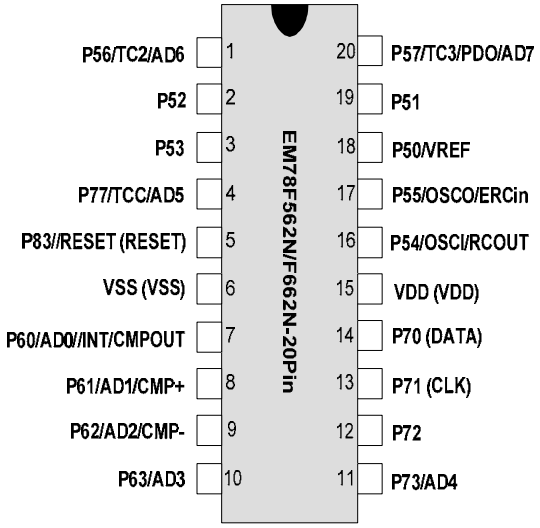

Figure 3-3 EM78F562/F662ND20/SO20

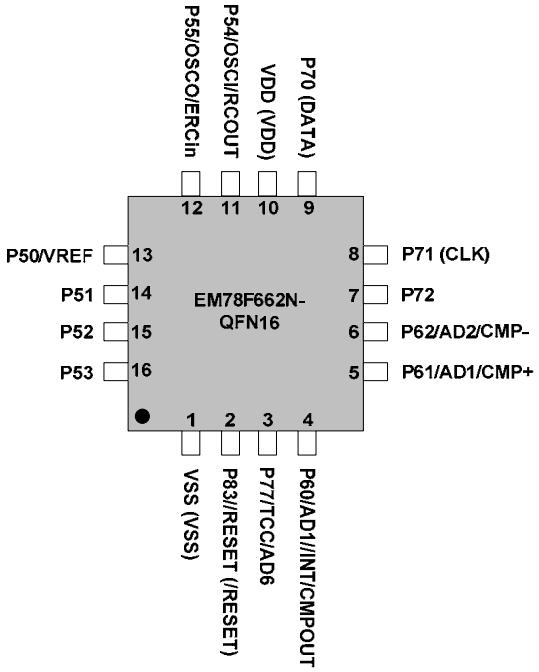

Figure 3-4 EM78F662NQN16A

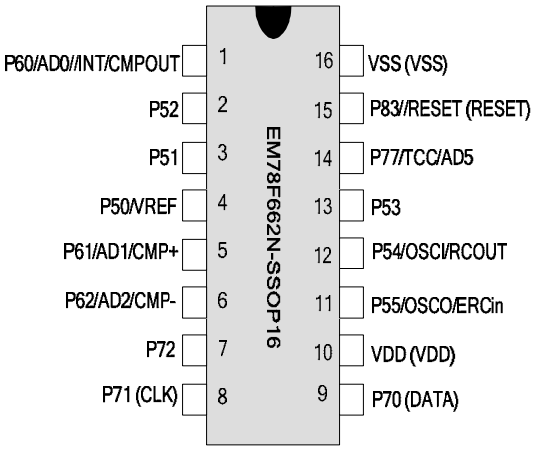

Figure 3-5 EM78F662NSS16

4 Pin Description

4.1 EM78F562N/F662N

Legend: ***ST:*** *Schmitt Trigger input* ***AN:*** *analog pin*
CMOS: *CMOS output* ***XTAL:*** *Oscillation pin for crystal / resonator*

Name	Function	Input Type	Output Type	Description
P50/VREF	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down
	VREF	AN	–	ADC external voltage reference
P51	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down
P52	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down
P53	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL	–	Clock input of crystal/resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin
	OSCO	–	XTAL	Clock output of crystal/resonator oscillator
	ERCin	AN	–	External RC input pin
P56/TC2/AD6	P56	ST	CMOS	Bidirectional I/O pin
	TC2	ST	–	Timer 2 clock input
	AD6	AN	–	ADC Input 6
P57/TC3/PDO/AD7	P57	ST	CMOS	Bidirectional I/O pin
	TC3	ST	–	Timer 3 clock input
	PDO	–	CMOS	Programmable divider output
	AD7	AN	–	ADC Input 7
P60/AD0//INT/CMPOUT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD0	AN	–	ADC Input 0
	/INT	ST	–	External interrupt pin
	CMPOUT	–	CMOS	Comparator output
P61/AD1/CMP+	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD1	AN	–	ADC Input 1
	CMP+	AN	–	Non-inverting end of comparator

(Continuation)

Name	Function	Input Type	Output Type	Description
P62/AD2/CMP-	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD2	AN	–	ADC Input 2
	CMP-	AN	–	Inverting end of comparator
P63/AD3	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD3	AN	–	ADC Input 3
P70	P70	ST	CMOS	Bidirectional I/O pin
(DATA)	**(DATA)**	ST	CMOS	DATA pin for Writer programming
P71	P71	ST	CMOS	Bidirectional I/O pin
(CLK)	**(CLK)**	ST	–	CLOCK pin for Writer programming
P72	P72	ST	CMOS	Bidirectional I/O pin
P73/AD4	P73	ST	CMOS	Bidirectional I/O pin
	AD4	AN	–	ADC Input 4
P77/TCC/AD5	P77	ST	CMOS	Bidirectional I/O pin
	TCC	ST	–	Real Time Clock/Counter clock input
	AD5	AN	–	ADC Input 5
P83//RESET	P83	ST	CMOS	Bidirectional I/O pin
	/RESET	ST	–	Internal pull-high reset pin
(/RESET)	**(/RESET)**	ST	–	/RESET pin for Writer programming
VDD	VDD	Power	–	Power
(VDD)	VDD	Power	–	VDD for Writer programming
VSS	VSS	Power	–	Ground
(VSS)	VSS	Power	–	VSS for Writer programming

5 Block Diagram

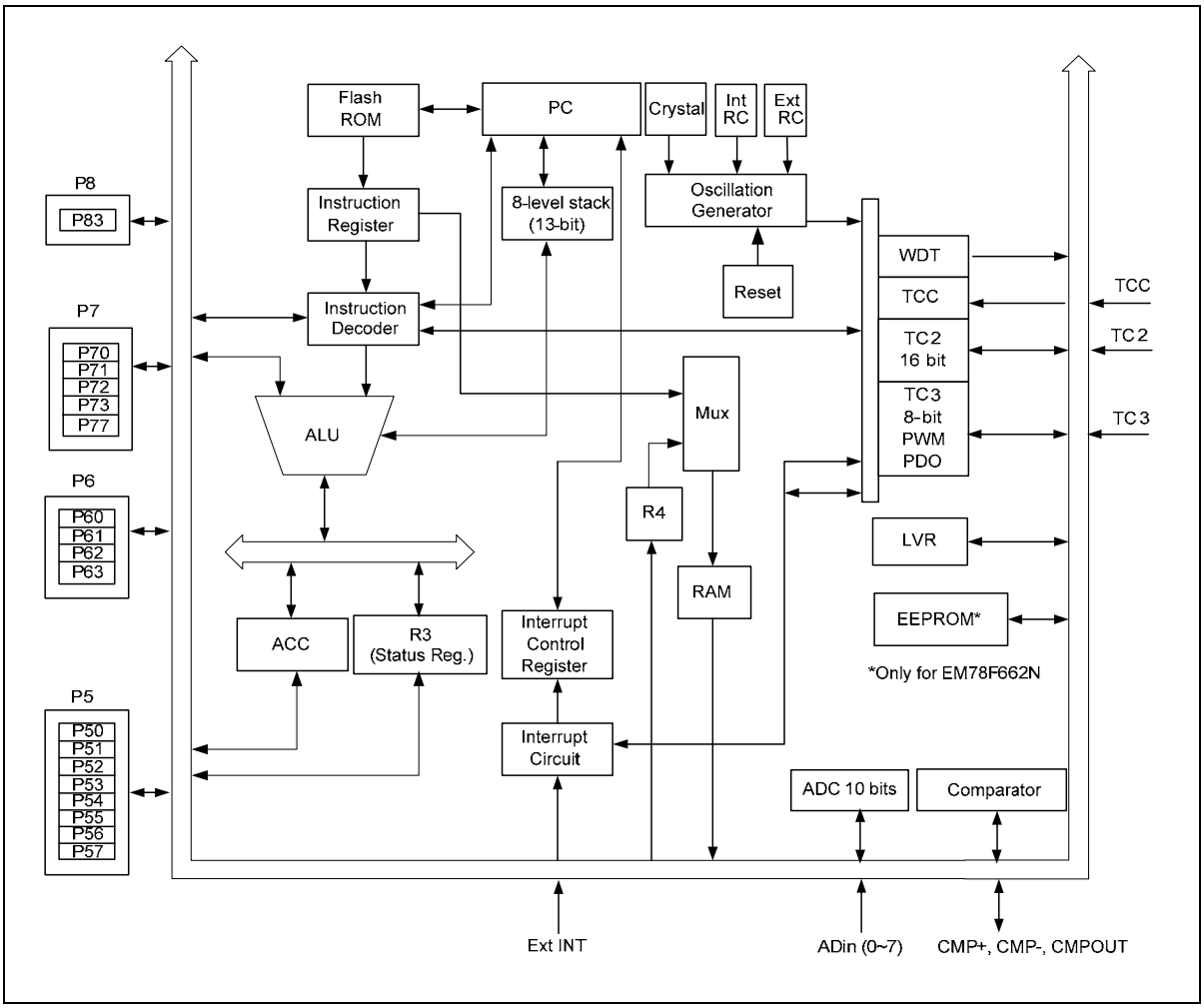

Figure 5-1 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

R1 is incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The contents of the prescaler counter are cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter) and Stack

Depending on the device type, R2 and hardware stack are **10**-bit wide. The structure is depicted in Figure 6-1.

The configuration structure generates **2K×13** bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is **1024** words long.

R2 is set as all “0”s when under a reset condition.

“JMP” instruction allows direct loading of the lower **10** program counter bits. Thus, “JMP” allows the PC to go to any location within a page (1K).

“CALL” instruction loads the lower 10 bits of the PC and PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.

“LJMP” instruction allows direct loading of the lower 11 program counter bits. Thus, “LJMP” allows the PC to go to any location within 2K.

“LCALL” instruction loads the lower 11 bits of the PC and PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 2K.

“RET” (“RETL k”, “RETI”) instruction loads the program counter with the contents of the top-level stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will be incremented progressively.

"MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC remain unchanged.

Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6") will cause the ninth bit and the tenth bits (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8 or fclk/16) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.

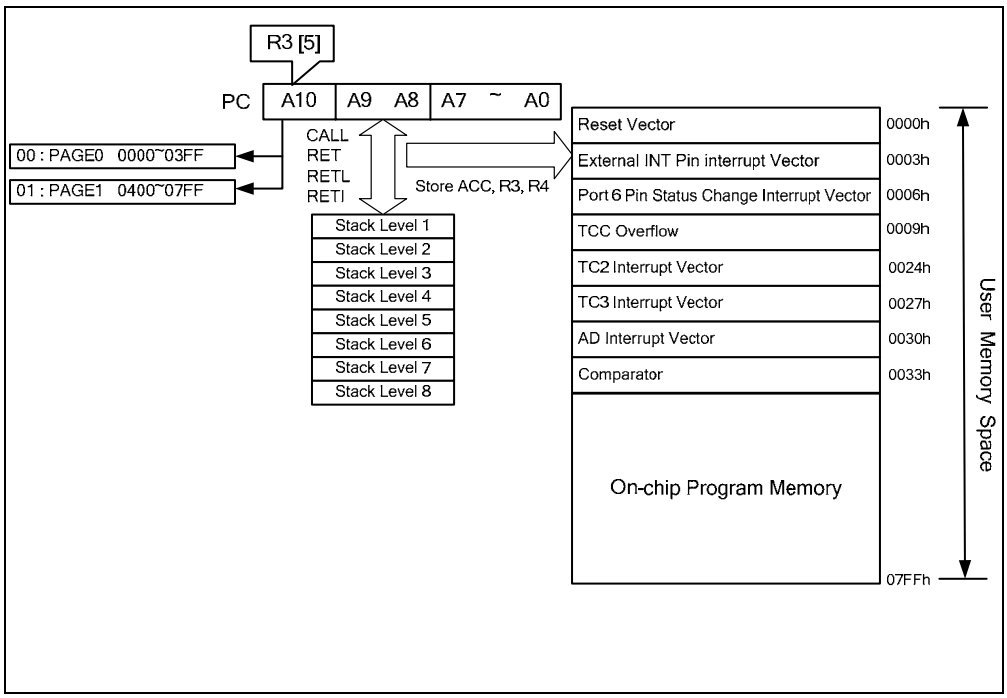

Figure 6-1 Program Counter Organization

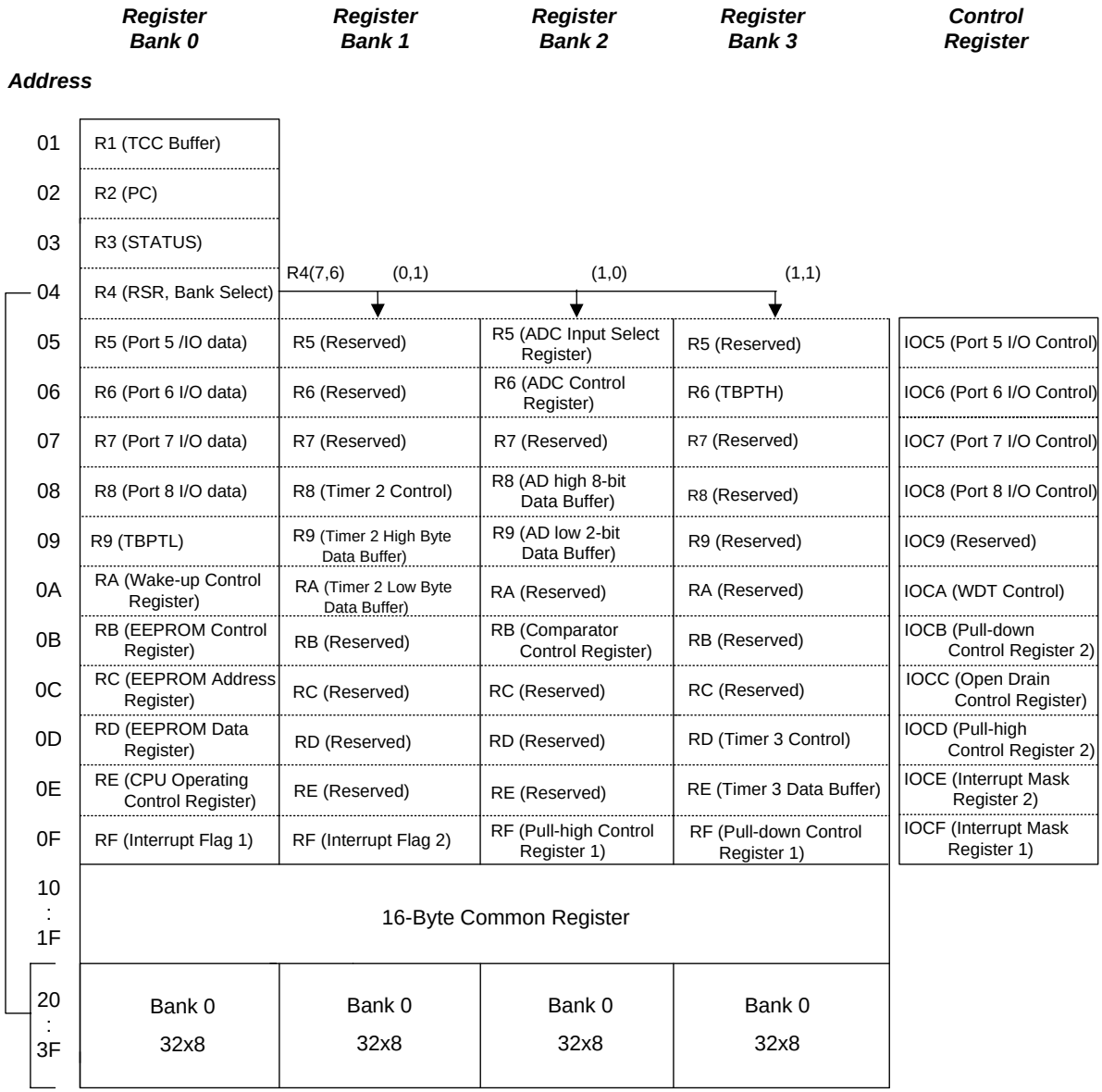

Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T	P	Z	DC	C

Bit 7 ~ Bit 5: Not used, set to "0" at all time.

Bit 4 (T): Time-out bit

Set to "1" with the "SLEP" and "WDTC" commands, or during power up and reset to "0" by WDT time-out.

Bit 3 (P): Power down bit

Set to "1" during power on or by a "WDTC" command and reset to "0" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

Bits 5 ~ 0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the *Data Memory Configuration* in Figure 6-2.

6.1.6 Bank 0 R5 ~ R8 (Port 5 ~ Port 8)

R5 ~ R7 are I/O registers.

6.1.7 Bank 0 R9 TBPTL (Low Byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

6.1.8 Bank 0 RA (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ICWE	ADWE	EXWE	-	-	CMPWE	-

Bit 7: Not used, set to "0" at all time.

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0 : Disable Port 6 input status change wake-up

1 : Enable Port 6 input status change wake-up

Bit 5 (ADWE): ADC wake-up enable bit

0 : Disable ADC wake-up

1 : Enable ADC wake-up

When ADC completed status is used to enter an interrupt vector or to wake-up the EM78F562N/F662N from sleep, with A/D conversion running, the ADWE bit must be set to "Enable".

Bit 4 (EXWE): External wake-up enable bit

0 : Disable External /INT pin wake-up

1 : Enable External /INT pin wake-up

Bit 2: Not used, set to "0" at all time

Bit 1 (CMPWE): Comparator wake-up enable bit

0 : Disable Comparator wake-up

1 : Enable Comparator wake-up

Bits 3, 0: Not used, set to "0" at all time

6.1.9 Bank 0 RB (EEPROM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0 : Does not execute EEPROM read

1 : Read EEPROM content, (RD can be set by software, and cleared by hardware after Read instruction is completed)

Bit 6 (WR): Write control register

0 : Write cycle to the EEPROM is complete.

1 : Initiate a write cycle, (WR can be set by software, WR is cleared by hardware after Write cycle is completed)

Bit 5 (EEWE): EEPROM Write Enable bit.

0 : Prohibit write to the EEPROM

1 : Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detective Flag

0 : Write cycle is completed

1 : Write cycle is unfinished

Bit 3 (EEPC): EEPROM power-down control bit

0 : Switch off the EEPROM

1 : EEPROM is operating

Bits 2 ~ 0: Not used, set to "0" at all time

***This register is only for EM78F662N.**

6.1.10 Bank 0 RC (128 Bytes EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 6 ~ 0: 128 bytes EEPROM address

****This register is only for EM78F662N.***

6.1.11 Bank 0 RD (128 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 128 bytes EEPROM data

****This register is only for EM78F662N.***

6.1.12 Bank 0 RE (CPU Operating Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE-	-	-	-	-

Bit 7: Not used, set to "0" at all time

Bit 6 (TIMERSC): TCC, TC2, TC3 clock source select

0 : Fs. Fs stands for the sub frequency for WDT internal RC time base.

1 : Fm. Fm stands for the main-oscillator clock

Bit 5 (CPUS): CPU Oscillator Source Select

0 : sub-oscillator (fs)

1 : main oscillator (fosc)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit. This bit will determine which mode to enter after SLEP instruction is executed.

0 : IDLE="0"+SLEP instruction → sleep mode

1 : IDLE="1"+SLEP instruction → idle mode

CPU Operation Mode

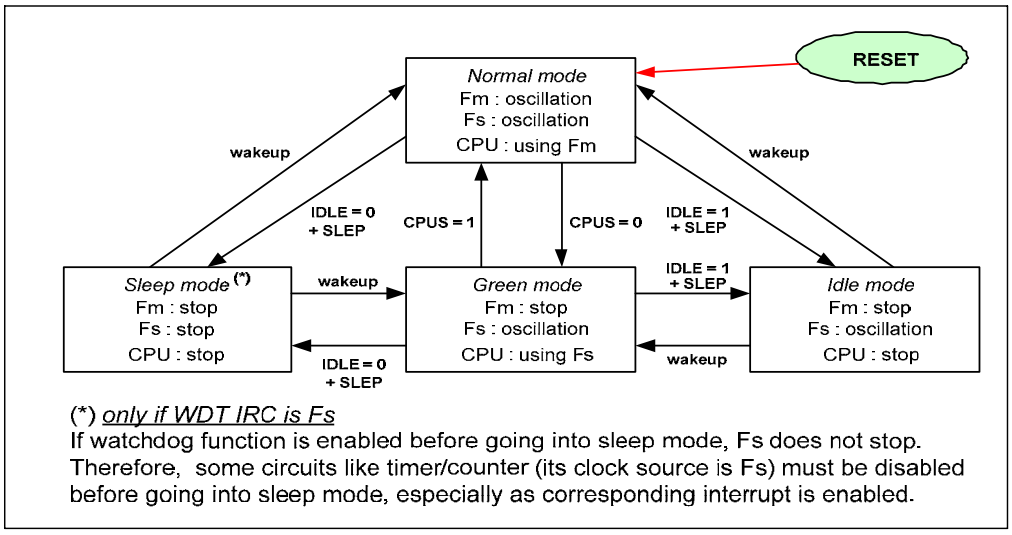

Figure 6-3 CPU Operation Mode

Bits 3 ~ 0: Not used, set to “0” at all time

6.1.13 Bank 0 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIF	ADIF	-	-	-	EXIF	ICIF	TCIF

***Note:* “ 1 ” means with interrupt request “ 0 ” means no interrupt occurs**

Bit 7 (CMPIF): Comparator Interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bits 5 ~ 3: Not used, set to “0” at all time.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, reset by software.

Bit 1 (ICIF): Port 6 Input Status Change Interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

Bank 0 RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

Note that the result of reading Bank 0 RF is the "Logic AND" of Bank 0 RF and IOCF.