Zywyn

ZD810

Universal High Brightness LED Driver

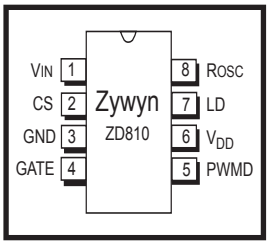
Features

- Low cost and high-efficiency LED driver
- Form and fit compatible with market solutions
- Open loop peak current controller
- Internal 8.0 to 450V linear regulator
- Constant frequency / constant off-time operation
- 0- 250 mV linear dimming
- 0 - 100% PWM dimming
- Requires few external components
- 8-Lead NSOIC Green Package

Applications

- AC/DC and DC/DC LED driver applications
- Lighting, recessed lighting, street lighting
- Signage and decorative lighting
- RGB backlighting, flat panel backlighting
- LED control powered by the Mains
- General purpose constant current source
- Chargers

Pin Configuration



8-Pin nSOIC

General Description

The ZD810 is a dimmable current-mode constant current LED driver IC. It drives an external MOSFET to accurately regulate the current in the LED string. The MOSFET can be sized for all types of LEDs including Power and HB LEDs beyond 1W. Its robust 450V rating makes it universally applicable to systems powered directly from Mains sources or from popular PFC sources. Its low voltage rating of 8V makes is suitable as well for low/medium voltage sources. The internal linear regulator generates 7.5V at the Vdd pin, which is also made available for external use, thus saving the cost of an external regulator.

Current dimming can be achieved through the 0 - 250mV linear dimming on Pin LD, or else by PWM methods on the PWMD pin with a duty cycle ratio of 0 - 100% and a frequency of up to a few kHz.

The ZD810 is ideally suited for buck topology based LED drivers. Since it operates in open loop current mode control, the controller achieves good output current regulation without the need for any loop compensation.

The ZD810 is an ideal and affordable driver for low cost LED string control solutions, requiring only three external components (apart from the power MOSFET).

Ordering Information

Part Number	Temperature Range	Package Type
ZD810LEN	–40°C to +85°C	8-Pin nSOIC
ZD810NEVB	n/a	For 8-Pin nSOIC

Please contact the factory for pricing and availabiliy on Tape-on-Reel option.

Typical Application

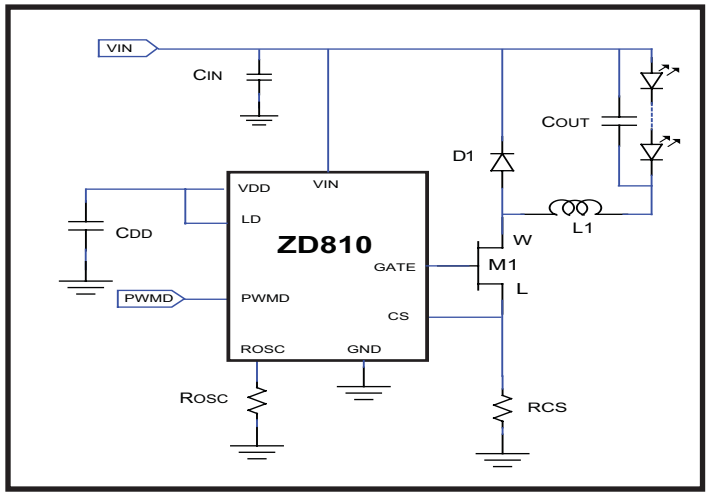


Figure 1. ZD810 Typical Application

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN} Voltage 480VDC
V_{DD} Voltage 12VDC
CS, LD, PWMD, GATE, R_{OSC} Voltage ..... VIN+0.7VDC

Extended Commercial
Operating Temperature ..... –40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... 300°C

Power Dissipation Per Package (T_A = 25°C)
8-pin nSOIC 630mW
Package Thermal Resistance
Θ_{JA} (8-PIN) ..... 128°C/W

Storage Considerations

Storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. Zywyn ships products in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH. The MSL of this product is 1 and has an unlimited amount of hours it can be stored outside of the bag.

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Electrical Characteristics

T_A = +25°C, V_{IN} = 12V unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
INPUT					
V_{IN}, Input DC supply voltage range *(1) (3)*	DC input voltage	8	-	450	V
I_{INSD}, Shut-down mode supply current *(3)*	Pin PWMD = GND	-	0.5	1.0	mA
INTERNAL REGULATOR					
V_{DD}, Internally regulated voltage	V_{IN} = 8V, I_{DD} = 0 *(2)*, 500pF @ Gate, R_{OSC} = 226kΩ, PWMD=V_{DD}	7.25	7.5	7.75	V
$\Delta V_{DD, LINE}$, Line regulation of V_{DD}	V_{IN} = 8V - 450V, I_{DD} = 0 *(2)*, 500pF @ Gate, R_{OSC} = 226kΩ, PWMD=V_{DD}	0	-	1	V
$\Delta V_{DD, Load}$, Load regulation of V_{DD}	I_{DD} = 0 ~ 1mA, 500pF @ Gate, R_{OSC} = 226kΩ, PWMD=V_{DD}	0	-	100	mV
UVLO, V_{DD} undervoltage lockout threshold *(3)*	V_{DD} Rising	6.45	6.7	6.95	V
ΔUVLO, V_{DD} undervoltage lock-out hysteresis	V_{DD} Falling	-	500	-	mV
$I_{IN, MAX}$, Current that the regulator can supply before IC goes into UVLO *(4)*	V_{IN} = 8V	5	-	-	mA
PWM DIMMING					
$V_{EN(LOW)}$, Pin PWMD input low voltage *(3)*	V_{IN} = 8 - 450V	-	-	0.8	V
$V_{EN(HIGH)}$, Pin PWMD input high voltage *(3)*	V_{IN} = 8 - 450V	2	-	-	V
R_{EN} , Pin PWMD pull-down resistance at PWMD	V_{PWMD} = 5V	50	100	150	kΩ
CURRENT SENSE COMPARATOR					
$V_{CS,TH}$, Current sense pull-in threshold voltage	-40°C < T_A < +85°C	225	250	275	mV
	T_A < +125°C	213	250	287	mV
V_{OFFSET} , Offset voltage for LD comparator *(3)*		-12	-	12	mV
t_{BLANK} , current sense blanking interval *(3)*	V_{LD} = V_{DD}, V_{CS}=$V_{CS,TH}$ +50mV after t_{BLANK}	150	215	280	ns
t_{DELAY} , Delay to output	V_{LD} = V_{DD}, V_{CS}=$V_{CS,TH}$ +50mV after t_{BLANK}	-	80	150	ns
OSCILLATOR					
f_{OSC} , oscillator frequency	R_{OSC} = 1MΩ	20	25	35	kHz
	R_{OSC} = 226KΩ	80	100	120	kHz
GATE DRIVER					
I_{SOURCE} , Gate sourcing current	V_{GATE}=0V, V_{DD}=7.5V	165	-	-	mA
I_{SINK} , Gate sinking current	V_{GATE}=V_{DD}, V_{DD}=7.5V	165	-	-	mA
t_{RISE} , Gate to output rise time	C_{GATE}=500pF, V_{DD}=7.5V	-	30	50	ns
t_{FALL} , Gate to output fall time	C_{GATE}=500pF, V_{DD}=7.5V	-	30	50	ns

Notes:
(1) Also limited by package power dissipation limit, whichever is lower.
(2) V_{DD} load current external to the ZD810.
(3) Denotes the specifications which apply over the full operating ambient temperature range of -40℃ < T_A < +125℃.
(4) Guaranteed by design.

Block Diagram

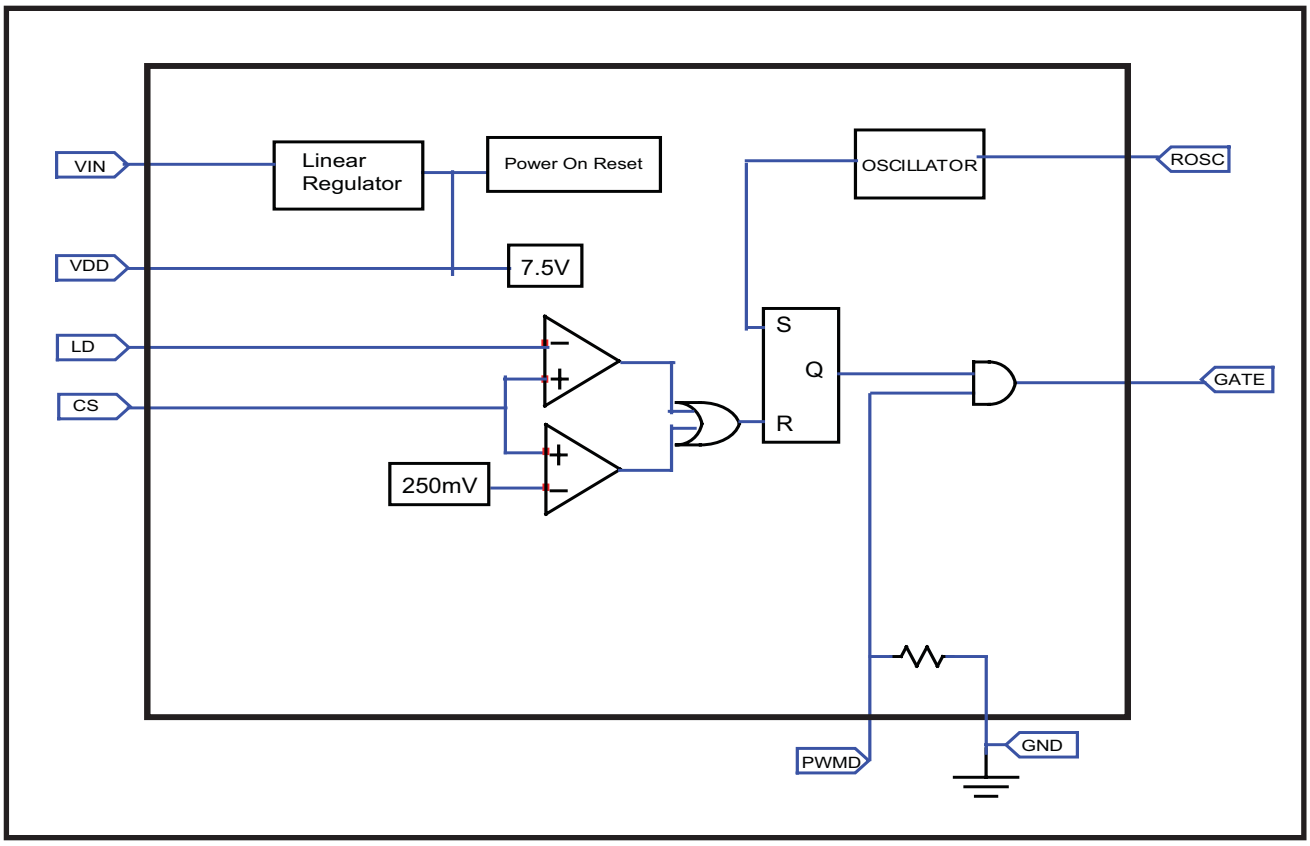


Fig.2. ZD810 Block Diagram

Pin Description

8-pin SOIC	Name	Description
1	V_{IN}	Input. Main power for the LED Driver system. It is the input for the High Voltage (8 ~ 450V) Linear Regulator
2	CS	Current Sense. Used to sense current peaks in the inductor, through a sense resistor to GND. Nominally, the current sensors will trip when the voltage at CS is 250mV, or else the Linear dimming value, if it is lower.
3	GND	Return point for all circuitry. This must be anchored to the lowest available potential in the system.
4	Gate	Gate Drive to the external Power MOSFET
5	PWMD	Pulse Width Modulation Dimming. PWM diming can be performed through this pin. Should be driven with square waves in the low kHz. A logic low input here will turn off the MOSFET driver. If this pin is tied to V_{DD}, PWMD is not operative.
6	V_{DD}	This internally-regulated DC voltage can provide up to 5mA for external circuitry.
7	LD	Linear Dimming. For input voltages less than 250mV, this can be used to linearly adjust the LED brightness. If tied to Vdd, then Linear Dimming is not operative.
8	R_{OSC}	A resistor from here to GND sets the oscillator frequency. From here to Gate sets Constant off-time.

Circuit Description

APPLICATION INFORMATION

The ZD810 is an optimized buck topology LED driver using an open-loop peak current mode control. Accurate LED current control can be achieved without the need for high side current sensing or the design of any closed loop controllers. The ZD810 can be dimmed using Linear and PWM dimming of the LED current.

The ROSC resistor sets the frequency of operation (or the off-time) of the ZD810. The internal oscillator produces pulses at regular intervals that set the SR flip-flop in the ZD810 which causes the Gate driver to turn on. These pulses also start the Blanking timer which controls the reset input of the SR flip flop to prevent false turn-offs due to turn-on spikes. When the MOSFET turns on, the current through the inductor starts ramping up and the current flows through the external sense resistor RCS, producing a ramp voltage at the CS pin. The two comparators are constantly comparing the CS pin voltage to both the voltage at the LD pin and the internal 250mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip flop. When the output of either one of the two comparators goes high, the flip flop is reset and the Gate output goes low. The Gate goes low until the SR flip flop is set by the oscillator.
Assuming a 30% ripple in the inductor, the current sense resistor RCS can be set using:

$$R_{CS} = \frac{0.25V\,(or\ V_{LD})}{1.15 \cdot ILED(A)}$$

Constant frequency peak current mode control goes into sub-harmonic oscillations when the duty cycle is greater than 0.5. An artificial slope is can be added to the current sense waveform but can affect the accuracy of the LED current.

A constant off-time peak current control can easily operate at duty cycles greater then 0.5 and also gives input voltage rejection making the LED current almost insensitive to input voltage variations. This can lead to variable frequency operation depending greatly on the input and output voltage variation. ZD810 allows for both constant frequency and constant off-time modes of operation by changing one connection (see oscillator section).

INPUT VOLTAGE REGULATOR

When a voltage is applied at the V_{IN} pin of 8.0 ~ 450VDC, the ZD810 maintains a constant 7.5V at the V_{DD} pin. This voltage is used to power the internal circuits of the IC and any external circuits needed to control the IC.
The V_{DD} pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The ZD810 can be operated without using the V_{IN} pin by supplying a voltage of 7.5V~12V at the V_{DD} pin. This will turn off the internal linear regulator of the IC and the ZD810 will operate directly off the voltage supplied at the V_{DD} pin.

The V_{IN} pin of the ZD810 is rated up to 450V, but is also limited by the power dissipation in the IC.

Example: 8-pin nSOIC has a junction to ambient thermal resistance $R_{\theta JA}$ = 128°C/W.

The ZD810 draws about I_{IN} = 2.0mA from the V_{IN} pin, and has a maximum allowable temperature rise of the junction temperature limited to about ΔT = 100°C, the maximum voltage at the V_{IN} pin would be:

$$V_{IN(MAX)} = \frac{\Delta T}{R_{\theta JA}} \cdot \frac{1}{I_{IN}} = \frac{100^{\circ}C}{128^{\circ}C/W} \cdot \frac{1}{2mA} = 390V$$

To operate the ZD810 at higher input voltages, a 100V Zener diode can be added in series with the V_{IN} pin to divert some of the power loss and allow for 450V operation.

The input current drawn from the V_{IN} pin is a sum of the 1.0mA current drawn by the internal circuit and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the external FET).

$I_{IN} \approx 1.0mA + Q_g \cdot f_S$

In the above equation, f_S is the switching frequency and Q_g is the GATE charge of the external FET (which can be obtained from the datasheet of the FET).

Circuit Description

CURRENT SENSE

The current sense input (CS pin) of the ZD810 goes to the noninverting inputs of two comparators. One comparator compares the CS pin with the LD pin and the other comparator compares the CS with the internal 250mV reference voltage. The outputs of these comparators input to the and OR GATE that is connected tot he reset pin of the SR flip-flop. The comparator with the lowest voltage at the inverting terminal determines when the GATE output is turned off.

The outputs of the comparators include a 150 ~ 280ns blanking time which prevents false turn-offs of the external MOSFET due to the turn-on spike normally present in peak current mode control. An RC filter may be added between the external sense resistor (R_{CS}) and the CS pin if the blanking time is not adequate enough to filter out the spikes. A proper layout of the PCB, minimizing external inductances, will prevent false triggering of these comparators.

OSCILLATOR

The ZD810 can operate in constant frequency mode or constant off-time mode by terminating the external resistor R_{OSC} in different locations. If the resistor is connected between R_{OSC} and GND, the ZD810 operates in a constant frequency mode and the equation below determines the time-period. If the resistor is connected between R_{OSC} and GATE, the ZD810 operates in a constant off-time mode and the equation below determines the offtime.

$$t_{OSC(\mu s)} = \frac{R_{OSC}(k\Omega) + 22}{25}$$

GATE OUTPUT

The GATE output of the ZD810 drives the GATE of the external MOSFET. It is recommended that the GATE charge of the external FET be less than 25nC for switching frequencies ≤100kHz and less than 15nC for switching frequencies > 100KHz

LINEAR DIMMING

The Linear Dimming pin (LD) is used to control the LED current. An external 0-250mV voltage can be connected to the LD pin to adjust the LED current. The LD pin should be connected to V_{DD} if linear dimming is not desired.
An external voltage divider from the V_{DD} pin can be connected to the LD pin to obtain a voltage (less than 250mV) corresponding to the desired voltage across R_{CS}.

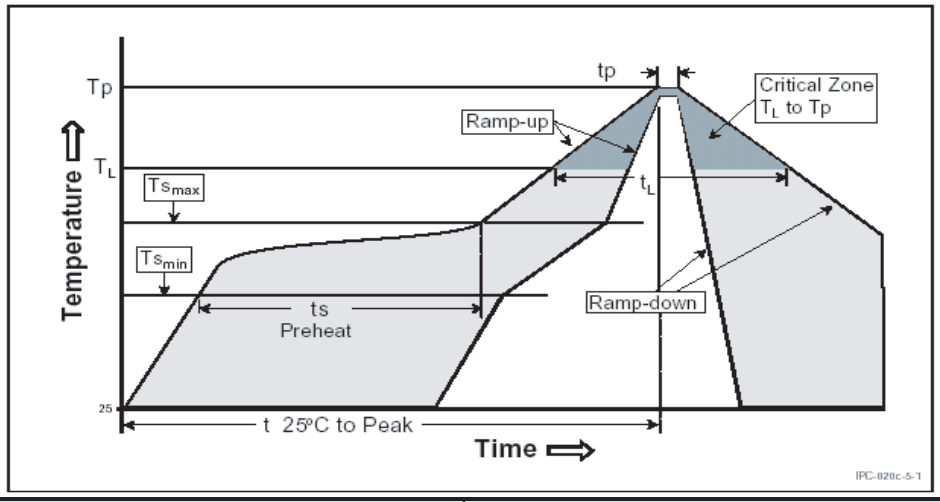
Note: Although the LD pin can be pulled to GND, the output current will not go to zero. This is due to the presence of a minimum on-time (which is equal to the sum of the blanking time and the delay to output time) which is about 450ns.
This will cause the FET to be on for a minimum of 450ns and thus the LED current when LD = GND will not be zero. This current is also dependent on the input voltage, inductance value, forward voltage of the LEDs and circuit parasitics. To get zero LED current, the PWMD pin has to be used.

PWM Dimming

PWM Dimming can be achieved by driving the PWMD pin with a low frequency square wave signal. A logic high and a logic low will enable and disable the GATE driver respectively. The PWMD does not affect other parts of the IC and the rate of rise and fall of the LED current is determined solely by the rise and fall times of the inductor current.
To disable PWM dimming and enable the ZD810 permanently, connect the PWMD pin to V_{DD}.

Green Package SMD IR Reflow Profile Information

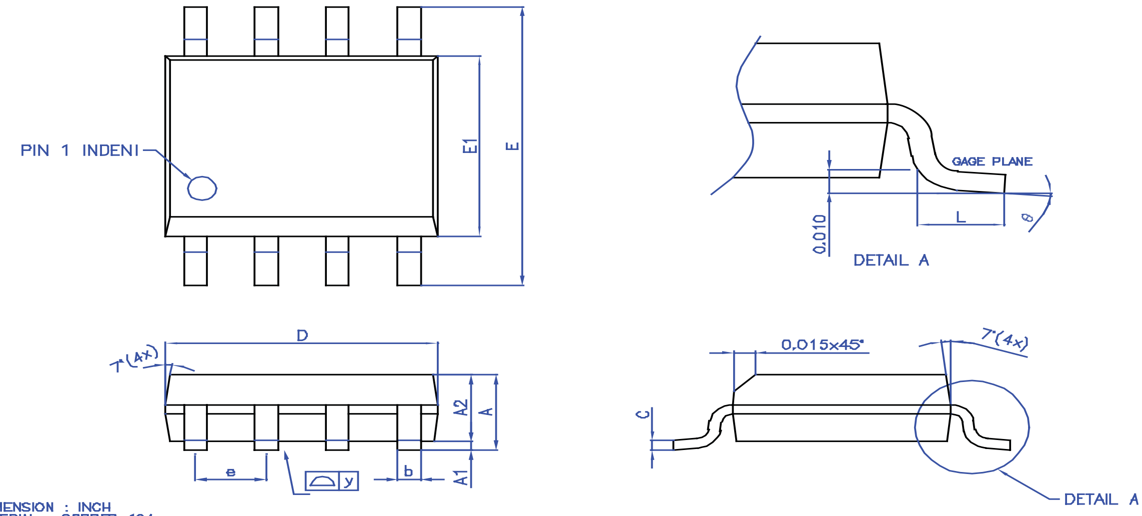
IR Reflow Profile Conditions



Profile Feature	JESD Sn-Pb Eutectic Assembly	JESD Pb-free Assembly
Average Ramp-Up Rate (T_{Smax} to T_P)	3°C/seconds max.	3°C/seconds max.
Pre-heat - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (T_{Smin} to t_{Smax})	 100°C 150°C 60~120 seconds	 150°C 200°C 60~180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60~150 seconds	 217°C 60~150 seconds
Peak/Classification Temperature (T_P)	235°C+5/-0°C	255°C+5/-0°C
Time within 5°C of actual Peak Temperature (t_P)	10~30 seconds	20~40 seconds
Ramp-Down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Zywyn Green Packages are Pb-free and RoHS compliance.

Package Information



NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH. TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH, INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

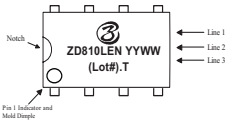
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
△1 L	0.40	0.71	1.27	0.015	0.028	0.050
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

8-Pin nSOIC

CUSTOMER :		ZYWYN CORPORATION	
APPROVED BY	DATE	TITLE: 8L NARROW BODY SMALL OUTLINE PACKAGE DRAWING	
DRAW BY: Vivi Chen	05/21/'01		
CHECK BY: Susan Liu	06/21/'01		
APPROVAL: Dean Tsai	06/21/'01	DWG. NO. PO-SOP-001	REV. 2
APPROVAL: Dean Tsai	06/21/'01	UNIT : INCH	SCALE : 15/1 · SHEET 1 OF 1

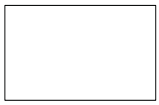
Part Marking Information

TOPSIDE MARK INSTRUCTIONS:



Line 1: Zywyn (logo)
Line 2: Zywyn Part Number "ZD810LEN", Space " ", Date Code (Prod Year & Week)
Line 3: Lot #, dot and Country ".T"
Note: Pin # 1 "△" Indicator Required if no mold dimple

BOTTOMSIDE MARK INSTRUCTIONS:



No backside marking

8-Pin nSOIC

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