Zywyn

ZD1680

High Efficiency Step-Up Controller for LEDs with 6 Channel Current Sink and Auxiliary Gate Drive

Features

- Drives 6 Strings of Up to 16, Serially Connected LEDs
- 6 Channels of Current Sink at **60mA** Each Channel
- Supports up to 15W with an External RSENSE Resistor
- Greater Than 90% Efficiency
- Adjustable LED Brightness with PWM or DC Voltage through the ISET Pin
- LED Currents Set By One External RSET Resistor
- CHIP ENABLE (CE) Pin for Enable or Shutdown
- VBST Pin to set a Higher Gate Drive Voltage (>VDD) for More Efficient and Versatile N-Channel Power FETs can be used
- Output Over-Voltage Protection (OVP) Limiting, Externally Adjustable
- Under Voltage Lockout, UVLO
- Internal Soft Start Inrush Current Limiting
- Internal Thermal Protection
- Simpler, Low Cost, More Reliable Compared to CCFL or EL Backlighting
- Available in a 5x5mm 32-pin VQFN or a 28-pin Exposed-TSSOP Green Package

Applications

- Battery-Powered Backlighting Applications
- LCD Panel And Monitor Display Backlighting And Plane-lighting
- GPS Navigation Panel Display Backlighting
- PMPs And Portable Handy Terminals
- Portable LED Projectors
- Street Lamp Industrial Lighting
- Solar Panel Lighting

General Description

The ZD1680 is a high efficiency step-up controller especially designed for driving multiple strings of serially connected LEDs. 6 channels of low dropout current sinks are included to provide excellent matching of currents for each LED string. The boost converter control loop regulates the current source outputs to 0.3V for maximum efficiency. All 6 channel LED current outputs are set by a resistor RSET to ground at the ISET pin. A CHIP ENABLE (CE) input provides an enable or shutdown function to the IC and the ISET pin can be used to adjust the LED string current with a PWM signal or a DC voltage. Each LED channel can be individually enabled for maximum flexibility. Unused channels must be disabled for proper circuit operation. Also included is an Under Voltage Lockout (UVLO) circuit to discontinue operation when input VDD falls below 2.7V and automatic soft start to limit inrush currents during power start-up or following a re-CHIP ENABLE function. Output Over-Voltage Protection (OVP) is available by user-defined resistor network setting to protect the LEDs and the IC.

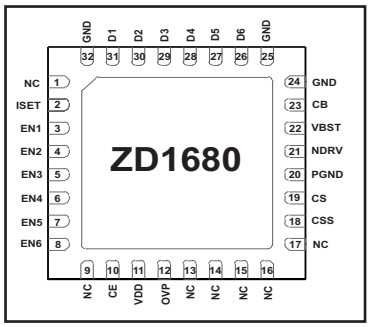
The ZD1680 is available in a 5x5mm 32-pin VQFN or 28-pin Exposed- TSSOP Green Package.

Ordering Information

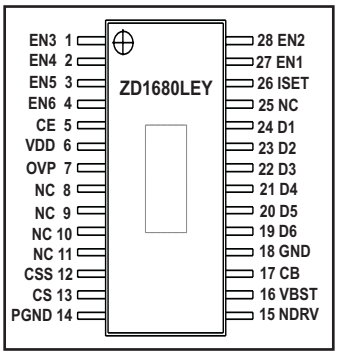
Part Number	Temperature Range	Package Type
ZD1680LEQ	–40℃ to +85℃	32-Pin 5x5 VQFN
ZD1680LEY	–40℃ to +85℃	28-EP-TSSOP
ZD1680YEVB	n/a	Evaluation Board for ZD1680LEY
ZD1680QEVB	n/a	Evaluation Board for ZD1680LEQ

Please contact the factory for pricing and availability on T&R option.

Pin Configuration



5x5 32-VQFN



28-Exposed-TSSOP

Typical Application

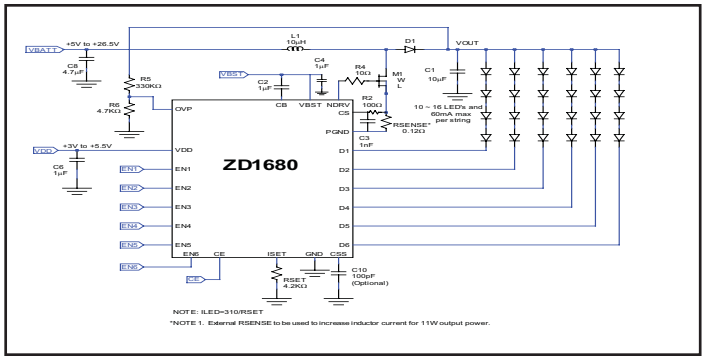


Figure 1. ZD1680 high efficiency step-up controller for LEDs with 6 channels of constant current sink and enables

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Input Voltages (VDD) ..... -0.3V to +6V

$EN_{1~6}$, CE, ISET, OVP..... ..... -0.3V to (VDD+0.3V)

VBST ..... +24V

$V_{D1~6}$ ..... +6V

Extended Commercial
Operating Temperature Range ..... –40℃ to +85℃

Maximum Junction Temperature, T_J..... +150℃

Storage Temperature Range ..... –65℃ to +150℃

Lead Temperature (Soldering, 10 sec.) ..... 300℃

Power Dissipation Per Package @ T_A=+25℃

5x5 32-pin VQFN..... 2.5W

28-pin Exposed TSSOP 3W

Thermal Resistance

Θ_{JA} (28-EP-TSSOP)..... 25℃/W

Θ_{JC} (28-EP-TSSOP)..... 9℃/W

Θ_{JA} (5x5 32-pin VQFN) ..... 34℃/W

Θ_{JC} (5x5 32-pin VQFN) ..... 1℃/W

Storage Considerations

Storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40℃ and 60%RH. If the parts are removed from the bag, they should be used within 168 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for 12 hours at 125℃ in order to remove moisture prior to soldering. Zywyn ships product in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH. The MSL of this product is 3.

The information furnished by Zywyn has been carefully reviewed for accuracy and reliability. Its application or use, however, is solely the responsibility of the user. No responsibility of the use of this information become part of the terms and conditions of any subsequent sales agreement with Zywyn. Specifications are subject to change without the responsibility for any infringement of patents or other rights of third parties which may result from its use. No license or proprietary rights are granted by implication or otherwise under any patent or patent rights of Zywyn Corporation.

Electrical Characteristics

T_A = +25℃, VDD = +3.6V, VBATT=5V, VOUT=30V, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage (VDD)		3.3		5.5	V
Operating Supply Current			0.6	1.2	mA
UVLO Threshold			2.7		V
UVLO Hysteresis			150		mV
FB (D1~6) Regulation Voltage			600		mV
CS Trip Voltage			230		mV
Minimum OFF Time			1.8		μs
Maximum ON Time			8		μS
NDRV Driver Sink/Source Current	VDD=5V, NDRV=2V		0.4		A
NDRV Driver RON	VDD=5V		4		Ω
CE, $EN_{1\sim6}$, V_{IH}		1.4			V
CE, $EN_{1\sim6}$, V_{IL}				0.4	V
ILED Scale Factor K	ILED=K/RSET	279	310	341	
ILED Output Current Sink (D1~6)	CE=VDD	10		60	mA
CE, $EN_{1\sim6}$, ISET PWM Frequency				10	kHz
Maximum Power Output	With External RSENSE (NOTE 1c)			15	W
VBST Range		VDD		13	V
Soft Start Time	From supply start-up or chip re-enable (CE); No external capacitor at CSS pin		250		μs
OVP Threshold Level			0.5		V
OVP Threshold Hysteresis	At OVP input pin		35		mV

Note 1. a) VOUT ranges from 6V to 60V, depending on the # of LEDs in series and the type of N-MOSFET power device used.

b) VBATT ranges: +5V ~ +12V; +12V ~ 18V; +18V ~ 26.5V.

c) Power Output depends on external RSENSE resistor to be used.
For RSENSE = 0.12Ω, POUT MAX = 11W
For RSENSE = 0.06Ω, POUT MAX = 15W

Note 2. See Table 1 for the suggested external components to be used for the VBATT ranges.

Table 1: Recommended external inductor values vs VBATT

VBATT Range	Recommended value for L1 inductor	Comments
5V to 12V	10μH	2 to 3 Li-Ion cells or car battery
12V to 18V	15μH	4 Li-Ion cells battery or car battery
18V to 26.5V	22μH	From CCFL power supply circuit or car battery

Block Diagram

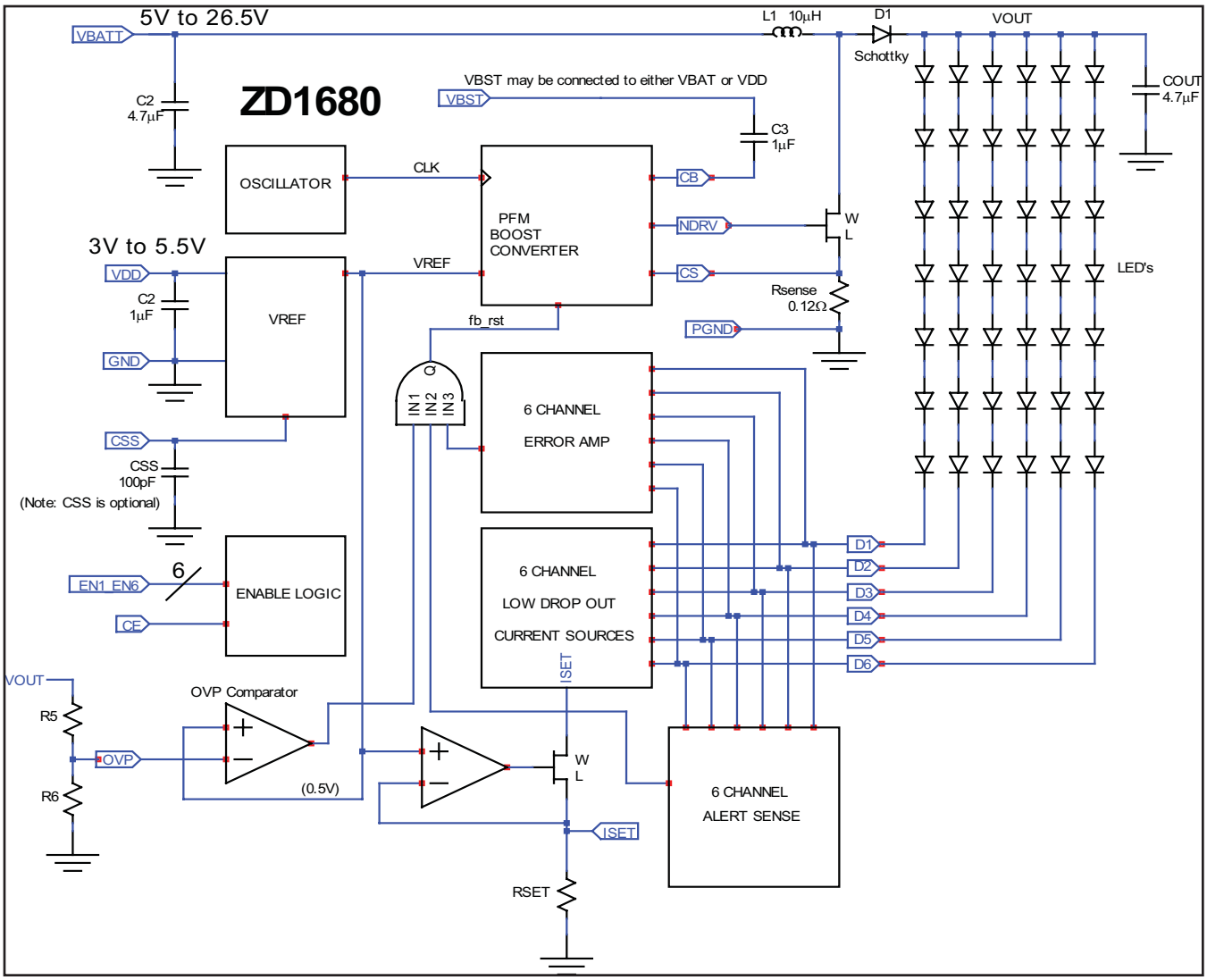


Figure 2. ZD1680 typical block diagram with 6 channel current sinks, 6 channel enables/shutdown, and Over-Voltage Protection (OVP)

Pin Description

Pin Number		Pin Name	Pin Function
32-VQFN	28-TSSOP		
1	25	NC	No Connect Pin. Do not use this pin for making connections.
2	26	ISET	Sets LED Current. Connects external resistor here. (ILED=310/RSET)
3	27	EN1	LED Channel 1 Enable.
4	28	EN2	LED Channel 2 Enable.
5	1	EN3	LED Channel 3 Enable.
6	2	EN4	LED Channel 4 Enable.
7	3	EN5	LED Channel 5 Enable.
8	4	EN6	LED Channel 6 ENable.
9		NC	No Connect Pin. Do not use this pin for making connections.
10	5	CE	Chip Enable Pin. Set HIGH to enable the chip.
11	6	VDD	Input Supply Voltage. Decouple with a 1μF capacitor min. 5.5V max or externally clamped with a 6V zener diode.
12	7	OVP	Output Over-Voltage Protection Input. Set OVP level with external R3//R4 resistor divider. (VOVP = [(R5+R6)/R6] x 0.5)
13	8	NC	No Connect Pin. Do not use this pin for making connections.
14	9	NC	No Connect Pin. Do not use this pin for making connections.
15	10	NC	No Connect Pin. Do not use this pin for making connections.
16	11	NC	No Connect Pin. Do not use this pin for making connections.
17		NC	No Connect Pin. Do not use this pin for making connections.
18	12	CSS	Place a capacitor here to increase the Soft Start time delay. Optional. Typical cap value is 100 pF. Note: Additional Soft Start time also increases the load and line step recovery time.
19	13	CS	Power FET Current-Sense Input. Connects a 0.12Ω, 1W resistor here to PGND for 11W power output capability. (See Note 1c)
20	14	PGND	Power Ground.
21	15	NDRV	Gate Driver Output for external N-channel power MOSFET.
22	16	VBST	Auxiliary Gate Drive Voltage. Connects to VBATT or VDD, 13V max. Decouple with a 1μF capacitor to GND if supplied separately from VDD or VBATT. An externally clamped 15V zener diode is suggested. See application notes for further information.
23	17	CB	High side logic decoupling capacitor, place a 1μF ceramic capacitor to VBST.
24	18	GND	Ground.
25		GND	Ground.
26	19	D6	LED Current Sink #6.
27	20	D5	LED Current Sink #5.
28	21	D4	LED Current Sink #4.
29	22	D3	LED Current Sink #3.
30	23	D2	LED Current Sink #2.
31	24	D1	LED Current Sink #1.
32		GND	Ground.

Circuit Description

The ZD1680 is a high power, high efficiency step-up controller IC especially designed for driving multiple strings of serially connected LEDs. 6 channels of low dropout current sinks are included to provide excellent matching of currents (typically 5% between channel-to-channel) for each LED string. The boost converter control loop regulates the current source outputs to 0.3V for maximum efficiency. The LED string with the largest forward drop will be the string that regulates the boost converter loop. The voltages at the other LED current outputs will be slightly higher. All 6 channel LED current outputs are set by a resistor RSET to ground at the ISET pin. A CHIP ENABLE (CE, enabled "H") logic input provides an enable or shutdown function of the IC and the ISET pin can be used to adjust the LED string current with a PWM signal or a DC voltage. Each LED channel can be individually enabled (active high) by the EN_X pin for maximum flexibility. Unused channels must be disabled (tied to GND) for proper circuit operation. Also included is an Under Voltage Lockout (UVLO) circuit to discontinue operation when input VDD falls below 2.7V and automatic soft start to limit inrush currents during power start-up or following a re-enable (CE only) function. In the case of an open LED, the LED current output for that string will be collapsed to 0V. This will cause the converter control loop to open and drive VOUT up to the OVP voltage limit which can be set by an user-defined external resistor network divider, R5 and R6, as shown in figure 1 in the typical application schematics. At the same time, each LED current source output is protected by an internal zener diode clamp which will also disable the DC-DC step-up converter if the clamp voltage of 6V is reached.

POWER SUPPLY CONNECTIONS

The 3 input supply voltage pins, VDD, VBST and VBATT can be powered in a variety of ways. The VBST input voltage is provided to create a higher gate drive voltage other than normally powered by internal VDD. In this way, the external power N-channel MOSFET can be driven up to 13V, where the main input supply, VDD, would typically be 3.6V to 5V (for example, taken from a common system supply voltage or a TTL logic driver). In some cases, only a single supply input voltage operation is desired. In other cases, it might be desirable to supply VBST from a third separate power supply different from VDD or VBATT, but this separate supply is not usually available. Therefore, in most application configurations, VBST is supplied either from VDD or VBATT (when higher gate drive is desired). The main output power is derived from VBATT which is usually connected directly to a battery source, such as a 2 or 3 cell Li-Ion battery pack or car battery. The exact battery voltage is not critical and the circuit automatically adjusts throughout the battery voltage range.

To facilitate single supply operation, the inputs VDD and VBST are externally shunted by zener diode clamps. Resistors can therefore be used to supply these two voltages from VBATT. The supply current from either VDD or VBST inputs are fairly constant during normal operation. This configuration is shown in figure 4. Note that decoupling capacitors are still needed at VDD and VBST in this configuration.

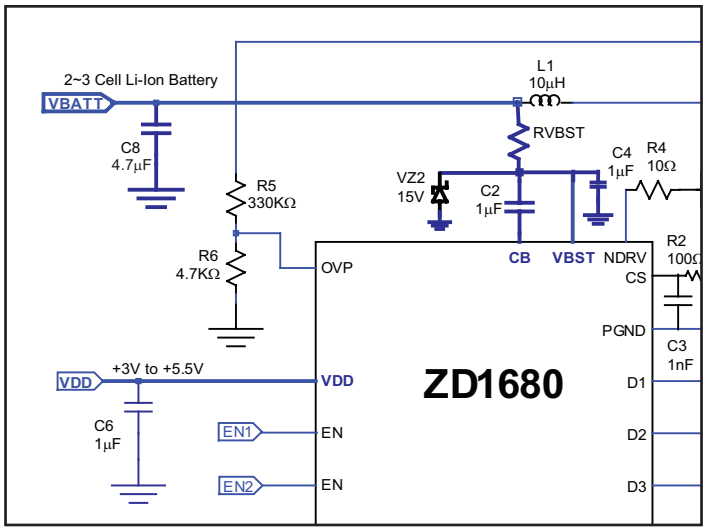


Figure 3, shows a typical application for the ZD1680 in a configuration with VDD supplied by a 3.6V to 5V system supply, VBST and VBATT are connected together from a 2-3 cell Li-Ion battery or some other second source.

Circuit Description

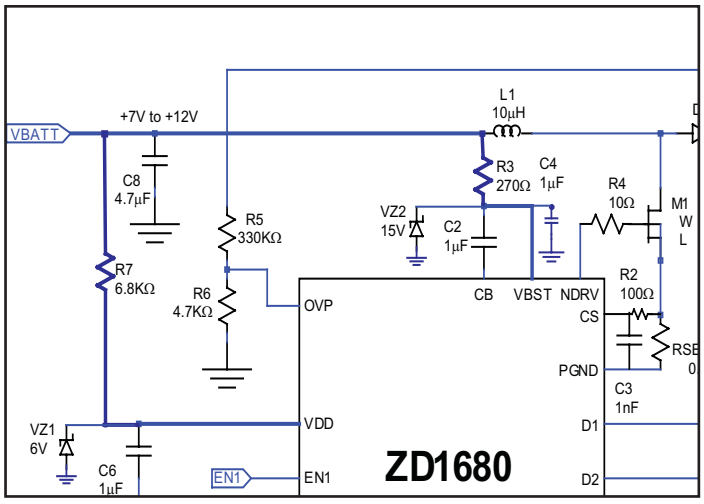


Figure 4, shows a ZD1680 application with a single input supply (VBATT), with VDD and VBST supplied thru resistors from VBATT.

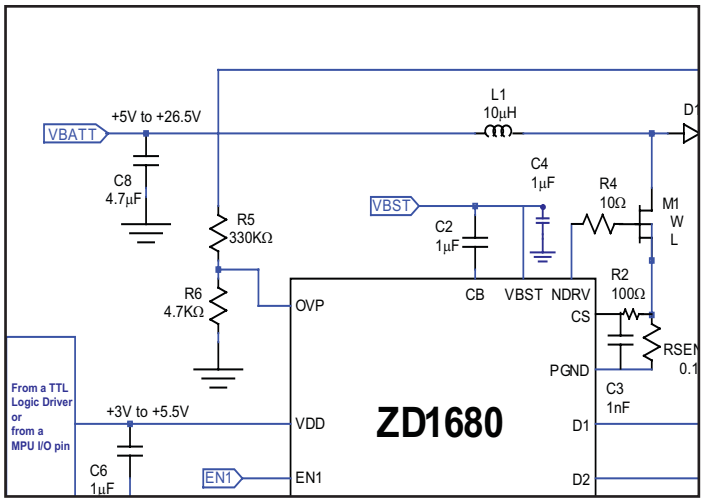


Figure 5, shows a ZD1680 application with VDD supplied by a TTL logic driver, and VBATT and VBST are supplied by separate power sources.

THERMAL SHUTDOWN

The ZD1680 is internally protected from high junction temperatures. If the junction temperature approaches 150℃, an internal temperature sensing circuit will disable the clock and discontinue the DC-DC boost converter operation. At this point, the output voltage will fall which causes the internal temperature to also fall. When the internal temperature has fallen sufficiently below the thermal sense hysteresis, the clock will be re-enabled, the DC-DC converter operation will start-up again and attempt regulation. This on-off cycle will continue until either the external temperature is reduced or the excessive internal power dissipation is reduced.

Excessive internal power dissipation can be a result from several different causes, but will most likely be caused by LED shorts or opens. For a LED short, the diode string that contains a shorted LED will cause the voltage at the current source output to rise by one LED voltage. The current source will still be active but the power dissipation across the current source (and therefore internal) will be much higher. In the event of a LED open, that string will be open circuit which will cause VOUT to boost up until either the OVP limit is reached or the zener diode clamp voltage is reached. Either case will cause the DC-DC boost converter to set a new, higher VOUT, which leads to higher internal power dissipation and possible thermal shutdown.

OVER-VOLTAGE PROTECTION, (OVP)

To protect the external power FET, the series Schottky diode and other external components from over-voltage stress and possible failure, an internal OVP comparator has been added to the ZD1680. An external resistor divider can be set to discontinue the DC-DC boost converter operation when the OVP voltage has been reached. Once the OVP voltage setting has been reached, (on any LED string) the boost converter will regulate to this VOUT value instead of regulating the LED current source output voltage. The proper OVP voltage should be determined by how many LED's per string will be used. In this way, a maximum VOUT for worst case conditions (i.e. temperature, VD spread, etc) can be determined. If it is desired to disable the OVP function, the OVP pin can be grounded. To set an OVP limit, the following equation should be used:

V_{OVP} = (0.5V)(R5+R6)/R6
V_{OVP} = VOUT voltage where OVP occurs

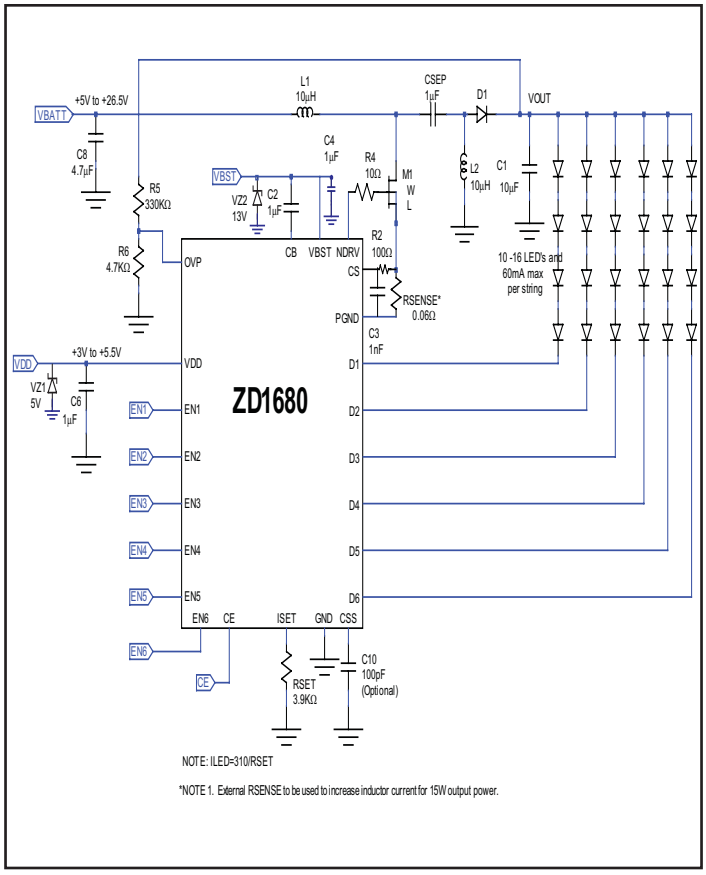
The V_{OVP} limit should be chosen to be just above the maximum expected VOUT as follows:

V_{OVP} = N*V_{Dmax} + 0.5V; where N = # of LED'S per string, V_{Dmax} is maximum LED voltage drop over temperature at 60mA per diode, and 0.5V is for the LED current source output headroom.

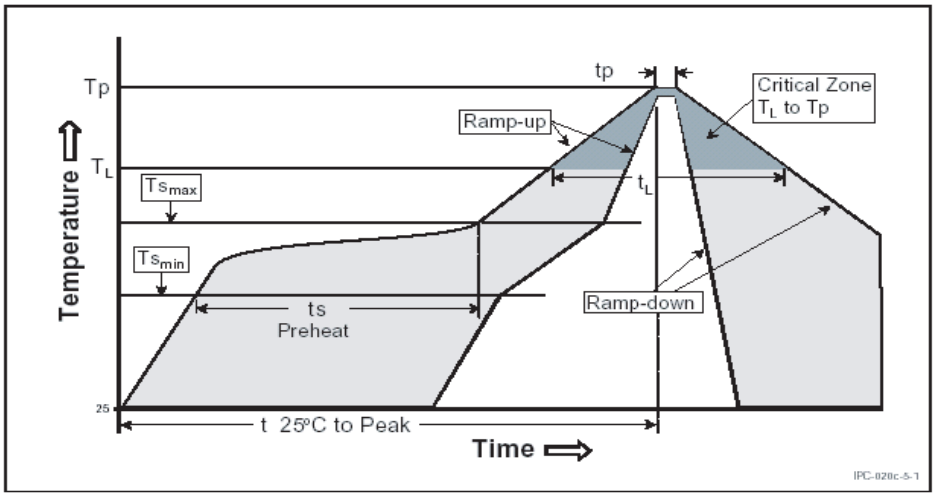
To calculate the total V_D for N number of LED's over process spreads, an RMS of the variation can be used. If V_{OVP} is chosen in this manner, the output power increase is minimized for a defective (open) LED over nominal operation. Any increase in power output for an open LED is dropped across the ZD1680 which increases the likelihood of a thermal shutdown.

BUCK-BOOST (SEPIC) OPERATION

Figure 6 shows a buck-boost application circuit using ZD1680 in a stand-alone mode of operation. The SEPIC topology configuration is needed when the total forward-bias voltage of the LEDs in a string is such that VOUT can be higher or lower than the VBATT.

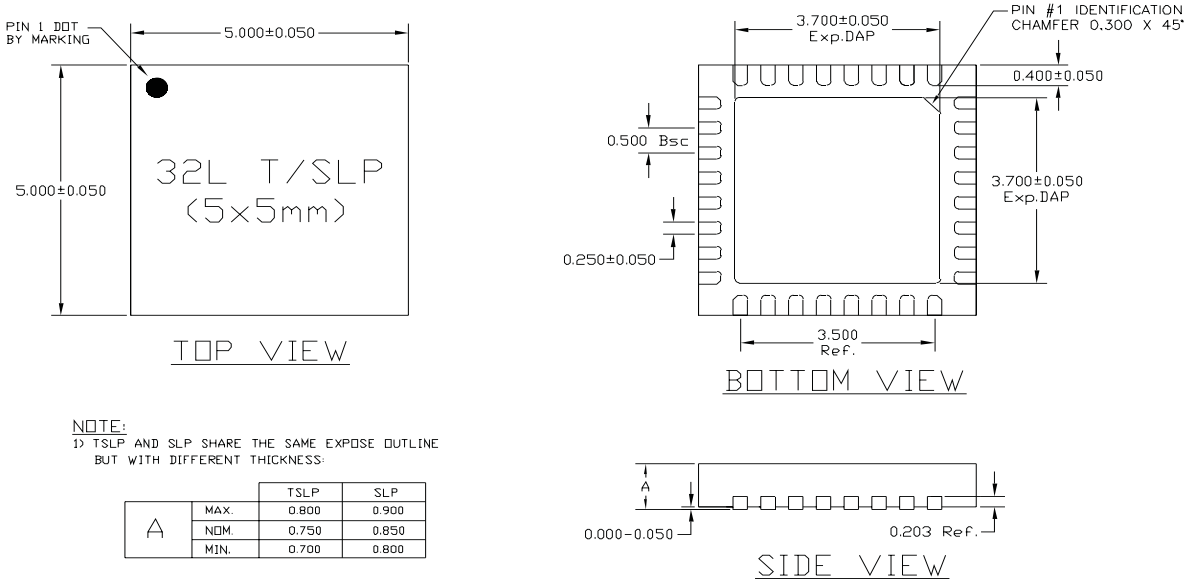


Green Package SMD IR Reflow Profile Information

IR Reflow Profile Conditions		
Profile Feature	JESD Sn-Pb Eutectic Assembly	**JESD Pb-free Assembly**
Average Ramp-Up Rate (T_{Smax} to T_P)	3°C/seconds max.	**3°C/seconds max.**
Pre-heat **- Temperature Min (T_{Smin})** **- Temperature Max (T_{Smax})** **- Time (T_{Smin} to t_{Smax})**	 100°C 150°C 60~120 seconds	 **150°C** **200°C** **60~180 seconds**
Time maintained above: **- Temperature (T_L)** **- Time (t_L)**	 183°C 60~150 seconds	 **217°C** **60~150 seconds**
Peak/Classification Temperature (T_P)	235°C+5/-0°C	**255°C+5/-0°C**
Time within 5°C of actual Peak Temperature (t_P)	10~30 seconds	**20~40 seconds**
Ramp-Down Rate	6°C/second max.	**6°C/second max.**
Time 25°C to Peak Temperature	6 minutes max.	**8 minutes max.**

Zywyn Green Packages are Pb-free and RoHS compliance.

Package Information



	TSLP	SLP
A MAX.	0.800	0.900
A NOM.	0.750	0.850
A MIN.	0.700	0.800

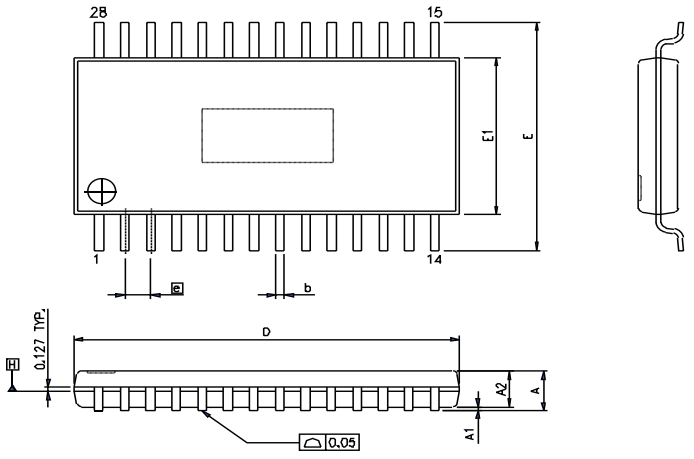
32-Pin 5x5mm VQFN

REV.	DESCRIPTION	DATE	BY	APPD
04	CHANGED DWG NO TO PO-32(T/SLP)5X5-3.70X3.70 AND GENERAL TOLERANCE	13/02/06	ANDREW	CB
03	ADDED TSLP PACKAGE IN THE PACKAGE OUTLINE	16/07/04	BENJAMIN	CB
02	CHANGED OF PACKAGE PROFILE 0.900mm TO 0.860mm	07/10/03	BENJAMIN	CB
01	CHANGED OF DRAWING DESCRIPTION AND #.	07/04/03	BENJAMIN	CB

TOLERANCES: REFER TO SPECIFICATION ABOVE
UNIT: MM SCALE: NTS
SYMBOL

DESIGNED: ANDREW TAN	DATE:
APPD: CW CHAI	DATE:
APPD: GC TAN	DATE:
APPD: RIZAL	DATE:
APPD: WH LAI	DATE:
DWG. NO: PO-32(T/SLP)5X5-3.70x3.70	REV.: 04

ZYWYN CORPORATION
32L (T/SLP) 5x5 mm (PACKAGE OUTLINE)
SHEET NO : 1 OF 1.



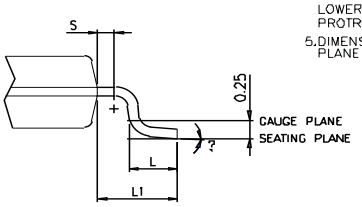
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
?	0°	–	8°

△THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

	PAD SIZE	E2	D1
	118X21E	2.70 REF	4.98 REF
△	105X14E	1.96 REF	2.57 REF

NOTES:
1. JEDEC OUTLINE : MO-153 AE/MO-153 AET(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.



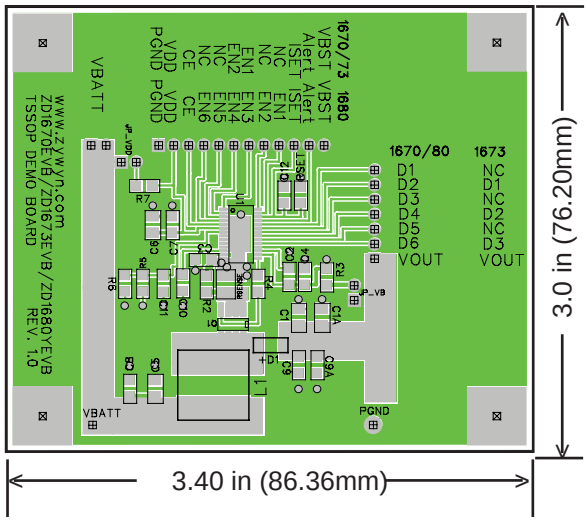
THERMALLY ENHANCED VARIATIONS ONLY

28-Pin Exposed TSSOP

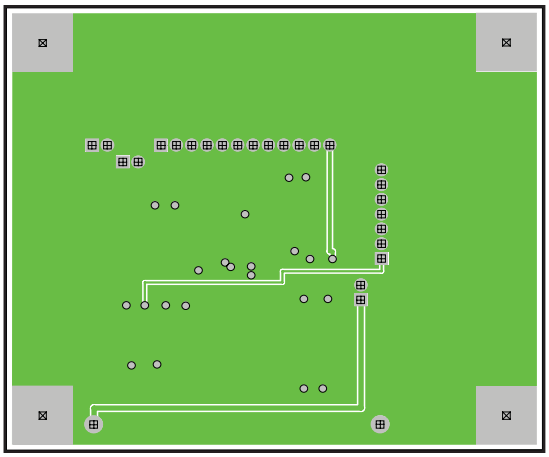
ZYWYN CORPORATION

3RD ANGLE SYS	比例 SCALE:	材質 MTRL:	製程 FINISH:
繪圖: 施佩杏 DWN 日期: 11/9/06	圖名: PLASTIC THIN SHRINK SMALL OUTLINE PACKAGE DATA SHEET 28 LEADS		
審核: 林正源 CHK 日期: 11/9/06	圖號: J1-072BU-001 DWG #		
核准: Erik APPL 日期: 11/10/06	檔名: J1-0728U-001-03 FILE	版次: 03 REV	張次: 1 QTY

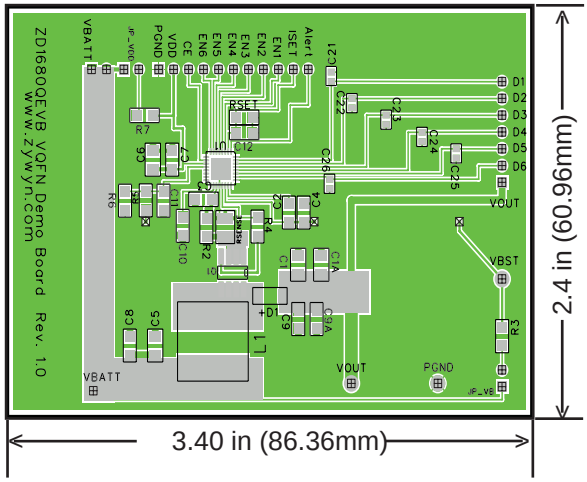
Evaluation Board Information



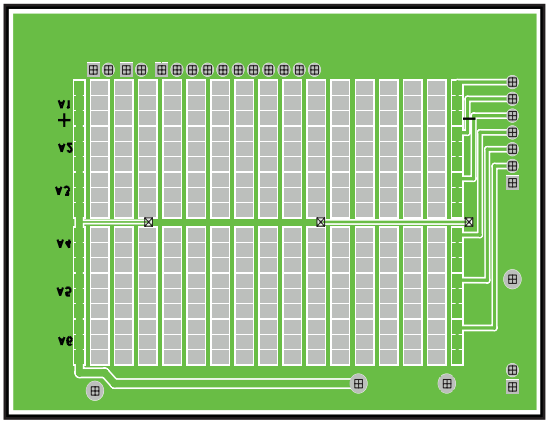
ZD1680YEVB Double-Layer Evaluation Board
Component Side Layout Topview (for 28-EP-TSSOP)



ZD1680YEVB Evaluation Board Backside Layout
Topview (for 28-EP-TSSOP)



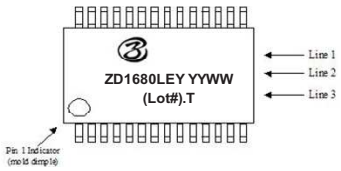
ZD1680QEVB Double-Layer Evaluation Board
Component Side Layout Topview (for 5x5 32-VQFN)



ZD1680QEVB Evaluation Board Backside Layout
Topview (for 5x5 32-VQFN)

Part Marking Information

TOPSIDE MARK INSTRUCTIONS:



Line 1: Zywyn (logo)
Line 2: Zywyn Part Number "ZD1680LEY", Space " ", Date Code (Prod Year & Week)
Line 3: Lot#, dot and Country ".T"

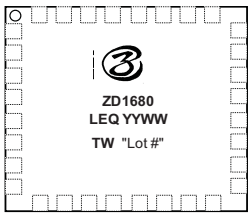
Note: Pin # 1 "◯" Indicator Required if no mold dimple

BOTTOMSIDE MARK INSTRUCTIONS:

No Backside Marking.

28-Pin Exposed TSSOP

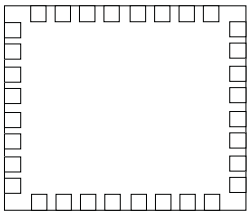
TOPSIDE MARK INSTRUCTIONS:



Line 1: Zywyn (logo)
Line 2: Zywyn Part Number "ZD1680"
Line 3: Zywyn Part Number cont. "LEQ", Space " ", Date Code: (Year & Work Week)
Line 4: Country of Origin "TW", Last 5-digit of Lot Number

Note: Pin # 1 "◯" Indicator Required if no Mold Dimple

BOTTOMSIDE MARK INSTRUCTIONS:



5 x 5 32-VQFN

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