

2N7002PW

60 V, 310 mA N-channel Trench MOSFET

Rev. 02 — 29 July 2010

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- AEC-Q101 qualified
- Logic-level compatible
- Trench MOSFET technology
- Very fast switching

1.3 Applications

- High-speed line driver
- Low-side loadswitch
- Relay driver
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

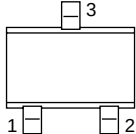
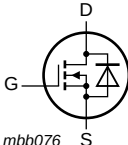
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	310	mA
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 500\text{ mA}; T_J = 25\text{ °C}; t_p \leq 300\text{ }\mu\text{s}; \text{ pulsed}; \delta \leq 0.01$	-	1	1.6	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		

SOT323 (SC-70)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002PW	SC-70	plastic surface-mounted package; 3 leads	SOT323

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
2N7002PW	X8%

[1] % = -: made in Hong Kong; % = p: made in Hong Kong; % = t: made in Malaysia; % = W: made in China

5. Limiting values

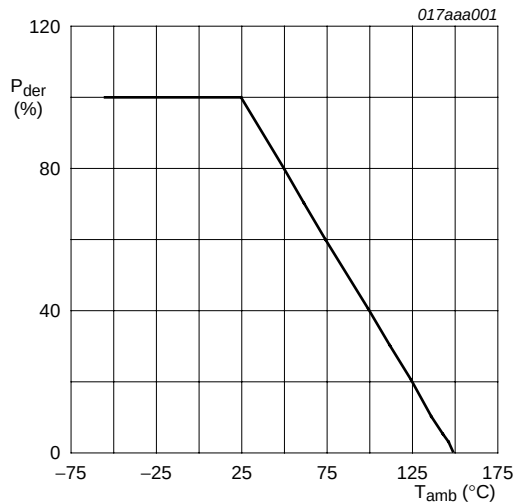
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	60	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	310	mA
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	240	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	1.2	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	260	mW
			[1]	310	mW
		$T_{sp} = 25\text{ °C}$	-	830	mW
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-55	150	°C
T_{stg}	storage temperature		-65	150	°C
Source-drain diode					
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	310	mA

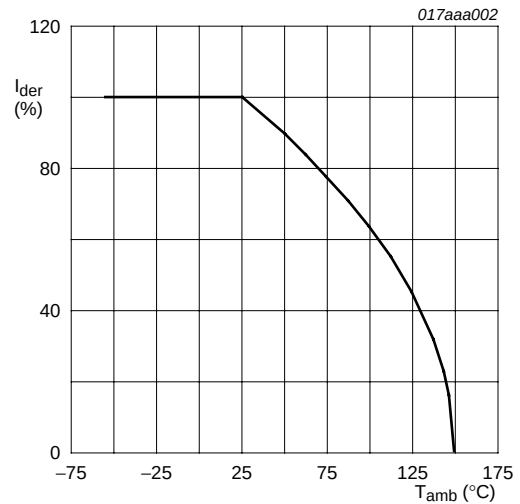
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



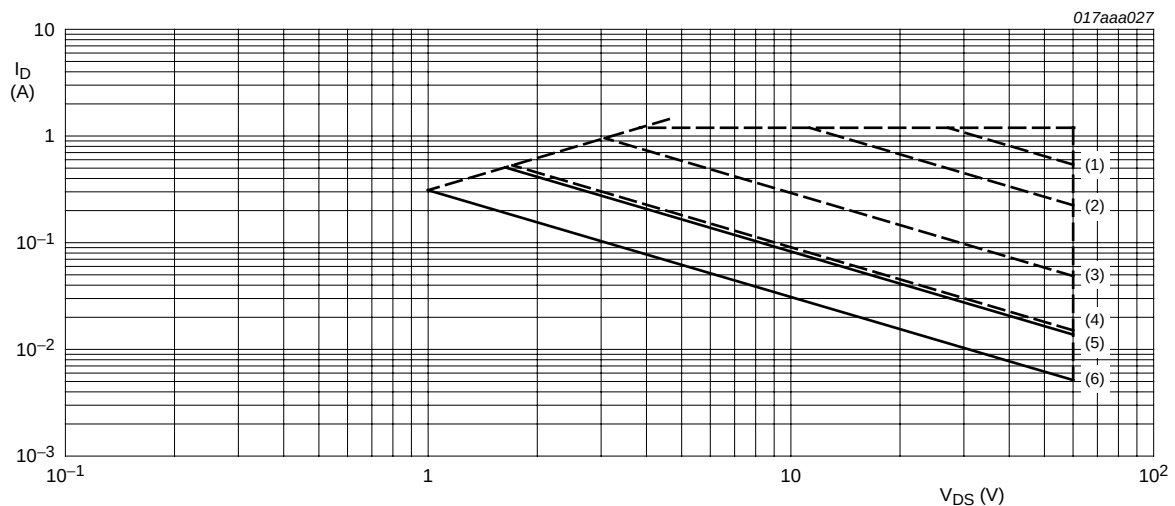
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature



I_{DM} = single pulse

(1) $t_p = 100\ \mu\text{s}$

(2) $t_p = 1\ \text{ms}$

(3) $t_p = 10\ \text{ms}$

(4) $t_p = 100\ \text{ms}$

(5) DC; $T_{sp} = 25^{\circ}\text{C}$

(6) DC; $T_{amb} = 25^{\circ}\text{C}$; drain mounting pad $1\ \text{cm}^2$

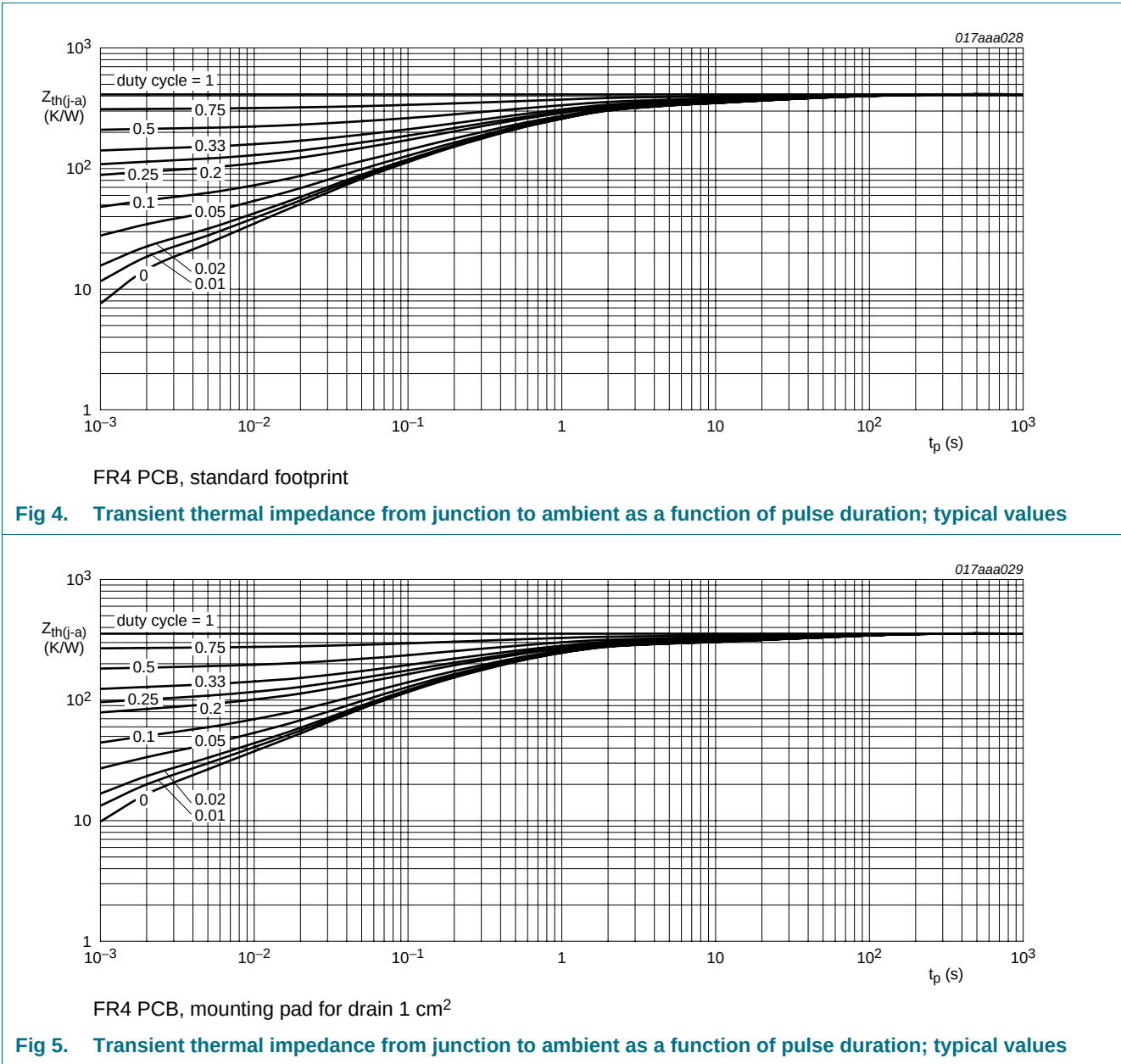
Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	415	480	K/W
			[2]	350	400	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	150	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 10 μA; V _{GS} = 0 V; T _j = 25 °C	60	-	-	V
V _{GStH}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C	1.1	1.75	2.4	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 150 °C	-	-	10	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.01 ; T _j = 25 °C	-	1.3	2	Ω
		V _{GS} = 10 V; I _D = 500 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.01 ; T _j = 25 °C	-	1	1.6	Ω
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 200 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.01 ; T _j = 25 °C	-	400	-	mS
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 300 mA; V _{DS} = 30 V; V _{GS} = 4.5 V; T _j = 25 °C	-	0.6	0.8	nC
Q _{GS}	gate-source charge		-	0.2	-	nC
Q _{GD}	gate-drain charge		-	0.2	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 10 V; f = 1 MHz; T _j = 25 °C	-	30	50	pF
C _{oss}	output capacitance		-	7	-	pF
C _{rss}	reverse transfer capacitance		-	4	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 250 Ω; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C	-	3	6	ns
t _r	rise time		-	4	-	ns
t _{d(off)}	turn-off delay time		-	10	20	ns
t _f	fall time		-	5	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 115 mA; V _{GS} = 0 V; T _j = 25 °C	0.47	0.75	1.1	V

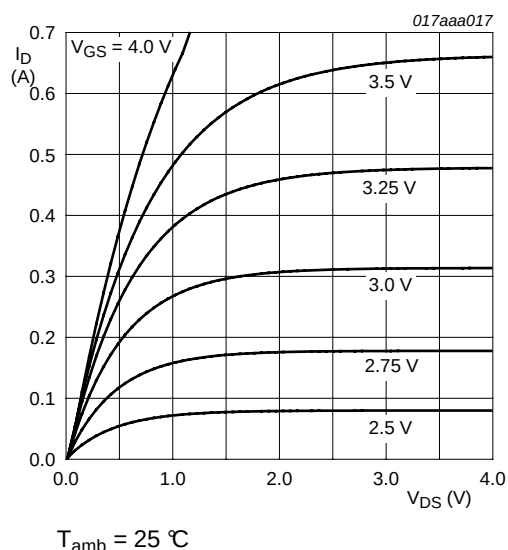


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

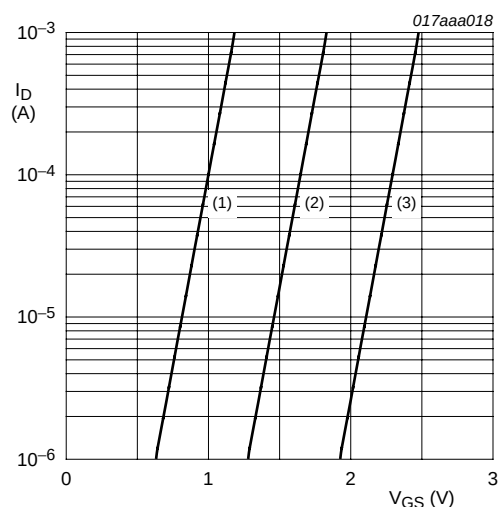


Fig 7. Sub-threshold drain current as a function of gate-source voltage

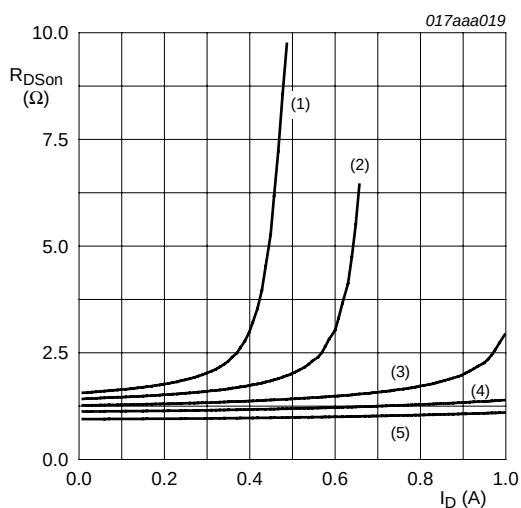


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

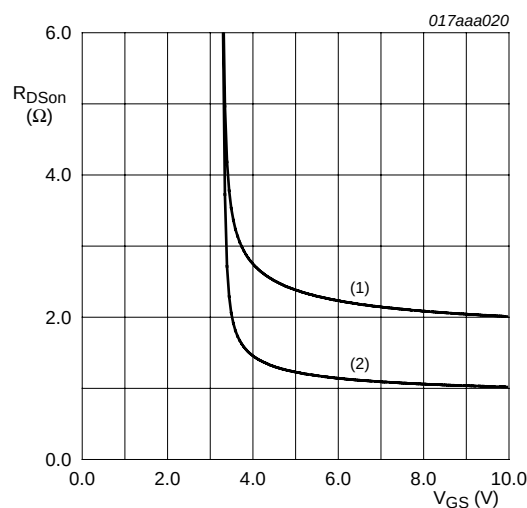


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

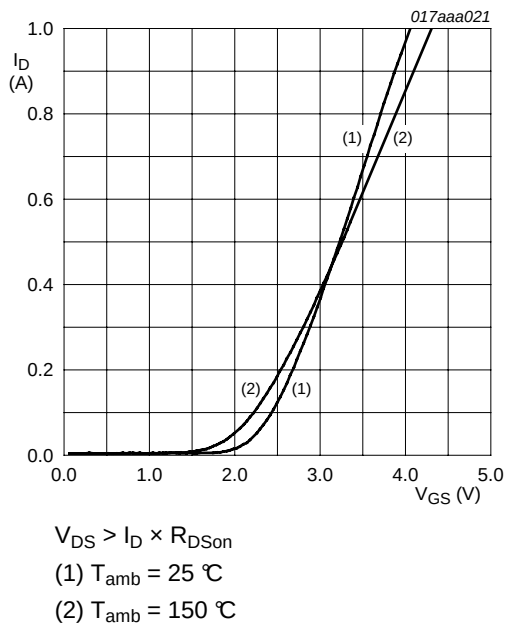


Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

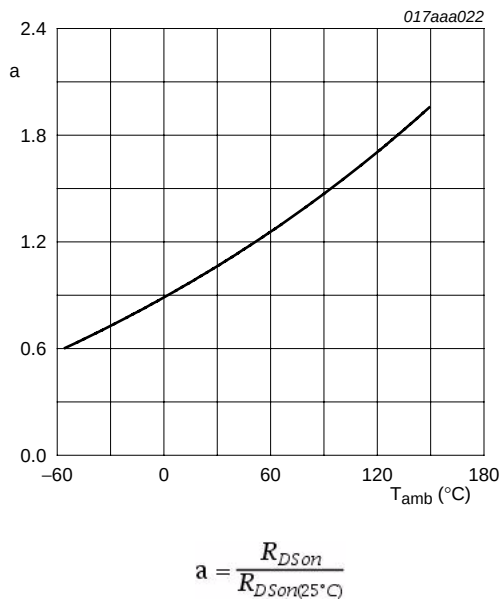


Fig 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

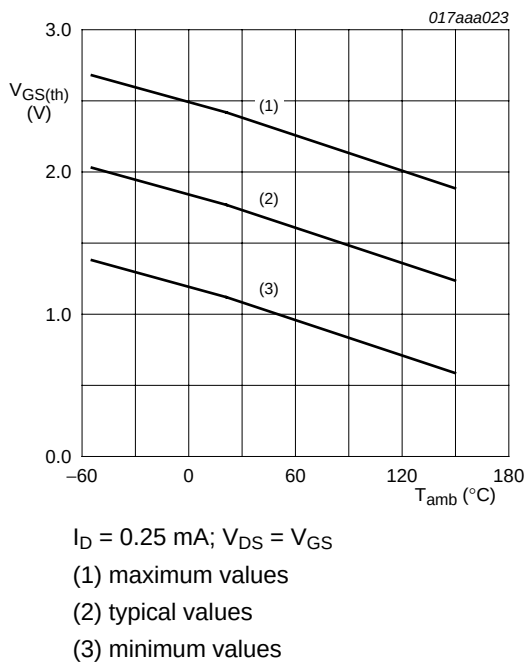


Fig 12. Gate-source threshold voltage as a function of ambient temperature

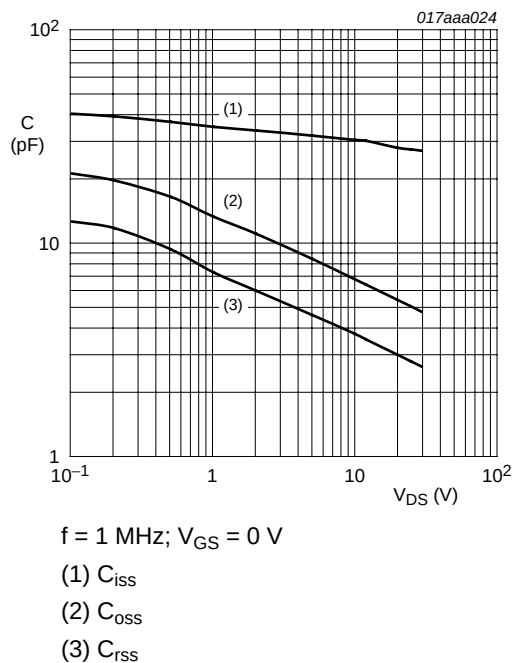
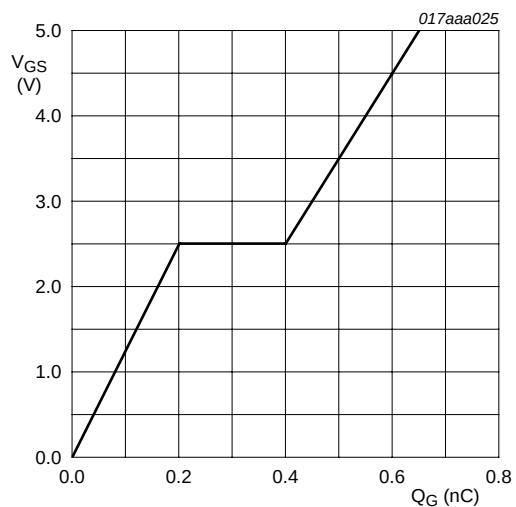


Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 300 \text{ mA}$; $V_{DS} = 30 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$

Fig 14. Gate-source voltage as a function of gate charge; typical values

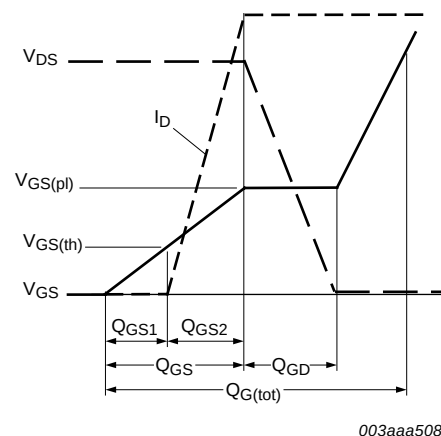
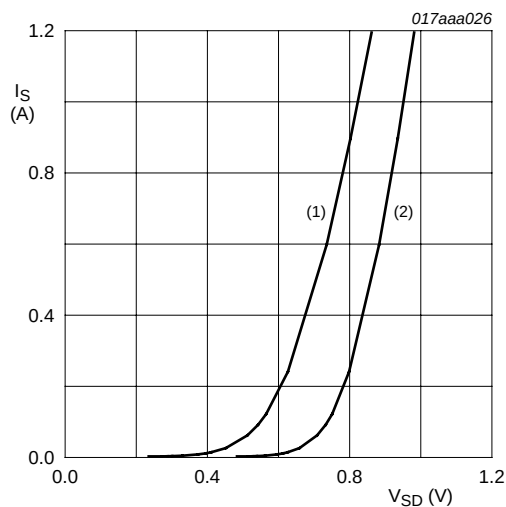


Fig 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

(1) $T_{amb} = 150 \text{ }^{\circ}\text{C}$

(2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

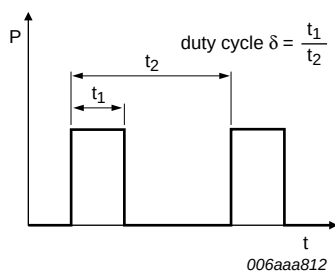


Fig 17. Duty cycle definition

9. Package outline

Plastic surface-mounted package; 3 leads

SOT323

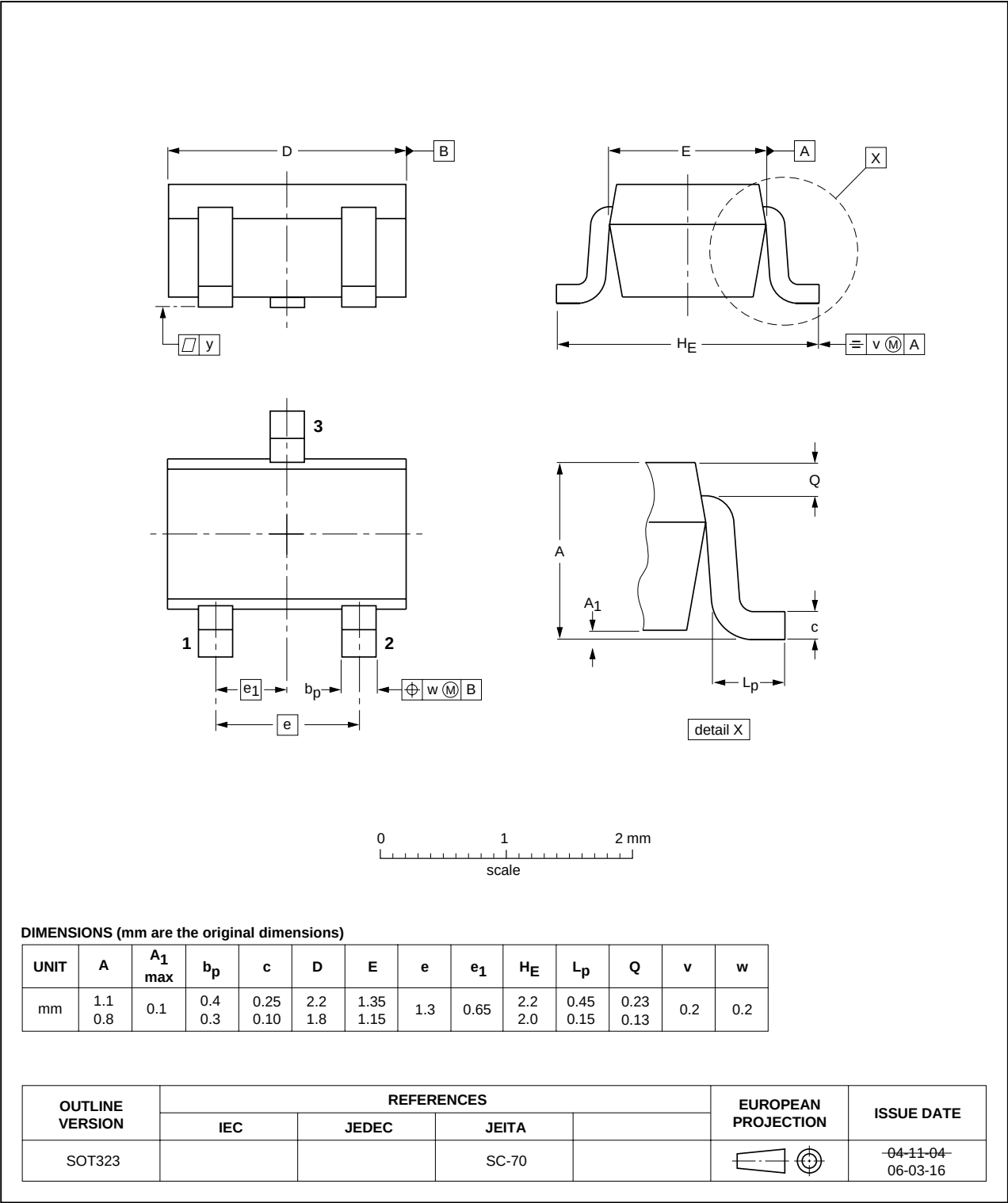
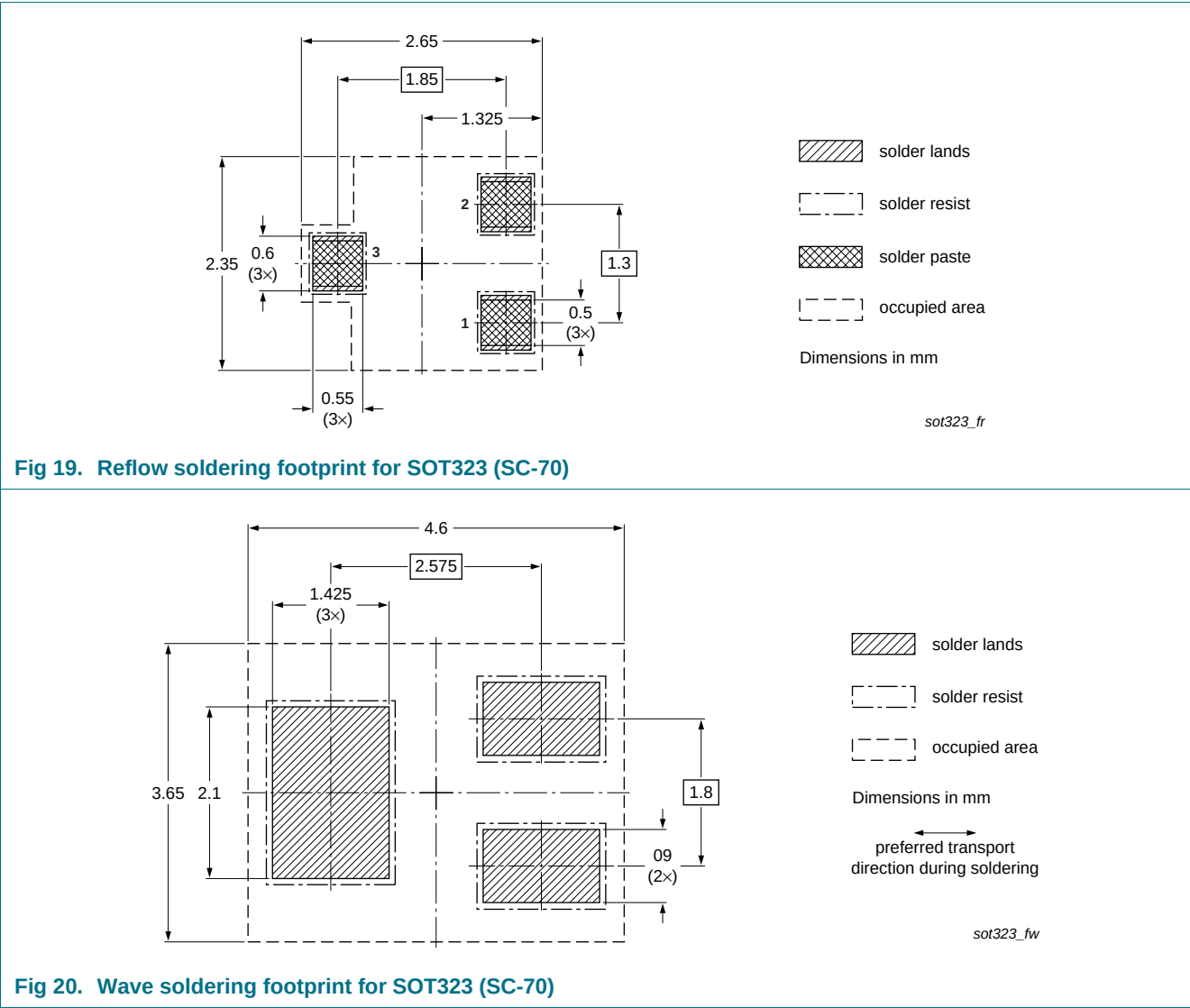


Fig 18. Package outline SOT323 (SC-70)

10. Soldering



11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
2N7002PW v.2	20100729	Product data sheet	-	2N7002PW_1
Modifications:	• Correction of thermal values. • Correction of various characteristics values including related graphs.			
2N7002PW_1	20100422	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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