ARCAL E+

Control module for three-phase IGBT or MOSFET converter "SCALE TECHNOLOGY"

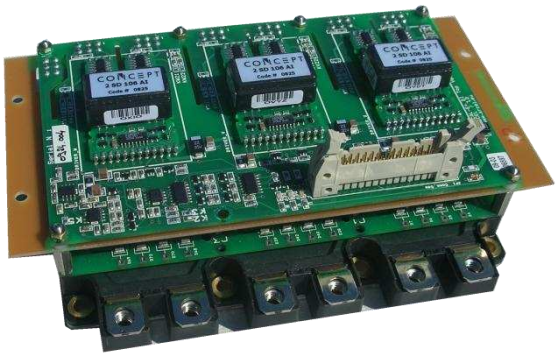
The control module ARCAL E+ includes 3 complementary boards:

- ARCAL E+ TOP
- ARCAL E+ SCREEN
- ARCAL E+ BOT

This module is designed to be used with IGBTs type ECONOPACK+©

On these 3 electronic boards, you have all the functionalities needed for the design of 3-phase converters.

- **High isolation and dv/dt immunity**
- **1W / ±6A per output**
- **Short-circuit protection**
- **'Active Clamping' protection**
- **Detection of supply default**
- **Adjustable dead times**
- **±15V grid input**



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Contents

1. Maximum Electrical Specifications 3
2. Electrical Specifications 3
2.1. Supplies 3
2.2. Input stage 4
2.3. Output stage 4
3. Functional Diagram 5
4. Mechanical Specifications 6
5. General Presentation 8
6. Detailed Technical Description 9
6.1. Supply of driver 9
6.2. Shielding (K1) 10
6.3. Operating mode 10
6.4. Logical inputs 14
6.5. Default signal 14
6.6. Grid Control 15
6.7. 'Active Clamping' Protection 16
6.8. Temperature Measurement 17
6.9. Monitoring of short circuits 18
6.10. Monitoring of auxiliary supplies 19
7. Standard Configuration 20

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1. MAXIMUM ELECTRICAL SPECIFICATIONS

Unless otherwise specified all data are given for 25°C.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power supply voltage (with reference to the exposed conductive part)[i]	0	16	V_{DC}
V_I	Control input	0	V_{DD}	V_{DC}
I_G	Peak trigger current	-6	+6	A
P_G	Average power per output [ii]		1	W
V_{ISO}	Isolation test voltage (AC / 50Hz /1min)		4000	Veff
V_{OP}	Permanent operating voltage[iii]		800	V_{DC}
dv/dt	dv/dt immunity at ΔV=1000V	100		KV/µs
T_A	Operating temperature	-40	+85	°C
T_S	Storage temperature	-40	+90	°C
V_{OC}	Max. voltage of default open collector		40	V
I_{OC}	Max. current of default open collector		10	mA

2. ELECTRICAL SPECIFICATIONS

Unless otherwise specified all data are given for 25°C.

2.1. Supplies

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Rated power supply	14.5	15	15.5	V_{DC}
I_{DD_0}	Total off-load supply current [iv]		150	180	mA
I_{DC_0}	Input current of off-load DC/DC converters		70		mA
I_{DD}	Total current of maximum supply[v]		550	600	mA
η	Efficiency of DC/DC converters		85		%
V_{TH_0}	Trigger threshold of default[vi]		11.5		V
H	Hysteresis of supply default[vii]		0.7		V

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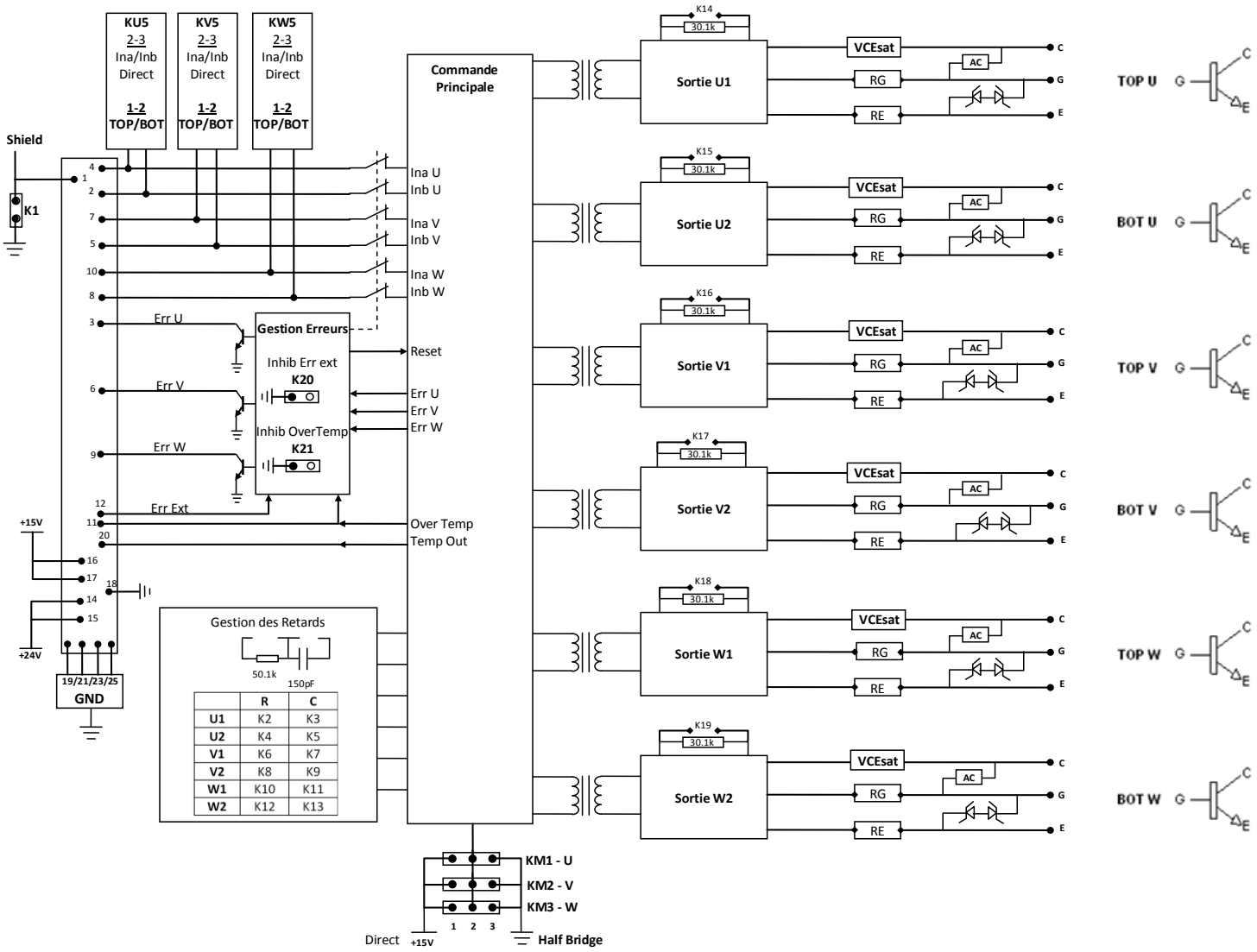
2.2. Input stage

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IM}	Maximum voltage on logical inputs[i]	0		V_{DD}	V_{DC}
V_{IT+}	Flow threshold at high level		10		V
V_{IT-}	Flow threshold at low level		5		V
F_{SW}	Commutation frequency[viii]	0		>100	KHz
α	Control duty cycle	0		100	%
T_{DT}	Standard dead time[ix]		5.5		µs

2.3. Output stage

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_G	Maximum grid current (per IGBT)	-6		+6	A
V_{G+}	Voltage for conduction setting		+15		V
V_{G-}	Cut off voltage		-15		V
T_R	Rising time[x]		110		ns
T_F	Downing time[x]		80		ns
T_{PD+}	Input/output propagation time at conduction setting		500		ns
T_{PD-}	Input/output propagation time at cut off		500		ns
T_B	Cut off time of the inputs after loss of the default		1		s
T_{ER}	Signalling delay of the defaults		70		ms
T_{CE}	Detection time on V_{CE}[ix]		10.4		µs
V_{THX}	Trigger thresholds on V_{CE}[xi]		8.2/6.6		V

3. FUNCTIONAL DIAGRAM



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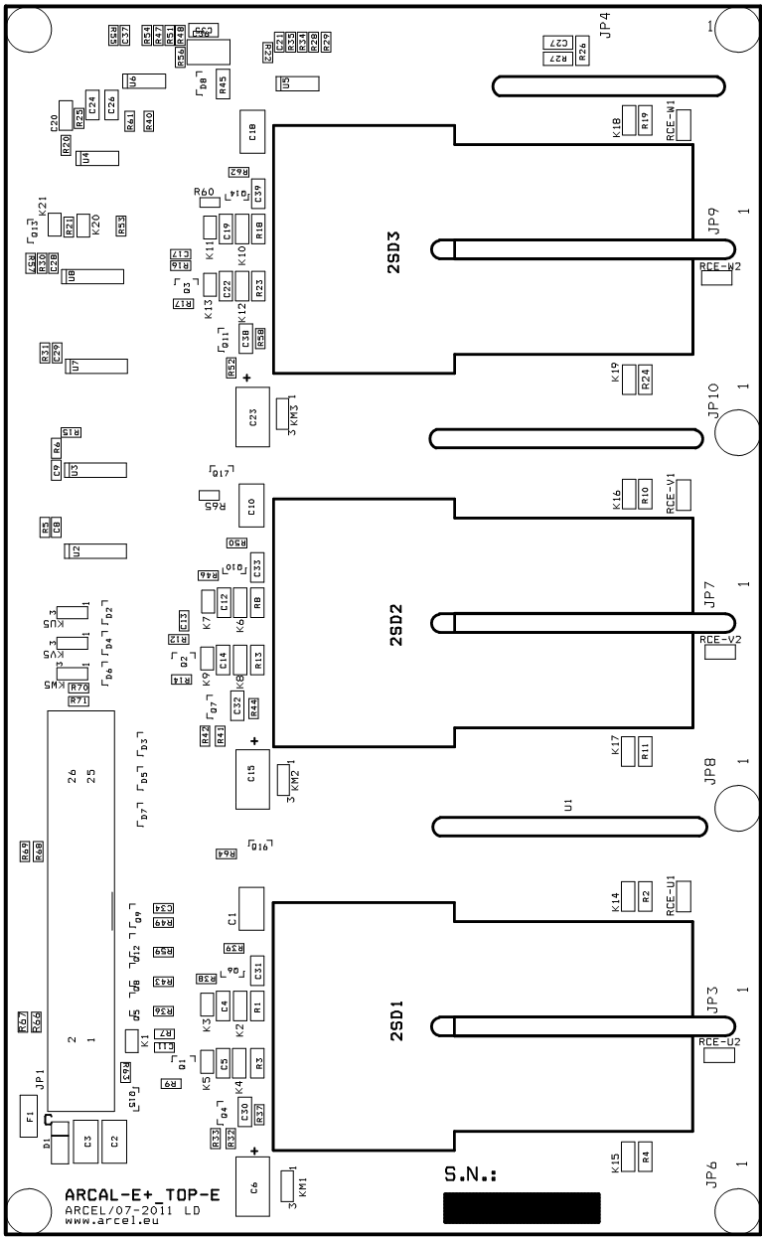
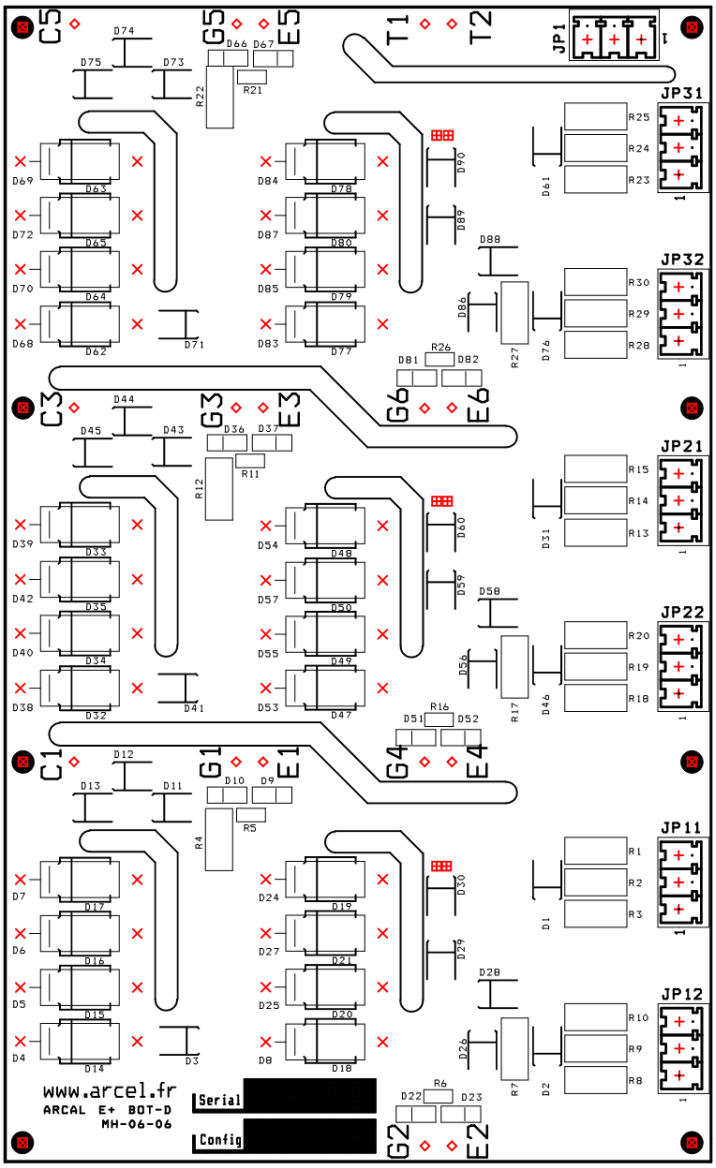
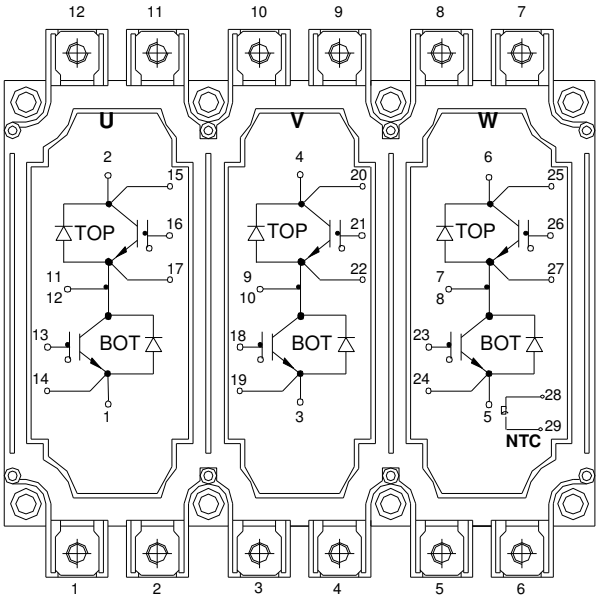
4. MECHANICAL SPECIFICATIONS



Max. height : 22 mm





Internal layout of the ECONOPACK + module

5. GENERAL PRESENTATION

The ARCAL E+ driver is based on three SCALE modules (Scalable, Compact, All purpose, Low cost and Easy to use), the latest generation of drivers which has been acknowledged as "the best project in power electronics" by ABB Switzerland in 1998.

All the functionalities required for driving power switches (IGBTs or MOSFETs) **in full safety** are gathered on one single board. Every single parameter which could depend on the application can be very easily configured.

Main Specifications

- The ARCAL E+ driver enables to drive six IGBTs or MOSFETs in a three-phase bridge configuration by using an ECONOPACK+© power module. This driver is suitable for 600V and 1200V IGBTs in its standard version. Upon request, the ARCAL E+ can be used with 1700V IGBTs.
- The IGBTs (MOSFETs) are controlled in ±15V.
- The IGBTs (MOSFETs) protection is ensured by monitoring of the $V_{CE}sat$ ($V_{DS}on$) and of power supplies.

- An 'Active Clamping' voltage protection is ensured by monitoring of the collector voltage.
- Only one V_{DD} direct supply of 15V ±0.5V is required. The isolated supplies which are required on the power side are internally generated.
- The logical inputs are equipped with Schmitt triggers.
- The logical level of these inputs is selected at 15V (CMOS compatibility).
- The dead time value of each channel can be adjusted by the user.
- The default signal, which is of type open collector, can be activated either by the driver itself (short circuit or supply default), or by an external signal (dry contact).
- The connectors have been selected according to their reliability and in order to rationalize the implementation of the driver in existing applications.
- An intermediary board enables to realize a chip layout which will afford a high EMC immunity, as well as an efficient mechanical protection of the module.

6. DETAILED TECHNICAL DESCRIPTION

6.1. Supply of driver

The ARCAL E+ driver requires a regulated supply of +15V ±0.5V. The maximum power used under normal operating conditions is about 9W.

The current used at the input can be calculated according to the following formula:

$$I_{DD}(A) \approx 3*(\frac{P_{GT}(W)}{0.85\times 15} + 0.035)$$

In which, P_{GT} = total power supplied by the driver to the IGBTs.

Remark:

This product is dedicated to highly impulsive applications and as such there can't be any efficient protection of the DC/DC converter against overloads. The board feeder however is equipped with a fuse which aims to control long-lasting overload risks. These overloads could possibly damage upstream systems.

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6.2. Shielding (K1)

You can use the shielded ribbon cable to link the board with the control unit. You can link the exposed conductive part of the board to the first strand of the ribbon cable (which is generally the shielding) by short-circuiting the terminals of the CMS sections which constitute **K6**.

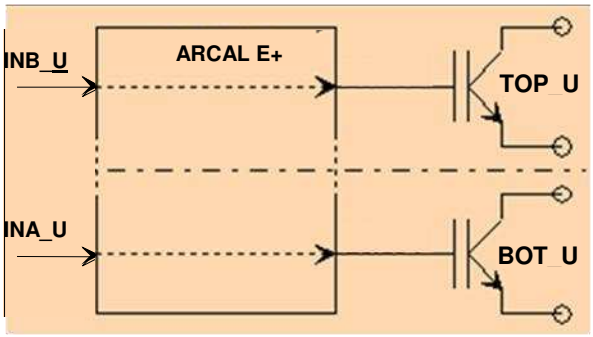
6.3. Operating mode

The ARCAL E+ driver can operate according to 3 different modes:

- The "DIRECT" mode which enables to drive the two outputs independently.
- The "HB" (half-bridge) mode is dedicated to "half-bridge" systems.
- HB modes can be both generated by TOP-BOT or INA-INB control

Direct Mode

In this mode, the outputs are driven independently one from the other by the InA and InB inputs. The different security systems however stop the two outputs and activate the unique default signal. A high logical level on one of the InX inputs maps to the conductive setting of the corresponding IGBT.

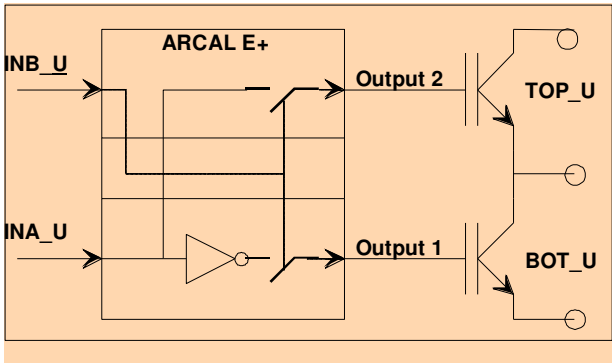


The two channels being independent, the driver won't generate any dead time. It is therefore possible to activate the two outputs at the same time.

The configuration of the driver in DIRECT mode can be done by short-circuiting pins 1 and 2 of KMX, and pins 2 and 3 of KX5 (phase U: KM1 and KU5; phase V: KM2 and KV5; phase W: KM3 and KW5).

HB mode and dead times

The "HALF BRIDGE" or "HB" mode is dedicated to applications which are based on an "ARM" type structure. In this type of structure you have two switches in series controlled in a complementary way. In the case of a 3-phase converter for example, 3 arms have to be controlled, which means that you will need 6 driving signals: InA_U, InB_U, InA_V, InB_V, InA_W, InB_W.



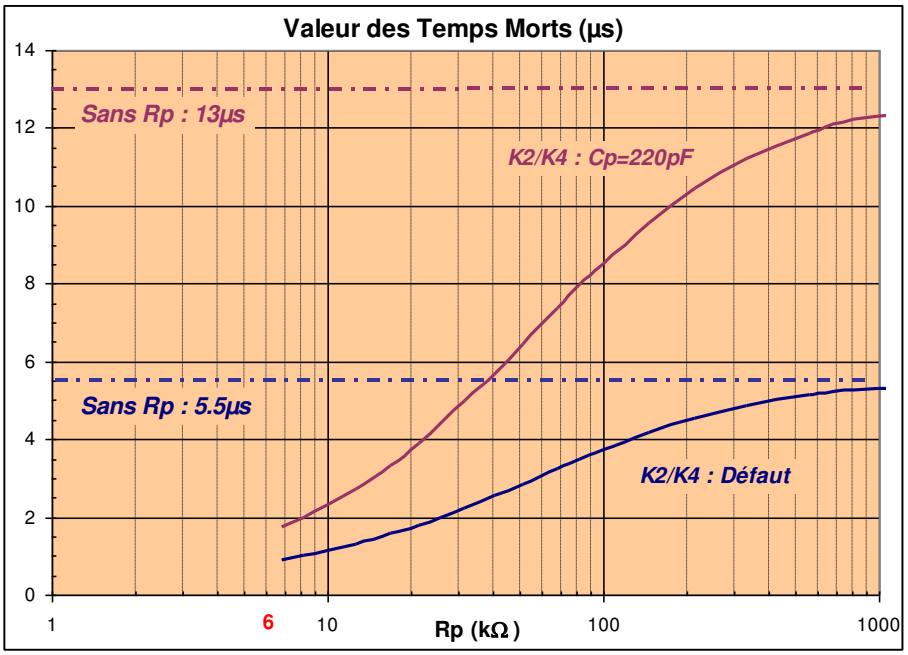
In this case, the two outputs are no longer independent: the InA_U input enables to control the state of the U arm and the InB_U input is used as an inhibition signal for the outputs. A low logical level on InB_U will force the two outputs to the low level, whatever the state of InA_U is.

When the InB_U input is at a high logical level, the state of the outputs will depend on the InA_U input. As the two switches are connected in series, for each change of state of the arm, the driver will ensure that no transitory short-circuit interferes in the arm by holding the two outputs at low level during a fixed period called *dead time*. This operating mode is identical for InA_V, InB_V, and InA_W, InB_W.

The user can interfere on the dead times values of each output owing to fixed contacts (RRCX/CRCX). Normally, the value of these dead times is set up at about 5.5µs. The following diagram will give you the names of the locations which can be used for the modification of dead times.

	TOP_U	BOT_U	TOP_V	BOT_V	TOP_W	BOT_W
RRCX	K2	K4	K6	K8	K10	K12
CRCX	K3	K5	K7	K9	K11	K13

The following figure enables to determine the Rp resistance which has to be added in RRCX according to the dead time that you want in two cases: without adding any capacitor or by adding a Cp capacitor of 220pF on the fixed contacts mentioned in the following diagram.



Outline 2 : Dead time value according to Rrc and Crc

Caution:

The Rp resistance must in no way be lower than 6KΩ.

TOP-BOT or Ina-Inb HB Mode

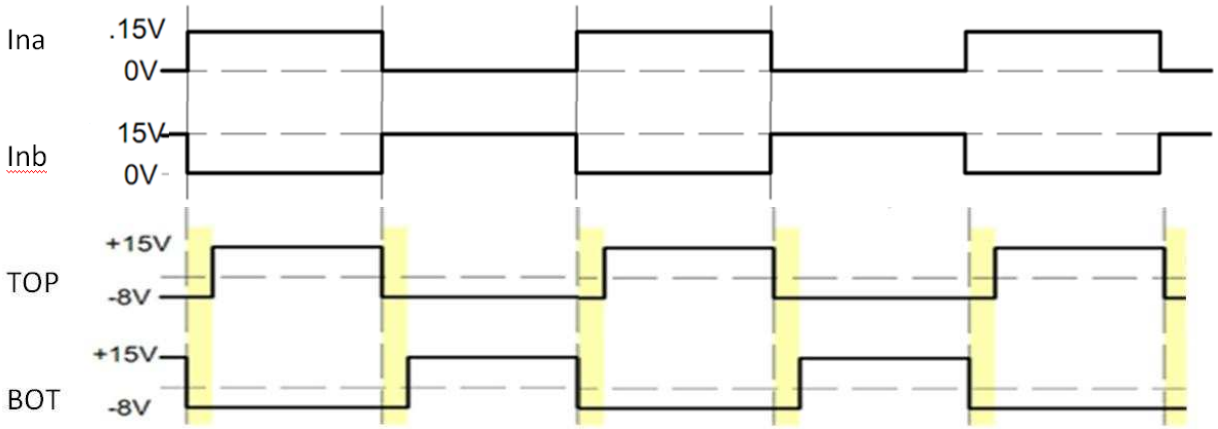
The HB mode allows two different control modes: TOP-BOT and Ina-Inb.

The TOP-BOT mode enables to send complementary signals Ina and Inb, in order to generate the “start/stop” signal on Inb channel from these two signals.

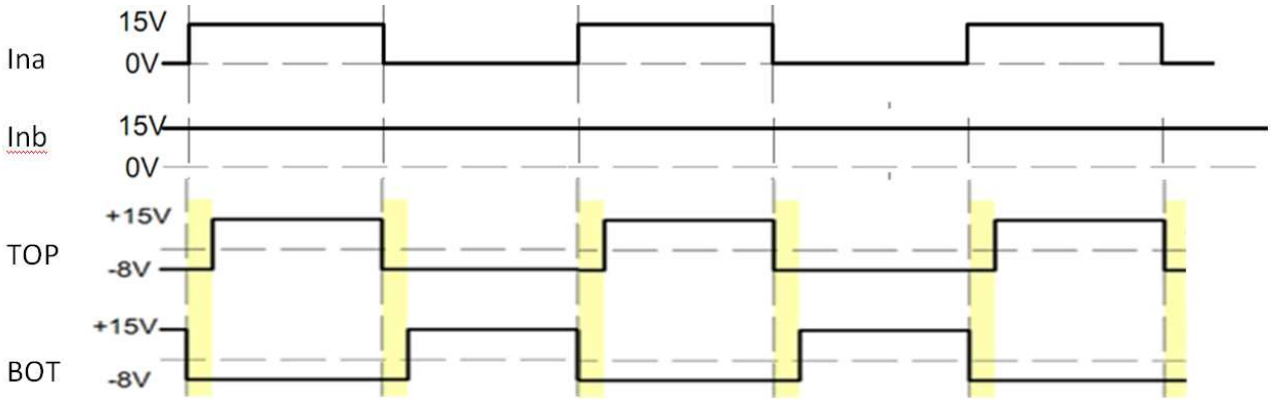
If the user only has InA_U, InA_V, InA_W signals and the InB_U, InB_V, InB_W complementary orders, pins 1 and 2 of **KU5**, **KV5**, and **KW5** must be shorted in order to re-create the 0 to 1 working order of HB mode. It is the Top/Bot setting.

A maximum delay of 4µs is accepted between the InA-U and InB-U, InA-V and InB-V, InA-W and InB-W input signals.

In case the InB_U, InB_V, InB_W inputs are directly attacked by an on/off order; pins 2 and 3 of **KU5**, **KV5**, **and KW5** must be shorted. It is the InA /InB setting.



Signals in TOP-BOT mode



Signals in Ina-Inb mode

NOTE: Ina and Inb correspond to output orders at the 26-pin connector JP1.

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6.4. Logical inputs

The InA and InB inputs are equipped with Schmitt triggers whose tilting thresholds are about 1/3 and 2/3 of the selected logical level (CMOS). A high logical level fits with an active input (positive logic).

The input stage of the driver includes protection diodes against negative voltages or against voltages higher than VDD. If the voltages exceed these limits, an abnormal temperature rise and/or over-consumption could occur. Safe practice should be taken in case of use of the driver with large lengths of cable.

6.5. Default signal

The "DEFAULT" output is of type open collector. It can resist to a 40V voltage and drain a 10mA current. An external draught loss must be provided.

The default signal is Active at high level: in case of a default, the output transistor is stopped (high impedance). This is the standard operating mode as a failure of the control cable will be interpreted as a default by the upstream control system.

In case of internal error

In case of an internal error, the default will be shown during an interval of about 70ms. The driver will be automatically restarted and the outputs will stay inactive for a minimum time of 1s. The upstream control system is supposed to stop the control pulses as soon as the default appears. Should the opposite happen, and after the default signalling delay, low-rate commutations (about 10µs) can occur on the non-default channel. The default will then be shown again by a 70ms pulse, etc… until the cause of the default has been found out and has disappeared or until the control pulses have stopped.

A default results in a reset of the concerned driver, and in a fault signal sent on JP1 connector (pin 3 for U, pin 6 for V, pin 9 for W).

Remark

The management of internal defaults is directly done at each output. Thus the default channel is immediately stopped for a minimum time of 1s. The information feedback towards the input however only takes place when there is a change of state of the InX_x (or InA_X in HB mode) inputs. After the blocking period of pulses the system will only start again on a pulse rise of the concerned InX_X (or InA_X in HB mode) input.

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External error and over temperature (K20, K21)

The user can use the JP1 connector's pin 12 to notify the card that an external error occurred in the system. Moreover, the CTN connector of the econopack+ is connected via the JP4 connector. Thanks to this temperature measurement performed and sent to JP1 connector's pin 20, it is possible to know if the temperature achieved or exceeded the maximal limit of 115°C. In that case, an overtemp signal is generated and sent on the JP1 connector's pin 11.

In these two cases, the error results in the inhibition of all control signals, as well as the reset of the three drivers, and a fault signal is sent on the three channels (pins 3, 6 and 9 of JP1).

If the user does not use one of these fault detection, the corresponding strap must be shorted: **K20** for the External Error, **K21** for the Overtemp.

Driver power up

A default pulse (about 70ms) is automatically generated when powering up the driver in order to enable the auxiliary supplies to settle.

6.6. Grid Control

In the standard version the IGBTs are controlled in ±15V.

For each output it is necessary to mount two resistors to limit the grid current. One of the resistors is connected to the grid (RG) and the second one to the emitter (RE). The total sum of these resistors is the grid resistance and its value depends on the IGBT which is used. RE and RG must have the same value.

These resistors are selected according to the recommendations of the manufacturer of the IGBT that is used. The following diagram gives you the references of the resistors.

	TOP_U	BOT_U	TOP_V	BOT_V	TOP_W	BOT_W
RG	R1	R2	R3	R4	R5	R6
RE	R8	R7	R10	R9	R12	R11

Peak current

The peak current provided by the driver depends on the total resistance of the Grid/Emitter loop. Its value can be estimated according to the following formula:

$$I_{Gp}(A) = \frac{\Delta V_{GE}(V)}{R_G(\Omega)}$$

In which, ΔV_{GE} represents the variation of the grid voltage (in this case, 30V).

As the I_{Gp} current mustn't exceed 6A, the theoretical low limit for R_G is 5Ω .

Average power

The average power, P_G, provided by a driver output depends on the gate charge, Q_G, of the component which is used, on the variation of the grid voltage, ΔV_{GE}, and on the commutation frequency, F_{SW} (SI units):

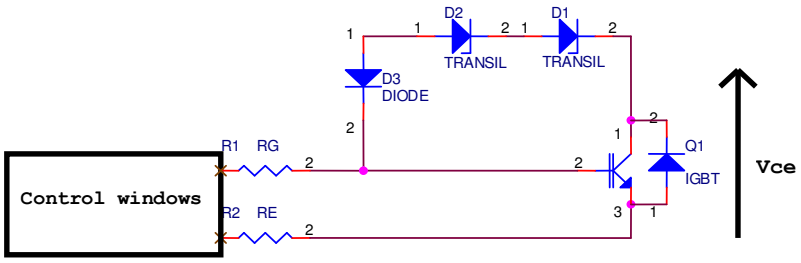
$$P_G = Q_G \times \Delta V_{GE} \times F_{SW}$$

This power must in no way exceed 1W.

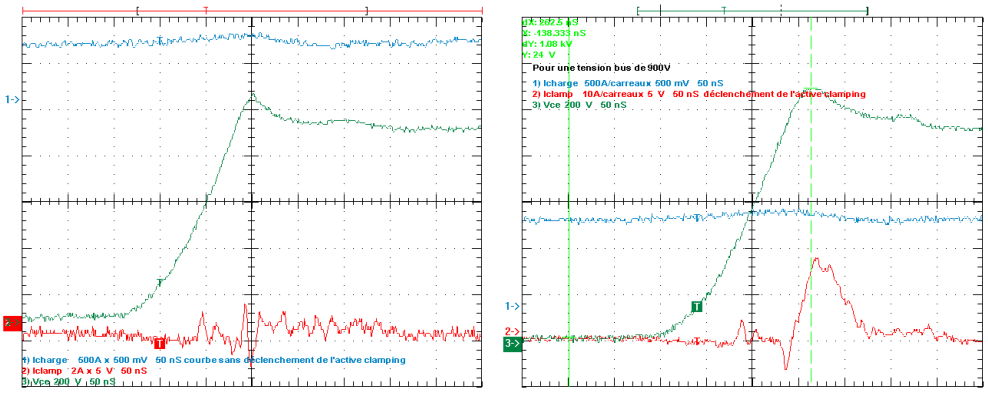
6.7. 'Active Clamping' Protection

This protection aims to limit the emitter collector overvoltage at the opening of the semiconductor. This overvoltage is the product of the interfering inductance of the loop by the di/dt imposed by the component.

The functional diagram is as follows:



As soon as the Vce voltage exceeds a value determined by the transils, a current is injected in the base of the IGBT thus generating a short renewal phase and enabling to limit de the tension at the terminals. **This device mustn't be used at continuous rating (i.e. at each commutation), as it introduces additional losses which can be damaging for the IGBT.**



The two above oscillograms (the first one with the device and the second one without it) show the influence of the device. You can clearly see the limitation of the overvoltage which results in a clipping.

In the standard version, the voltage protection is set for a 1200V IGBT module. Upon request it is possible to get a protection for a different voltage (1700V for example).

This device enables to limit the overvoltage at the opening to a value close to 1100 volts (according to the dispersion of the components and the energy that has to be dissipated, the clipping voltage varies from 1020V to 1100V). (The board can be configured upon request for IGBTs 600V or 1700V).

6.8. Temperature Measurement

A CTN is included in the econopack+ housing. The board includes a linearization of this CTN in the useful operating area. The temperature information is available on pin 12 of the HE14 connector.

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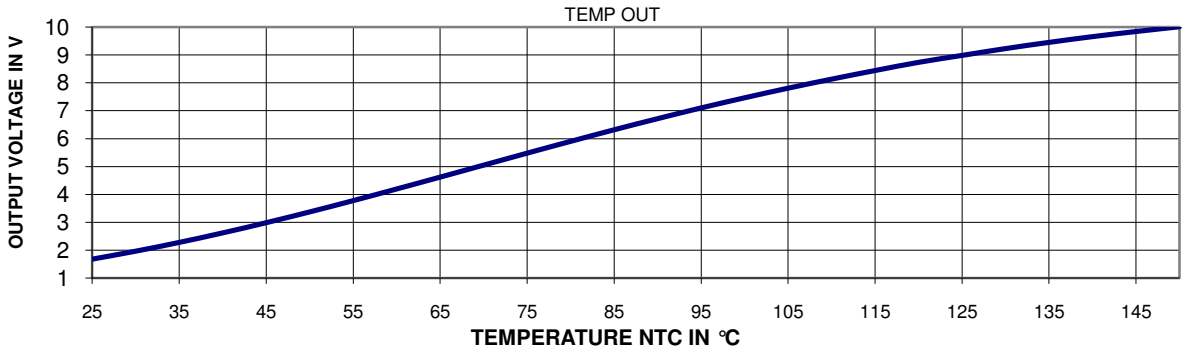


Outline 5: Voltage on pin 12 according to the CTN temperature

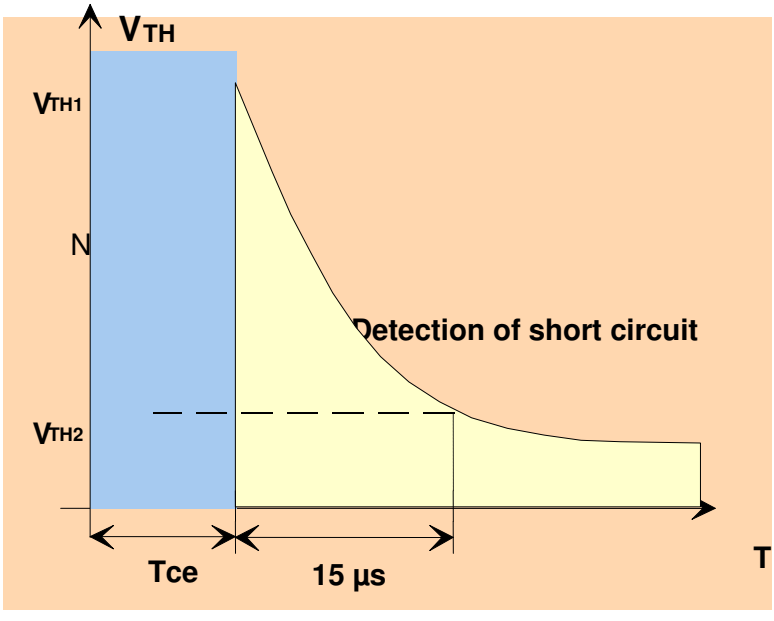
When the NTC temperature exceeds a 115°C threshold, the potential on output 11 of connector is brought to 0V, through the collector of the output transistor, and the orders are inhibited (in standard configuration, adjustable thanks to the strap **K21**).

6.9. Monitoring of short circuits

The detection of short circuits is done by comparing the VCEsat voltage of the device with a reference voltage. If this threshold level is exceeded, the concerned channel is stopped and the default signal is activated.

In order to better fit with the IGBT commutation profile, the reference voltage varies according to the elapsed time since the conduction setting.

First of all the detection has to be deactivated during a fixed TCE period. Once this period is over, the detection threshold is equal to VTH1 and will progressively decrease (in about 15µs) until it reaches the VTH2 value.



Outline 3 : Profile of the reference voltage

For each channel, a resistor (RTH) enables to configure the VCEsat detection. The user can modify the default value by adding a parallel resistor. The default value is 30.1k. The following diagram gives you the names of the RTH locations.

	TOP U	BOT U	TOP V	BOT V	TOP W	BOT W
RTH	K14	K15	K16	K17	K18	K19

The following diagram gives you an indication of some values of VCEsat detection in relation to the RTH resistance in use.

	TCE	VTH1	VTH2
défaut	**10.4 µs**	**8.2 V**	**6.6 V**
180 KΩ	8.8 µs	6.9 V	4.8 V
82 KΩ	7.5 µs	5.6 V	3.5 V
39 KΩ	6.2 µs	4 V	2 V

Table 1 : Choice of RTH for the VCEsat detection parameters

6.10. Monitoring of auxiliary supplies

A monitoring of the supply values is directly realised on each output channel. If one of the two secondary supplies doesn't exceed 11.5V, the concerned channel is stopped and the default signal is activated.

As the hysteresis of the detection system is 0.7V, the re-start will only occur once the voltage has gone up again of about 12.2V.

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7. STANDARD CONFIGURATION

The standard configuration is as follows:

- HB mode
- Top/Bot mode
- Dead times : 5.5 µs
- Beginning of active clamping around 1020V for a 1200V module

Parameter		*Strap*								
		K1	KM1	KM2	KM3	KU5	KV5	KW5	K20	K21
Mode	DIRECT		1-2	1-2	1-2	2-3	2-3	2-3		
	HB TOP-BOT		2-3	2-3	2-3	1-2	1-2	1-2		
	HB INA-INB		2-3	2-3	2-3	2-3	2-3	2-3		
External Error	ACCOUNTED								OC	
	NOT ACCOUNTED								SC	
Overtemp	ACCOUNTED									OC
	NOT ACCOUNTED									SC
Shielding	NON	OC								
	YES	SC								

	R	C	Rth
U1	K2	K3	K14
U2	K4	K5	K15
V1	K6	K7	K16
V2	K8	K9	K17
W1	K10	K11	K18
W2	K12	K13	K19

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[i] The system is protected by zener and bipolar diodes. Exceeding these values can therefore lead to overheating and/or over consumption. Safe practice should be taken in case of use with large lengths of cable.

[ii] Available power at the output of DC/DC converters.

[iii] Direct voltage or peak value of the alternating voltage executed in a permanent way between the secondaries or between the secondary and the primary. This value can be increased to 1200VDC (or even more) owing to a partial loss of load test (which is not done in standard).

[iv] This value is given for 25KHz control signals.

[v] If the output power is exceeded, the DC/DC converter will be in an overload state.

[vi] This security aims at protecting the semi-conductors. Each secondary voltage is individually monitored.

[vii] This security aims at protecting the semi-conductors. Each secondary voltage is individually monitored.

[viii] Within the limit of maximum output power.

[ix] Can be adjusted by the user.

[x] With a load made up with a 5.6Ω resistor in series with a 39nF capacitor.

[xi] Can be adjusted by the user. The two values fit with the detection threshold at Tce and at continuous rating (about 15µs later).

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