

# IP4773CZ14

## VGA Interface with integrated buffer, ESD protection and termination resistor

Rev. 01 — 24 February 2009

Product data sheet

### 1. General description

---

The IP4773CZ14 is a VGA or DVI-I interface intended to be connected between a video transmitter such as a PC graphics card and a VGA or DVI-I receiver, such as a PC monitor. The IP4773CZ14 has ESD protection for the DDC lines, ESD protection plus buffering for the h-sync and v-sync lines and high-level ESD protection diodes for the R, G, B video signal lines.

The synchronizing signals are buffered by non-inverting buffers which can accept TTL-level input. The buffers convert TTL-level input to CMOS-level output which swings between  $V_{CC(SYNC)}$  and GND.

An external termination resistor can be added to achieve the desired termination, which is typically required for the h-sync and v-sync lines of the video interface.

The IP4773CZ14 has a typical output resistance ( $R_O$ ) of 10  $\Omega$ .

### 2. Features

---

- Integrated high-level ESD protection, buffering, sync-signal impedance matching
- All pin connections have integrated rail-to-rail clamping diodes providing downstream ESD protection of  $\pm 8$  kV according to IEC 61000-4-2, level 4
- Drivers for h-sync and v-sync lines
- Line capacitance < 4 pF per channel

### 3. Applications

---

Buffer and terminating channels, reduce EMI and RFI, and provide downstream ESD protection for:

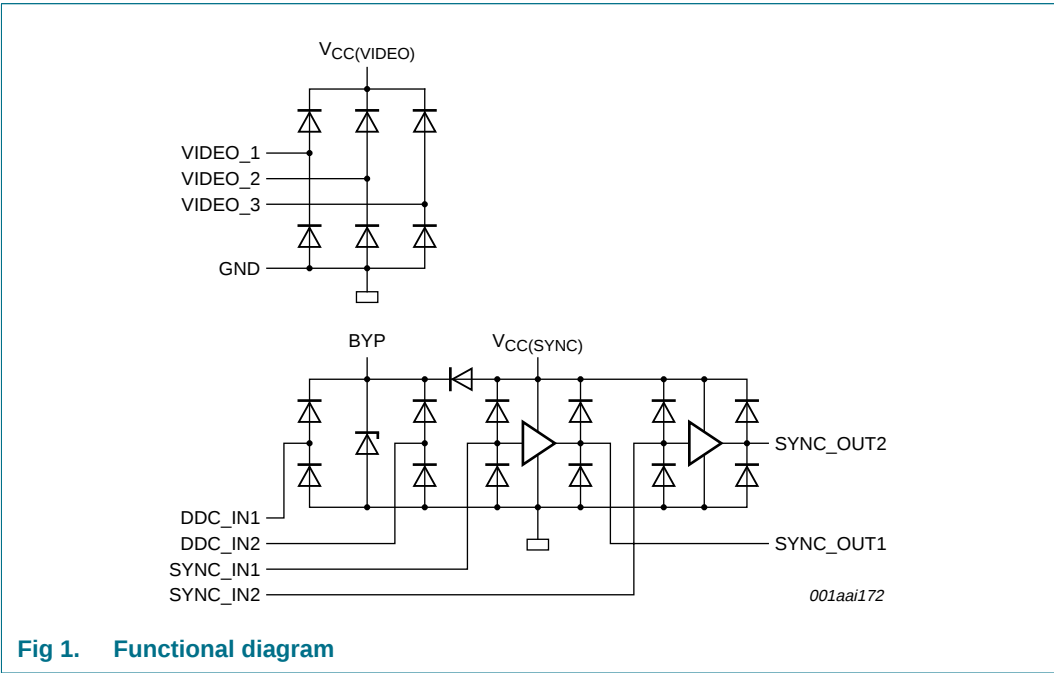
- VGA interfaces including DDC channels
- Desktop and notebook PCs, LCD TVs and PC monitors
- Graphics cards
- Set-top boxes
- Game consoles
- DVD players

4. Ordering information

Table 1. Ordering information

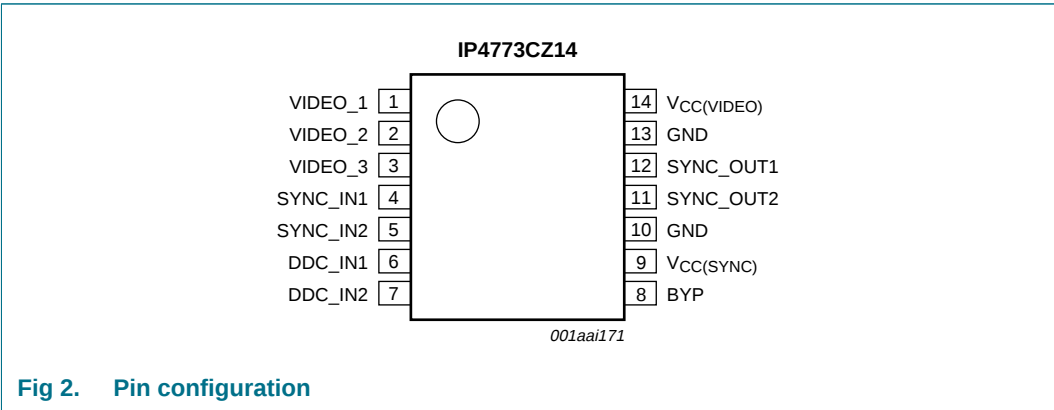
| Type number | Package |                                                                   | Version  |
|-------------|---------|-------------------------------------------------------------------|----------|
|             | Name    | Description                                                       |          |
| IP4773CZ14  | SSOP14  | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |

5. Functional diagram



6. Pinning information

6.1 Pinning



## 6.2 Pin description

**Table 2. Pin description**

| Symbol                 | Pin | Description                                                                                      |
|------------------------|-----|--------------------------------------------------------------------------------------------------|
| VIDEO_1                | 1   | ESD protection for video channel 1                                                               |
| VIDEO_2                | 2   | ESD protection for video channel 2                                                               |
| VIDEO_3                | 3   | ESD protection for video channel 3                                                               |
| SYNC_IN1               | 4   | sync signal input 1                                                                              |
| SYNC_IN2               | 5   | sync signal input 2                                                                              |
| DDC_IN1                | 6   | DDC signal input 1                                                                               |
| DDC_IN2                | 7   | DDC signal input 2                                                                               |
| BYP                    | 8   | for connecting a 100 nF bypass capacitor to increase ESD clamping performance of the DDC outputs |
| V <sub>CC(SYNC)</sub>  | 9   | supply voltage for sync buffer                                                                   |
| GND                    | 10  | ground                                                                                           |
| SYNC_OUT2              | 11  | sync signal output 2                                                                             |
| SYNC_OUT1              | 12  | sync signal output 1                                                                             |
| GND                    | 13  | ground                                                                                           |
| V <sub>CC(VIDEO)</sub> | 14  | supply voltage for video protection circuit                                                      |

## 7. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol                 | Parameter                       | Conditions                                                                                                 | Min       | Max                    | Unit |
|------------------------|---------------------------------|------------------------------------------------------------------------------------------------------------|-----------|------------------------|------|
| V <sub>CC(VIDEO)</sub> | video supply voltage            |                                                                                                            | GND – 0.5 | 5.5                    | V    |
| V <sub>CC(SYNC)</sub>  | synchronization supply voltage  |                                                                                                            | 3.0       | 5.5                    | V    |
| V <sub>I</sub>         | input voltage                   | pins VIDEO_1, VIDEO_2, VIDEO_3                                                                             | GND – 0.5 | V <sub>CC(VIDEO)</sub> | V    |
|                        |                                 | pins SYNC_IN1, SYNC_IN2, DDC_IN1, DDC_IN2                                                                  | GND – 0.5 | V <sub>CC(SYNC)</sub>  | V    |
| V <sub>ESD</sub>       | electrostatic discharge voltage | IEC 61000-4-2, level 4, contact                                                                            | [1] –8    | +8                     | kV   |
| P <sub>tot</sub>       | total power dissipation         | T <sub>amb</sub> = 25 °C;<br>f <sub>sync</sub> = 100 kHz,<br>C <sub>L</sub> = 6 nF, R <sub>L</sub> = 10 kΩ | -         | 50                     | mW   |
| T <sub>stg</sub>       | storage temperature             |                                                                                                            | –55       | +125                   | °C   |

- [1] Pins BYP, V<sub>CC(VIDEO)</sub> and V<sub>CC(SYNC)</sub> must be bypassed to GND via a low-impedance ground plane with 100 nF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between pins (VIDEO\_1, VIDEO\_2, VIDEO\_3, SYNC\_OUT1, SYNC\_OUT2) and GND.

## 8. Characteristics

**Table 4. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

| Symbol                    | Parameter                             | Conditions                                                                                                  | Min     | Typ | Max     | Unit          |
|---------------------------|---------------------------------------|-------------------------------------------------------------------------------------------------------------|---------|-----|---------|---------------|
| <b>Analog video (RGB)</b> |                                       |                                                                                                             |         |     |         |               |
| $I_{CC(VIDEO)}$           | supply current on pin $V_{CC(VIDEO)}$ | $V_{CC(VIDEO)} = 5.0\text{ V}$ ; static input signals                                                       | -       | -   | 10      | $\mu\text{A}$ |
| $C_{ch}$                  | channel capacitance                   | $V_{CC(VIDEO)} = 5.0\text{ V}$ ; $f = 1\text{ MHz}$ ; $V_I = 2.5\text{ V}$ (p-p); $V_{bias} = 2.5\text{ V}$ | [1] -   | -   | 4       | pF            |
| $I_I$                     | input current                         | $V_{CC(VIDEO)} = 5.0\text{ V}$ ; $V_I = V_{CC(VIDEO)}$ or GND                                               | -       | -   | $\pm 1$ | $\mu\text{A}$ |
| $V_{Fd}$                  | diode forward voltage                 | $I_F = 1\text{ mA}$                                                                                         | -       | 0.7 | -       | V             |
| <b>DDC</b>                |                                       |                                                                                                             |         |     |         |               |
| $C_{ch}$                  | channel capacitance                   | $f = 1\text{ MHz}$ ; $V_I = 2.5\text{ V}$ (p-p); $V_{bias} = 2.5\text{ V}$                                  | [1] -   | -   | 4       | pF            |
| $I_I$                     | input current                         | $V_I = 5.0\text{ V}$                                                                                        | -       | -   | $\pm 1$ | $\mu\text{A}$ |
| $V_{Fd}$                  | diode forward voltage                 | $I_F = 1\text{ mA}$                                                                                         | -       | 0.7 | -       | V             |
| <b>Sync buffer</b>        |                                       |                                                                                                             |         |     |         |               |
| $V_{CC(SYNC)}$            | synchronization supply voltage        |                                                                                                             | 3.0     | 5.0 | 5.5     | V             |
| $I_{CC(SYNC)}$            | supply current on pin $V_{CC(SYNC)}$  | $V_{CC(SYNC)} = 5.0\text{ V}$ ; static input signals                                                        | [2] -   | -   | 10      | $\mu\text{A}$ |
| $C_{ch}$                  | channel capacitance                   | $V_{CC(SYNC)} = 5.0\text{ V}$ ; $f = 1\text{ MHz}$ ; $V_{bias} = 1.65\text{ V}$                             | [1] -   | -   | 4       | pF            |
| $I_I$                     | input current                         | $V_{CC(SYNC)} = 5.0\text{ V}$ ; $V_I = V_{CC(SYNC)}$ or GND                                                 | -       | -   | $\pm 1$ | $\mu\text{A}$ |
| $V_{Fd}$                  | diode forward voltage                 | $I_F = 1\text{ mA}$                                                                                         | -       | 0.7 | -       | V             |
| $V_{IH}$                  | HIGH-level input voltage              | $V_{CC(SYNC)} = 5.0\text{ V}$                                                                               | [3] 2.0 | -   | -       | V             |
| $V_{IL}$                  | LOW-level input voltage               | $V_{CC(SYNC)} = 5.0\text{ V}$                                                                               | [3] -   | -   | 0.6     | V             |
| $V_{OH}$                  | HIGH-level output voltage             | $V_{CC(SYNC)} = 5.0\text{ V}$ ; $I_{OH} = 24\text{ mA}$                                                     | [3] 2.0 | -   | -       | V             |
| $V_{OL}$                  | LOW-level output voltage              | $V_{CC(SYNC)} = 5.0\text{ V}$ ; $I_{OL} = 24\text{ mA}$                                                     | [3] -   | -   | 0.8     | V             |
| $R_O$                     | output resistance                     |                                                                                                             | [3] -   | 10  | -       | $\Omega$      |
| $t_{PLH}$                 | LOW to HIGH propagation delay         | $V_{CC(SYNC)} = 5.0\text{ V}$ ; $C_L = 50\text{ pF}$ ; $t_{r(i)}$ and $t_{f(i)} \leq 5\text{ ns}$           | [1] -   | -   | 12      | ns            |
| $t_{PHL}$                 | HIGH to LOW propagation delay         | $V_{CC(SYNC)} = 5.0\text{ V}$ ; $C_L = 50\text{ pF}$ ; $t_{r(i)}$ and $t_{f(i)} \leq 5\text{ ns}$           | [1] -   | -   | 12      | ns            |
| $t_{r(o)}$                | output rise time                      | $V_{CC(SYNC)} = 5.0\text{ V}$ ; $C_L = 50\text{ pF}$ ; $t_{r(i)}$ and $t_{f(i)} \leq 5\text{ ns}$           | -       | 4   | -       | ns            |
| $t_{f(o)}$                | output fall time                      | $V_{CC(SYNC)} = 5.0\text{ V}$ ; $C_L = 50\text{ pF}$ ; $t_{r(i)}$ and $t_{f(i)} \leq 5\text{ ns}$           | -       | 4   | -       | ns            |

[1] Guaranteed by design and characterization.

[2] Sync buffer outputs unloaded.

[3] Applies only to the Sync buffer; note that  $R_O = R_{buffer}$ .

## 9. Application information

### 9.1 Connections

The IP4773CZ14 should be placed as close as possible to the VGA or DVI-I interface connector. The ESD-protected channels on pins VIDEO\_1, VIDEO\_2 and VIDEO\_3 can be connected in any order to R, G, B signals. The sync buffers are equivalent and can be connected to either h-sync or v-sync signals.

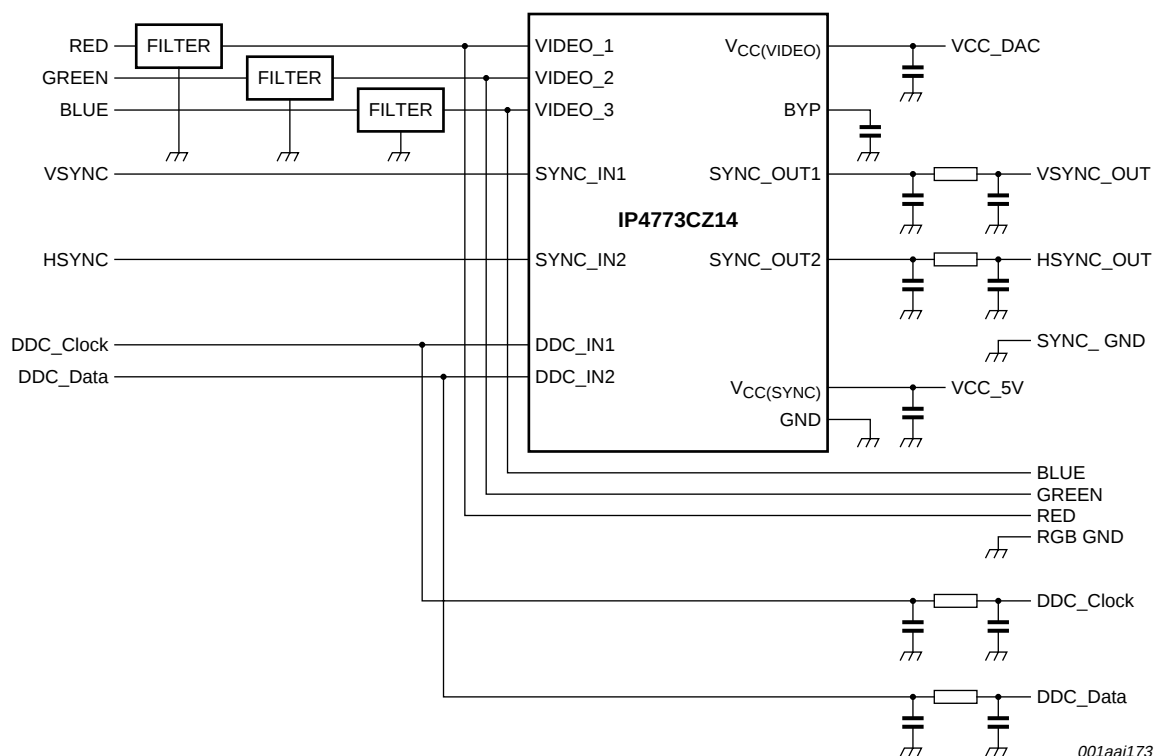


Fig 3. Transmitter application

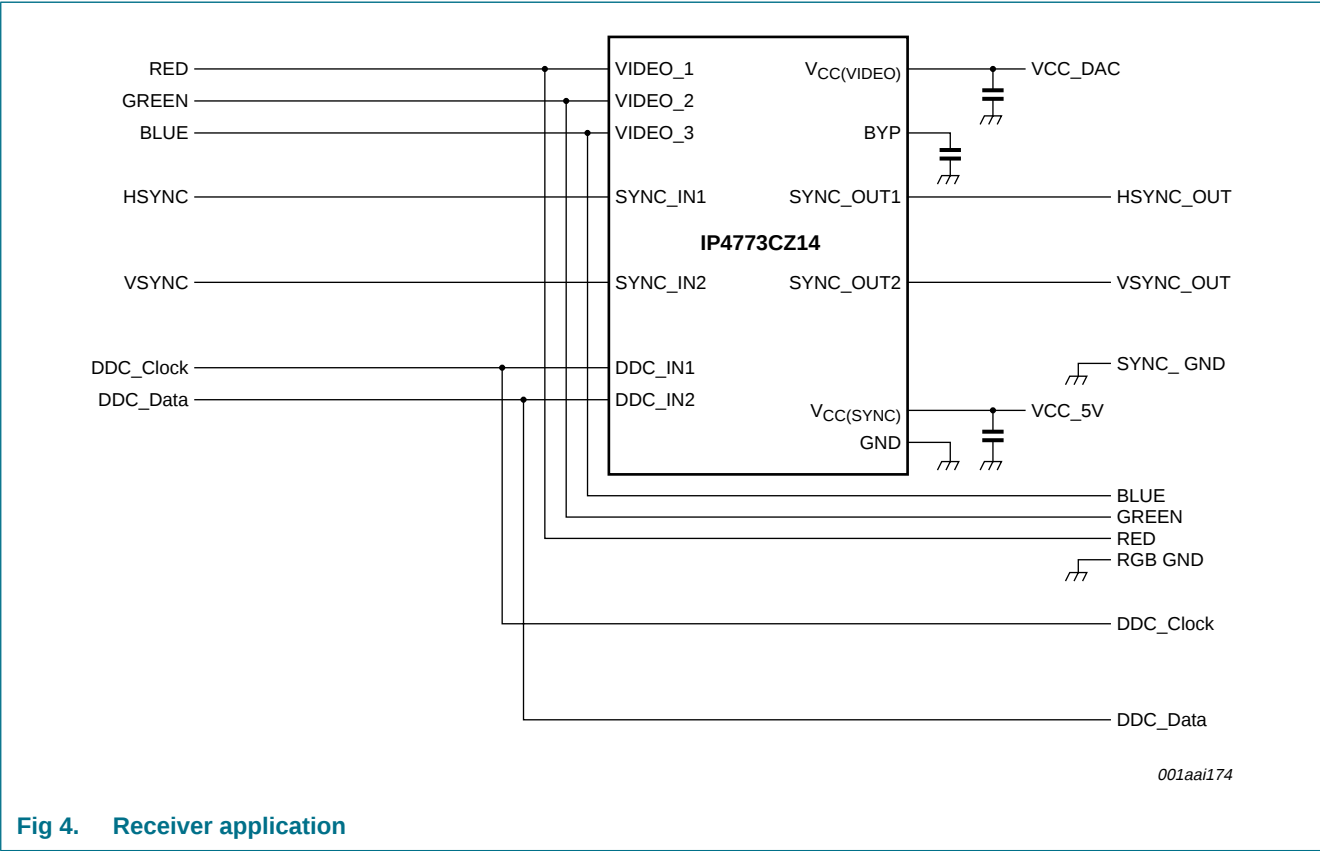


Fig 4. Receiver application

The receiver application simplifies VGA input circuit applications.

10. Package outline

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm SOT337-1

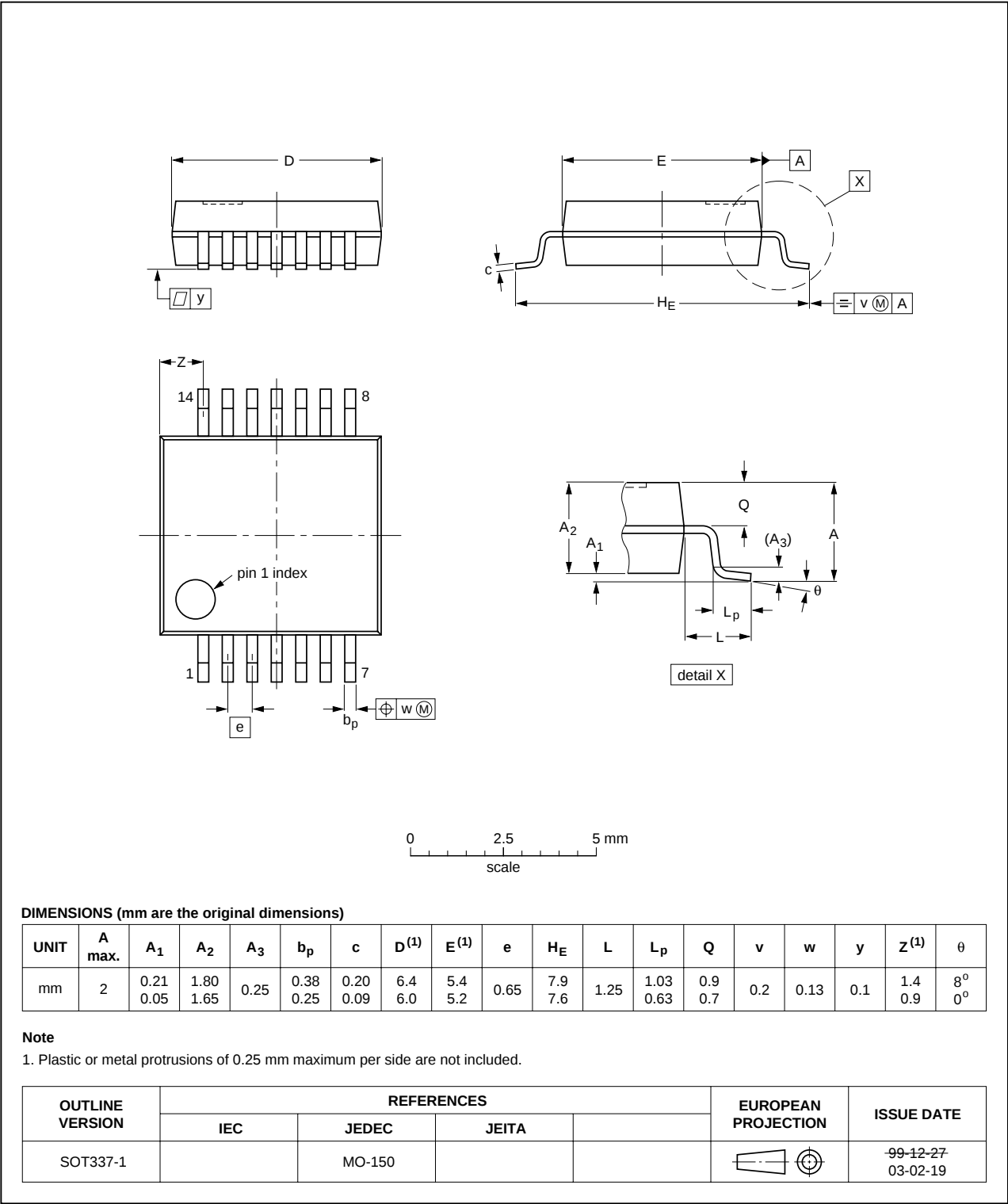


Fig 5. Package outline SOT337-1 (SSOP14)

## 11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 6](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 5](#) and [6](#)

**Table 5. SnPb eutectic process (from J-STD-020C)**

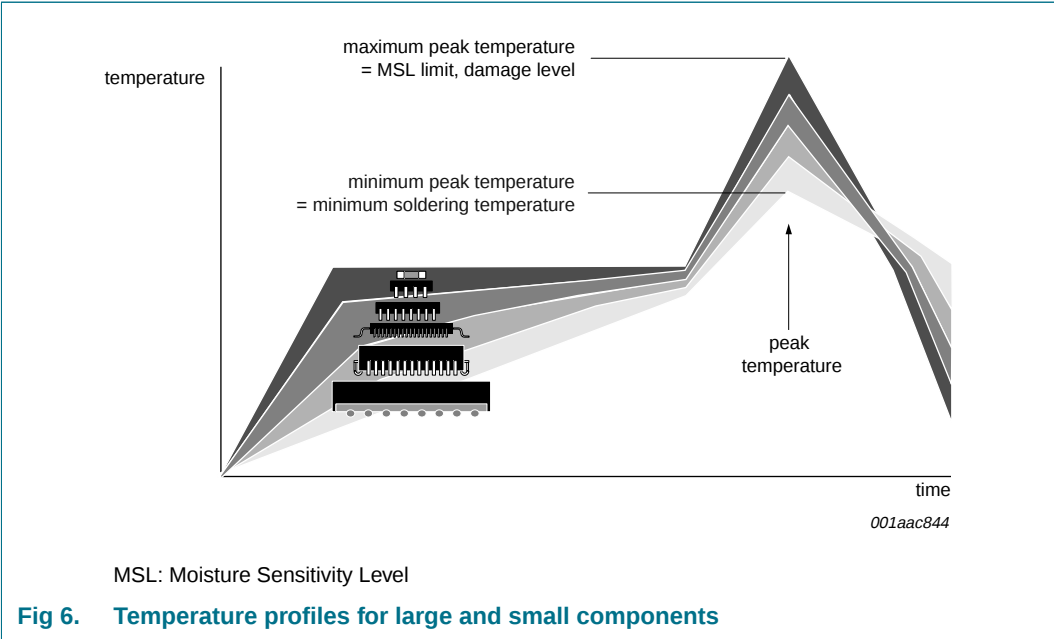
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 6. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 6](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

12. Abbreviations

Table 7. Abbreviations

| Acronym | Description                                              |
|---------|----------------------------------------------------------|
| DDC     | Display Data Channel                                     |
| DVI-I   | Digital Visual Interface Integrated (Analog and Digital) |
| EMI     | ElectroMagnetic Interference                             |
| ESD     | ElectroStatic Discharge                                  |
| RGB     | Red, Green, Blue                                         |
| RFI     | Radio Frequency Interference                             |
| TTL     | Transistor-Transistor Logic                              |
| VGA     | Video Graphics Array                                     |

13. Revision history

Table 8. Revision history

| Document ID  | Release date | Data sheet status  | Change notice | Supersedes |
|--------------|--------------|--------------------|---------------|------------|
| IP4773CZ14_1 | 20090224     | Product data sheet | -             | -          |

## 14. Legal information

### 14.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 14.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 14.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 15. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 16. Contents

|           |                                        |           |
|-----------|----------------------------------------|-----------|
| <b>1</b>  | <b>General description</b> .....       | <b>1</b>  |
| <b>2</b>  | <b>Features</b> .....                  | <b>1</b>  |
| <b>3</b>  | <b>Applications</b> .....              | <b>1</b>  |
| <b>4</b>  | <b>Ordering information</b> .....      | <b>2</b>  |
| <b>5</b>  | <b>Functional diagram</b> .....        | <b>2</b>  |
| <b>6</b>  | <b>Pinning information</b> .....       | <b>2</b>  |
| 6.1       | Pinning .....                          | 2         |
| 6.2       | Pin description .....                  | 3         |
| <b>7</b>  | <b>Limiting values</b> .....           | <b>3</b>  |
| <b>8</b>  | <b>Characteristics</b> .....           | <b>4</b>  |
| <b>9</b>  | <b>Application information</b> .....   | <b>5</b>  |
| 9.1       | Connections .....                      | 5         |
| <b>10</b> | <b>Package outline</b> .....           | <b>7</b>  |
| <b>11</b> | <b>Soldering of SMD packages</b> ..... | <b>8</b>  |
| 11.1      | Introduction to soldering .....        | 8         |
| 11.2      | Wave and reflow soldering .....        | 8         |
| 11.3      | Wave soldering .....                   | 8         |
| 11.4      | Reflow soldering .....                 | 9         |
| <b>12</b> | <b>Abbreviations</b> .....             | <b>10</b> |
| <b>13</b> | <b>Revision history</b> .....          | <b>10</b> |
| <b>14</b> | <b>Legal information</b> .....         | <b>11</b> |
| 14.1      | Data sheet status .....                | 11        |
| 14.2      | Definitions .....                      | 11        |
| 14.3      | Disclaimers .....                      | 11        |
| 14.4      | Trademarks .....                       | 11        |
| <b>15</b> | <b>Contact information</b> .....       | <b>11</b> |
| <b>16</b> | <b>Contents</b> .....                  | <b>12</b> |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

founded by

**PHILIPS**

© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 24 February 2009

Document identifier: IP4773CZ14\_1