PCF85134

Universal 60 x 4 LCD segment driver for multiplex rates up to 1:4

Rev. 2 — 25 July 2011   **Product data sheet**

1. General description

The PCF85134 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 60 segments. It can be easily cascaded for larger LCD applications. The PCF85134 is compatible with most microcontrollers and communicates via the two-line bidirectional I^{2}C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).
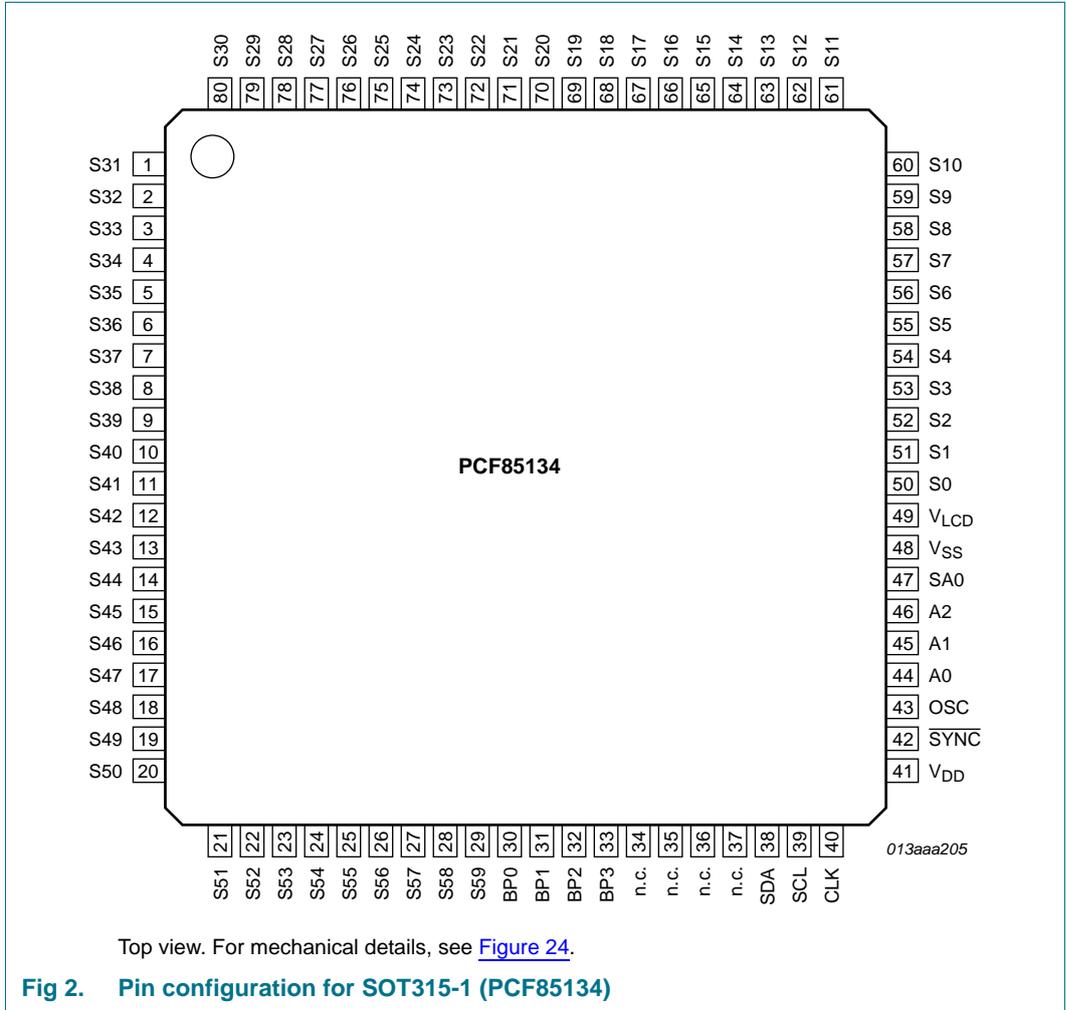
2. Features and benefits

- Single-chip LCD controller and driver
- Selectable backplane drive configurations: static, 2, 3, or 4 backplane multiplexing
- 60 segment outputs allowing to drive:
  - ◆ 30 7-segment alphanumeric characters
  - ◆ 15 14-segment alphanumeric characters
  - ◆ Any graphics of up to 240 elements
- Cascading supported for larger applications
- 60×4-bit display data storage RAM
- Wide LCD supply range: from 2.5 V for low threshold LCDs up to 6.5 V for high threshold twisted nematic LCDs
- Internal LCD bias generation with voltage follower buffers
- Selectable display bias configurations: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Wide logic power supply range: from 1.8 V to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption
- 400 kHz I^{2}C-bus interface
- No external components required
- Display memory bank switching in static and duplex drive mode
- Versatile blinking modes
- Silicon gate CMOS process

---

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 17.

3. Ordering information

Table 1.   Ordering information

Type number	Package				
	Name	**Description**		**Delivery form**	**Version**
PCF85134HL/1	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm		tape and reel	SOT315-1

4. Marking

Table 2.   Marking codes

Type number	Marking code
PCF85134HL/1	PCF85134HL

5. Block diagram

Fig 1.   Block diagram of PCF85134

PCF85134

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet

Rev. 2 — 25 July 2011

2 of 45

6. Pinning information

6.1 Pinning

Top view. For mechanical details, see Figure 24.

Fig 2. Pin configuration for SOT315-1 (PCF85134)

6.2 Pin description

Table 3. **Pin description**

Symbol	Pin	Type	Description
S31 to S59	1 to 29	output	LCD segment output 31 to 59
BP0 to BP3	30 to 33	output	LCD backplane output 0 to 3
n.c.	34 to 37	-	not connected; do not connect and do not use as feed through
SDA	38	input/output	I^{2}C-bus serial data input and output
SCL	39	input	I^{2}C-bus serial clock input
CLK	40	input/output	external clock input and internal clock output
V_{DD}	41	supply	supply voltage
$\overline{SYNC}$	42	input/output	cascade synchronization input and output (active LOW)
OSC	43	input	enable input for internal oscillator
A0 to A2	44 to 46	input	subaddress counter input 0 to 2
SA0	47	input	I^{2}C-bus slave address input 0
V_{SS}	48	supply	ground supply voltage
V_{LCD}	49	supply	input of LCD supply voltage
S0 to S30	50 to 80	output	LCD segment output 0 to 30

PCF85134

Product data sheet **Rev. 2 — 25 July 2011** **4 of 45**

7. Functional description

The PCF85134 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 3). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 60 segments.

The display configurations possible with the PCF85134 depend on the required number of active backplane outputs. A selection of display configurations is given in Table 4.

All of the display configurations given in Table 4 can be implemented in a typical system as shown in Figure 4.

dot matrix

7-segment with dot   14-segment with dot and accent

013aaa312
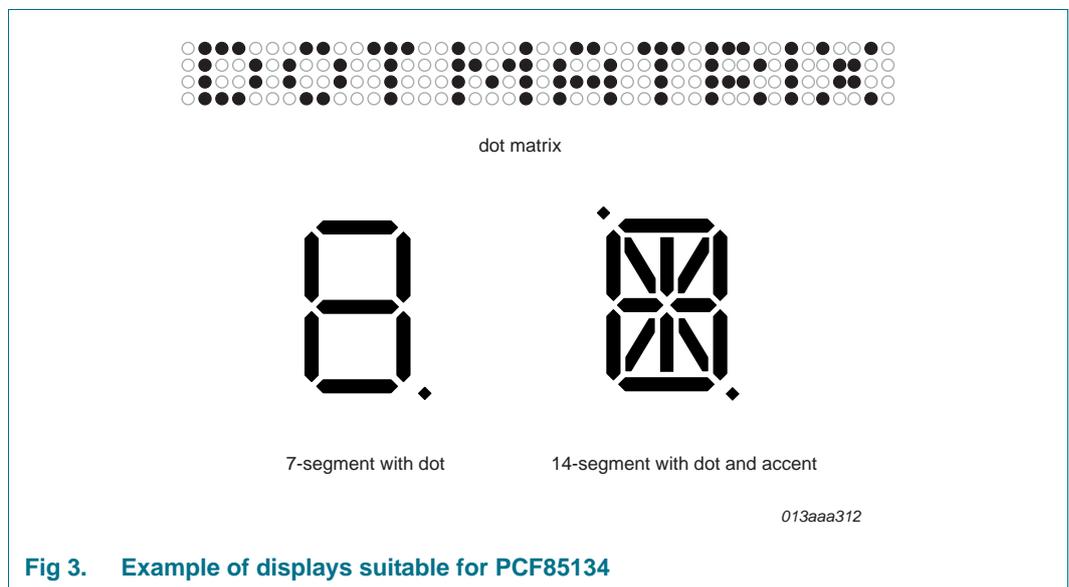
Fig 3.   Example of displays suitable for PCF85134

Table 4.   Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/ Elements**
		7-segment[1]	**14-segment**[2]	
4	240	30	15	240 (4 × 60)
3	180	22	11	180 (3 × 60)
2	120	15	7	120 (2 × 60)
1	60	7	3	60 (1 × 60)

[1]   7-segment display has eight elements including the decimal point.

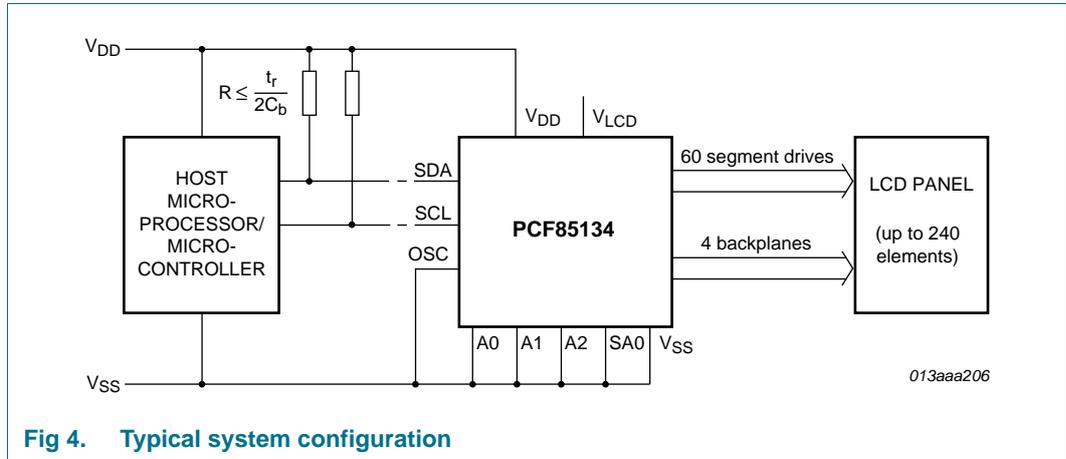[2]   14-segment display has 16 elements including decimal point and accent dot.

Fig 4.   Typical system configuration

The host microcontroller maintains the 2-line I2C-bus communication channel with the PCF85134.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (pins V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel selected for the application.

7.1 Power-On Reset (POR)

At power-on the PCF85134 resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- Display is disabled

Remark: Do not transfer data on the I2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three impedances connected in series between V_{LCD} and V_{SS}. If the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex drive mode configuration is selected, the center impedance is bypassed by switch. The LCD voltage can be temperature compensated externally, using the supply to pin V_{LCD}.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 5.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 5.   Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\dfrac{V_{off(RMS)}}{V_{LCD}}$	$\dfrac{V_{on(RMS)}}{V_{LCD}}$	$D = \dfrac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	**Levels**				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\dfrac{1}{1+a}$, where the values for a are

  a = 1 for $\frac{1}{2}$ bias

  a = 2 for $\frac{1}{3}$ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \tag{1}$$

where the values for n are

  n = 1 for static drive mode

  n = 2 for 1:2 multiplex drive mode

  n = 3 for 1:3 multiplex drive mode

  n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1+a)^2}} \tag{2}$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

PCF85134

Product data sheet **Rev. 2 — 25 July 2011** **7 of 45**

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \qquad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$

- 1:4 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3 V_{off(RMS)}$ when $\frac{1}{3}$ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determines the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 5. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \qquad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \qquad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer.

It is important to match the module properties to those of the driver in order to achieve optimum performance.
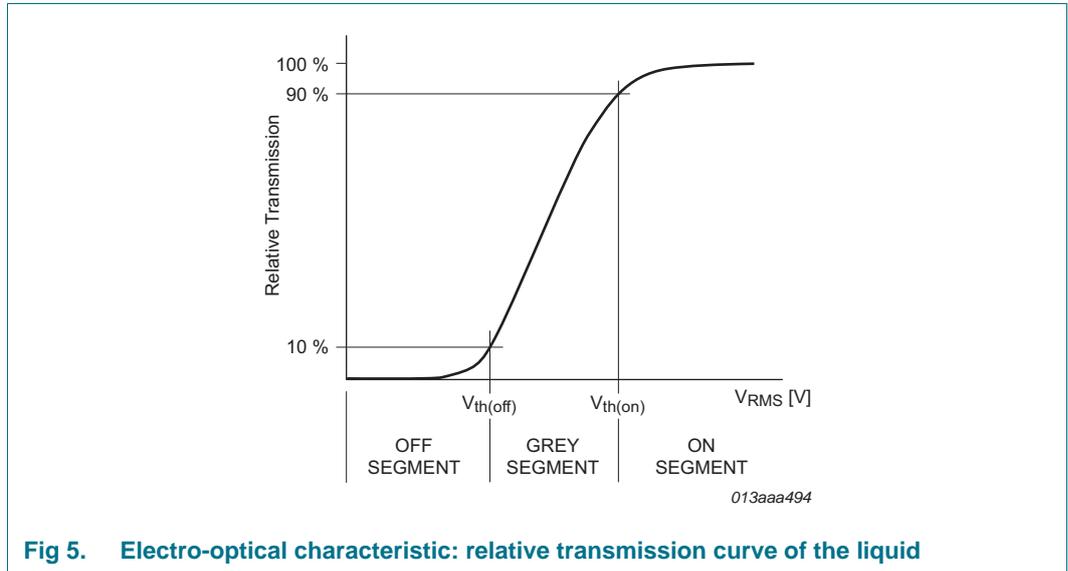
PCF85134

Product data sheet **Rev. 2 — 25 July 2011** **8 of 45**

Fig 5.   Electro-optical characteristic: relative transmission curve of the liquid

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 6.
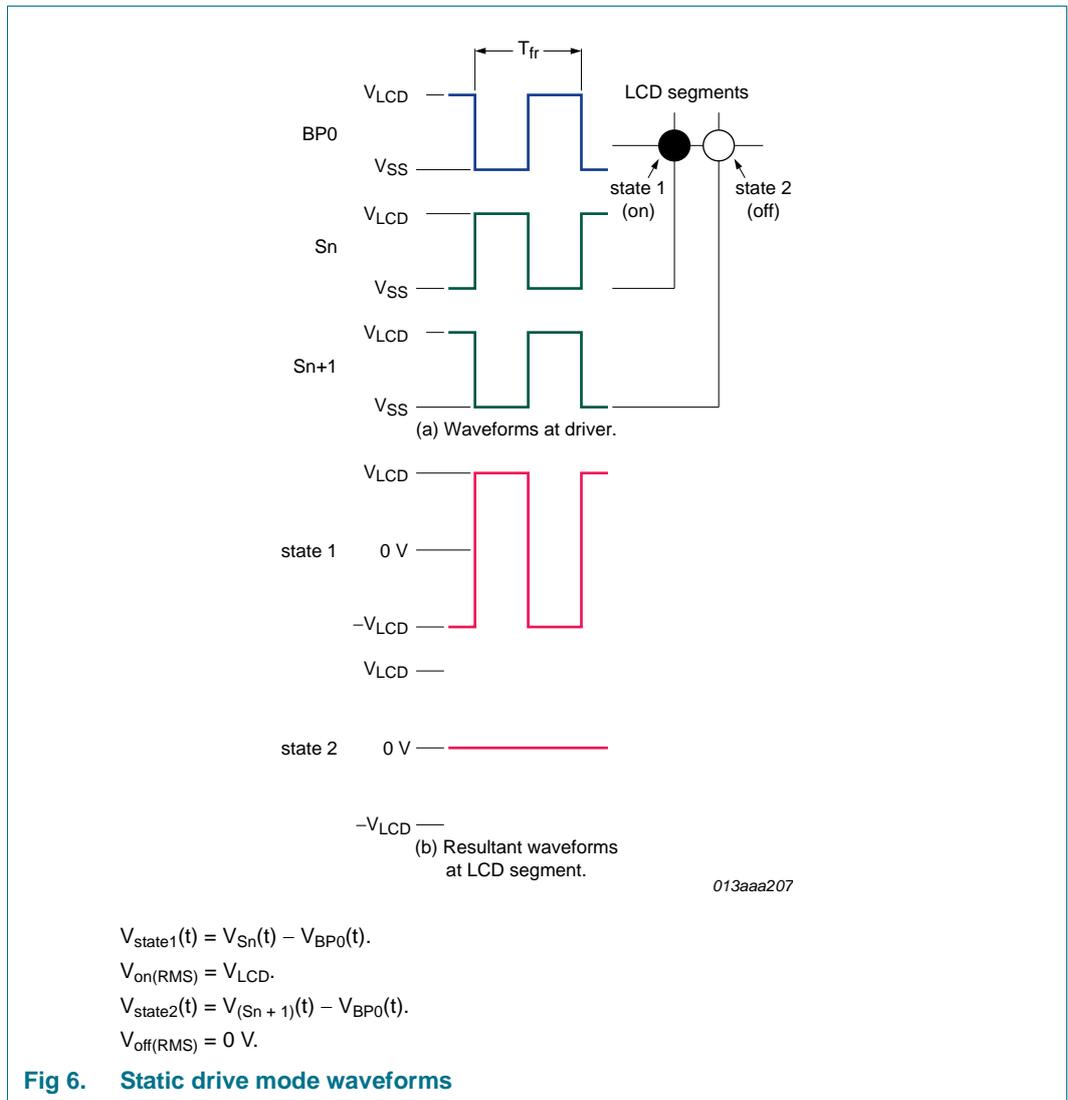

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 6. **Static drive mode waveforms**

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF85134 allows the use of $\frac{1}{2}$ bias or $\frac{1}{3}$ bias in this mode as shown in Figure 7 and Figure 8.

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$

$V_{on(RMS)} = 0.791 V_{LCD}.$

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t).$

$V_{off(RMS)} = 0.354 V_{LCD}.$
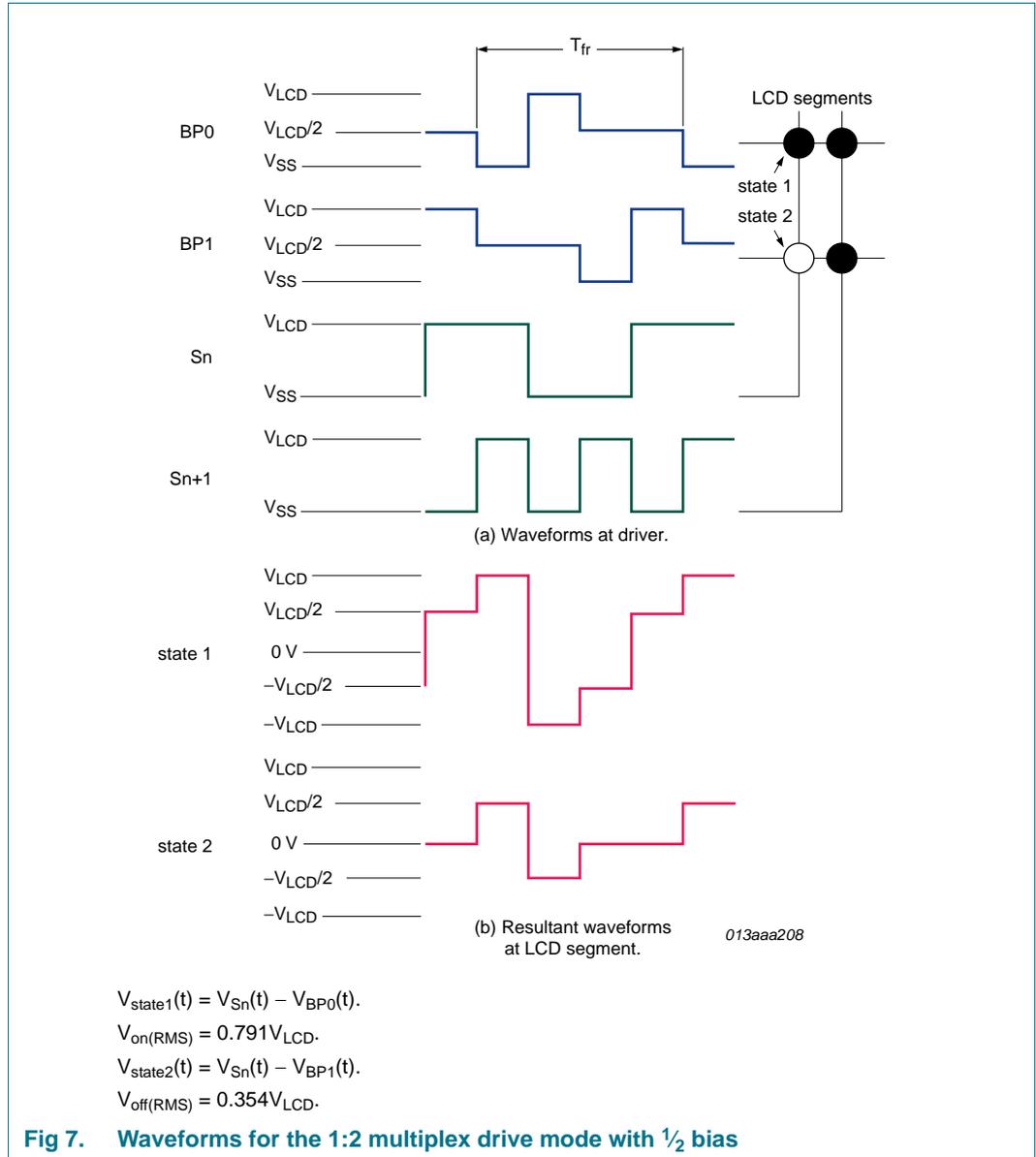
Fig 7.   Waveforms for the 1:2 multiplex drive mode with $\frac{1}{2}$ bias

(a) Waveforms at driver.

(b) Resultant waveforms at LCD segment.

013aaa209

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745 V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333 V_{LCD}$.
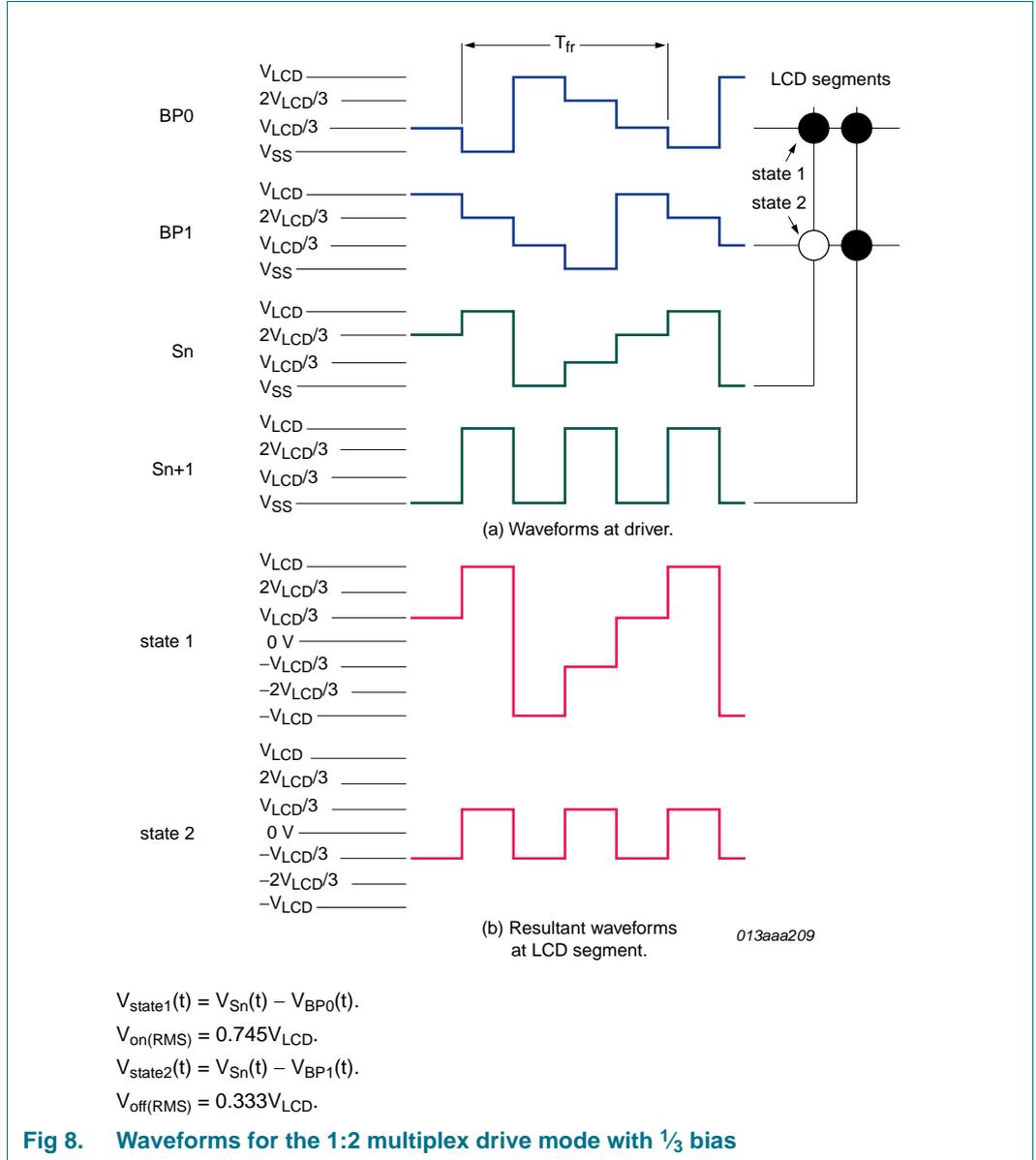
Fig 8.   **Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias**

7.4.3 1:3 Multiplex drive mode

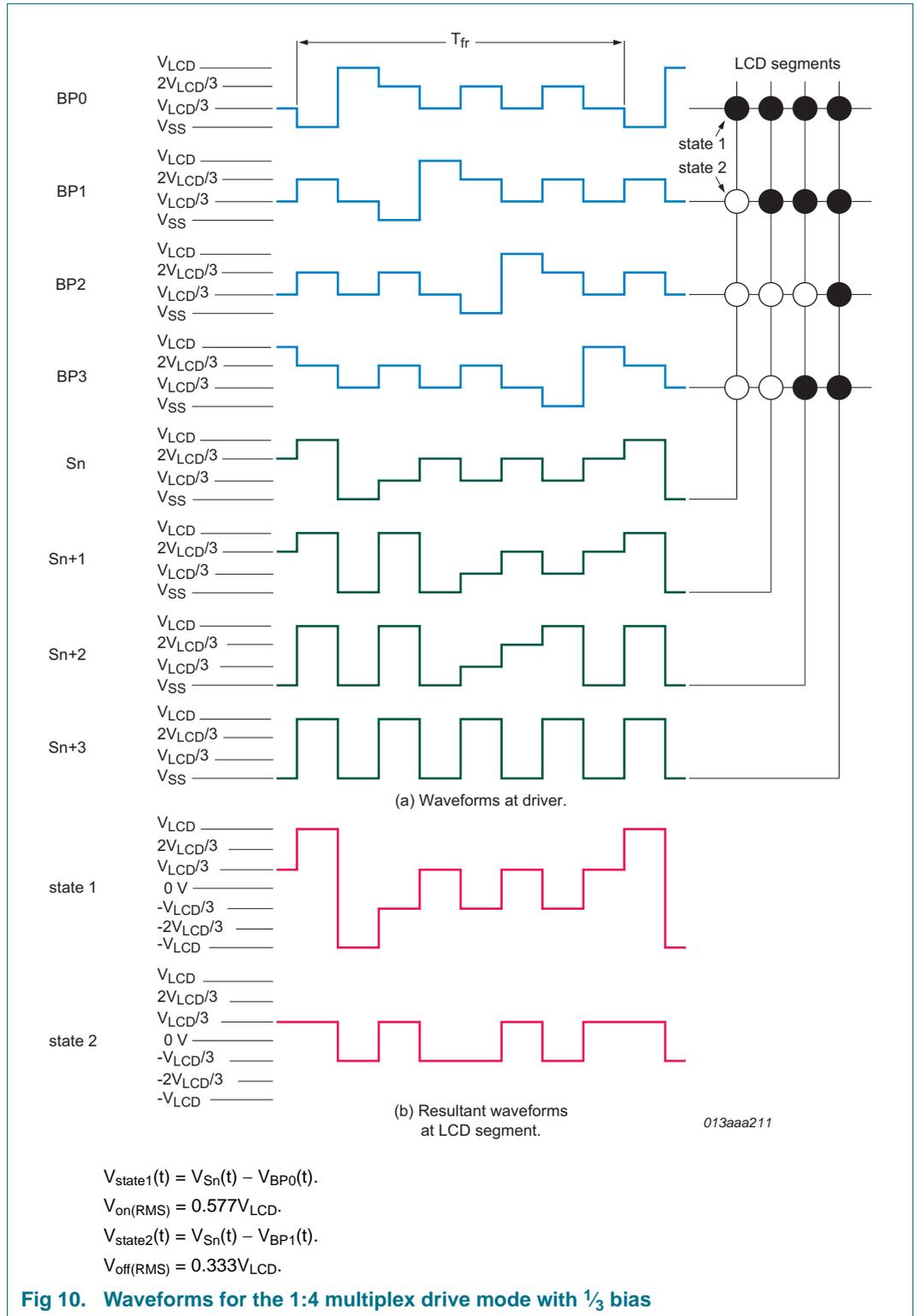When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 9.

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$

$V_{on(RMS)} = 0.638V_{LCD}.$

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t).$

$V_{off(RMS)} = 0.333V_{LCD}.$
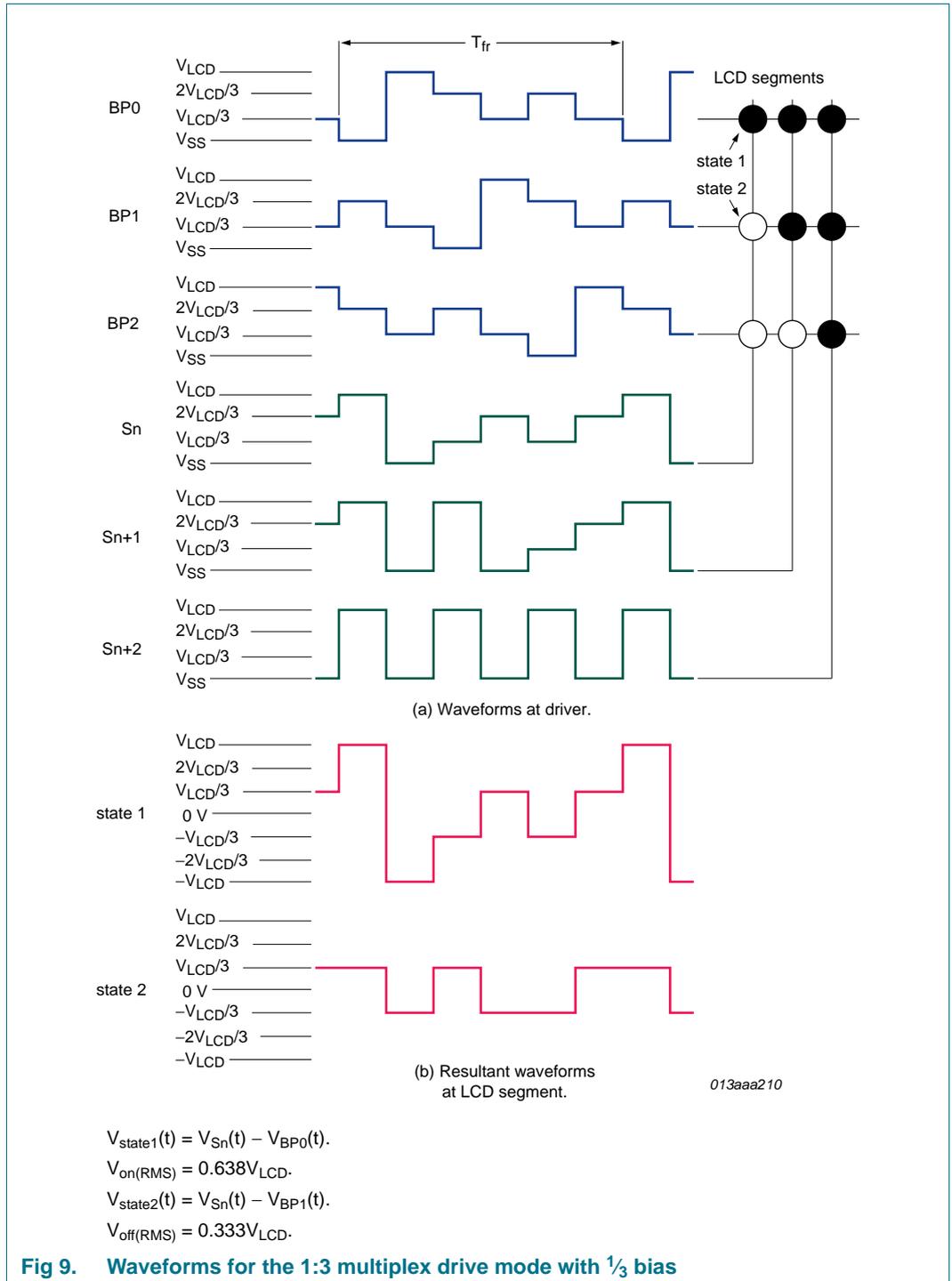
Fig 9.   Waveforms for the 1:3 multiplex drive mode with $\frac{1}{3}$ bias

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 10.

(a) Waveforms at driver.

(b) Resultant waveforms at LCD segment.

013aaa211

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$

$V_{on(RMS)} = 0.577V_{LCD}.$

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t).$

$V_{off(RMS)} = 0.333V_{LCD}.$

Fig 10. Waveforms for the 1:4 multiplex drive mode with $\frac{1}{3}$ bias

7.5 Oscillator

The internal logic and the LCD drive signals of the PCF85134 are timed by the frequency f_{clk}. It equals either the built-in oscillator frequency f_{osc} or the external clock frequency $f_{clk(ext)}$. The clock frequency f_{clk} determines the LCD frame frequency (f_{fr}).

7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. In this case, the output from pin CLK is the clock signal for any cascaded PCF85134 in the system.

7.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

Remark: A clock signal must always be supplied to the device. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing and frame frequency

The PCF85134 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF85134 in the system is maintained by the synchronization signal at pin $\overline{SYNC}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock.

Table 6.   LCD frame frequencies

Operating mode ratio	Frame frequency with respect to f_{clk} (typical)	Unit
	$f_{clk} = 1970$ Hz	
$f_{fr} = \dfrac{f_{clk}}{24}$	82	Hz

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.8 Segment outputs

The LCD drive section includes 60 segment outputs (S0 to S59) which should be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less than 60 segment outputs are required, the unused segment outputs must be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode BP0 and BP2, respectively, BP1 and BP3 carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

The display RAM is a static 60×4-bit RAM which stores LCD data. A logic 1 in the RAM bit map indicates the on-state ($V_{on(RMS)}$) of the corresponding LCD element. Similarly, a logic 0 indicates the off-state ($V_{off(RMS)}$). For more information on $V_{on(RMS)}$ and $V_{off(RMS)}$, see Section 7.3.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

The display RAM bit map, Figure 11, shows row 0 to row 3 which correspond with the backplane outputs BP0 to BP3, and column 0 to column 59 which correspond with the segment outputs S0 to S59. In multiplexed LCD applications, the data of each row of the display RAM is time-multiplexed with the corresponding backplane (row 0 with BP0, row 1 with BP1, and so on).

The display RAM bit map shows the direct relationship between the display RAM addresses and the segment outputs and between the bits in a RAM word and the backplane outputs.

Fig 11. Display RAM bit map

PCF85134

Product data sheet **Rev. 2 — 25 July 2011** **16 of 45**

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte

static

display RAM address/segment outputs (s) — byte1

rows (BP)	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
0	c	b	a	f	g	e	d	DP
1	x	x	x	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x	x

MSB ... LSB: c b a f g e d DP

1:2 multiplex

display RAM address/segment outputs (s) — byte1

rows (BP)	n	n+1	n+2	n+3
0	a	f	e	d
1	b	g	c	DP
2	x	x	x	x
3	x	x	x	x

MSB ... LSB: a b f g e c d DP

1:3 multiplex

display RAM address/segment outputs (s) — byte1

rows (BP)	n	n+1	n+2
0	b	a	f
1	DP	d	e
2	c	g	x
3	x	x	x

MSB ... LSB: b DP c a d g f e

1:4 multiplex

display RAM address/segment outputs (s) — byte1

rows (BP)	n	n+1
0	a	f
1	c	e
2	b	g
3	DP	d

MSB ... LSB: a c b DP f e g d

001aaj646

x = data bit unchanged.

Fig 12. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

When display data is transmitted to the PCF85134, the display bytes received are stored in the display RAM in accordance with the selected LCD multiplex drive mode. The data is stored as it arrives and depending on the current multiplex drive mode, data is stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 12. The RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 12:

- In static drive mode the eight transmitted data bits are placed into row 0 as one byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and row 1 as two successive 4-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, row 1, and row 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address. But care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 7.10.3).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, row 1, row 2, and row 3 as two successive 4-bit RAM words.

7.10.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 10). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 12. After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I^{2}C-bus data access terminates early, then the state of the data pointer is unknown. Consequently, the data pointer must be rewritten before further RAM accesses.

7.10.2 Subaddress counter

The storage of display data is determined by the content of the subaddress counter. Storage is allowed only when the content of the subaddress counter matches with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 13). If the content of the subaddress counter and the hardware subaddress do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

PCF85134

Product data sheet **Rev. 2 — 25 July 2011** **18 of 45**

In cascaded applications each PCF85134 in the cascade must be addressed separately. Initially, the first PCF85134 is selected by sending the device-select command matching the first hardware subaddress. Then the data pointer is set to the preferred display RAM address by sending the load-data-pointer command.

Once the display RAM of the first PCF85134 has been written, the second PCF85134 is selected by sending the device-select command again. This time however the command matches the hardware subaddress of the second device. Next the load-data-pointer command is sent to select the preferred display RAM address of the second PCF85134.

This last step is very important because during writing data to the first PCF85134, the data pointer of the second PCF85134 is incremented. In addition, the hardware subaddress should not be changed while the device is being accessed on the I²C-bus interface.

7.10.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 7 (see Figure 12 as well).

Table 7.   Standard RAM filling in 1:3 multiplex drive mode
*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are not connected** to any elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 8.

Table 8.   Entire RAM filling by rewriting in 1:3 multiplex drive mode
*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are connected** to elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 8 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8, and so on, have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written.

- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6.

- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6.

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used. But it has to be considered in the module layout process as well as in the driver software design.

7.10.4 Bank selector

7.10.4.1 Output bank selector

The output bank selector (see Table 14) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The $\overline{\text{SYNC}}$ signal resets these sequences to the following starting points:

- row 3 for 1:4 multiplex
- row 2 for 1:3 multiplex
- row 1 for 1:2 multiplex
- row 0 for static mode

The PCF85134 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.10.4.2 Input bank selector

The input bank selector loads display data into the display data in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 14). The input bank selector functions independently to the output bank selector.

7.11 Blinking

The display blinking capabilities of the PCF85134 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 15). The blink frequencies are derived from the clock frequency. The ratio between the clock and blink frequency depends on the blink mode selected (see Table 9).

Table 9.   Blink frequencies

Blink mode	Operating mode ratio	Blink frequency with respect to f_{clk} (typical) f_{clk} = 1970 Hz	Unit
off	-	blinking off	Hz
1	$f_{blink} = \dfrac{f_{clk}}{768}$	2.5	Hz
2	$f_{blink} = \dfrac{f_{clk}}{1536}$	1.3	Hz
3	$f_{blink} = \dfrac{f_{clk}}{3072}$	0.6	Hz

An additional feature is for an arbitrary selection of LCD segments to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. With the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD elements can blink by selectively changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 11).

7.12 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. There are five commands:

Table 10.   Definition of commands

Command	Operation code								Reference
Bit	7	6	5	4	3	2	1	0	
mode-set	1	1	0	0	E	B	M[1:0]		Table 11
load-data-pointer	0	P[6:0]							Table 12
device-select	1	1	1	0	0	A[2:0]			Table 13
bank-select	1	1	1	1	1	0	I	O	Table 14
blink-select	1	1	1	1	0	AB	BF[1:0]		Table 15

Table 11. **Mode-set command bit description**

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status**
		0[1]	disabled (blank)[2]
		1	enable
2	B		**LCD bias configuration**[3]
		0[1]	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; one backplane
		10	1:2 multiplex; two backplanes
		11	1:3 multiplex; three backplanes
		00[1]	1:4 multiplex; four backplanes

[1] Default value.

[2] The possibility to disable the display allows implementation of blinking under external control.

[3] Not applicable for static drive mode.

Table 12. **Load-data-pointer command bit description**
See Section 7.10.1 on page 18.

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	0000000[1] to 0111011	7-bit binary value, 0 to 59; transferred to the data pointer to define one of 60 display RAM addresses

[1] Default value.

Table 13. **Device-select command bit description**
See Section 7.10.2 on page 18.

Bit	Symbol	Value	Description
7 to 3	-	11100	fixed value
2 to 0	A[2:0]	000[1] to 111	3-bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

[1] Default value.

Table 14. Bank-select command bit description
See Section 7.10.4 on page 20.

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7 to 2	-	111110	fixed value	
1	I		**input bank selection**: storage of arriving display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		**output bank selection**: retrieval of LCD display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 or 1:4 multiplex drive modes.

[2] Default value.

Table 15. Blink-select command bit description
See Section 7.11 on page 20.

Bit	Symbol	Value	Description
7 to 3	-	11110	fixed value
2	AB		**blink mode selection**
		0[1]	normal blinking[2]
		1	alternate RAM bank blinking[3]
1 to 0	BF[1:0]		**blink frequency selection**[4]
		00[1]	off
		01	1
		10	2
		11	3

[1] Default value.

[2] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[3] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

[4] For the blink frequencies, see Table 9.

7.13 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF85134 and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

PCF85134

Product data sheet **Rev. 2 — 25 July 2011** **23 of 45**

8. Characteristics of the I^{2}C-bus

The I^{2}C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 13.

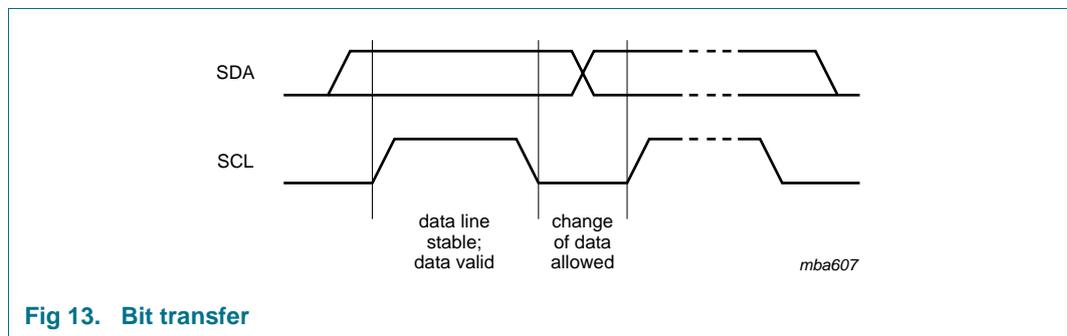**Fig 13. Bit transfer**

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P).

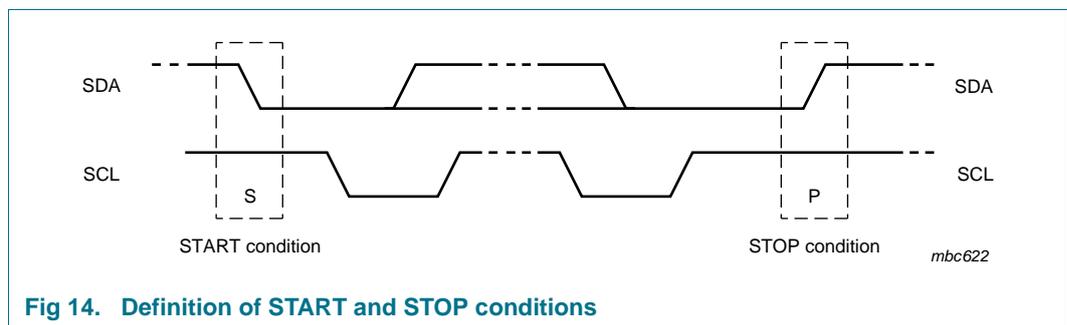The START and STOP conditions are illustrated in Figure 14.

Fig 14. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 15.
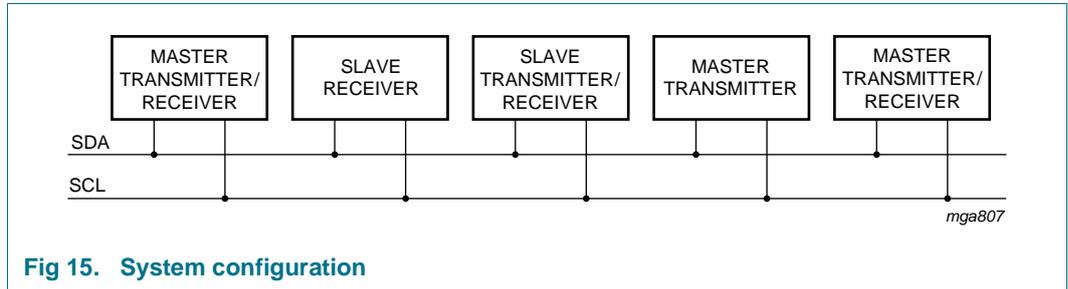
PCF85134

© NXP B.V. 2011. All rights reserved.

Product data sheet **Rev. 2 — 25 July 2011** **24 of 45**

Fig 15. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.

- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).

- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

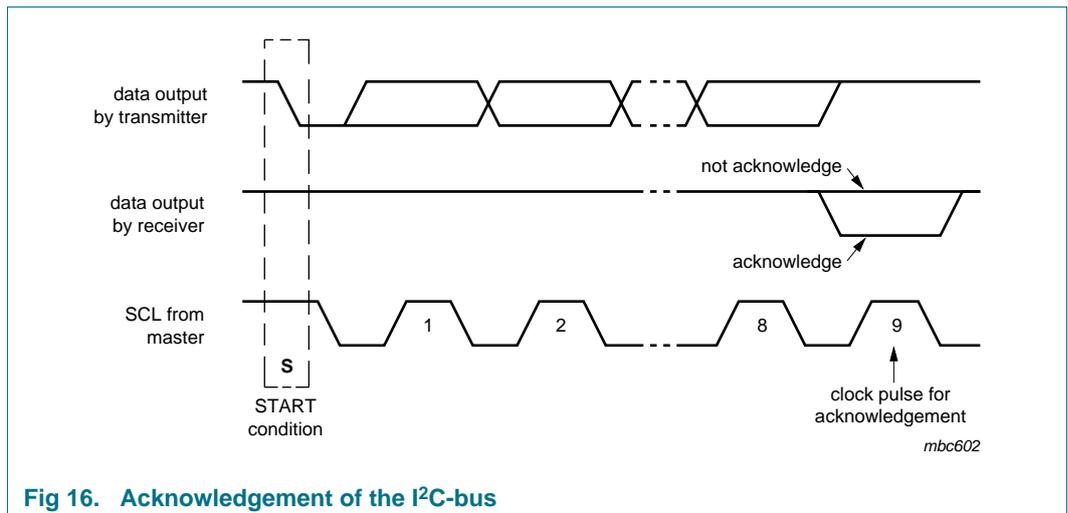Acknowledgement on the I^{2}C-bus is illustrated in Figure 16.

Fig 16. Acknowledgement of the I^{2}C-bus

8.4 I^{2}C-bus controller

The PCF85134 acts as an I^{2}C-bus slave receiver. It does not initiate I^{2}C-bus transfers or transmit data to an I^{2}C-bus master receiver. The only data output from the PCF85134 are the acknowledge signals of the selected devices. Device selection depends on the I^{2}C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme, so that no two devices with a common I^{2}C-bus slave address have the same hardware subaddress.

8.5 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.6 I^{2}C-bus protocol

Two I^{2}C-bus slave addresses (0111 000 and 0111 001) are used to address the PCF85134. The entire I^{2}C-bus slave address byte is shown in Table 16.

Table 16.   I^{2}C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
	0	1	1	1	0	0	SA0	R/$\overline{\text{W}}$

The PCF85134 is a write-only device and does not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the slave address byte, that a PCF85134 will respond to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

Having two reserved slave addresses allows the following on the same I^{2}C-bus:

- Up to 16 PCF85134 for very large LCD applications
- The use of two types of LCD multiplex drive

The I^{2}C-bus protocol is shown in Figure 17. The sequence is initiated with a START condition (S) from the I^{2}C-bus master which is followed by one of the available PCF85134 slave addresses. All PCF85134 with the same SA0 level acknowledge in parallel to the slave address. All PCF85134 with the alternative SA0 level ignore the whole I^{2}C-bus transfer.

PCF85134
Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 2 — 25 July 2011

© NXP B.V. 2011. All rights reserved.

26 of 45

R/W̄ = 0

slave address ↓ control byte RAM/command byte

| S | 0 1 1 1 0 0 | SA0 | 0 | A | CO | RS | | A | MSB | ... | LSB | P |

EXAMPLES
a) transmit two bytes of RAM data

| S | 0 1 1 1 0 0 | SA0 | 0 | A | 0 1 | A | RAM DATA | A | RAM DATA | A | P |

b) transmit two command bytes

| S | 0 1 1 1 0 0 | SA0 | 0 | A | 1 0 | A | COMMAND | A | 0 0 | A | COMMAND | A | P |

c) transmit one command byte and two RAM date bytes

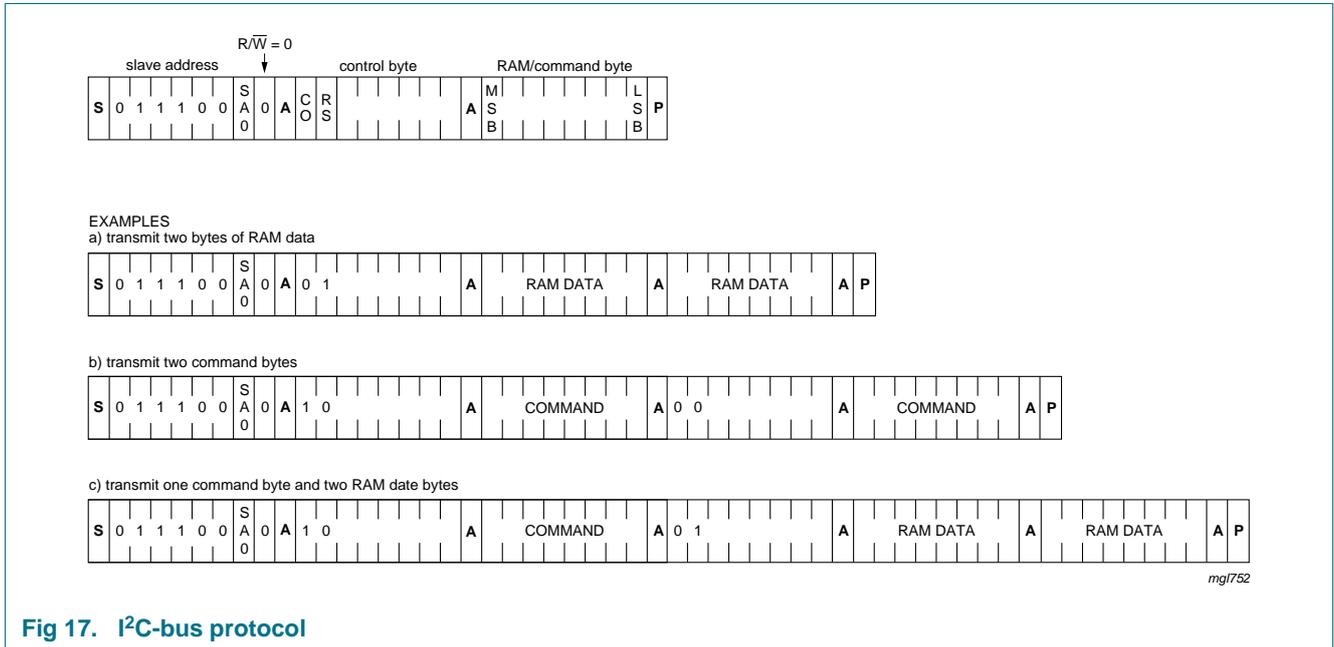| S | 0 1 1 1 0 0 | SA0 | 0 | A | 1 0 | A | COMMAND | A | 0 1 | A | RAM DATA | A | RAM DATA | A | P |

mgl752

Fig 17. I²C-bus protocol

After acknowledgement, the control byte is sent defining if the next byte is a RAM or command information. The control byte also defines if the next byte is a control byte or further RAM or command data (see Figure 18 and Table 17). In this way, it is possible to configure the device and then fill the display RAM with little overhead.
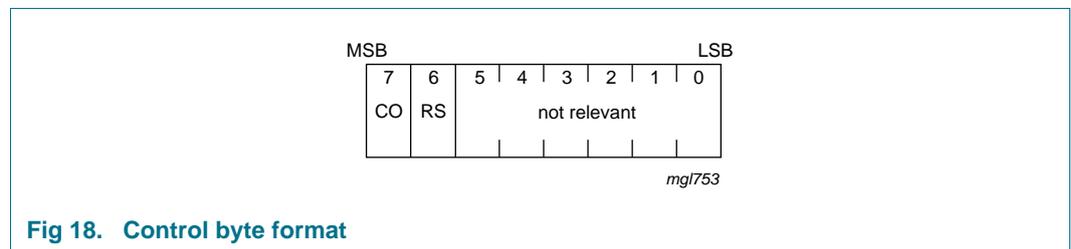
MSB LSB

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CO | RS | not relevant |

mgl753

Fig 18. Control byte format

Table 17. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		**register selection**
		0	command register
		1	data register
5 to 0	-		unused

The command bytes and control bytes are also acknowledged by all addressed PCF85134 connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated.

PCF85134

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet **Rev. 2 — 25 July 2011** **27 of 45**

The acknowledgement, after each byte, is made only by the A0, A1, and A2 addressed PCF85134. After the last display byte, the I^{2}C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART I^{2}C-bus access.
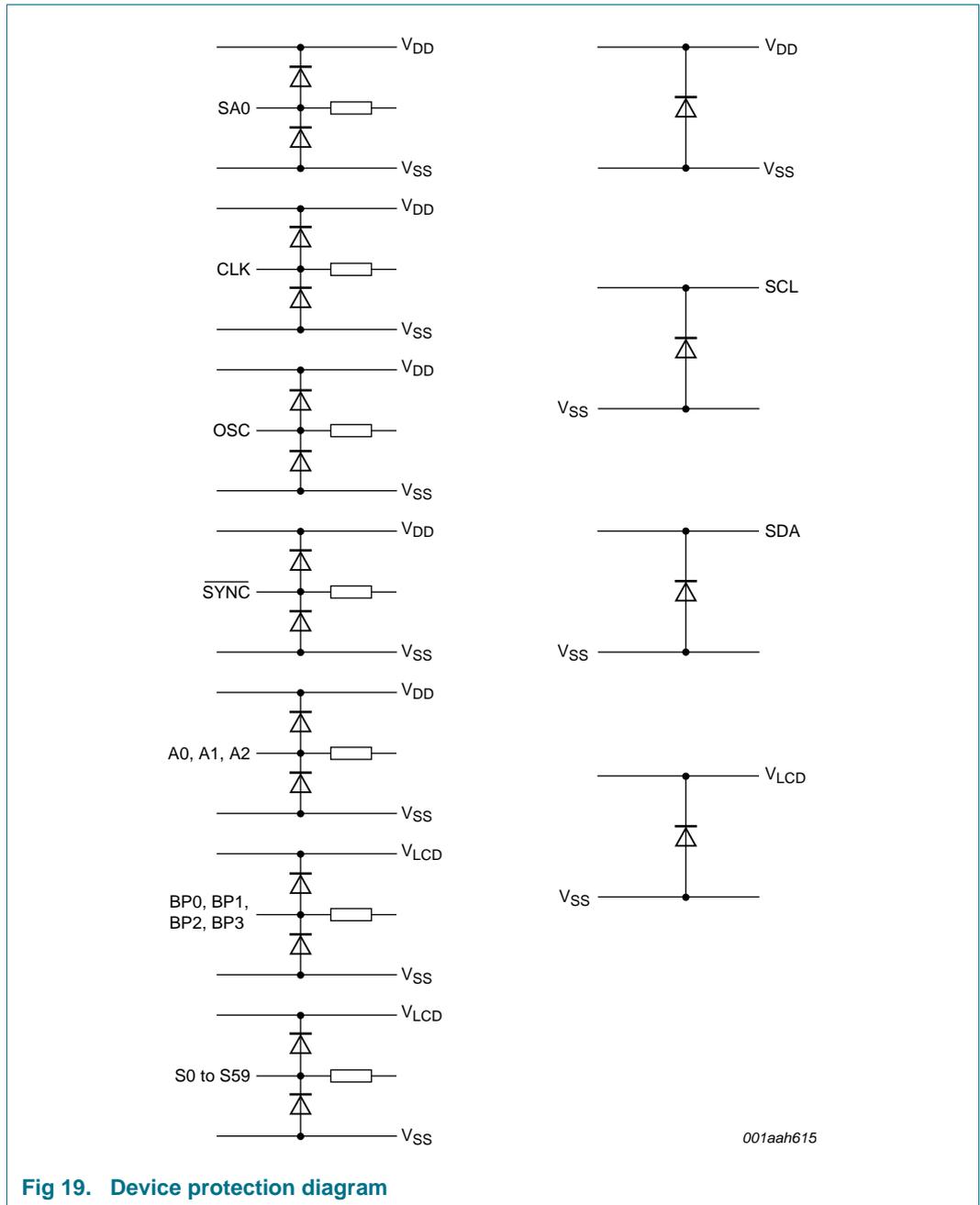
9. Internal circuitry

Fig 19. Device protection diagram

10. Limiting values

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 18. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.5	V
I_{DD}	supply current			−50	+50	mA
V_{LCD}	LCD supply voltage			−0.5	+7.5	V
$I_{DD(LCD)}$	LCD supply current			−50	+50	mA
I_{SS}	ground supply current			−50	+50	mA
V_I	input voltage		[2]	−0.5	+6.5	V
I_I	input current		[2]	−10	+10	mA
V_O	output voltage		[2]	−0.5	+6.5	V
			[3]	−0.5	+7.5	V
I_O	output current		[2][3]	−10	+10	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[4]	-	±2500	V
		MM	[5]	-	±200	V
I_{lu}	latch-up current		[6]	-	200	mA
T_{stg}	storage temperature		[7]	−65	+150	°C
T_{amb}	ambient temperature	operating device		−40	+85	°C

[1] Stresses above these values listed may cause permanent damage to the device.

[2] Pins SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC, and A0 to A2.

[3] Pins S0 to S59 and BP0 to BP3.

[4] Pass level; Human Body Model (HBM), according to Ref. 5 "JESD22-A114".

[5] Pass level; Machine Model (MM), according to Ref. 6 "JESD22-A115".

[6] Pass level; latch-up testing according to Ref. 7 "JESD78" at maximum ambient temperature ($T_{amb(max)}$).

[7] According to the NXP store and transport requirements (see Ref. 9 "NX3-00092") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long-term storage products deviant conditions are described in that document.

11. Static characteristics

Table 19.   Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage			2.5	-	6.5	V
I_{DD}	supply current	$f_{clk(ext)}$ = 1536 Hz	[1]	-	8	20	μA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 1536 Hz	[1]	-	24	60	μA
Logic							
V_I	input voltage			V_{SS} − 0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		$0.7V_{DD}$	-	V_{DD}	V
V_{POR}	power-on reset voltage			1.0	1.3	1.6	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V; on pins CLK and $\overline{SYNC}$		1	-	-	mA
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD} = 5 V; on pin CLK		1	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}; on pins SA0, A0 to A2 and CLK		−1	-	+1	μA
		V_I = V_{DD}; on pin OSC		−1	-	+1	μA
C_I	input capacitance		[2]	-	-	7	pF
I²C-bus; pins SDA and SCL[3]							
V_I	input voltage			V_{SS} − 0.5	-	5.5	V
V_{IL}	LOW-level input voltage	pin SCL		V_{SS}	-	$0.3V_{DD}$	V
		pin SDA		V_{SS}	-	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V; on pin SDA		3	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	μA
C_i	input capacitance		[2]	-	-	7	pF
LCD outputs							
Output pins BP0 to BP3							
V_{BP}	voltage on pin BP	C_{bpl} = 35 nF	[4]	−100	-	+100	mV
R_{BP}	resistance on pin BP	V_{LCD} = 5 V	[5]	-	1.5	10	kΩ
Output pins S0 to S59							
V_S	voltage on pin S	C_{sgm} = 35 nF	[6]	−100	-	+100	mV
R_S	resistance on pin S	V_{LCD} = 5 V	[5]	-	6.0	13.5	kΩ

[1]   LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I²C-bus inactive.

[2]   Not tested, design specification only.

[3]   The I²C-bus interface of PCF85134 is 5 V tolerant.

[4] C_{bpl} = backplane capacitance.

[5]   Measured on sample basis only.

[6] C_{sgm} = segment capacitance.

12. Dynamic characteristics

Table 20.   Dynamic characteristics
V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
Internal: output pin CLK						
f_{osc}	oscillator frequency	V_{DD} = 5 V	[1] 1440	1970	2640	Hz
External: input pin CLK						
$f_{clk(ext)}$	external clock frequency	V_{DD} = 5 V	800	-	3600	Hz
$t_{clk(H)}$	HIGH-level clock time		130	-	-	μs
$t_{clk(L)}$	LOW-level clock time		130	-	-	μs
Synchronization: input pin SYNC						
$t_{PD(SYNC\_N)}$	SYNC propagation delay		-	30	-	ns
t_{SYNC_NL}	SYNC LOW time		1	-	-	μs
Outputs: pins BP0 to BP3 and S0 to S59						
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V	-	-	30	μs
I²C-bus: timing[2]						
Pin SCL						
f_{SCL}	SCL frequency		-	-	400	kHz
t_{LOW}	LOW period of the SCL clock		1.3	-	-	μs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	μs
Pin SDA						
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
Pins SCL and SDA						
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	μs
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	μs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	μs
t_r	rise time of both SDA and SCL signals		-	-	0.3	μs
t_f	fall time of both SDA and SCL signals		-	-	0.3	μs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{w(spike)}$	spike pulse width		-	-	50	ns

[1]   Typical output (duty cycle δ = 50 %).

[2]   All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
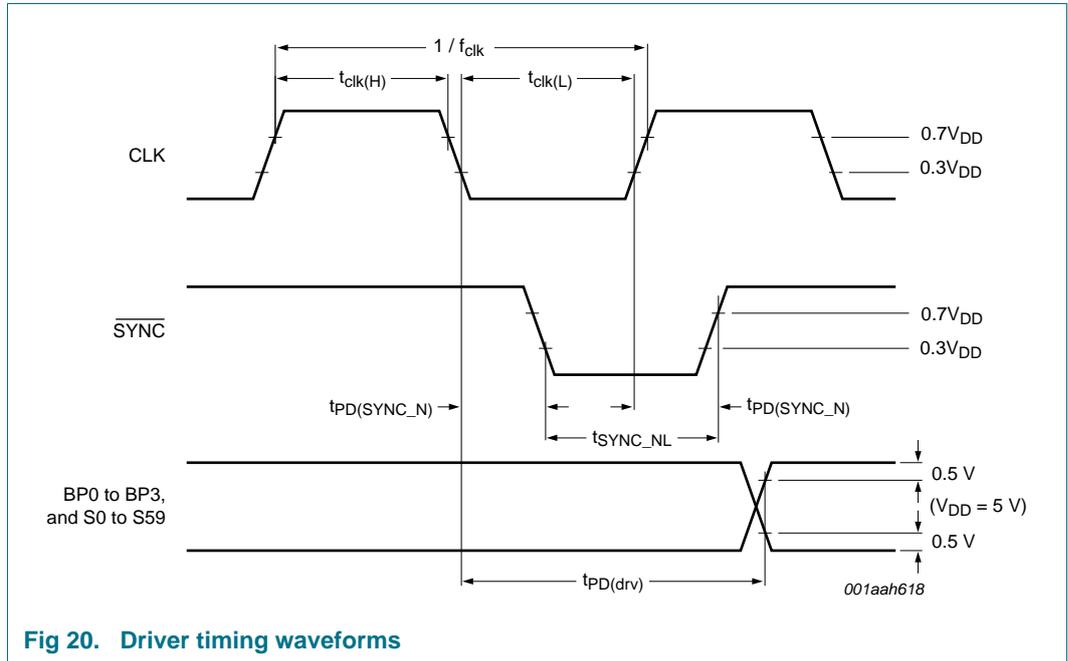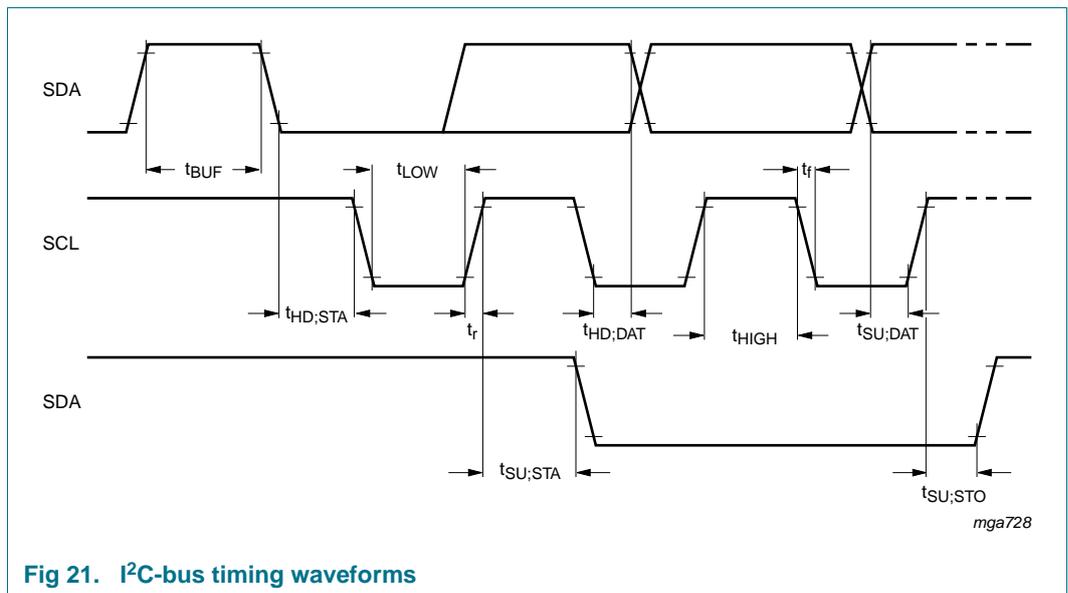
Fig 20. Driver timing waveforms

Fig 21. I²C-bus timing waveforms

PCF85134

Product data sheet **Rev. 2 — 25 July 2011** 32 of 45
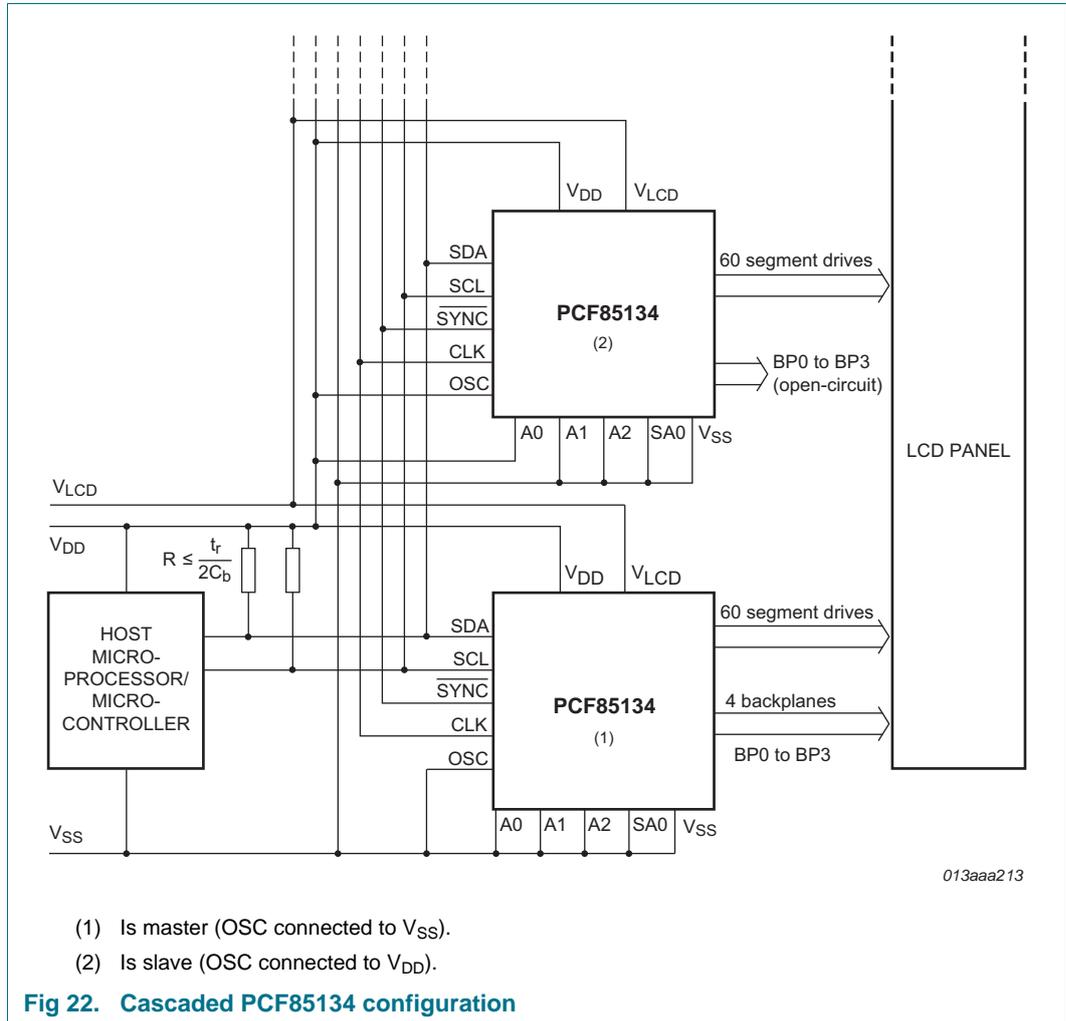
13. Application information

13.1 Cascaded operation

Large display configurations of up to 16 PCF85134s can be recognized on the same I^{2}C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I^{2}C-bus slave address (SA0).

Table 21. Addressing cascaded PCF85134

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

When cascaded PCF85134 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF85134 of the cascade contribute additional segment outputs, but their backplane outputs are left open-circuit (see Figure 22).

PCF85134

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet **Rev. 2 — 25 July 2011** 33 of 45

(1) Is master (OSC connected to V_{SS}).

(2) Is slave (OSC connected to V_{DD}).

Fig 22. Cascaded PCF85134 configuration

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF85134. Synchronization is guaranteed after a power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidentally lost (for example, by noise in adverse electrical environments or by defining a multiplex drive mode when PCF85134 with different SA0 levels are cascaded).

$\overline{SYNC}$ is organized as an input/output pin. The output selection is realized as an open-drain driver with an internal pull-up resistor. A PCF85134 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCF85134 to assert $\overline{SYNC}$. The timing relationship between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF85134 are shown in Figure 23.

The contact resistance between the $\overline{SYNC}$ on each cascaded device must be controlled. If the resistance is too high, the device is not able to synchronize properly; this is applicable to chip-on-glass applications. The maximum $\overline{SYNC}$ contact resistance allowed for the number of devices in cascade is given in Table 22.

Table 22.   SYNC contact resistance

Number of devices	Maximum contact resistance
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
11 to 16	700 Ω

The PCF85134 can always be cascaded with other devices of the same type or conditionally with other devices of the same family. This allows optimal drive selection for a given number of pixels to display. Figure 21 and Figure 23 show the timing of the synchronization signals.
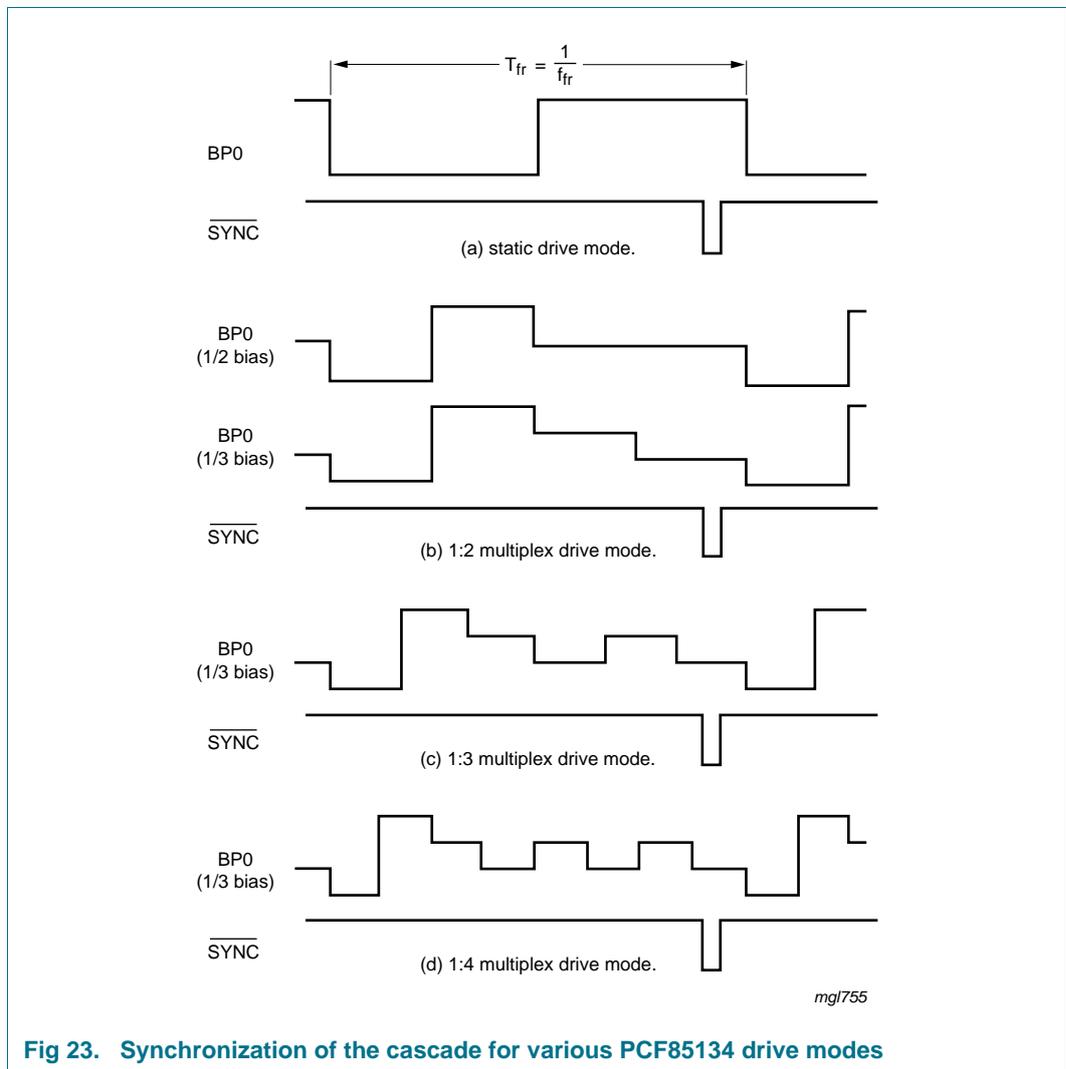

Fig 23.   Synchronization of the cascade for various PCF85134 drive modes

In a cascaded configuration, only one PCF85134 master must be used as clock source. All other PCF85134 in the cascade must be configured as slave such that they receive the clock from the master.

PCF85134

© NXP B.V. 2011. All rights reserved.

Product data sheet   **Rev. 2 — 25 July 2011**   **35 of 45**

If an external clock source is used, all PCF85134 in the cascade must be configured such as to receive the clock from that external source (pin OSC connected to V_{DD}). It must be ensured that the clock tree is designed such that on all PCF85134 the clock propagation delay from the clock source to all PCF85134 in the cascade is as equal as possible since otherwise synchronization artifacts may occur.

In mixed cascading configurations, care has to be taken that the specifications of the individual cascaded devices are met at all times.

PCF85134

Product data sheet **Rev. 2 — 25 July 2011** **36 of 45**

14. Package outline

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

Fig 24. Package outline SOT315-1 (LQFP80)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 23 and 24

Table 23. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 24. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.

MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components
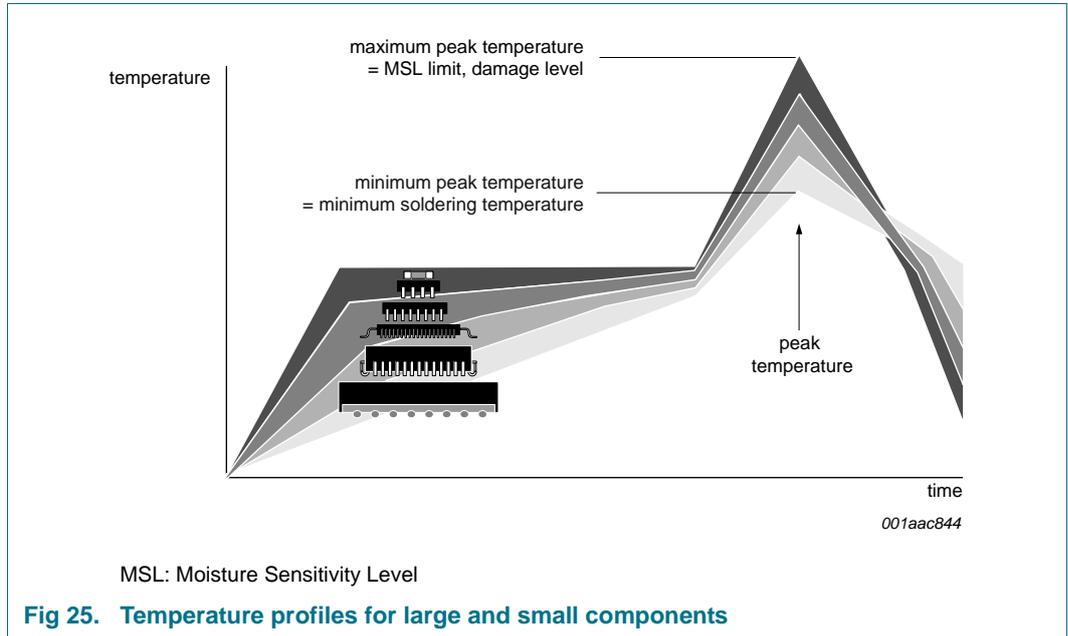
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

PCF85134

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet **Rev. 2 — 25 July 2011** **40 of 45**

17. Abbreviations

Table 25. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
EMC	ElectroMagnetic Compatibility
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^{2}C	Inter-Integrated Circuit bus
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MOS	Metal-Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
POR	Power-On Reset
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
RTC	Real-Time Clock
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface-Mount Device

PCF85134

Product data sheet **Rev. 2 — 25 July 2011** **41 of 45**

18. References

[1] AN10365 — Surface mount reflow soldering description

[2] IEC 60134 — Rating systems for electronic tubes and valves and analogous semiconductor devices

[3] IEC 61340-5 — Protection of electronic devices from electrostatic phenomena

[4] IPC/JEDEC J-STD-020D — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[5] JESD22-A114 — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] JESD22-A115 — Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[7] JESD78 — IC Latch-Up Test

[8] JESD625-A — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[9] NX3-00092 — NXP store and transport requirements

[10] SNV-FA-01-02 — Marking Formats Integrated Circuits

[11] UM10204 — I^2C-bus specification and user manual

19. Revision history

Table 26. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF85134 v.2	20110725	Product data sheet	-	PCF85134_1
Modifications:	• Added Section 7.10.3			
PCF85134_1	20091217	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^{2}C-bus — logo is a trademark of NXP B.V.

21. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

22. Contents