DSP Development Kit, Cyclone II Edition

Getting Started User Guide

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
P25-36029-00

Document Version: 6.0.1
Document Date: August 2006

UG-DSP011205-1.1

Contents

About This User Guide

Revision History

The following table displays the revision history for the chapters in this user guide.

Chapter	Date	Version	Changes Made
All	May 2005	1.0.0	First publication
All	August 2006	6.0.1	Updated for Quartus II Release 6.0 Service Pack 1

For late-breaking information not available in this user guide, see the README file on the *DSP Development Kit, Cyclone II Edition Version 6.0.1 CD-ROM*.

How to Contact Altera

For technical support or other information about Altera products, go to the Altera world-wide Web site at www.altera.com. You can also contact Altera through your local sales representative or any of the following sources.

Information Type	USA and Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
Non-technical customer service	800-767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	ftp.altera.com	ftp.altera.com

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: **f_{MAX}**, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, for example, `resetn`. Anything that must be typed exactly as it appears is shown in Courier type (for example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), as well as logic function names (for example, `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., and so on	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Chapter 1. About This Kit

Release Information

Table 1–1 provides information about this release of the *DSP Development Kit, Cyclone II Edition*.

Table 1–1. DSP Development Kit, Cyclone II Edition Release Information

Item	Description
Version	6.0.1
Release Date	August 2006
Ordering Code	DK-DSP-2C70N

Introduction

The *DSP Development Kit, Cyclone II Edition* provides everything you need to develop complete system-on-a-programmable-chip (SOPC) solutions. This document describes how to install the software provided with the kit, how to connect the Cyclone™ II DSP development board to your PC, and how to test the board.

Kit Contents

The *DSP Development Kit, Cyclone II Edition* includes:

- *Cyclone II DSP development board*—a prototyping platform that allows you to develop high-performance digital signal processing (DSP) designs. Key features of the Cyclone II DSP development board include a EP2C70 FPGA, high-speed analog-to-digital (A/D) and digital-to-analog (D/A) converters, and connectors for the Spectrum Digital *DSP Starter Kit (DSK) for the TMS320C6416*, Revision E.

For detailed information about the components and interfaces included on the Cyclone II DSP development board, and about their locations on the board, refer to the *Cyclone II DSP Development Board Reference Manual*.

- *DSP Builder Version 6.0.1 CD-ROM*—DSP system design in Altera® devices requires both high-level algorithms and hardware description language (HDL) development tools. Altera's DSP Builder is a system-level DSP design tool that provides an interface between the MathWorks MATLAB/Simulink software and the Altera Quartus® II software. DSP Builder integrates these tools by combining the algorithm development, simulation, and verification capabilities of the MATLAB/Simulink system-level design tools with Altera's HDL synthesis, simulation, and place-and-route tools.

DSP Builder shortens DSP design cycles by helping you create the hardware realization of a DSP design in an algorithm-friendly development environment, allowing system, algorithm, and hardware designers to share a common development platform.

For more information about DSP Builder, refer to the *DSP Builder User Guide*.

- *Quartus II Software Development Kit Edition (DKE) Version 6.0 SP1 CD-ROM*—The Quartus II software provides a comprehensive environment for SOPC design. The Quartus II software integrates into nearly any design environment, with interfaces to industry-standard EDA tools.

- *MegaCore® IP Library version 6.0.1 CD-ROM*—This CD-ROM contains Altera intellectual property (IP) MegaCore functions, including DSP MegaCore functions. You can evaluate the MegaCore functions using the OpenCore® Plus feature, which allows you to:

  - Simulate the behavior of a MegaCore function within your system
  - Verify the functionality of your design, as well as quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Configure a device and verify your design in hardware

  You may only need to purchase a license for a MegaCore function when you are completely satisfied with its functionality and performance, and want to take your design to production.

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use an Altera IP function in production designs.

  For details on licensing the OpenCore Plus hardware evaluation feature, refer to the application note, *AN 320: OpenCore Plus Evaluation of Megafunctions*.

- *Nios® II Embedded Processor Evaluation Edition Version 6.0.1 CD-ROM*—This CD-ROM contains the following:
  - *The Nios II CPU Component & Peripherals for SOPC Builder*—The CPU component provides three processor IP variations for the SOPC Builder hardware component library.
  - *Nios II IDE*—An integrated platform for embedded software development including multiple run configurations and project management.

- *MathWorks MATLAB and Simulink CD-ROM Release 2006a*—This CD-ROM contains third-party tools that are used in conjunction with DSP Builder as part of Altera's DSP development flow. MATLAB is a high-level technical computing language environment for algorithm development, data visualization, data analysis, and numerical computation. Simulink provides an interactive graphical environment and a customizable set of block libraries that let you accurately design, simulate, implement, and test signal processing systems.

  A 30-day license for MATLAB/Simulink is included as part of the DSP Development Kit, Stratix II Edition. To obtain the personal license password and for more information, please visit the MathWorks at: www.mathworks.com/products/connections/trials/altera.shtml.

- *DSP Development Kit, Cyclone II Edition version 6.0.1 CD-ROM*—This CD-ROM includes several reference designs and one lab to help you get started building applications and the contains the following documentation:
  - Cyclone II DSP development board schematic
  - *Cyclone II DSP Development Board Reference Manual*
  - This document (*DSP Development Kit, Cyclone II Edition Getting Started User Guide*)
  - *AN 376: Cyclone II Filtering Lab*
  - Nios II example designs

  For more information about the reference designs and the lab, refer to "Using the Reference Designs & Lab" on page 2–12.

Chapter 2. Getting Started

System Requirements

Before using the kit or installing the software, be sure to check the contents of the kit and inspect the board to verify that you received all of the items. If any of these items are missing, contact Altera before you proceed. You should also verify that the hardware and software in your computer meets the kit's requirements.

DSP Development Kit, Cyclone II Edition Contents

The *DSP Development Kit, Cyclone II Edition* contains the following items:

- Cyclone® II DSP development board with an EP2C70 device
- *DSP Development Kit, Cyclone II Edition Version 6.0.1 CD-ROM*
- *DSP Builder Version 6.0.1 CD-ROM*
- *The MathWorks MATLAB and Simulink CD-ROM Release 2006a (2006a)*
- *Quartus® II Software Development Kit Edition (DKE) Version 6.0 SP1 CD-ROM*
- *Nios® II Embedded Processor Windows Evaluation Edition version 6.0.1 CD-ROM*
- *IP MegaCore® Library version 6.0.1 CD-ROM*
- SLP-50 anti-aliasing filter from Mini-Circuits
- SMA cable
- USB-Blaster™ download cable and USB cable
- Power supply and adapters for North America/Japan, Europe, and the United Kingdom
- *Quartus II Design Software Installation & Licensing for PCs* manual

Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Verify that all components are on the board and appear intact.

The Cyclone II DSP development board can be damaged without proper anti-static handling.

Refer to the *Cyclone II DSP Development Board Reference Manual* (available on the *DSP Development Kit, Cyclone II Edition Version 6.0.1 CD-ROM*) for information on the board components and their locations.

Software Requirements

You must install the following software before you begin developing designs for the kit.

- The Quartus II software version 6.0. Refer to "Installing the Quartus II Software & MegaCore Functions" on page 2–3.

  Your system must meet the Quartus II software minimum requirements. Refer to the *Quartus II System Requirements* section in the *Quartus II Design Software Installation & Licensing for PCs* manual, which is included with the *DSP Development Kit, Cyclone II Edition*.

- Internet Explorer 4.01 with Service Pack 2 or later is required to use the Quartus II online Help system.
- Internet access for online registration of the Quartus II software and request license files. If you do not have Internet access, contact your local Altera representative.
- The MegaCore® functions on the *IP MegaCore® Library version 6.0.1 CD-ROM*. Refer to "Installing the Quartus II Software & MegaCore Functions" on page 2–3.
- The software on the *DSP Development Kit, Cyclone II EditionVersion 6.0.1 CD-ROM*. Refer to "Installing the Reference Designs & Lab" on page 2–4.
- The MathWorks MATLAB and Simulink DSP system design and modeling tools provided on the *MathWorks MATLAB and Simulink CD-ROM Release 2006a (2006a)*. This software is required to create hardware description language (HDL) designs that use blocks from DSP Builder. Refer to "Installing The MathWorks MATLAB/Simulink CD-ROM" on page 2–3.

Installing the Software

The instructions in this section explain how to install the following software:

- The Quartus II software, Development Kit Edition, including MegaCore functions from the *IP MegaCore® Library version 6.0.1 CD-ROM*
- MATLAB/Simulink software
- DSP Builder
- The Nios II embedded processor
- DSP reference designs and labs

Installing the Quartus II Software & MegaCore Functions

Refer to *Installing the Quartus II Software* in the *Quartus II Installation & Licensing Manual for PCs* for software installation instructions. After installing the software, request and install a license to enable it. Refer to "Set up Licensing" on page 2–6 for more information.

During the installation of the Quartus II software, you are given the option to install the MegaCore IP Library. When prompted to do so, choose to install the MegaCore IP Library and follow the on-screen instructions.

Installing The MathWorks MATLAB/Simulink CD-ROM

To install The MathWorks software, follow these steps:

1. Before installing, make sure that you have your Personal License Password (PLP) available. To obtain the 30-day evaluation license and for more information, please visit the MathWorks at: www.mathworks.com/products/connections/trials/altera.shtml.
2. If it is running, close the MATLAB/Simulink software.
3. Insert *MathWorks MATLAB and Simulink CD-ROM Release 2006a (2006a)*. The MathWorks Installer automatically starts, displaying the **Welcome to The MathWorks Installer** dialog box. Choose **Install** and click **Next**.
4. Enter your name, company name, and PLP in the **License Information** dialog box and click **Next**.
5. Review the software licensing agreement. If you agree with the terms, select the **Yes** check box and click **Next**.
6. Select **Typical** or **Custom** installation (for any user-specific selections) and click **Next**.
7. Click **Install**.
8. Click **Finish**.

Installing DSP Builder

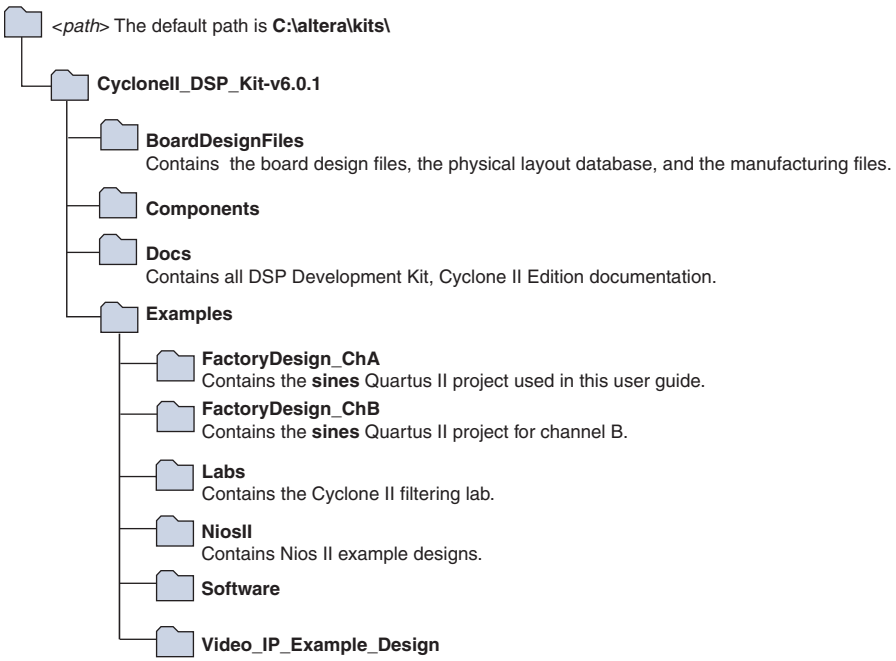
To install DSP Builder, refer to the *DSP Builder User Guide* for installation instructions.

Installing the Reference Designs & Lab

To install the reference designs and lab, insert the *DSP Development Kit, Cyclone II Edition Version 6.0.1 CD-ROM* into your CD-ROM drive. The installation program runs automatically.

Figure 2–1 shows the DSP Development Kit, Cyclone II Edition directory structure, where <*path*> is the DSP Development Kit, Cyclone II Edition installation directory.

Figure 2–1. DSP Development Kit Directory Structure



Installing the Nios II Embedded Processor

The Nios II CPU component and integrated development environment may be installed from the CD-ROM included in the kit.

1. Insert the *Nios® II Embedded Processor Windows Evaluation Edition version 6.0.1 CD-ROM*. If the install program does not automatically start, browse to your CD-ROM drive and double-click on the program **launcher.exe**.

2. Select which components to install. Altera recommends installing the default options.

3. Follow the on-screen instructions to select the installation directory and program group.

4. When installation completes, copy the board components for the Cyclone II DSP development board into the **Nios** directory so that they will be available in SOPC builder as board components. Perform the following steps to copy the components:

    a. Browse to <*drive letter*>**:\altera\kits\CycloneII_DSP_DK_v6.0.1\Components**, where <*drive letter*> is the drive on which you have installed your Altera software.

    b. Shift-click to select the **altera_dsp_dev_board_cyclone_2C70** directory.

    c. Press Ctrl + C to copy the directories.

    d. Browse to the <*drive letter*>**:\altera\kits** directory.

    e. Press Ctrl + V to paste the directories.

You can create, compile and generate time-limited Nios II processor systems using the OpenCore Plus hardware evaluation feature without obtaining a license file. You must obtain a license for the Nios II processor core and the Quartus II software to generate non-time-limited programming files and flash programming files for new Nios II hardware systems. You do not need a license if you will only develop software using the Nios II integrated development environment (IDE). For licensing information, look on the Altera web site at **www.altera.com**.

Set up Licensing

This section describes the software licensing procedures.

Licensing the DSP Development Kit, Cyclone II Edition

Before using the Quartus II software, you must obtain a license file from the Altera web site at **www.altera.com** and install the license file on your PC.

The Quartus II DKE software license allows you to use the product for 12 months. After 12 months, you must purchase a Fixed PC or FloatNet subscription.

To obtain a license, follow these steps:

If you have a Fixed PC or FloatNet Quartus II subscription, you can use that software instead of the Quartus II DKE software. If you intend to use your existing licensed software, you can skip the instructions below to obtain the license for the Quartus II Software Development Kit Edition included in your development kit.

1. Select the Licensing link at the top-right corner on the home page of the Altera Web site at **www.altera.com**.
2. Click **Cyclone II Development Kits**.
3. Follow the instructions to request your license. Altera will e-mail you a license file that enables the software. You need your network identification card (NIC) ID and the kit serial number to license the Quartus II software.

   Your network interface card (NIC) ID is a 12-character hexadecimal number that uniquely identifies your computer. You can find the NIC ID for your card by typing `ipconfig /all` at a command prompt. Your NIC ID is the number on the physical address line.

   The kit serial number is an 11-digit code of the form 2C70SPXXXXX where the X's represent decimal numbers. This serial number is located in three places: on the external shipping box, internal box, and Quartus II CD- ROM jacket. Refer to the serial number sticker in Figure 2–2.

Figure 2–2. Serial Number Example

The serial number is the bottom-most number, which is 2C70SPXXXXX in the above example.

4. After receiving your license that Altera e-mails you, close the following software applications if they are open:

   - Quartus II software
   - MAX+PLUS II software
   - LeonardoSpectrum synthesis tool
   - Synplify synthesis software
   - ModelSim simulator software
   - Precision RTL synthesis software

5. To install your license, refer to *Specifying the License File* in the *Quartus II Design Software Installation & Licensing for PCs* manual, which is included in the *DSP Development Kit, Cyclone II Edition*.

Licensing MegaCore Functions

You only need to purchase a license for a MegaCore function when you are completely satisfied with its functionality and performance, and want to take your design to production.

The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use an Altera IP function in production designs.

For details on licensing the OpenCore Plus hardware feature, refer to the application note, *AN 320: OpenCore Plus Evaluation of Megafunctions*.

Licensing DSP Builder

The DSP Builder software license included with the *DSP Development Kit, Cyclone II Edition* is a perpetual license with free software upgrades for the first 12 months. After 12 months, you must purchase a renewal subscription for access to future software upgrades. For more information, see the Licensing link on the Altera Web site at **www.altera.com**.

Connect the Cables to the Board & PC

The instructions in this section explain how to set up the following hardware:

- USB Blaster™ cable
- SLP-50 anti-aliasing filter
- SMA cable
- Power supply cable

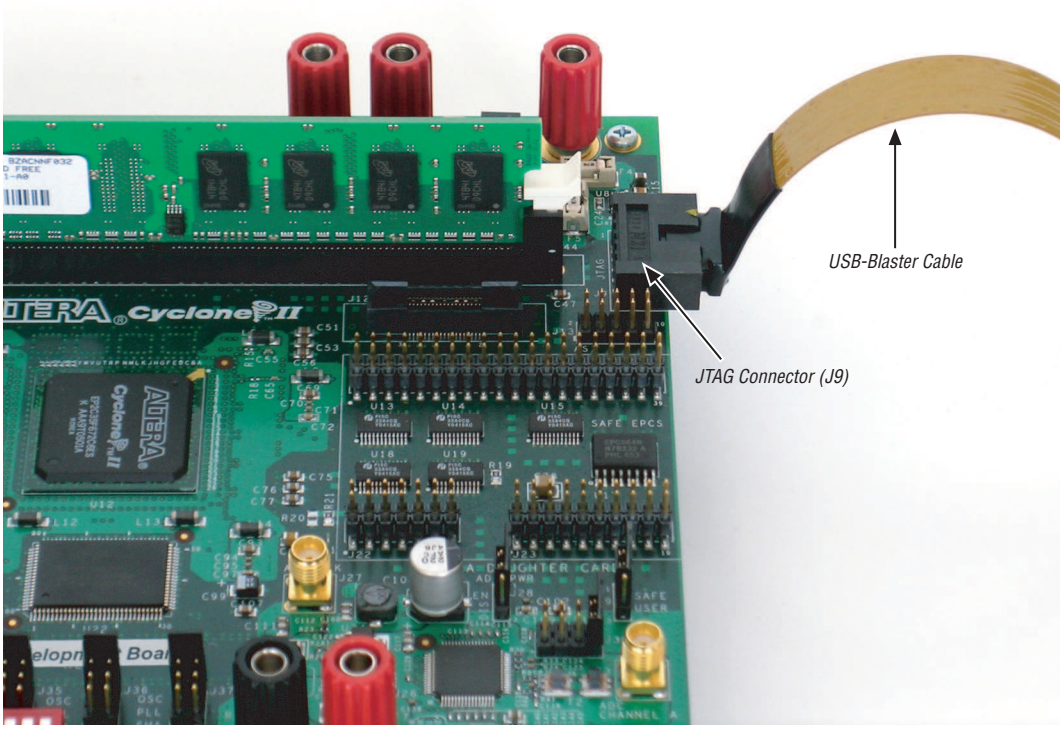
USB Blaster Cable

You must install the USB-Blaster download cable driver before you can use the USB-Blaster download cable.

For instructions on installing the USB-Blaster driver on your PC, refer to the *USB-Blaster Download Cable User Guide*. The driver files are installed at *<quartus-install-dir>***\drivers\usb-blaster**.

Connect the USB-Blaster cable's 10-pin female plug to the Cyclone II JTAG connector (J9) on the Cyclone II DSP development board and connect the other end to the USB port on your PC. See Figure 2–3. This connection allows you to configure the Cyclone II device directly using an SRAM Object File (**.sof**). The reference designs and the lab provided with the *DSP Development Kit, Cyclone II Edition* include SOFs for configuring the Cyclone II device directly.

Figure 2–3. Connecting the USB-Blaster Download Cable to J9



SLP-50 Anti-Aliasing Filter

The SLP-50 anti-aliasing filter from Mini-Circuits provides a 55 MHz cutoff frequency. To use the anti-aliasing filter, connect the filter to one end of the SMA cable. You can perform an external loopback from the output of the digital-to-analog (D/A) converter to the input of the analog-to-digital (A/D) converter using the filter and cable assembly. If the cutoff frequency must be lower than 55 MHz, other filters may be used.

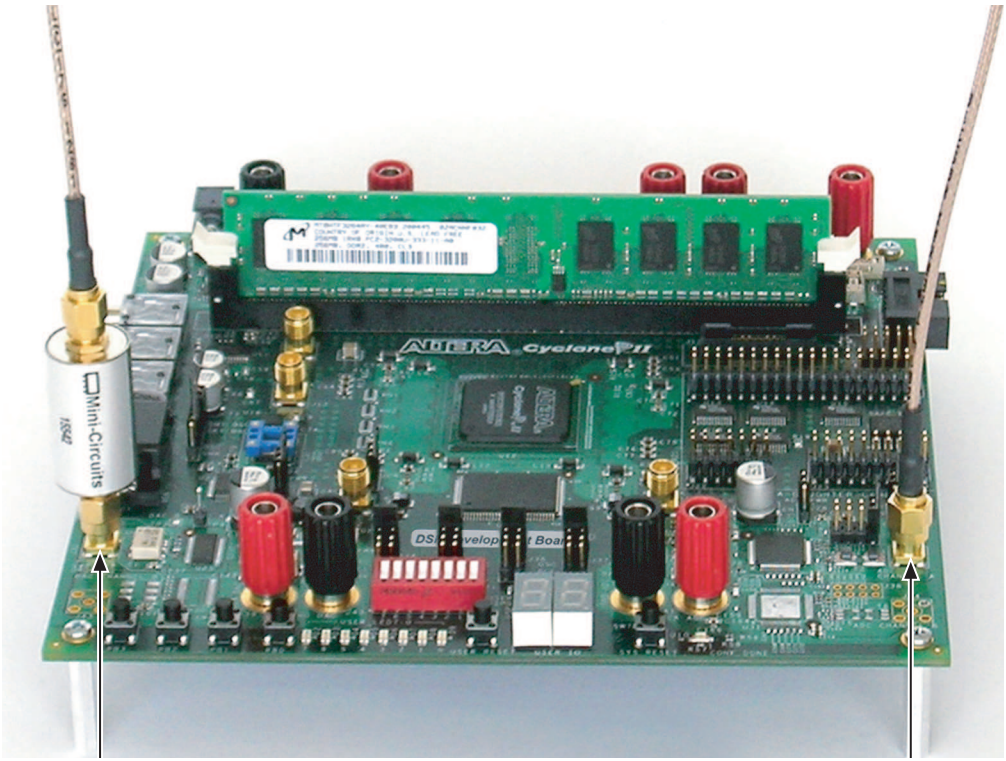
Connecting the SMA Cable

After attaching the SLP-50 (or other) anti-aliasing filter to one end of the the SMA cable, connect the SMA cable to the D/A and A/D connectors on the Cyclone II development board:

- The SMA D/A output converter DAC CHANNEL A (J31)
- The SMA A/D input converter ADC CHANNEL A (J32)

Figure 2–4 shows the cable and the SLP-50 anti-aliasing filter installed as required in "Performing the A/D & D/A Converter Performance Test" on page 2–16.

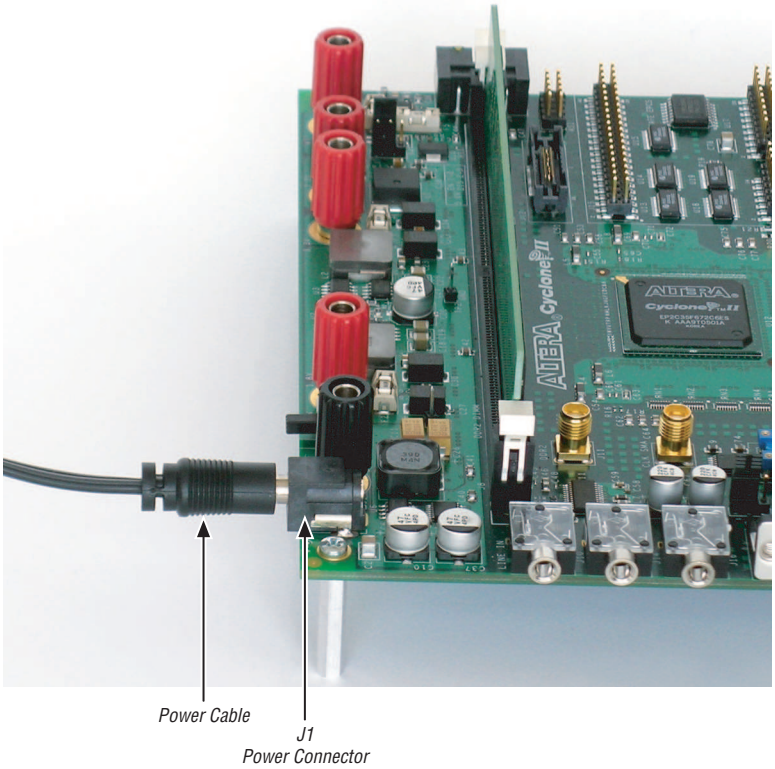
Figure 2–4. SMA Cable & SLP-50 Filter Installed to Connect DAC CHANNEL A (J31) with ADC CHANNEL A (J32)



Power Supply Cable

Connect the power cable to the Cyclone II DSP development board as shown in Figure 2–5 and plug the transformer end into a power outlet.

Figure 2–5. Connected Power Supply Cable



To power-up the Cyclone II DSP development board, place SW1 (POWER switch) in the ON position. When power is supplied to the Cyclone II DSP development board, LED D1 turns on, indicating the board has power.

Using the Reference Designs & Lab

Altera provides one lab with the *DSP Development Kit, Cyclone II Edition* to help you get started building applications. The lab is described *AN376: Cyclone II Filtering La*b. You can find the design in the **Examples** directory. Check for additional reference designs on the Altera web site.

Setting Unused Pins in the Reference and User Designs

In the factory design and in the lab included with the *DSP Development Kit, Cyclone II Edition*, all unused pins are set as tri-stated inputs and the following procedure is not necessary. However, when compiling your own designs, Altera recommends that you set all unused pins as tri-stated inputs.

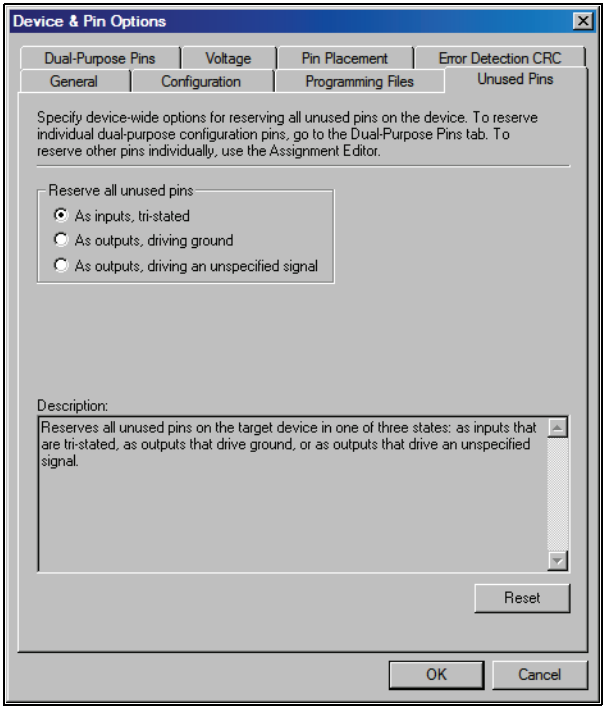
The Quartus II software default settings configure unused pins as outputs driving ground. The Cyclone II DSP development board components may be damaged by having ground signals driven onto pins that drive V_{CC}. You must complete the following procedure.

To set unused pins as tri-stated inputs, follow these steps:

1. Run the Quartus II software.
2. Choose **Device** (Assignments menu).
3. On the **Device** page of the **Settings** dialog box, click **Device & Pin Options**, then click the **Unused Pins** tab.

4. Under **Reserve all unused pins**, select **As inputs, tri-stated** (Figure 2–6).

Figure 2–6. Device & Pin Options Dialog Box



5. Click **OK** to close the **Device & Pin Options** dialog box.

6. Click **OK** to close the **Settings** dialog box.

For more information on configuring the EP2C70 FPGA, refer to the *Cyclone II DSP Development Board Reference Manual*.

For more information about configuring Cyclone II devices, refer to the *Configuring Cyclone II Devices* chapter of the *Cyclone II Device Handbook*.

Setting SAFE & USER Configuration Modes

Before starting board testing in "Testing the Board Using the Factory Design", you should have a brief understanding of the two configuration modes of the Cyclone II DSP development board.

The EP2C70 device on the Cyclone II DSP development board can be configured by using one of two EPCS64 devices. One EPCS64 device contains a factory configuration referred to as the "SAFE" configuration; the other EPCS64 device referred to as "USER" configuration is available to you to store your custom configuration.

Information about SAFE and USER configuration modes is provided in the *Cyclone II DSP Development Board Reference Manual*.

- J29 controls which EPCS64 device to configure.
  - Jumper J29, pins 1 and 2 set SAFE EPCS configuration mode to run the factory design.
  - Jumper J29, pins 2 and 3 set USER EPCS configuration mode to run a user design.
- The factory design stored on U17 (SAFE EPCS) configures the device each time the Cyclone II DSP development board is powered up in SAFE EPCS configuration mode.

  You can also reconfigure the device with the factory design stored in U17 (SAFE EPCS) by pressing SW7, which resets the hardware and reconfigures the Cyclone II DSP development board in SYS RESET mode.

  If you overwrite the factory design stored on U17, refer to the *Restoring the Factory Design* appendix in the *Cyclone II DSP Development Board Reference Manual*.
- A user design stored on U36 (USER EPCS) configures the device each time the Cyclone II DSP development board is powered up in USER EPCS configuration mode.

For more information on the factory design, and on SAFE and USER configuration modes, refer to "Testing the Board Using the Factory Design" on page 2–15.

Testing the Board Using the Factory Design

Put the Cyclone II DSP development board in SAFE configuration mode by putting a jumper on J29, pins 1 and 2. Then apply power and the Cyclone II device will be configured with the factory design stored in the EPCS64 flash memory, serial configuration device (U17). When configuration is complete, LEDs D9 through D5 (`USER_LED0` through `USER_LED4`, respectively), flash yellow, functioning as a binary counter that counts down to zero. This indicates that the Cyclone II DSP development board is functional and the EP2C70 device was successfully configured with the factory design.

If the Cyclone II DSP development board does not start as described above, follow these steps:

- Turn off the power to the board by placing SW1 (POWER switch) in the OFF position.
- Place the board in SAFE configuration mode by placing a jumper on pins 1 and 2 on jumper J29.
- Power-up the board by placing SW1 (POWER switch) in the ON position.

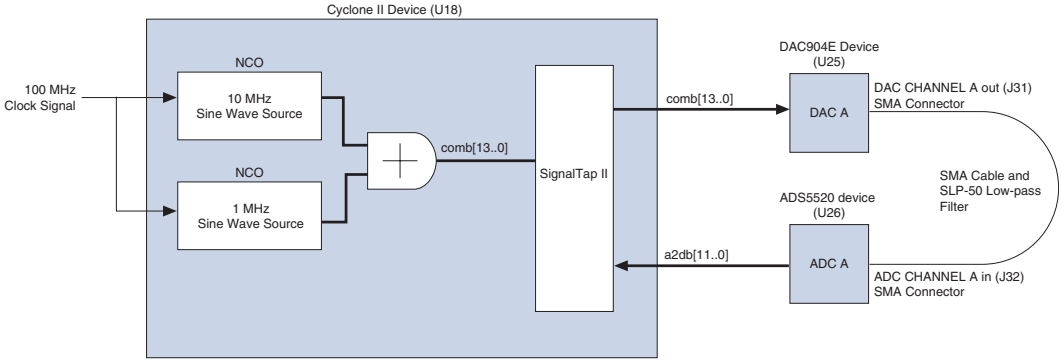
CAUTION

If you overwrite the factory design stored on U17, refer to the *Restoring the Factory Design* appendix in the *Cyclone II DSP Development Board Reference Manual*.

Understanding the Factory Design

In the factory design, two sine waves are generated by two instances of the Altera numerically controlled oscillator (NCO) MegaCore. One of these oscillators is running at 10 times the frequency of the other, but both of them have the same amplitude, covering 13 bits of dynamic range. The two sine waves output from these blocks are added together and the output is converted from a two's complement representation into unsigned integer format. This combined sine wave signal of 14-bits dynamic range is sent to a 14-bit D/A converter. The analog output of a D/A converter is connected, via the included SMA cable, with the analog input of a 12-bit A/D converter. The A/D converter's digital output is looped back to the Cyclone II device. The design converts this loopback input from two's complement format to unsigned integer format. The converted loopback data is captured by an instance of the SignalTap® II logic analyzer in the design for display and analysis. Figure 2–7 shows a high-level view of the factory design and how it interacts with the D/A and A/D converters on the Cyclone II DSP development board in the following sections.

Figure 2–7. Factory Design Functional Block Diagram



The design files for the factory design are installed from the *DSP Development Kit, Cyclone II Edition Version 6.0.1 CD-ROM* in the directory:

*<path>***CycloneII_DSP_Kit-v6.0.1****Examples****FactoryDesign_ChA**

Testing LEDs & Pushbutton Switches

In the factory design, switches SW2 through SW5 (`USER_PB3` through `USER_PB0`) are connected via inverters to LEDs D9 through D6 (`USER_LED0` to `USER_LED3`, respectively). When a switch is pressed, the corresponding LED turns off. You can test this functionality on the Cyclone II DSP development board.

Performing the A/D & D/A Converter Performance Test

To test the A/D and D/A converter performance using the factory design, follow these steps:

1. "Configuring the Board" on page 2–17
2. "Collecting Data Using the SignalTap II Logic Analyzer" on page 2–20
3. "Analyzing the Data in the MATLAB Software" on page 2–20

Configuring the Board

To configure the Cyclone II DSP development board, follow these steps:

1. Connect the SLP-50 filter (low pass filter) to one end of the SMA cable.
2. Use the cable-filter assembly to connect DAC CHANNEL A (J31) with ADC CHANNEL A (J32).
3. Add the correct jumpers for the clocks (see Figure 2–8 and Figure 2–9).
    a. For the DAC CHANNEL A Clock Select (J35), place a jumper on pins 1 and 2.
    b. For the ADC CHANNEL A Clock Select (J37), place a jumper on pins 1 and 2.
4. For the ADC Output Data Format Select (J30) place a jumper on pins 5 and 6. This sets the data output format to two's complement.

For more information about the data output format from the ADC, refer to the *Analog-to-Digital Converter (U26)* section in the *Cyclone II DSP Development Board Reference Manual*.

Figure 2–8 shows the location of jumpers J30, J35 and J37 on the Cyclone II DSP development board.

Figure 2–8. Locations of Jumpers J30, J35 & J37

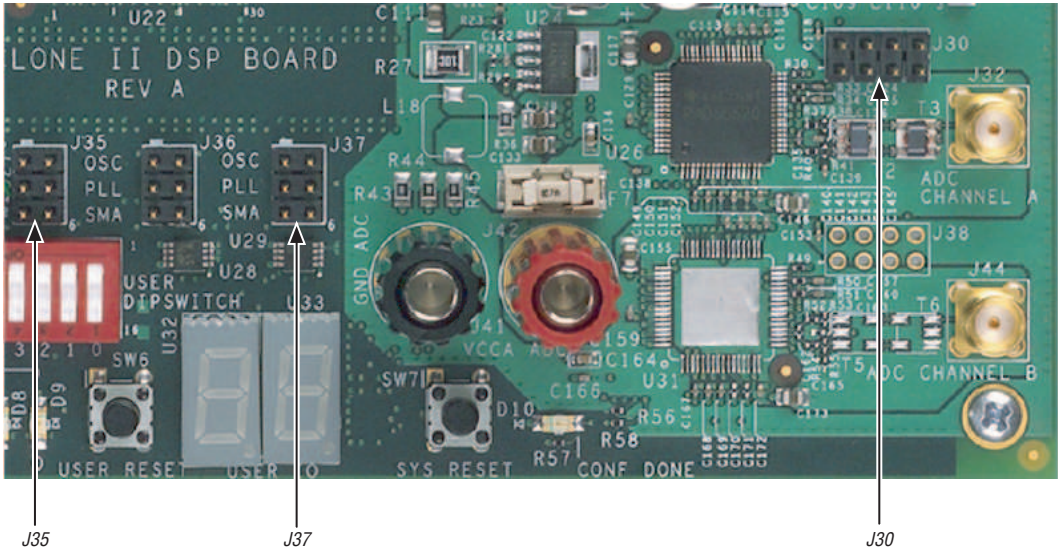
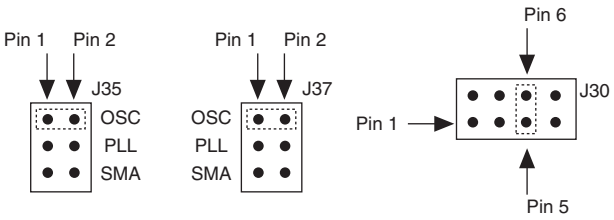


Figure 2–9 shows the jumper settings described in step 3 and step 4.

Figure 2–9. Jumper Connections for J35, J37 & J30



5. Start the Quartus II software.

6. Choose **Open Project** (File menu). In the **Open Project** dialog box, browse to the directory:

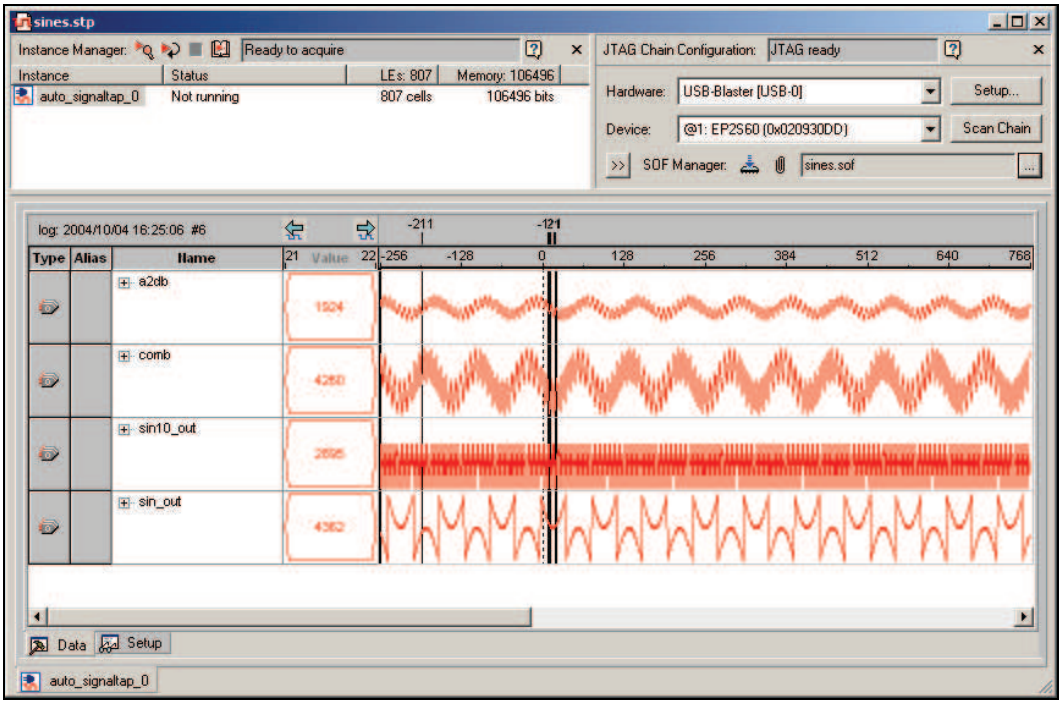
   <*path*>**\CycloneII_DSP_Kit-v.6.0.1\Examples\FactoryDesign_ChA**

7. Select **sines.qpf**, which contains project definitions for the edge detection reference design, and click **Open**.

8. The Signal Tap II file (**.stp**) provided with the design, **sines.stp**, automatically opens when you open the **sines** project. To bring it to the front, choose **sines.stp** (Window menu).

9. Expand the bus signals. Figure 2–10 shows **sines.stp** displayed in the SignalTap II logic analyzer.

Figure 2–10. Sines.stp Displayed in the SignalTap II Logic Analyzer



If you modify and recompile the design, specify your new SOF and click **Progam Device** in the SignalTap II window to configure the device with your SOF.

Collecting Data Using the SignalTap II Logic Analyzer

To collect data from the design for analysis, follow these steps.

1. In the Instance Manager section of the SignalTap II window, click **Run Analysis** and observe the following:

   a. Observe the D/A converter input on `comb[13..0]`. It shows a combination of two sine waves.

   b. Observe the A/D converter output on `a2db[11..0]`. It shows an attenuated combination of two sine waves.

   The A/D converter output is attenuated because the bit resolution is reduced from 14 bits to 12 bits. Analog circuitry on the Cyclone II DSP development board also causes some additional attenuation.

2. Choose **Create SignalTap II List File** from **Create / Update** (File Menu). The Quartus II software generates the file **sines_auto_signaltap_0.txt** in the project directory.

Analyzing the Data in the MATLAB Software

To analyze the `a2db` data from **sines_auto_signaltap_0.txt** in MATLAB, follow these steps:

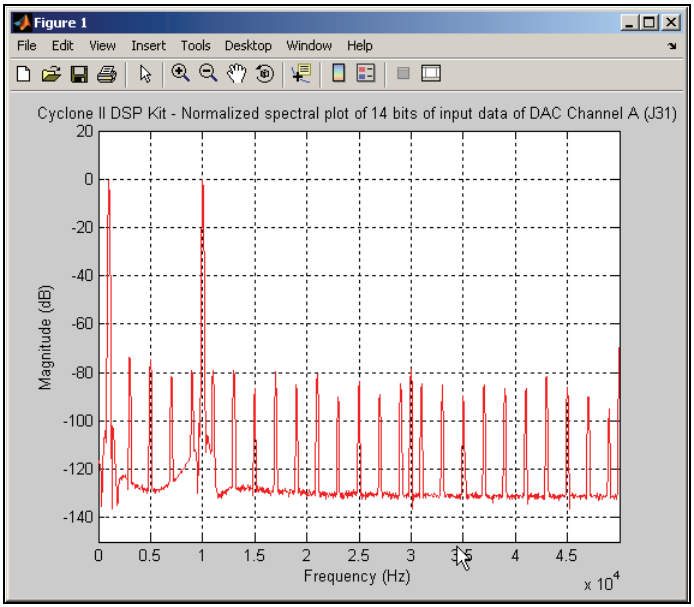
1. Start the MATLAB software.

2. At the MATLAB Command Window, type the following command:

   ```
   nstp_plot('sines_auto_signaltap_0.txt') ↵
   ```

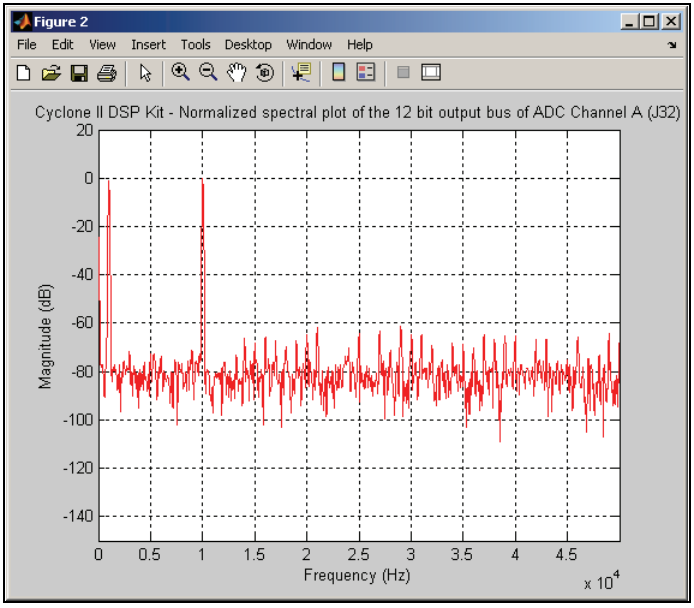
   The MATLAB software displays a normalized plot of the DAC CHANNEL A input similar to Figure 2–11.

Figure 2–11. Normalized Spectral Plot of 14-Bit DAC Channel A Input Data



The plotted graph of the peak spur level is below 60 db. A normalized FFT plot of ADC CHANNEL A output is shown in Figure 2–12.

Figure 2–12. Normalized Spectral Plot of 12-bit ADC Channel A Output Data



Conclusion

This Getting Started User Guide walks you through the software installation process, obtaining the license for the *DSP Development Kit, Cyclone II Edition*, and other software, as well as board setup, configuration, and testing of the Cyclone II DSP development board.