Enpirion EN2340QI DC-DC Converter w/Integrated Inductor Evaluation Board

Introduction

Thank you for choosing Altera Enpirion power products!

This evaluation board user guide applies to the EN2340 devices mounted on PCB's with the part number 06905 rev A, and three components on the backside. In addition to this document, you will also need the latest device datasheet.

- The EN2340QI features integrated inductor, power MOSFETS, controller, a bulk of the compensation network, and protection circuitry against system faults. This level of integration delivers a substantial reduction in footprint and parts count over competing solutions. The evaluation board is optimized for engineering ease of testing through programming options, clip leads, test points etc.

- The EN2340QI features a customer programmable output voltage by means of a resistor divider. The resistor divider allows the user to set the output voltage to any value within the range 0.75V to 5V. The evaluation board, as shipped is populated with a 4 resistor divider option. The upper resistor is fixed and has a phase lead capacitor in parallel. One of the 4 lower resistors is selected with the jumper option for different output voltages. To change V_{OUT}, retain the upper resistor and capacitor and change only the lower resistor.

- The input and output capacitors are X5R or X7R multi-layer ceramic chip capacitors. The Soft-start capacitor is a small value X7R MLCC. Pads are available to have multiple input and output capacitors. This allows for evaluation of performance over a wide range of input/output capacitor combinations.

- Clip-on terminals are provided for ENA and POK. Banana jacks are provided for $12V_{IN}$, AVIN, and V_{OUT} terminals. Several signal and GND clip-on test points are also provided to measure V_{IN}, V_{OUT}, and GND nodes.

- The Enable pin is pre-wired with a resistor divider to PVIN and GND according to the datasheet recommendation. Enable may also be controlled by applying an external signal to the ENA clip-on terminal.

- Foot print is also provided for a SMA connector to S_IN input. A switching input to this pin allows the device clock to be phase locked to an external signal. This external clock synchronization allows for moving any offending beat frequency to be moved out-of-band. A swept frequency applied to this pin results in spread spectrum operation and reduces the peaks in the noise spectrum of emitted EMI.

- A two pin header footprint is provided for the S_OUT pin. This signal can be used to synchronize another EN2340 to the switching frequency coming out of the S_OUT pin.

- The board comes with input decoupling and PVIN (12VIN) reverse polarity protection to guard the device against common setup mishaps. Please note there is no reverse polarity protection on AVIN input.

Quick Start Guide

STEP 1: This board has some additional components on the back side including a resistor divider from PVIN to Enable to GND (indicated as NR1 & NR2 in the schematic). As a result of these components, there is no need for a jumper on J3 (see Figure 1), and the component FB1 (to the left of AVIN test point TP28) should not be populated. Please contact Altera Power Applications support if your board does not have these components added on the back side, or if FB1 is still populated.

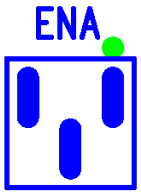


Figure 1: Enable header without any jumpers

STEP 2: Connect the 12V nominal Power Supply to the input power connectors, 12VIN (J7) and GND (J11) as indicated in Figure 4 and set the supply to the desired voltage.

> **CAUTION**: Be mindful of the polarity. Even though the evaluation board comes with reverse polarity protection diodes, it may not protect the device under all conditions.

STEP 3: Make sure the two-in header J1 is properly populated depending on how you want to power AVIN. If you want to use the device in a single input supply mode, and use the on-chip AVINO pin, then populate J1 with a shorting jumper. If you want to supply your own external AVIN, then remove the jumper from J1, and connect a 3.3V nominal power supply to the AVIN (J9) and GND (J11).

CAUTION: With the resistor divider between PVIN and Enable and GND, if you decide to supply an external AVIN, then AVIN has to be turned on before PVIN, and turned off after PVIN. Not following this sequence can damage the device.

CAUTION: Be mindful of the AVIN input polarity. There is no reverse polarity protection on this input.

CAUTION: Do not apply an external AVIN to the device with the J1 jumper populated. Doing so will damage the device.

STEP 4: Connect the load to the output connectors VOUT (J6) and GND (J10), as indicated in Figure 4.

STEP 5: Select the output voltage setting jumper. Figure 2 shows what output voltages are achieved by selecting each jumper position. Note that depending on the tolerance of the resistors populated on the board, each output voltage setting may have a larger tolerance than just the VFB pin as specified in the datasheet. Please see Figure 5 and the Bill of Materials section.

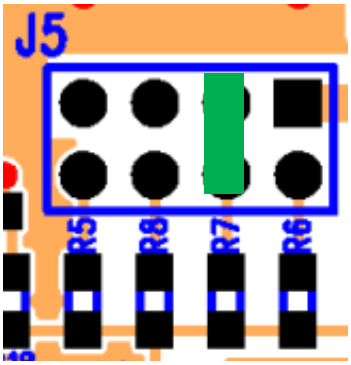


Figure 2: Output Voltage selection jumpers J5. Nominal jumper position voltages from left to right are: 3.29V, 2.48V, 1.2V and 1.0V. Jumper shown selects 1.20V output. Do not change jumper positions while the board is powered.

Please note: The loop compensation circuit for this version of evaluation board has been chosen for a wide range of PVIN and V_{OUT} values. In order to optimize the loop for any specific PVIN/V_{OUT} operating point, please see the compensation table in the datasheet. See Figures 4 and 5.

STEP 6: Apply AVIN first, and then $12V_{IN}$ if using dual supply mode. For single supply mode, just apply $12V_{IN}$. The EN2340QI is now powered up since there is a resistor divider from PVIN to Enable. Various measurements such as efficiency, line and load regulation, input / output ripple, load transient, drop-out voltage measurements may be conducted at this point. The over current trip level, short circuit protection, under voltage lock out thresholds, temperature coefficient of the output voltage may also be measured in this configuration.

Alternatively, you can control the ENA jumper with an external source. For dual supply mode, you can also tie Enable to AVIN by removing NR1 from the back side, putting a short across the FB1 footprint, and connecting the middle point of J3 to the left pin using a shorting jumper. Please review the Power Up Sequence section in the datasheet before experimenting with various turn on/off combinations.

CAUTION: Please refer to the datasheet for the maximum voltages on the 12V (PVIN) and AVIN inputs, and maximum slew rates for the PVIN input.

STEP 6A: Power Up/Down Behavior – Connect a pulse generator (output disabled) signal to the clip-on test point below ENA and Ground. Set the pulse amplitude to swing from 0 to 2.5 volts. Set the pulse period to 10msec. and duty cycle to 50%. Hook up oscilloscope probes to ENA, SS, POK and VOUT with clean ground returns. Apply power to evaluation board. Enable pulse generator output. Observe the SS capacitor and VOUT voltage ramps as ENA goes high and again as ENA goes low. The device when powered down ramps down the output voltage in a controlled manner before fully shutting down. The output voltage level when POK is asserted /de-asserted as the device is powered up / down may be observed as well as the clean output voltage ramp and POK signals.

STEP 7: External Clock Synchronization / Spread Spectrum Modes: In order to activate this mode, it may be necessary to a solder a SMA connector at J4. Alternately the input clock signal leads may be directly soldered to the through holes of J4 as shown below.

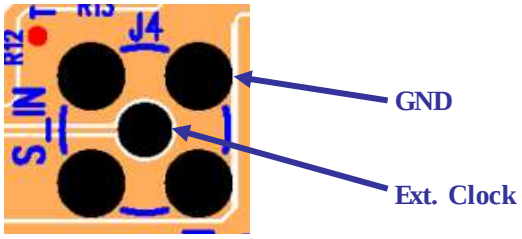


Figure 3: SMA Connector for External Clock Input

Power down the device. Move ENA into disable position. Connect the clock signal as just indicated. The clock signal should be clean and have a frequency range specified in the datasheet, and an amplitude 0 to 2.5 volts with a duty cycle between 20 and 80%. With S_IN signal disabled, power up the device and move ENA jumper to Enabled position. The device is now powered up and outputting the desired voltage. The device is switching at its free running frequency. The switching waveform may be observed between test points SW and GND. Now enabling the S_IN signal will automatically phase lock the internal switching frequency to the externally applied frequency as long as the external clock parameters are within the specified range. To observe phase-lock connect oscilloscope probes to the input clock as well as to the SW test point. Phase lock range can be determined by sweeping the external clock frequency up / down until the device just goes out of lock at the two extremes of its range.

For spread spectrum operation the input clock frequency may be swept between two frequencies that are within the lock range. The sweep (jitter) repetition rate should be limited to 10 kHz. The radiated EMI spectrum may be now measured in various states – free running, phase locked to a fixed frequency and spread spectrum.

Before measuring radiated EMI, place a 10uF/0805, X7R capacitor at the input and output edges of the PCB (C8 and C9 positions), and connect the PVIN power and the load to the board at or near these capacitors. The added capacitor at the input edge is for high-frequency decoupling of the input cables. The one added at the output edge is meant to represent a typical load decoupling capacitor. We recommend doing EMI testing in single-supply mode only as this will simplify the test setup.

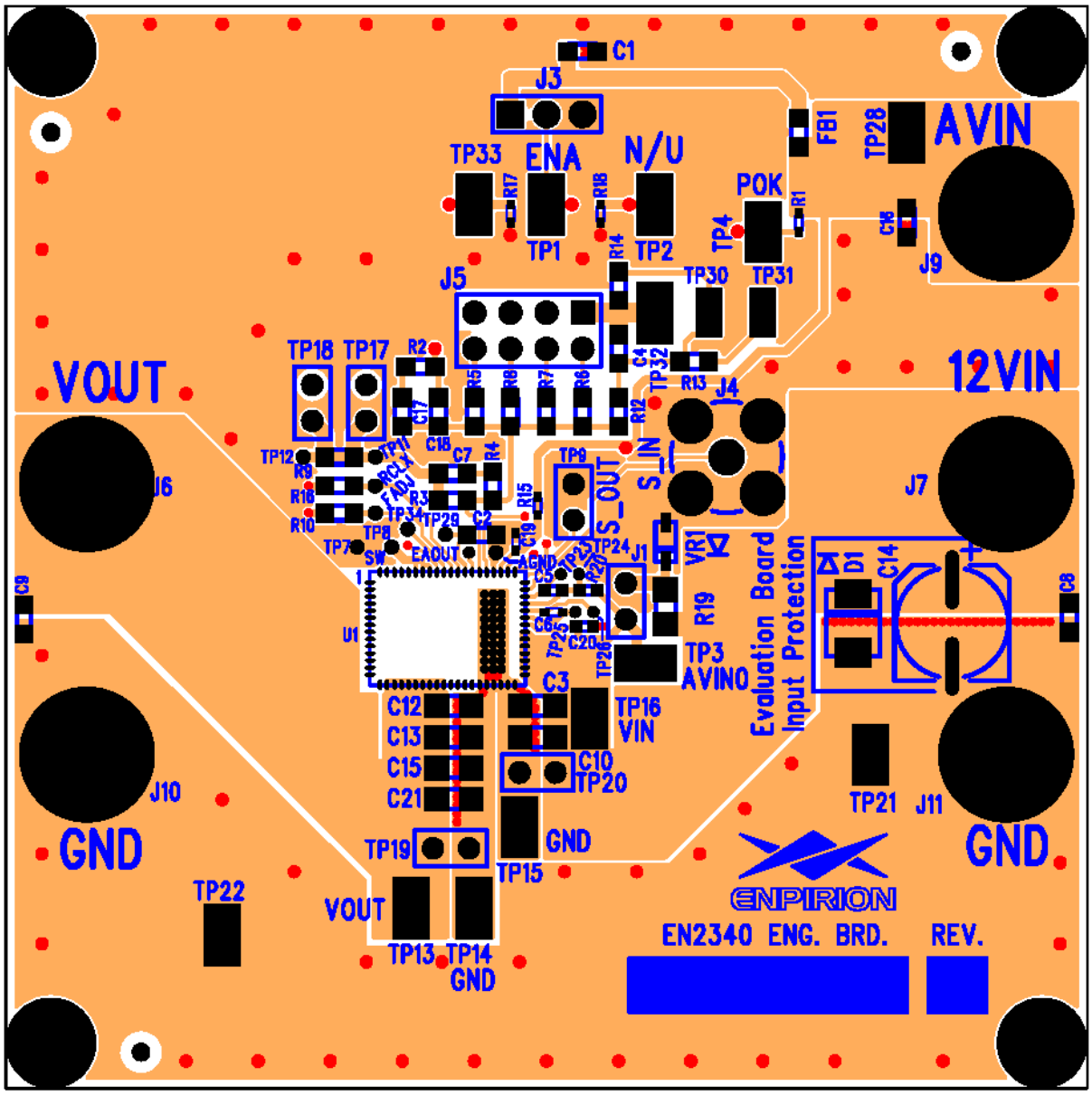


Figure 4: Evaluation Board Top and Assembly Layers.

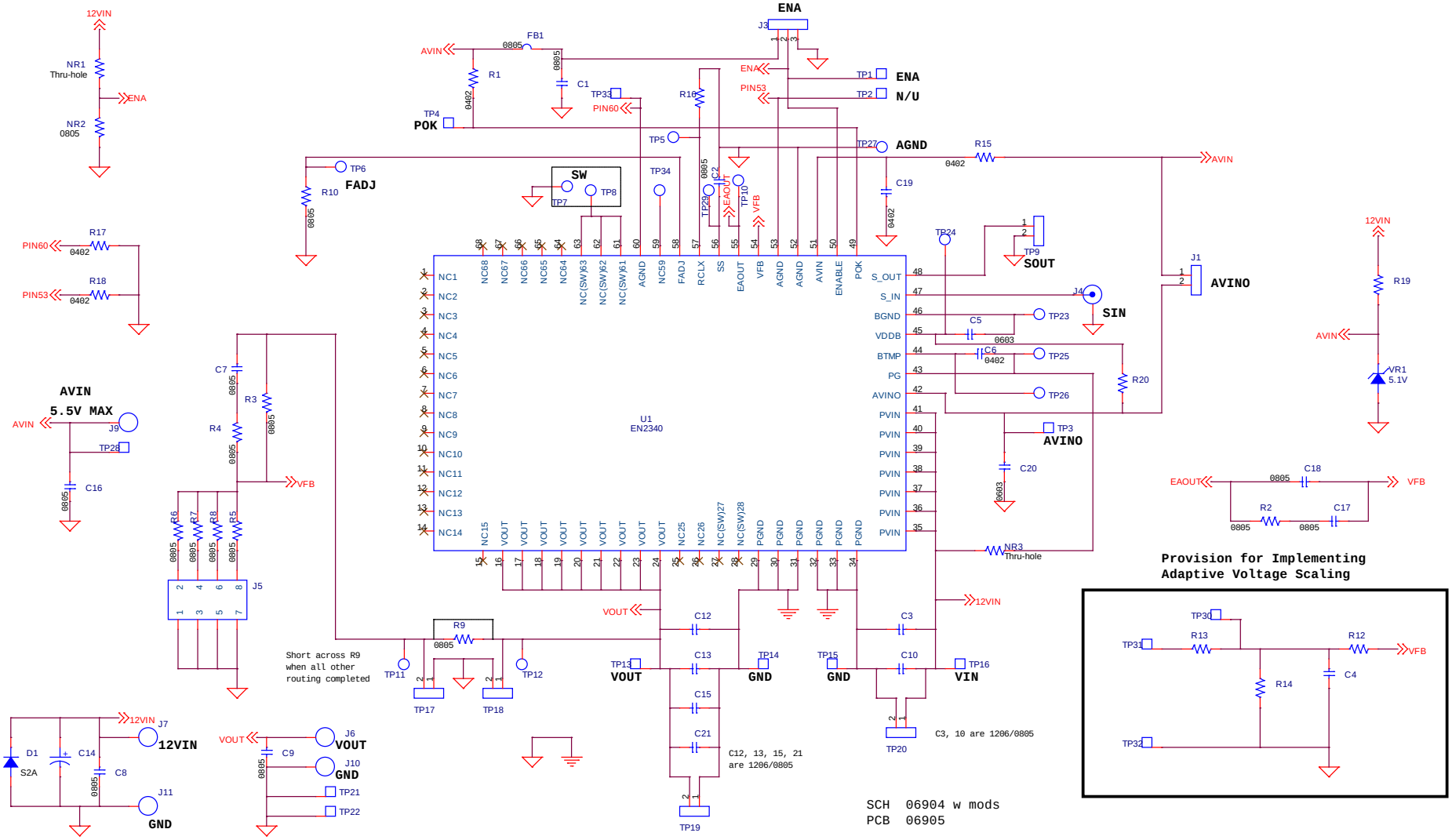
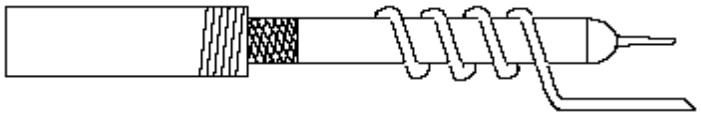


Figure 5: EN2340 Evaluation Board Schematic (NR1-NR3 are additional components on the back side)

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided (TP13 to TP16). This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a low-loop-inductance scope probe tip similar to the one shown below to measure switching signals and input / output ripple to avoid noise coupling into the probe ground lead. Input ripple, output ripple, and load transient deviation are best measured near the respective input / output capacitors. For more accurate ripple measurement, please see Enpirion App Note regarding this subject.



4. The board includes a pull-up resistor for the POK signal and ready to monitor the power OK status at clip lead marked POK.
5. The over-current protection circuit typically limits the maximum load current to approximately 1.5X the rated value. For the EN2340, the OCP trip point can be programmed via the RCLX pin. Table 1 below shows the RCLX value that should be used to achieve a nominal 6A OCP trip point as a function of PVIN & V_{OUT}. The board as shipped is populated with a 31.6kΩ RCLX resistor. If the board does not deliver full load for some input and output combinations, you may have to change the RCLX resistor according to Table 1. Please see the datasheet for further details.

PVIN	V_{OUT} Range	R_{CLX} Value
5V	$0.75V < V_{OUT} \leq 1.2V$	30.1kΩ
	$1.2V < V_{OUT} \leq 2.0V$	31.6kΩ
	$2.0V < V_{OUT} \leq 2.5V$	33.2kΩ
8V	$0.75V < V_{OUT} \leq 1.2V$	30.9kΩ
	$1.2V < V_{OUT} \leq 2.0V$	32.4kΩ
	$2.0V < V_{OUT} \leq 3.0V$	35.7kΩ
	$3.0V < V_{OUT} \leq 4.0V$	38.3kΩ
	$4.0V < V_{OUT} \leq 5.0V$	40.2kΩ
12V	$0.75V < V_{OUT} \leq 1.2V$	31.6kΩ
	$1.2V < V_{OUT} \leq 2.0V$	33.2kΩ
	$2.0V < V_{OUT} \leq 3.0V$	36.5kΩ
	$3.0V < V_{OUT} \leq 4.0V$	39.2kΩ
	$4.0V < V_{OUT} \leq 5.0V$	41.2kΩ

Table 1: Recommended RCLX values

Bill of Materials

Designator	Qty	Description
C2	1	CAP, 47000PF 0805 X7R 10% 50V CERAMIC
C3	1	CAP, 22UF 1206 X5R 10% 25V CERAMIC
C5	1	CAP CER 0.22UF 16V X5R 0402
C6	1	CAP CER 22000PF 16V X7R 0402
C7	1	CAP, 68PF 0805 NP0 5% 50V CERAMIC
C12, C13	2	CAP, 47UF 1206 X5R 20% 10V CERAMIC
C14	1	CAP, SMT ELECTROLYTIC, 150UF, 25V
C19, C20	2	CAP, 1UF 0402 X5R 10% 10V CERAMIC
C1, C4, C8-C11, C15-C18, C21, FB1, J4, R2, R9, R11-R15, R19, TP3, TP34, VR1	24	NOT USED
D1	1	S2A DIODE, Micro Commercial S2A-TP
J1	1	CONNECTOR HEADER, 2 POSITION, Samtec TSW-102-07-T-S
J3	1	CONNECTOR HEADER, 3 POSITION, Samtec TSW-103-07-T-S
J5	1	CONNECTOR HEADER, 8 POSITION Dual, Samtec TSW-104-24-T-D
J6, J7, J9-J11	5	BANANA JACK, KEYSTONE 575-4
R1	1	RES 100K OHM 1/16W 1% 0402 SMD
R3	1	RES 200K OHM 1/8W 0.1% 0805 SMD
R4	1	RES 10K OHM 1/8W 0.1% 0805 SMD
R5	1	RES 59K OHM 1/8W 1% 0805 SMD
R6	1	RES 604K OHM 1/8W 1% 0805 SMD
R7	1	RES 332K OHM 1/8W 1% 0805 SMD
R8	1	RES 86.6K OHM 1/8W 1% 0805 SMD
R10	1	RES 3.01K OHM 1/8W 1% 0805 SMD
R16	1	RES 31.6K OHM 1/8W 0.1% 0805 SMD
R17, R18	2	RES ZERO OHM 1/10W 5% 0402 SMD
TP1, TP2, TP4, TP13-TP16, TP21,TP22, TP28,TP32, TP33	12	TEST POINT SURFACE MOUNT, KEYSTONE 5016
TP30, TP31	2	TEST POINT SURFACE MOUNT, KEYSTONE 5015
U1	1	EN2340QI QFN 4A
NR1	1	RES 10.0K OHM 1/4W 1% AXIAL
NR2	1	RES 4.02KOHM 1/4W1% 0805 SMD
NR3	1	RES 562 OHM 1/4W 1% AXIAL

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