



Identification

4GB 1Rx8 PC3-12800S-11-11-B3
DTM64617A 512Mx64

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}

800 MHz / DDR3-1600 / 11-11-11
667 MHz / DDR3-1333 / 10-10-10
667 MHz / DDR3-1333 / 9-9-9
533 MHz / DDR3-1066 / 8-8-8
533 MHz / DDR3-1066 / 7-7-7
400 MHz / DDR3-800 / 6-6-6
333 MHz / DDR3-667 / 5-5-5

Features

204-pin SO-DIMM. Dual-sided assembly 67.60 mm [2.661"] wide by 30.0 mm [1.181"] high

Operating Voltage: 1.5 V ±0.075 V

I/O Type: SSTL_15

Data Transfer Rate: 12.8 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 5, 6, 7, 8, 9, 10, and 11

Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 16/10/3

Fully RoHS Compliant

Description

DTM64617A is a non-ECC Unbuffered DDR3-1600, 512Mx64 memory module which conforms to JEDEC's PC3-12800 standard. The assembly is comprised of one Rank. The Rank is comprised of eight Hynix 512Mx8 DDR3 SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals.

The assembly is a Small Outline Dual In-line Memory Module intended for mounting into 204-pin edge connector sockets.

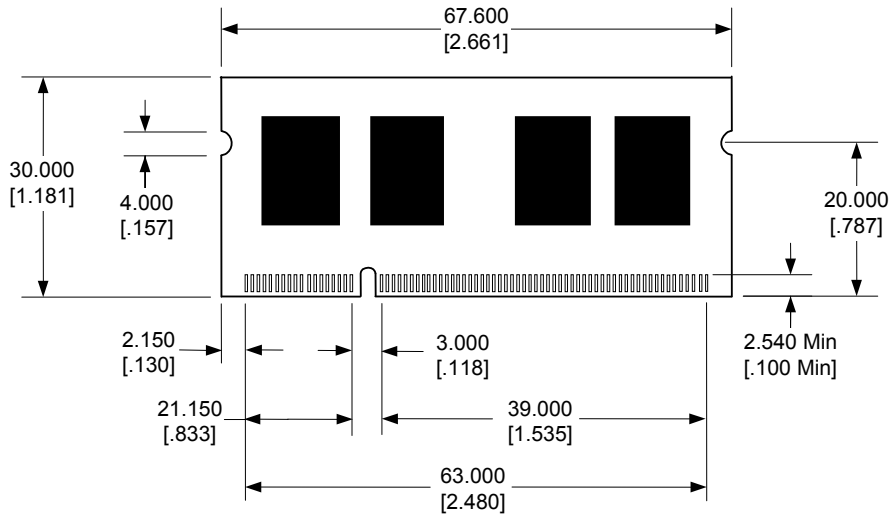
Pin Configuration

Pin Description

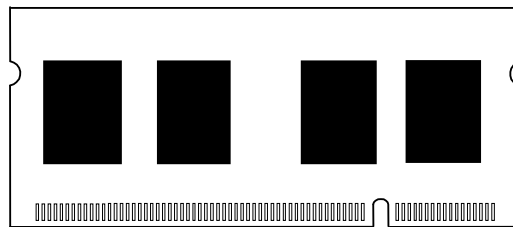
Front Side				Back Side				Name	Function								
1	V _{REFDQ}	53	DQ19	105	V _{DD}	157	DQ42	2	V _{SS}	54	V _{SS}	106	V _{DD}	158	DQ46	DQ[63:0]	Data Bits
3	V _{SS}	55	V _{SS}	107	A10/AP	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47	DQS[7:0], /DQS[7:0]	Differential Data Strobes
5	DQ0	57	DQ24	109	BA0	161	V _{SS}	6	DQ5	58	DQ29	110	/RAS	162	V _{SS}	DM[7:0]	Data Mask
7	DQ1	59	DQ25	111	V _{DD}	163	DQ48	8	V _{SS}	60	V _{SS}	112	V _{DD}	164	DQ52	CK[1:0], /CK[1:0]	Differential Clock Inputs
9	V _{SS}	61	V _{SS}	113	/WE	165	DQ49	10	/DQS0	62	/DQS3	114	/S0	166	DQ53	CKE[1:0]	Clock Enables
11	DM0	63	DM3	115	/CAS	167	V _{SS}	12	DQS0	64	DQS3	116	ODT0	168	V _{SS}	/CAS	Column Address Strobe
13	V _{SS}	65	V _{SS}	117	V _{DD}	169	/DQS6	14	V _{SS}	66	V _{SS}	118	V _{DD}	170	DM6	/RAS	Row Address Strobe
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	ODT1*	172	V _{SS}	/S[1:0]	Chip Selects
17	DQ3	69	DQ27	121	/S1*	173	V _{SS}	18	DQ7	70	DQ31	122	NC	174	DQ54	/WE	Write Enable
19	V _{SS}	71	V _{SS}	123	V _{DD}	175	DQ50	20	V _{SS}	72	V _{SS}	124	V _{DD}	176	DQ55	A[15:0]	Address Inputs
21	DQ8	73	CKE0	125	NC/TEST	177	DQ51	22	DQ12	74	CKE1*	126	V _{REFCA}	178	V _{SS}	BA[2:0]	Bank Addresses
23	DQ9	75	V _{DD}	127	V _{SS}	179	V _{SS}	24	DQ13	76	V _{DD}	128	V _{SS}	180	DQ60	ODT[1:0]	On Die Termination Inputs
25	V _{SS}	77	NC	129	DQ32	181	DQ56	26	V _{SS}	78	A15*	130	DQ36	182	DQ61	SA[1:0]	SPD Address
27	/DQS1	79	BA2	131	DQ33	183	DQ57	28	DM1	80	A14	132	DQ37	184	V _{SS}	SCL	SPD Clock Input
29	DQS1	81	V _{DD}	133	V _{SS}	185	V _{SS}	30	/RESET	82	V _{DD}	134	V _{SS}	186	/DQS7	SDA	SPD Data Input/Output
31	V _{SS}	83	A12/BC	135	/DQS4	187	DM7	32	V _{SS}	84	A11	136	DM4	188	DQS7	TEST	Logic Analyzer specific
33	DQ10	85	A9	137	DQS4	189	V _{SS}	34	DQ14	86	A7	138	V _{SS}	190	V _{SS}	V _{SS}	Ground
35	DQ11	87	V _{DD}	139	V _{SS}	191	DQ58	36	DQ15	88	V _{DD}	140	DQ38	192	DQ62	V _{DD}	Power
37	V _{SS}	89	A8	141	DQ34	193	DQ59	38	V _{SS}	90	A6	142	DQ39	194	DQ63	V _{DDSPD}	SPD EEPROM Power
39	DQ16	91	A5	143	DQ35	195	V _{SS}	40	DQ20	92	A4	144	V _{SS}	196	V _{SS}	V _{REFDQ}	Reference Voltage for DQ
41	DQ17	93	V _{DD}	145	V _{SS}	197	SA0	42	DQ21	94	V _{DD}	146	DQ44	198	NC	V _{REFCA}	Reference Voltage for CA
43	V _{SS}	95	A3	147	DQ40	199	V _{DDSPD}	44	V _{SS}	96	A2	148	DQ45	200	SDA	V _{TT}	Termination Voltage
45	/DQS2	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V _{SS}	202	SCL	NC	No Connection
47	DQS2	99	V _{DD}	151	V _{SS}	203	V _{TT}	48	V _{SS}	100	V _{DD}	152	/DQS5	204	V _{TT}		
49	V _{SS}	101	CK0	153	DM5			50	DQ22	102	CK1*	154	DQS5				
51	DQ18	103	/CK0	155	V _{SS}			52	DQ23	104	/CK1*	156	V _{SS}				

* = Not Used

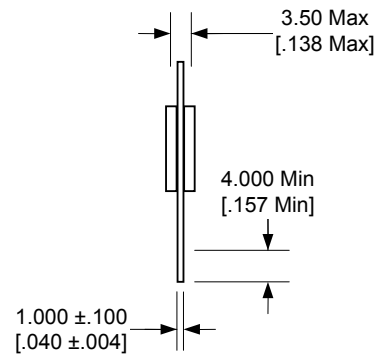
Front view



Back view



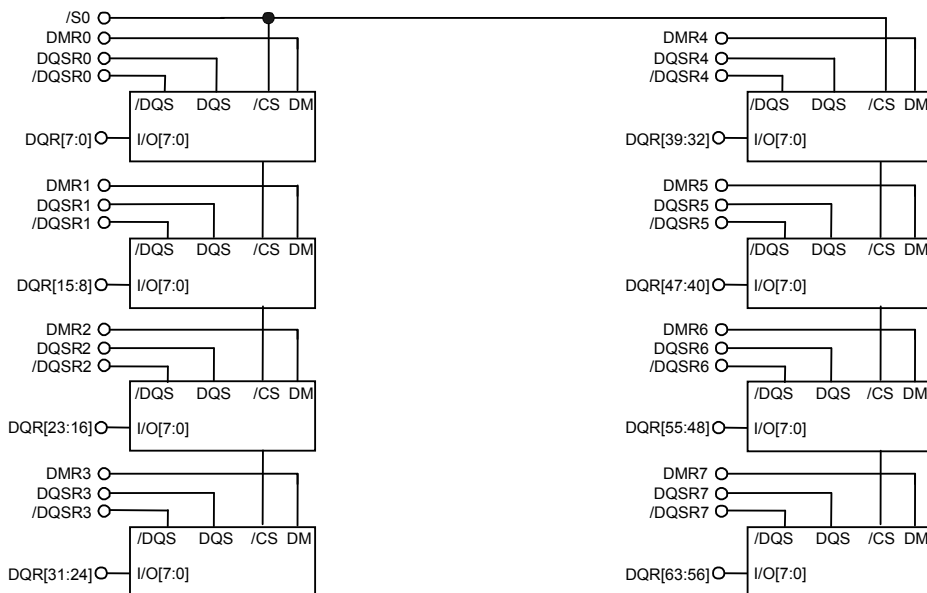
Side view



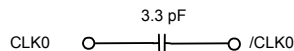
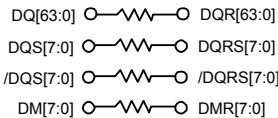
Notes

Tolerances on all dimensions except where otherwise indicated are ± 0.15 (.0059).

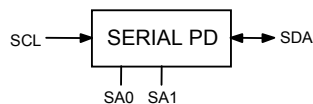
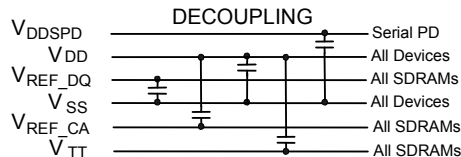
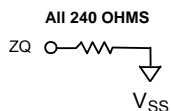
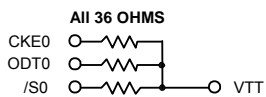
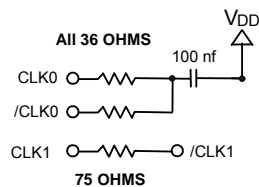
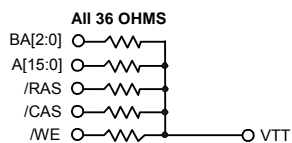
All dimensions are expressed: millimeters [inches]



All 15 OHMS



GLOBAL SDRAM CONNECTS



Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	T _{STORAGE}	-55	100	C
Module Ambient Temperature, Operating	T _A	-40	95	C
DRAM Case Temperature, Operating	T _{CASE}	-40	95	C
Voltage on V _{DD} relative to V _{SS}	V _{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V _{DD}	1.425	1.5	1.575	V	
I/O Reference Voltage	V _{REFDQ}	0.49 V _{DD}	0.50 V _{DD}	0.51 V _{DD}	V	1
I/O Reference Voltage	V _{REFCA}	0.49 V _{DD}	0.50 V _{DD}	0.51 V _{DD}	V	1

Notes:

The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% of its DC value. For Reference: V_{DD}/2 ± 15 mV.

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	V _{IH(DC)}	V _{REF} + 0.1	V _{DD}	V
Logical Low (Logic 0)	V _{IL(DC)}	V _{SS}	V _{REF} - 0.1	V

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	V _{IH(AC)}	V _{REF} + 0.175	-	V
Logical Low (Logic 0)	V _{IL(AC)}	-	V _{REF} - 0.175	V

Differential Input Logic Levels ($T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Differential Input Logic High	$V_{IH,DIFF}$	+0.200	DC: V_{DD} AC: $V_{DD}+0.4$	V	1
Differential Input Logic Low	$V_{IL,DIFF}$	DC: V_{SS} AC: $V_{SS}-0.4$	-0.200	V	2
Differential Input Cross Point Voltage relative to $V_{DD}/2$	V_{IX}	- 0.150	+ 0.150	V	4

Capacitance ($T_A = 25$ C, $f = 100$ MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	C_{CK}	6.4	12.8	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	C_I	6	10.4	pF
Input Capacitance Control	/S0, CKE0, ODT0	C_I	6	10.4	pF
Input/Output Capacitance	DQ[63:0], DQS[7:0], /DQS[7:0], DM[7:0]	C_{IO}	1.5	2.5	pF

DC Characteristics ($T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input 0 V < V_{IN} < V_{DD})	I_{IL}	-8	+8	μ A	1,2
Output Leakage Current (0 V < V_{OUT} < V_{DDQ})	I_{OL}	-5	+5	μ A	2,3

Notes:

- 1) All other pins not under test = 0 V
- 2) Values are shown per pin
- 3) DQ's, DQS, DQS and ODT are disabled

I_{DD} Specifications and Conditions (T_A = 0 to 70 C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	I _{DD0}	Operating current : One bank ACTIVATE-to-PRECHARGE	264	mA
Operating One Bank Active-Read-Precharge Current	I _{DD1}	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	320	mA
Precharge Power-Down Current	I _{DD2P}	Precharge power down current: (Slow exit)	64	mA
Precharge Power-Down Current	I _{DD2P}	Precharge power down current: (Fast exit)	80	mA
Precharge Quiet Standby Current	I _{DD2Q}	Precharge quiet standby current	136	mA
Precharge Standby Current	I _{DD2N}	Precharge standby current	136	mA
Active Power-Down Current	I _{DD3P}	Active power-down current	144	mA
Active Standby Current	I _{DD3N}	Active standby current	208	mA
Operating Burst Write Current	I _{DD4W}	Burst write operating current	720	mA
Operating Burst Read Current	I _{DD4R}	Burst read operating current	680	mA
Burst Refresh Current	I _{DD5}	Refresh current	1600	mA
Self Refresh Current	I _{DD6}	Self-refresh temperature current: MAX T _c = 85°C	96	mA
Operating Bank Interleave Read Current	I _{DD7}	All bank interleaved read current	1080	mA

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.125	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.25	2.5	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	45	-	ps
DQ Input Pulse Width	t_{DIPW}	360	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-225	+225	ps
Write DQS High Level Width	t_{DQSH}	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	125	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	10	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.9	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.3	-	$t_{CK(avg)}$
Address and Command Hold Time after Clock	t_{IH}	120	-	ps
Address and Command Setup Time before Clock	t_{IS}	45	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	35	$9 \cdot t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	48.125	-	ns
RAS-to-CAS Delay	t_{RCD}	13.125	-	ns
Average Periodic Refresh Interval $0^{\circ} C \leq T_{CASE} < 85^{\circ} C$	t_{REFI}	-	7.8	μs
Average Periodic Refresh Interval $85^{\circ} C \leq T_{CASE} < 95^{\circ} C$	t_{REFI}	-	3.9	μs
Auto Refresh Row Cycle Time	t_{RFC}	160	-	ns
Row Precharge Time	t_{RP}	13.125	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note 1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note 2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:

1. The maximum preamble is bound by $t_{LZDQS}(\min)$
2. The maximum postamble is bound by $t_{HZDQS}(\max)$

SPD available upon request.



DTM64617A

4GB - 512Mx64 204-pin non-ECC DDR3 Unbuffered SO-DIMM



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